

74AUP1T57

Low-power configurable gate with voltage-level translator

Rev. 7 — 26 January 2022

Product data sheet

1. General description

The 74AUP1T57 is a configurable multiple function gate with level translating, Schmitt-trigger inputs. The device can be configured as any of the following logic functions AND, OR, NAND, NOR, XNOR, inverter and buffer; using the 3-bit input. All inputs can be connected directly to V_{CC} or GND. Low threshold Schmitt trigger inputs allow these devices to be driven by 1.8 V logic levels in 3.3 V applications.

This device ensures very low static and dynamic power consumption across the entire V_{CC} range from 2.3 V to 3.6 V. This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Low static power consumption; $I_{CC} = 1.5 \mu\text{A}$ (maximum)
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Overvoltage tolerant inputs to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial power-down mode operation
- ESD protection:
 - HBM JESD22-A114F Class 3A exceeds 5000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM JESD22-C101E exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AUP1T57GW	-40 °C to +125 °C	TSSOP6	plastic thin shrink small outline package; 6 leads; body width 1.25 mm	SOT363-2
74AUP1T57GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74AUP1T57GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74AUP1T57GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202

4. Marking

Table 2. Marking

Type number	Marking code [1]
74AUP1T57GW	a7
74AUP1T57GM	a7
74AUP1T57GN	a7
74AUP1T57GS	a7

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

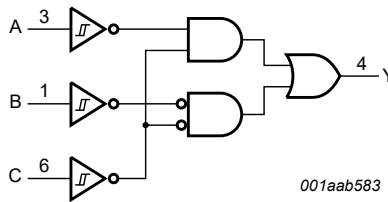


Fig. 1. Logic symbol

6. Pinning information

6.1. Pinning

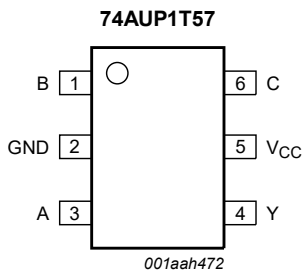


Fig. 2. Pin configuration SOT363-2 (TSSOP6)

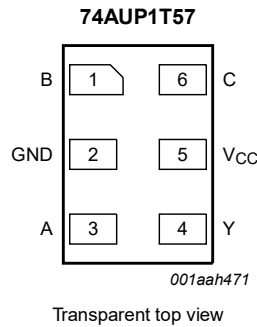


Fig. 3. Pin configuration SOT886 (XSON6)

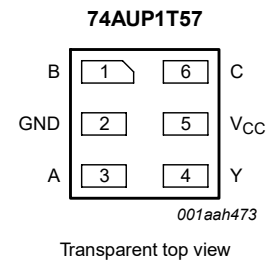


Fig. 4. Pin configuration SOT1115 and SOT1202 (XSON6)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
GND	2	ground (0 V)
A	3	data input
Y	4	data output
V _{CC}	5	supply voltage
C	6	data input

7. Functional description

Table 4. Function table

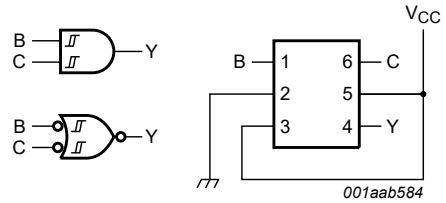
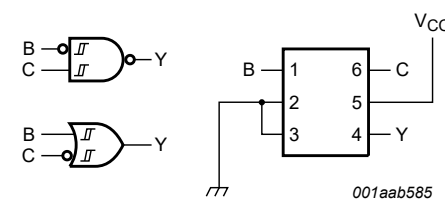
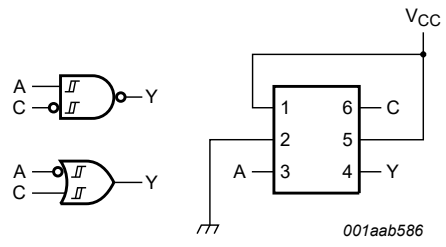
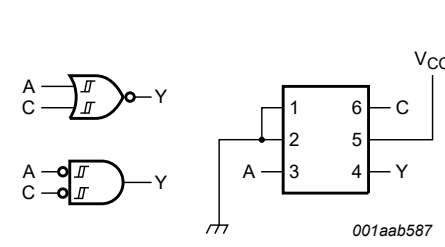
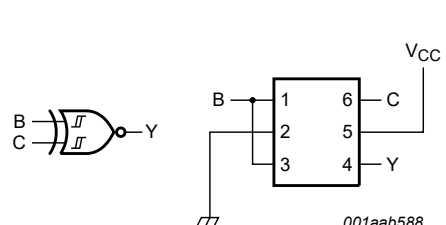
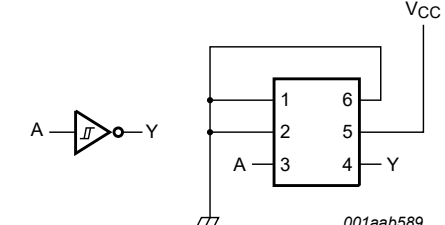
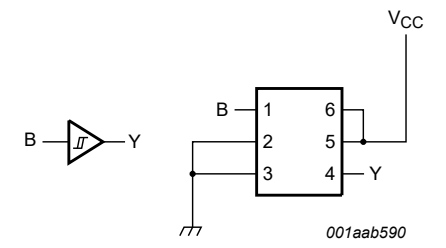
H = HIGH voltage level; L = LOW voltage level.

Input			Output
C	B	A	Y
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

7.1. Logic configurations

Table 5. Function selection table

Logic function	Figure
2-input AND	see Fig. 5
2-input AND with both inputs inverted	see Fig. 8
2-input NAND with inverted input	see Fig. 6 and Fig. 7
2-input OR with inverted input	see Fig. 6 and Fig. 7
2-input NOR	see Fig. 8
2-input NOR with both inputs inverted	see Fig. 5
2-input XNOR	see Fig. 9
Inverter	see Fig. 10
Buffer	see Fig. 11

 <p>Fig. 5. 2-input AND gate or 2-input NOR gate with both inputs inverted</p>	 <p>Fig. 6. 2-input NAND gate with input B inverted or 2-input OR gate with inverted C input</p>
 <p>Fig. 7. 2-input NAND gate with input C inverted or 2-input OR gate with inverted A input</p>	 <p>Fig. 8. 2-input NOR gate or 2-input AND gate with both inputs inverted</p>
 <p>Fig. 9. 2-input XNOR gate</p>	 <p>Fig. 10. Inverter</p>
 <p>Fig. 11. Buffer</p>	

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		-0.5	+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
V_O	output voltage	Active mode and Power-down mode	-0.5	+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 20	mA
I_{CC}	supply current		-	50	mA
I_{GND}	ground current		-50	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT363-2 (TSSOP6) package: P_{tot} derates linearly with 3.7 mW/K above 83 °C.

For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.

For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

9. Recommended operating conditions

Table 7. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		-40	+125	°C

10. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.16	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	(V _H = V _{T+} - V _{T-})				
		V _{CC} = 2.3 V to 2.7 V	0.23	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.25	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	2.05	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.72	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.6	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 2.3 V to 3.6 V	-	-	0.10	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.31	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.44	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.31	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.44	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.1	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.1	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.2	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	1.2	μA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 2.7 V; I _O = 0 A [1]	-	-	-	μA
		V _{CC} = 3.0 V to 3.6 V; I _O = 0 A [2]	-	-	-	μA
C _I	input capacitance	V _{CC} = 0 V to 3.6 V; V _I = GND or V _{CC}	-	0.8	-	pF
C _O	output capacitance	V _O = GND; V _{CC} = 0 V	-	1.7	-	pF

Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.35	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.50	-	0.85	V
V _H	hysteresis voltage	(V _H = V _{T+} - V _{T-})				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.1	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.97	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.85	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.67	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.55	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 2.3 V to 3.6 V	-	-	0.1	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.33	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.33	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.45	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.5	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.5	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.5	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	1.5	μA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 2.7 V; I _O = 0 A [1]	-	-	4	μA
		V _{CC} = 3.0 V to 3.6 V; I _O = 0 A [2]	-	-	12	μA

Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V _{T+}	positive-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.60	-	1.10	V
		V _{CC} = 3.0 V to 3.6 V	0.75	-	1.19	V
V _{T-}	negative-going threshold voltage	V _{CC} = 2.3 V to 2.7 V	0.33	-	0.64	V
		V _{CC} = 3.0 V to 3.6 V	0.46	-	0.85	V
V _H	hysteresis voltage	(V _H = V _{T+} - V _{T-})				
		V _{CC} = 2.3 V to 2.7 V	0.10	-	0.60	V
		V _{CC} = 3.0 V to 3.6 V	0.15	-	0.56	V
V _{OH}	HIGH-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = -20 μA; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.11	-	-	V
		I _O = -2.3 mA; V _{CC} = 2.3 V	1.77	-	-	V
		I _O = -3.1 mA; V _{CC} = 2.3 V	1.67	-	-	V
		I _O = -2.7 mA; V _{CC} = 3.0 V	2.40	-	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.30	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{T+} or V _{T-}				
		I _O = 20 μA; V _{CC} = 2.3 V to 3.6 V	-	-	0.11	V
		I _O = 2.3 mA; V _{CC} = 2.3 V	-	-	0.36	V
		I _O = 3.1 mA; V _{CC} = 2.3 V	-	-	0.50	V
		I _O = 2.7 mA; V _{CC} = 3.0 V	-	-	0.36	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.50	V
I _I	input leakage current	V _I = GND to 3.6 V; V _{CC} = 0 V to 3.6 V	-	-	±0.75	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±0.75	μA
ΔI _{OFF}	additional power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V to 0.2 V	-	-	±0.75	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{CC} = 2.3 V to 3.6 V	-	-	3.5	μA
ΔI _{CC}	additional supply current	V _{CC} = 2.3 V to 2.7 V; I _O = 0 A [1]	-	-	7	μA
		V _{CC} = 3.0 V to 3.6 V; I _O = 0 A [2]	-	-	22	μA

[1] One input at 0.3 V or 1.1 V, other input at V_{CC} or GND.

[2] One input at 0.45 V or 1.2 V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 9. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 13.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
V_{CC} = 2.3 V to 2.7 V; V_I = 1.65 V to 1.95 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 12 [2]								
		C _L = 5 pF	2.1	3.6	5.5	0.5	6.8	0.5	7.5	ns
		C _L = 10 pF	2.6	4.1	6.2	1.0	7.9	1.0	8.7	ns
		C _L = 15 pF	2.9	4.6	6.8	1.0	8.7	1.0	9.6	ns
		C _L = 30 pF	3.8	5.8	8.2	1.5	10.8	1.5	11.9	ns

Low-power configurable gate with voltage-level translator

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
V_{CC} = 2.3 V to 2.7 V; V_I = 2.3 V to 2.7 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 12 [2]								
		C _L = 5 pF	1.7	3.4	5.4	0.5	6.0	0.5	6.6	ns
		C _L = 10 pF	2.1	4.0	6.2	1.0	7.1	1.0	7.9	ns
		C _L = 15 pF	2.5	4.5	6.7	1.0	7.9	1.0	8.7	ns
		C _L = 30 pF	3.3	5.6	8.2	1.5	10.0	1.5	11.0	ns
V_{CC} = 2.3 V to 2.7 V; V_I = 3.0 V to 3.6 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 12 [2]								
		C _L = 5 pF	1.4	3.2	4.9	0.5	5.5	0.5	6.1	ns
		C _L = 10 pF	1.8	3.7	5.7	1.0	6.5	1.0	7.2	ns
		C _L = 15 pF	2.2	4.2	6.3	1.0	7.4	1.0	8.2	ns
		C _L = 30 pF	3.0	5.4	7.8	1.5	9.5	1.5	10.5	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 1.65 V to 1.95 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 12 [2]								
		C _L = 5 pF	2.0	2.9	3.9	0.5	8.0	0.5	8.8	ns
		C _L = 10 pF	2.5	3.5	4.6	1.0	8.5	1.0	9.4	ns
		C _L = 15 pF	2.8	3.9	5.2	1.0	9.1	1.0	10.1	ns
		C _L = 30 pF	3.6	5.1	6.6	1.5	9.8	1.5	10.8	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 2.3 V to 2.7 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 12 [2]								
		C _L = 5 pF	1.6	2.8	4.2	0.5	5.3	0.5	5.9	ns
		C _L = 10 pF	2.0	3.4	4.9	1.0	6.1	1.0	6.8	ns
		C _L = 15 pF	2.3	3.9	5.5	1.0	6.8	1.0	7.5	ns
		C _L = 30 pF	3.1	5.0	6.9	1.5	8.5	1.5	9.4	ns
V_{CC} = 3.0 V to 3.6 V; V_I = 3.0 V to 3.6 V										
t _{pd}	propagation delay	A, B, C to Y; see Fig. 12 [2]								
		C _L = 5 pF	1.3	2.8	4.2	0.5	4.7	0.5	5.2	ns
		C _L = 10 pF	1.7	3.3	4.9	1.0	5.7	1.0	6.3	ns
		C _L = 15 pF	2.0	3.8	5.5	1.0	6.2	1.0	6.9	ns
		C _L = 30 pF	2.8	4.9	7.0	1.5	7.8	1.5	8.6	ns
T_{amb} = 25 °C										
C _{PD}	power dissipation capacitance	f _i = 1 MHz; V _I = GND to V _{CC} [3]								
		V _{CC} = 2.3 V to 2.7 V	-	3.6	-	-	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	4.3	-	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.
 [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
 [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

11.1. Waveforms and test circuit

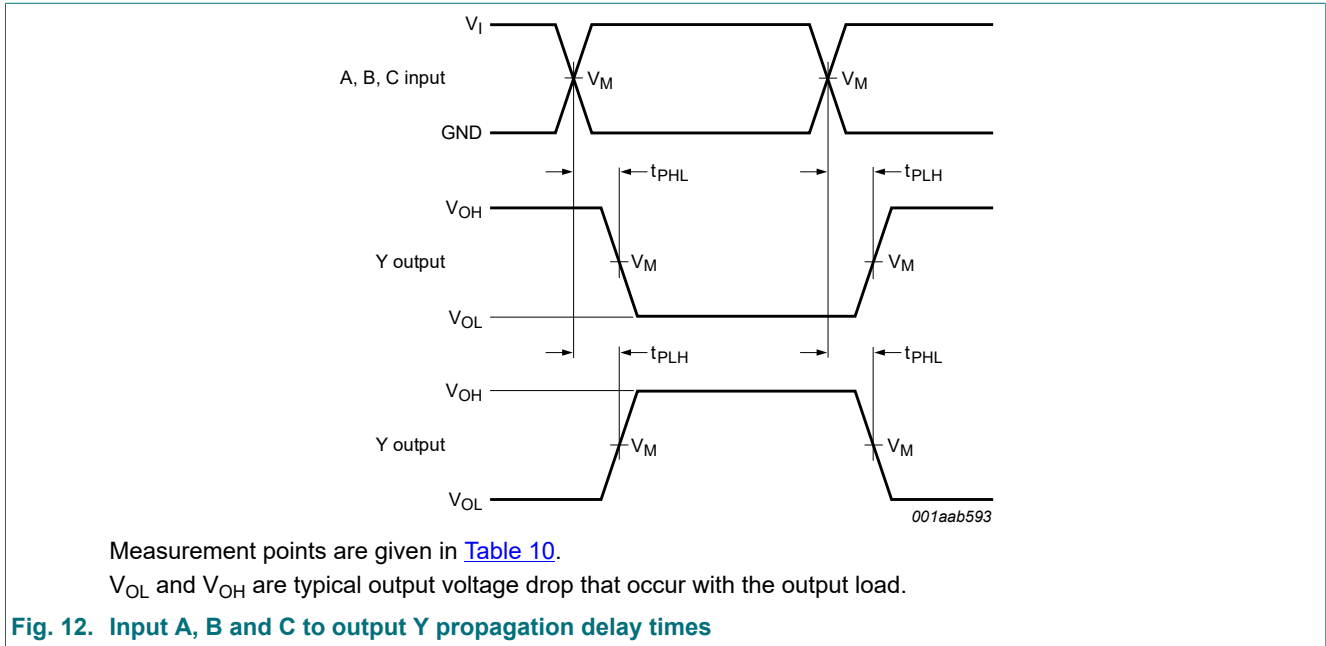


Table 10. Measurement points

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
2.3 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_I$	1.65 V to 3.6 V	≤ 3.0 ns

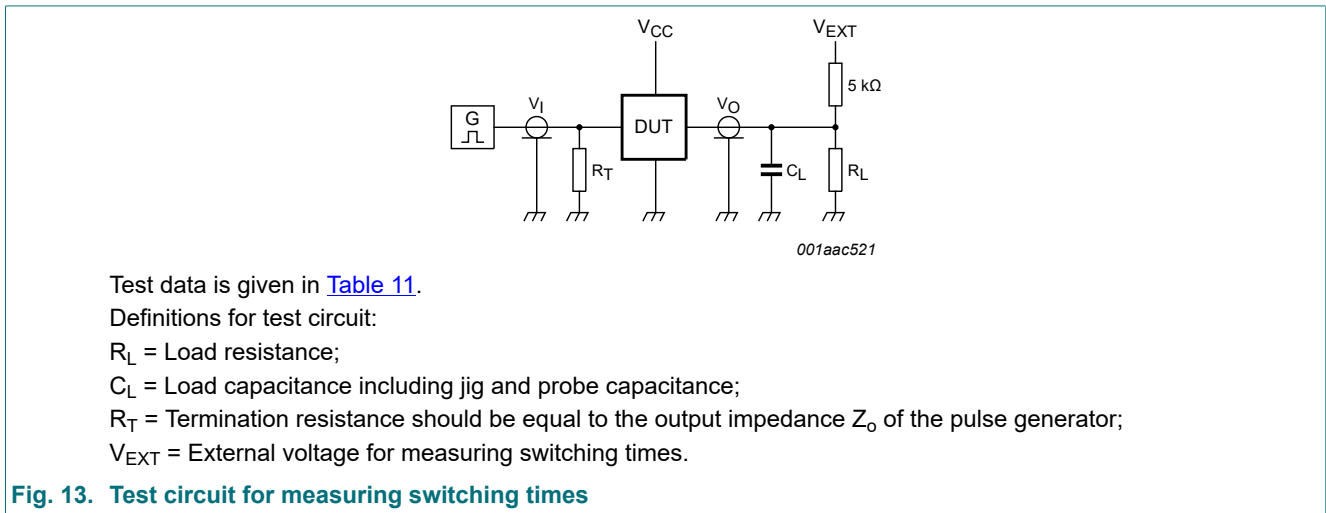


Table 11. Test data

Supply voltage	Load		V_{EXT}		
V_{CC}	C_L	R_L [1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
2.3 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 k Ω or 1 M Ω	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times $R_L = 5\text{ k}\Omega$.
 For measuring propagation delays, setup and hold times and pulse width $R_L = 1\text{ M}\Omega$.

12. Package outline

TSSOP6: plastic thin shrink small outline package; 6 leads; body width 1.25 mm

SOT363-2



Fig. 14. Package outline SOT363-2 (TSSOP6)

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm

SOT886



Fig. 15. Package outline SOT886 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 0.9 x 1.0 x 0.35 mm

SOT1115



Fig. 16. Package outline SOT1115 (XSON6)

XSON6: extremely thin small outline package; no leads;
6 terminals; body 1.0 x 1.0 x 0.35 mm

SOT1202



Fig. 17. Package outline SOT1202 (XSON6)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP1T57 v.7	20220126	Product data sheet	-	74AUP1T57 v.6
Modifications:	<ul style="list-style-type: none"> Package SOT363 (SC-88) changed to SOT363-2 (TSSOP6). 			
74AUP1T57 v.6	20210526	Product data sheet	-	74AUP1T57 v.5
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74AUP1T57GF (SOT891 / XSON6) removed. Section 1 and Section 2 updated. Section 8: Derating values for P_{tot} total power dissipation updated. 			
74AUP1T57 v.5	20120815	Product data sheet	-	74AUP1T57 v.4
Modifications:	<ul style="list-style-type: none"> Package outline drawing of SOT886 (Fig. 15) modified. 			
74AUP1T57 v.4	20111201	Product data sheet	-	74AUP1T57 v.3
74AUP1T57 v.3	20100721	Product data sheet	-	74AUP1T57 v.2
74AUP1T57 v.2	20090803	Product data sheet	-	74AUP1T57 v.1
74AUP1T57 v.1	20080103	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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