30V P-CHANNEL ENHANCEMENT MODE MOSFET
PowerDI5060-8

Product Summary

BV_{DSS}	$R_{DS(ON)}$	I_D T_C = +25°C
-30V	2.6mΩ @ V_{GS} = -10V	-100A
	3.75mΩ @ V_{GS} = -4.5V	-70A

Description

This new generation MOSFET is designed to minimize $R_{DS(ON)}$ and yet maintain superior switching performance. This device is ideal for use in notebook battery power management and load switch.

Applications

- Switch

Features

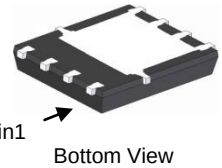
- 100% Unclamped Inductive Switch (UIS) Test in Production
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low $R_{DS(ON)}$ – Minimizes On State Losses
- <1.1mm Package Profile – Ideal for Thin Applications
- **Lead-Free Finish; RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

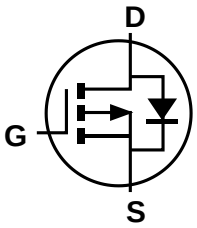
- Case: PowerDI®5060-8
- Case Material: Molded Plastic, "Green" Molding Compound; UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish - Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.097 grams (Approximate)

PowerDI5060-8 (Type K)

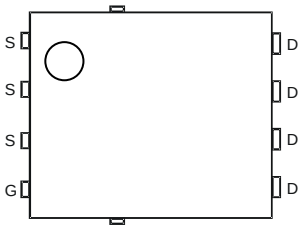
Top View



Bottom View



Internal Schematic



Top View
Pin Configuration

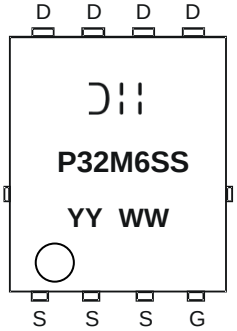
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP32M6SPS-13	PowerDI5060-8 (Type K)	2,500 / Tape & Reel

Notes:
1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

PowerDI5060-8 (Type K)



= Manufacturer's Marking
P32M6SS = Product Type Marking Code
YYWW = Date Code Marking
YY = Last Two Digits of Year (ex: 19 = 2019)
WW = Week Code (01 to 53)

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Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic			Symbol	Value	Unit
Drain-Source Voltage			V_{DSS}	-30	V
Gate-Source Voltage			V_{GSS}	±20	V
Continuous Drain Current, V_{GS} = -10V (Note 7) (Package Limited)	Steady State	T_C = +25°C T_C = +70°C	I_D	-100 -70	A
Continuous Drain Current, V_{GS} = -10V (Note 6)	t ≤ 10s	T_A = +25°C T_A = +70°C	I_D	-37 -30	A
Pulsed Drain Current (380µs Pulse, Duty Cycle = 1%)			I_{DM}	-400	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	-2.7	A
Pulsed Body Diode Forward Current (380µs Pulse, Duty Cycle = 1%)			I_{SM}	-400	A
Avalanche Current, L = 0.1mH (Note 8)			I_{AS}	-80	A
Avalanche Energy, L = 0.1mH (Note 8)			E_{AS}	250	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)		P_D	1.3	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	98	°C/W
	t ≤ 10s		49	
Total Power Dissipation (Note 6)		P_D	2.3	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	54	°C/W
	t ≤ 10s		27	
Thermal Resistance, Junction to Case (Note 7)		$R_{\theta JC}$	0.9	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	-30	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1	µA	V_{DS} = -24V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	-1.0	—	-2.5	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	1.8	2.6	mΩ	V_{GS} = -10V, I_D = -20A
		—	2.4	3.75		V_{GS} = -4.5V, I_D = -20A
Diode Forward Voltage	V_{SD}	—	-0.6	-1.2	V	V_{GS} = 0V, I_S = -1A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	8594	—	pF	V_{DS} = -15V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	1491	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	874	—	pF	
Gate Resistance	R_g	—	6.38	—	Ω	V_{DS} = 0V, V_{GS} = -15mV, f = 1MHz
Total Gate Charge (V_{GS} = -4.5V)	Q_g	—	75	—	nC	V_{DS} = -15V, I_D = -25A
Total Gate Charge (V_{GS} = -10V)	Q_g	—	158	—	nC	
Gate-Source Charge	Q_{gs}	—	23.0	—	nC	
Gate-Drain Charge	Q_{gd}	—	25.5	—	nC	
Turn-On Delay Time	$t_{D(ON)}$	—	6.74	—	ns	V_{DS} = -15V, V_{GS} = -10V, R_{GS} = 2.7Ω, I_D = -1A
Turn-On Rise Time	t_R	—	5.46	—	ns	
Turn-Off Delay Time	$t_{D(OFF)}$	—	227	—	ns	
Turn-Off Fall Time	t_F	—	108	—	ns	
Reverse Recovery Time	t_{RR}	—	37.4	—	ns	I_F = -25A, di/dt = 100A/µs
Reverse Recovery Charge	Q_{RR}	—	36.8	—	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J = +25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

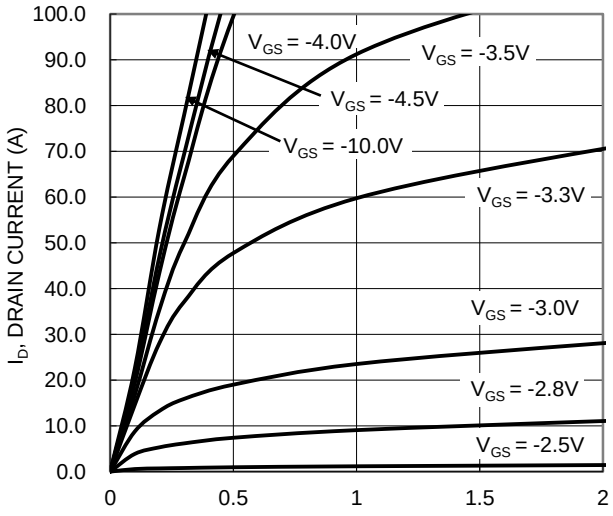


Figure 1. Typical Output Characteristic

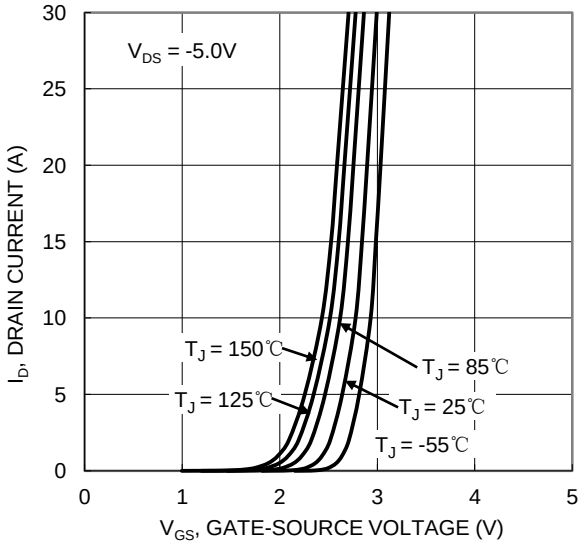


Figure 2. Typical Transfer Characteristic

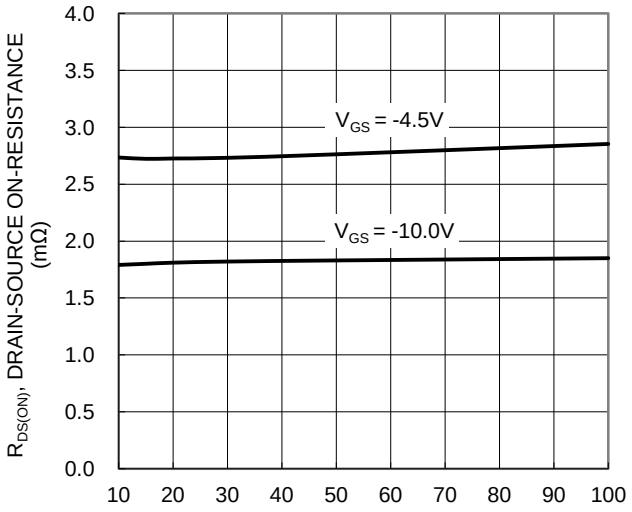


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

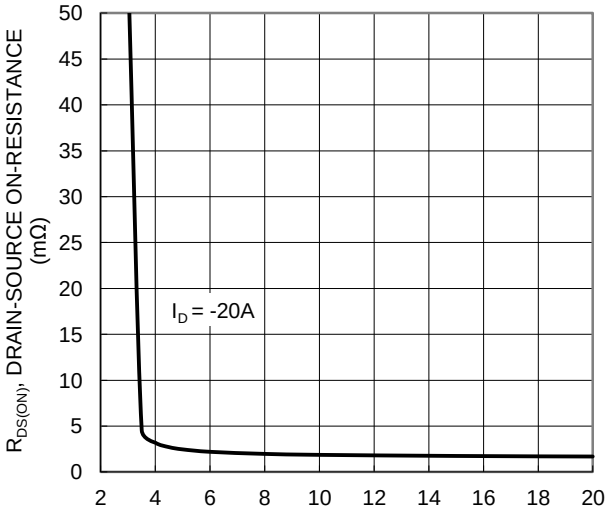


Figure 4. Typical Transfer Characteristic

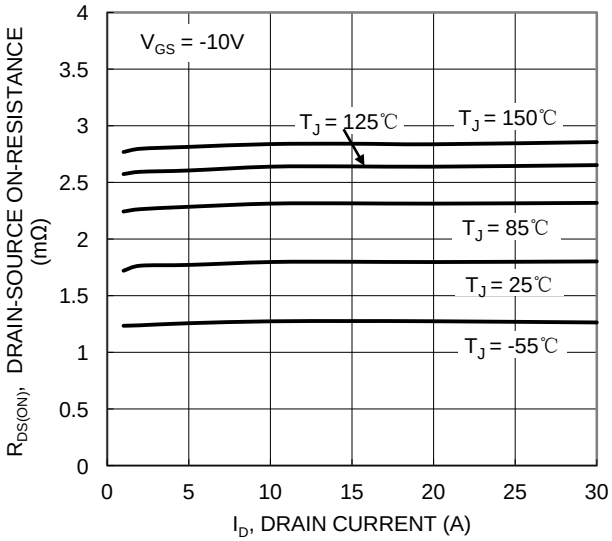


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

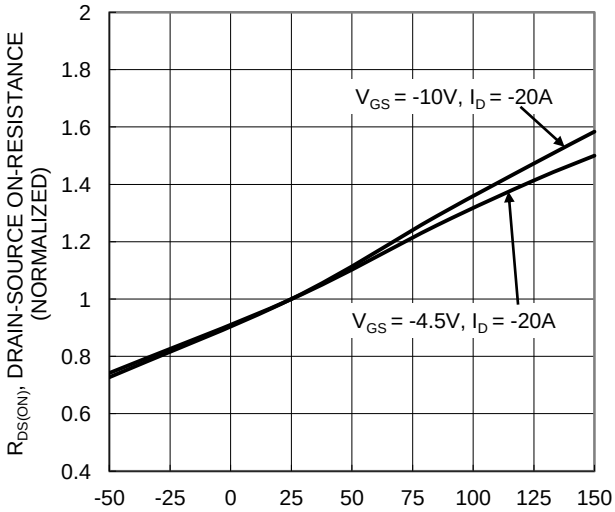


Figure 6. On-Resistance Variation with Junction Temperature

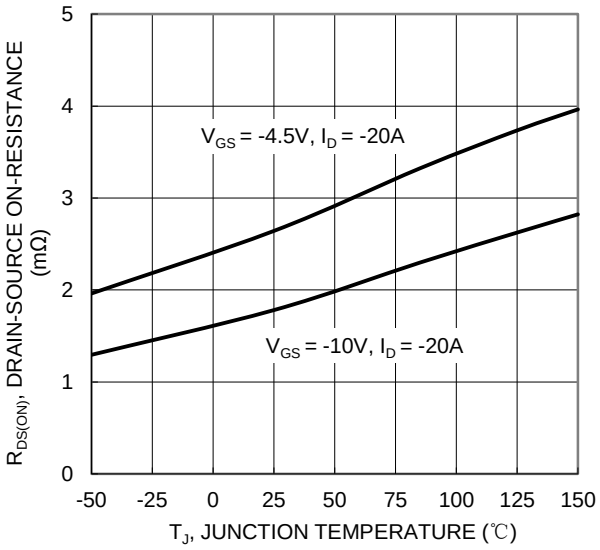


Figure 7. On-Resistance Variation with Junction Temperature

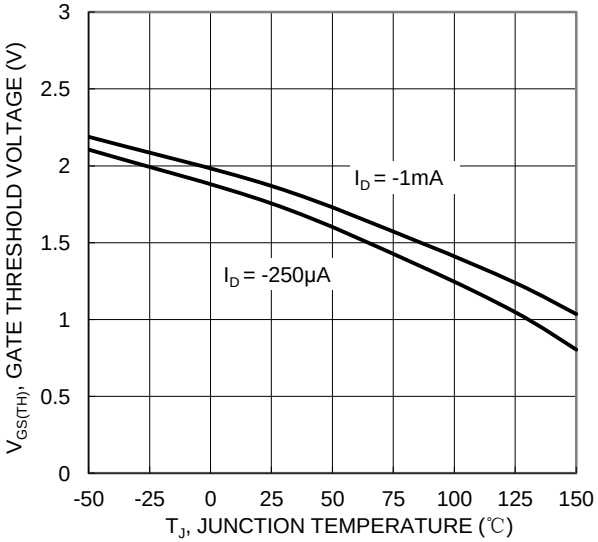


Figure 8. Gate Threshold Variation vs. Junction Temperature

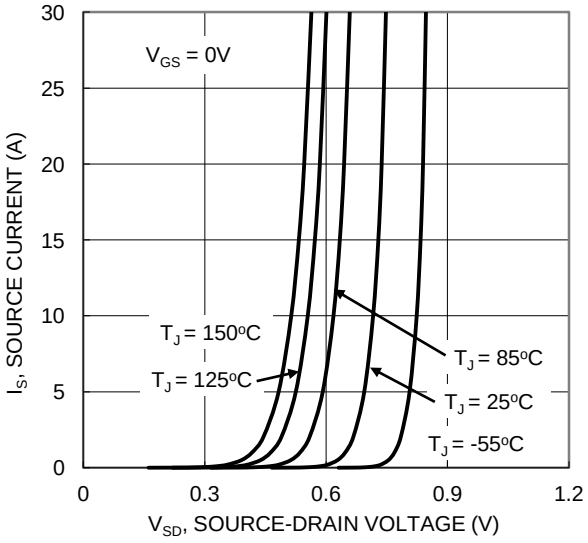


Figure 9. Diode Forward Voltage vs. Current

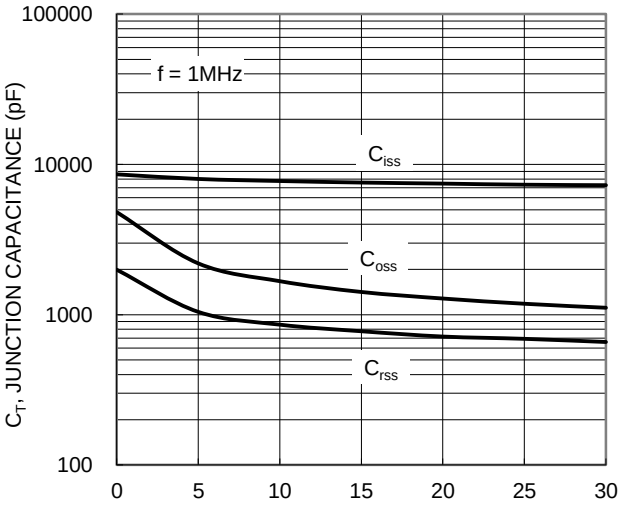


Figure 10. Typical Junction Capacitance

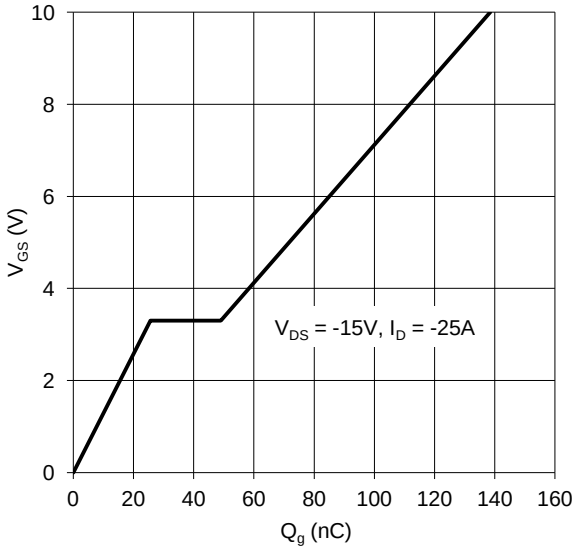


Figure 11. Gate Charge

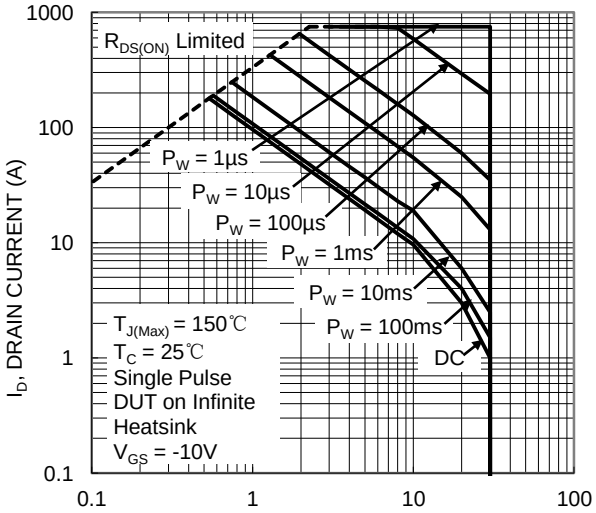


Figure 12. SOA, Safe Operation Area

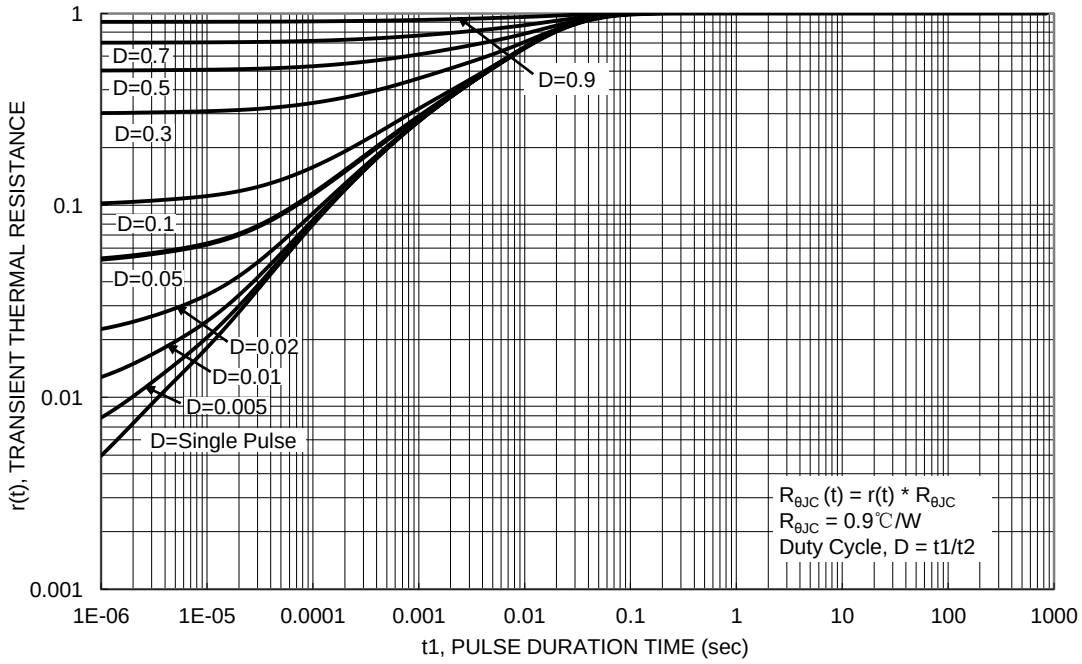
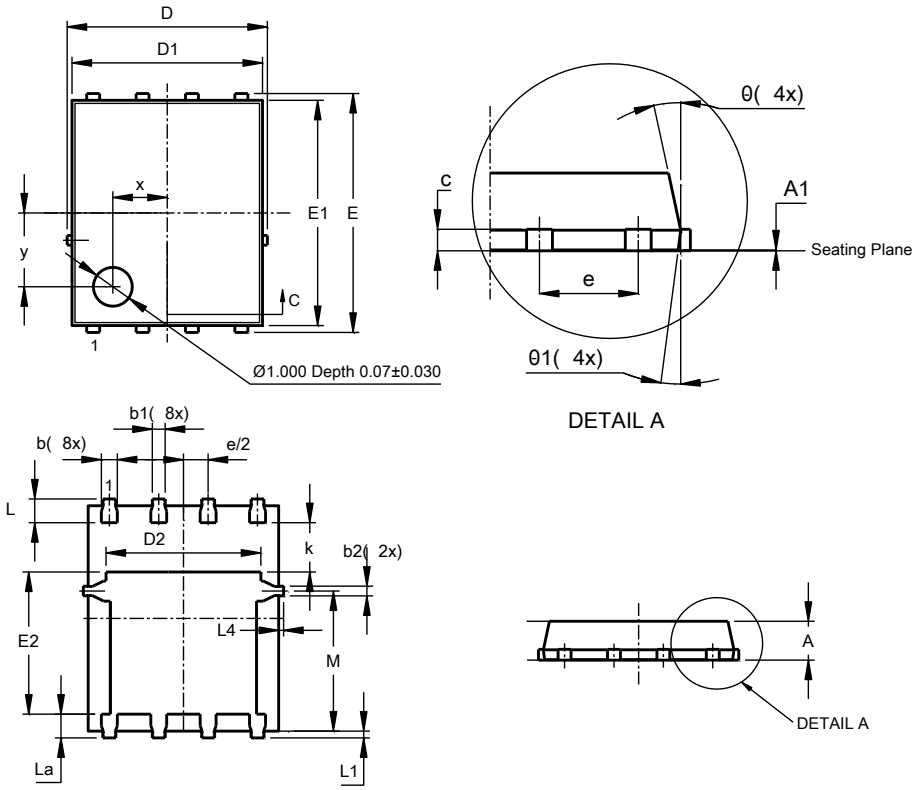


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (Type K)

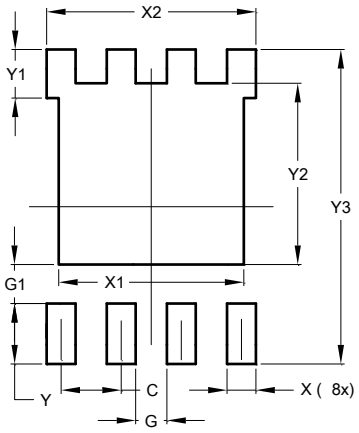


PowerDI5060-8 (Type K)			
Dim	**Min**	**Max**	**Typ**
A	0.90	1.10	1.00
A1	0	0.05	0.02
b	0.33	0.51	0.41
b1	0.300	0.366	0.333
b2	0.20	0.35	0.25
c	0.23	0.33	0.277
D	5.15 BSC		
D1	4.85	4.95	4.90
D2	-	-	3.98
E	6.15 BSC		
E1	5.75	5.85	5.80
E2	3.56	3.725	3.66
e	1.27BSC		
k	-	-	1.27
L	0.51	0.71	0.61
La	0.51	0.675	0.61
L1	0.05	0.20	0.175
L4	-	-	0.125
M	3.50	3.71	3.605
x	-	-	1.400
y	-	-	1.900
θ	10°	12°	11°
θ1	6°	8°	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (Type K)



Dimensions	Value (in mm)
C	1.270
G	0.660
G1	0.820
X	0.610
X1	3.910
X2	4.420
Y	1.270
Y1	1.020
Y2	3.810
Y3	6.610

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