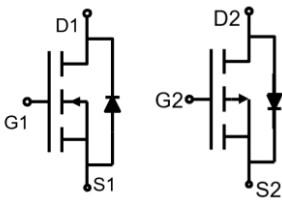
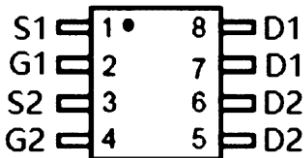
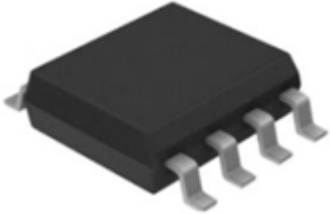


N and P Channel Enhancement Mode Power MOSFET

<p>Description This Product uses advanced trench technology MOSFETs to provide excellent $R_{DS(ON)}$ and low gate charge. The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.</p> <p>General Features</p> <ul style="list-style-type: none"> ● NMOS <ul style="list-style-type: none"> ● V_{DS} 60V ● I_D (at $V_{GS} = 10V$) 5A ● $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 36mΩ ● $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 40mΩ ● PMOS <ul style="list-style-type: none"> ● V_{DS} -60V ● I_D (at $V_{GS} = -10V$) -3.1A ● $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 80mΩ ● $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 95mΩ ● RoHS Compliant <p>Application</p> <ul style="list-style-type: none"> ● Power switch ● DC/DC converters 		 <p>Schematic diagram</p>  <p>Marking and pin assignment</p>  <p>SOP-8</p>	
Device	Package	Marking	Packaging
G05NP06S2	SOP-8双基	G05NP06	4000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ C$, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	60	-60	V
Continuous Drain Current	I_D	5	-3.1	A
Pulsed Drain Current (note1)	I_{DM}	20	-12.4	A
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Power Dissipation	P_D	2.5	1.9	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	$^\circ C$

Thermal Resistance

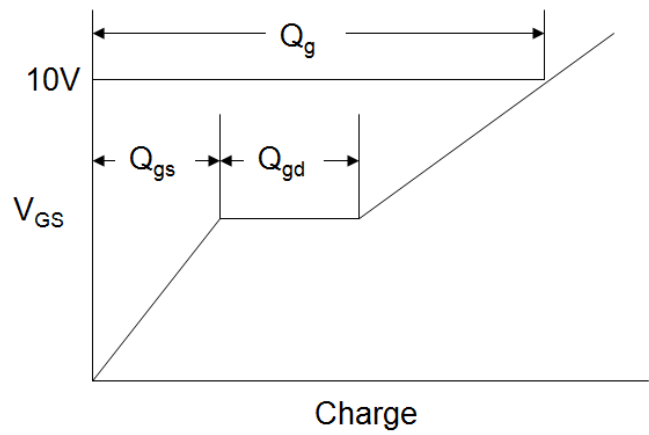
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	50	65	$^\circ C/W$

NMOS Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu\text{A}$	60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	1.0	1.5	2.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 4.3A$	--	28	36	m Ω
		$V_{GS} = 4.5V, I_D = 3.9A$	--	31	40	
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=4.3A$	--	9.6	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 30V,$ $f = 1.0\text{MHz}$	--	1336	--	pF
Output Capacitance	C_{oss}		--	56	--	
Reverse Transfer Capacitance	C_{rss}		--	52	--	
Total Gate Charge	Q_g	$V_{DS} = 30V,$ $I_D = 5A,$ $V_{GS} = 10V$	--	22	--	nC
Gate-Source Charge	Q_{gs}		--	3.3	--	
Gate-Drain Charge	Q_{gd}		--	5.2	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 30V,$ $I_D = 5A,$ $R_G = 3\Omega$	--	5.2	--	ns
Turn-on Rise Time	t_r		--	3	--	
Turn-off Delay Time	$t_{d(off)}$		--	17	--	
Turn-off Fall Time	t_f		--	2.5	--	
Drain-Source Body Diode Characteristics						
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 1.7A, V_{GS} = 0V$	--	--	1.2	V
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	5	A

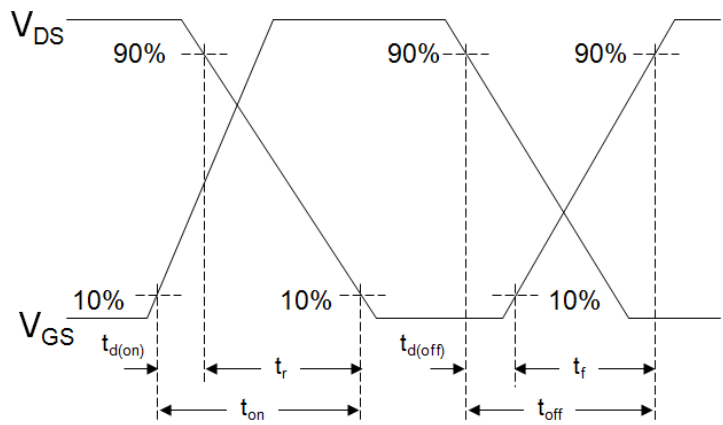
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

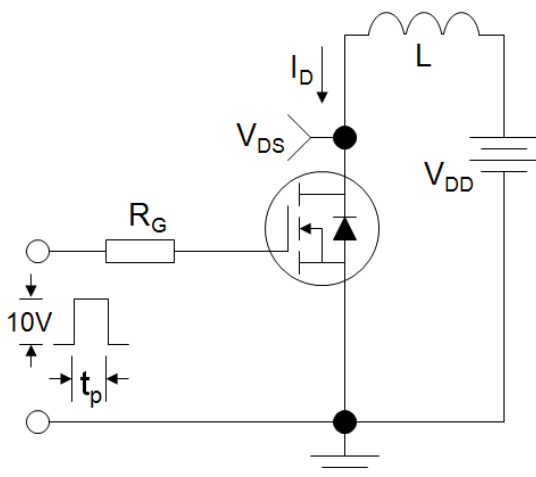
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

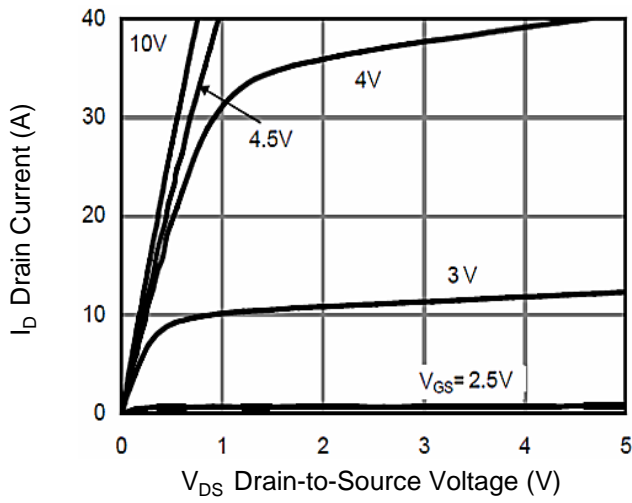


Figure 2. Transfer Characteristics

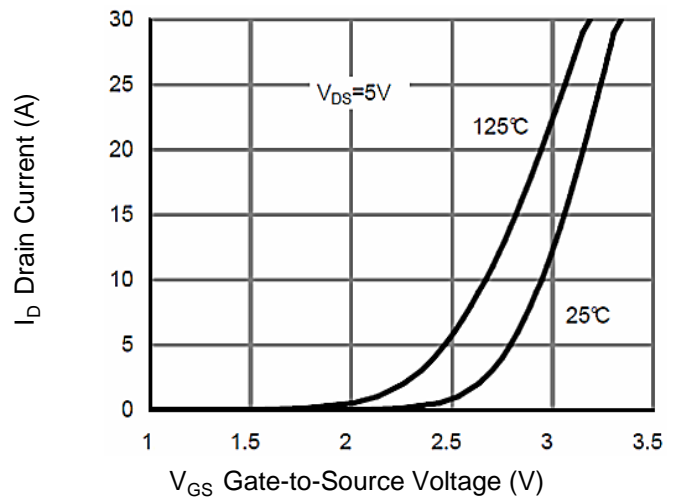


Figure 3. Drain-Source On-Resistance

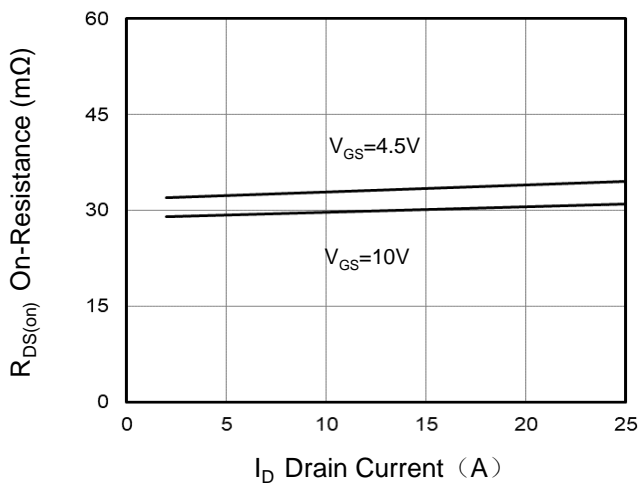


Figure 4. Gate Charge

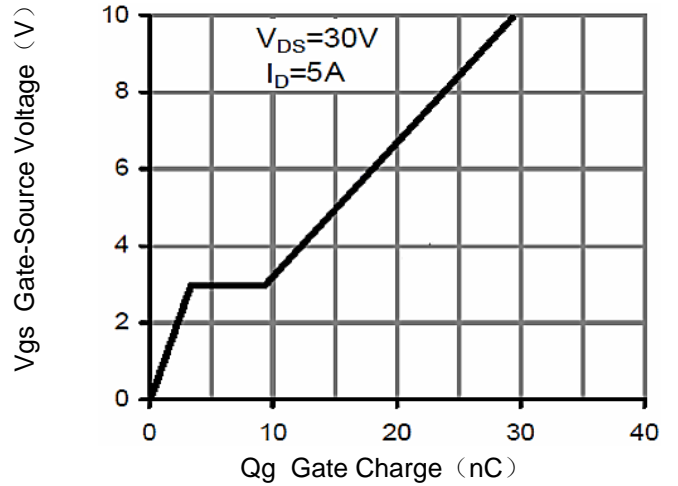


Figure 5. Capacitance

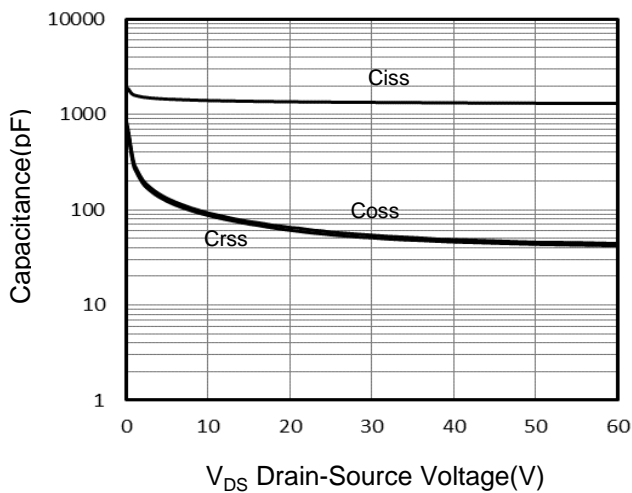
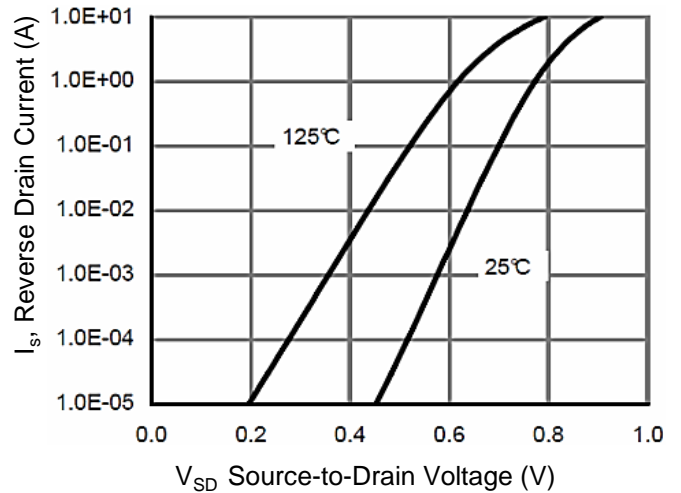


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

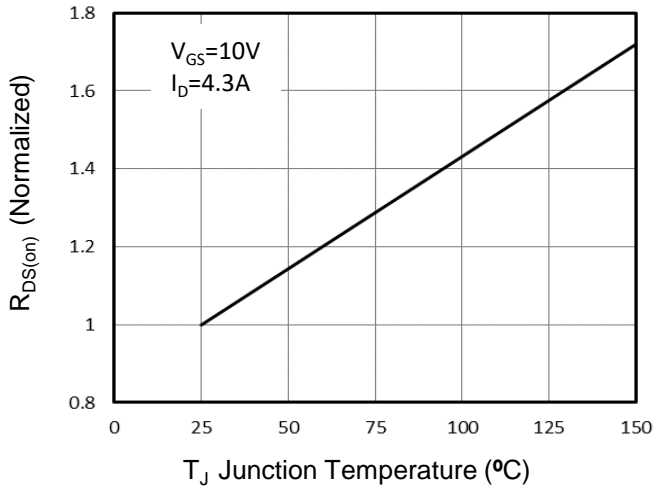


Figure 8. Safe Operation Area

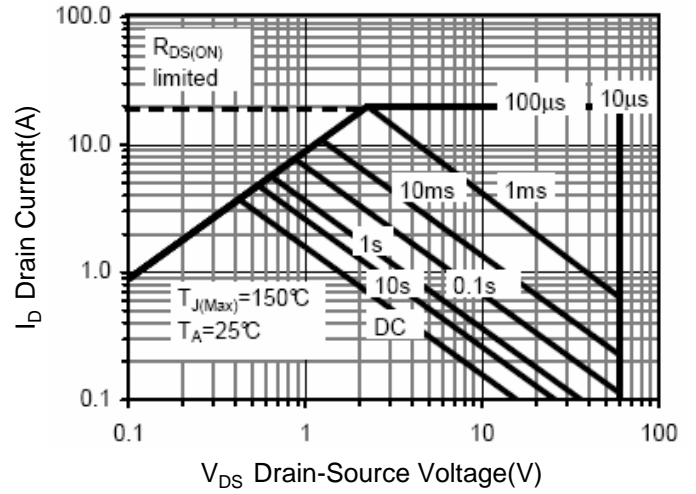
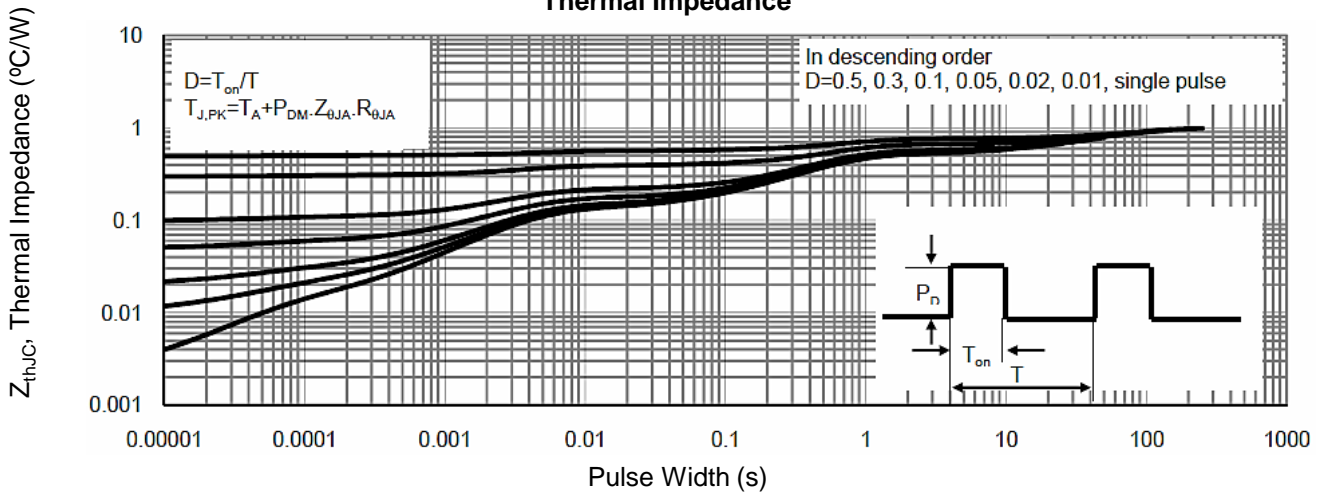


Figure 9. Normalized Maximum Transient Thermal Impedance

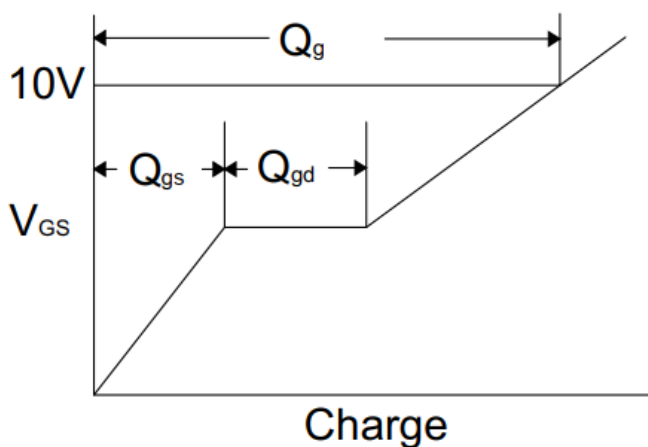
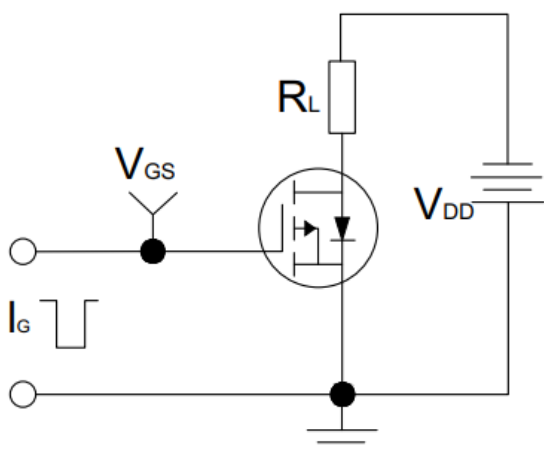


PMOS Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-60	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -60V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1.2	-1.7	-2.2	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -3.1A$	--	62	80	m Ω
		$V_{GS} = -4.5V, I_D = -0.2A$	--	72	95	
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_D = -3.1A$	--	6.6	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = -30V,$ $f = 1.0\text{MHz}$	--	1454	--	pF
Output Capacitance	C_{oss}		--	62	--	
Reverse Transfer Capacitance	C_{rss}		--	58	--	
Total Gate Charge	Q_g	$V_{DD} = -30V,$ $I_D = -3A,$ $V_{GS} = -10V$	--	37	--	nC
Gate-Source Charge	Q_{gs}		--	4.5	--	
Gate-Drain Charge	Q_{gd}		--	10.5	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -30V,$ $I_D = -3A,$ $R_G = 3\Omega$	--	8	--	ns
Turn-on Rise Time	t_r		--	4	--	
Turn-off Delay Time	$t_{d(off)}$		--	32	--	
Turn-off Fall Time	t_f		--	7	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-3.1	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = -2A, V_{GS} = 0V$	--	--	-1.2	V

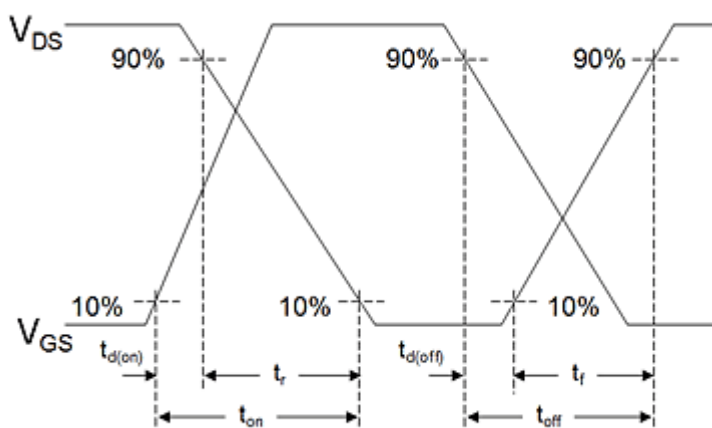
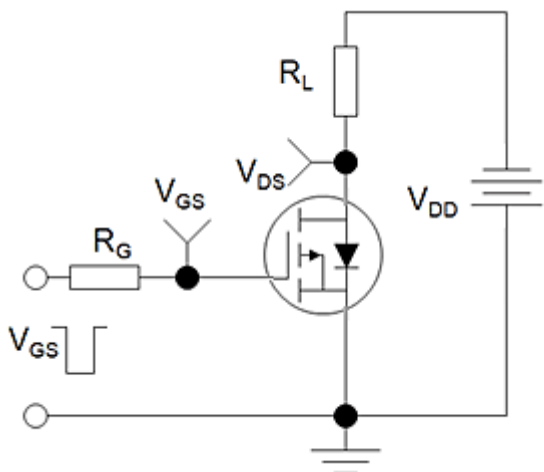
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

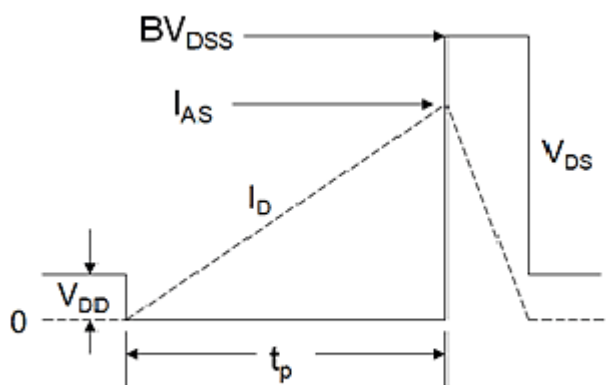
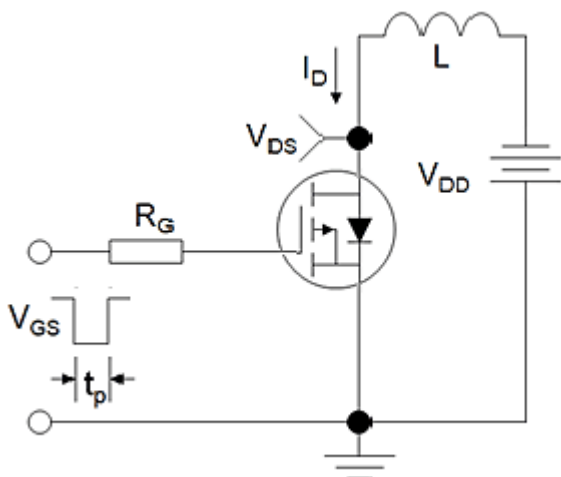
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics $T_J = 25^{\circ}\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

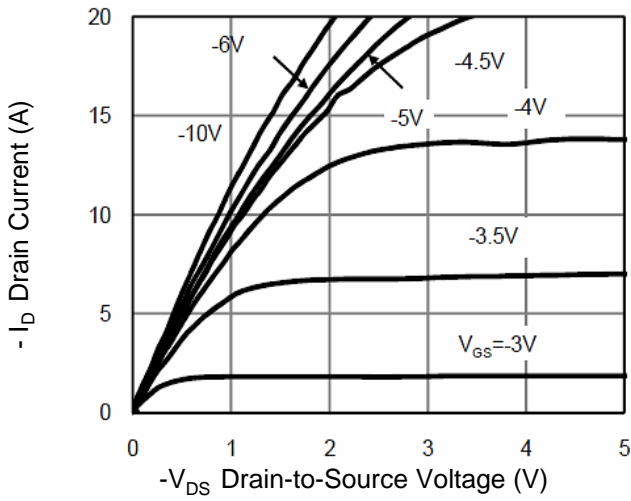


Figure 2. Transfer Characteristics

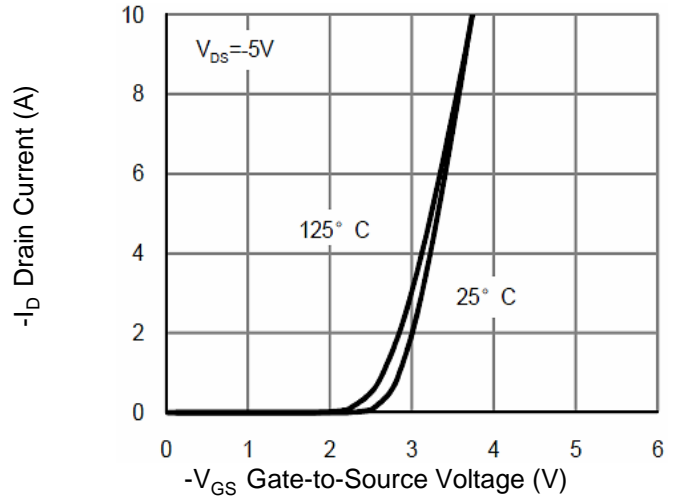


Figure 3. Rds(on)-Drain Current

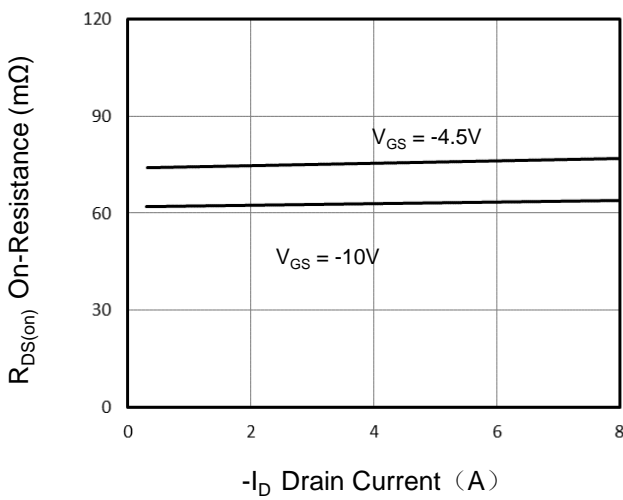


Figure 4. Gate Charge

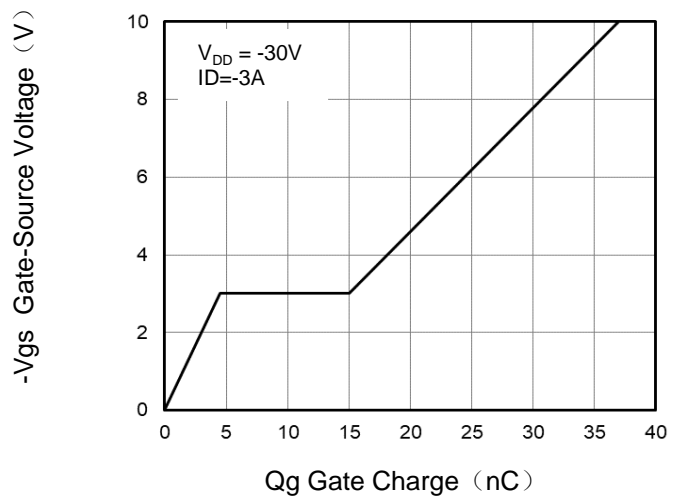


Figure 5. Capacitance

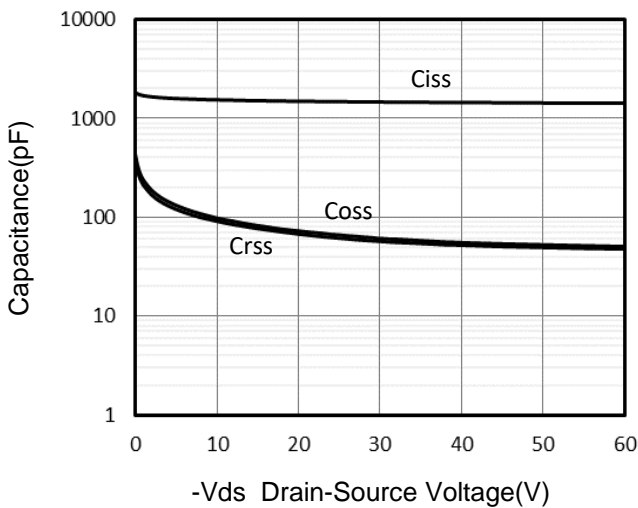
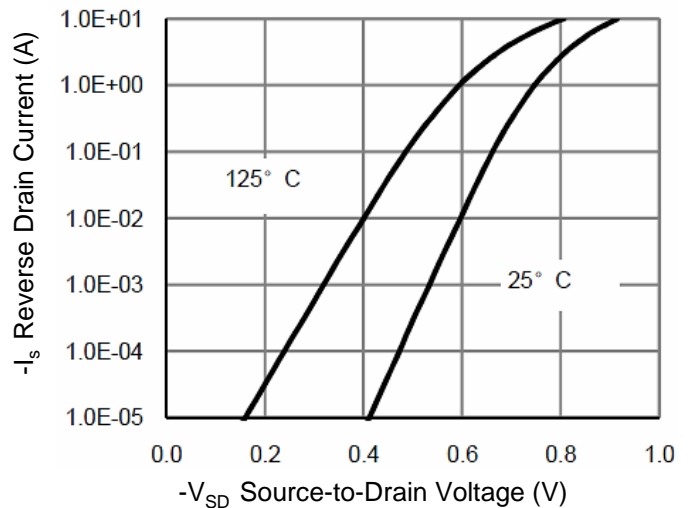


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

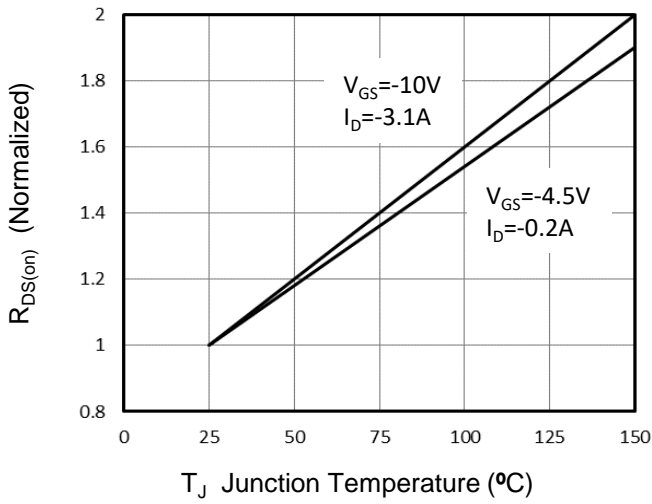


Figure 8. Safe Operation Area

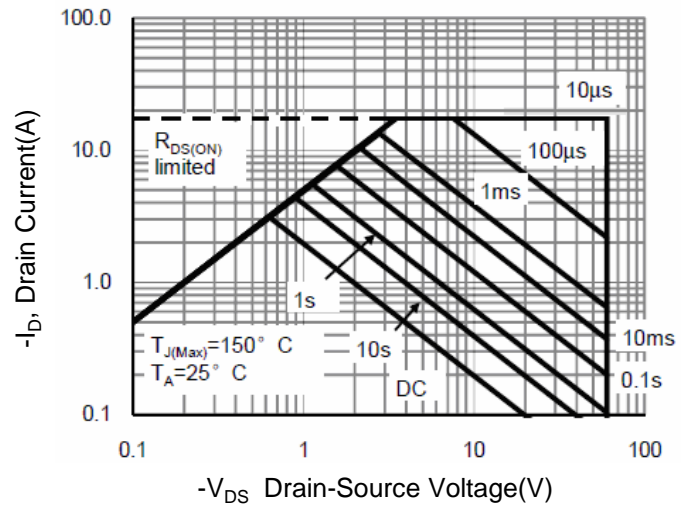
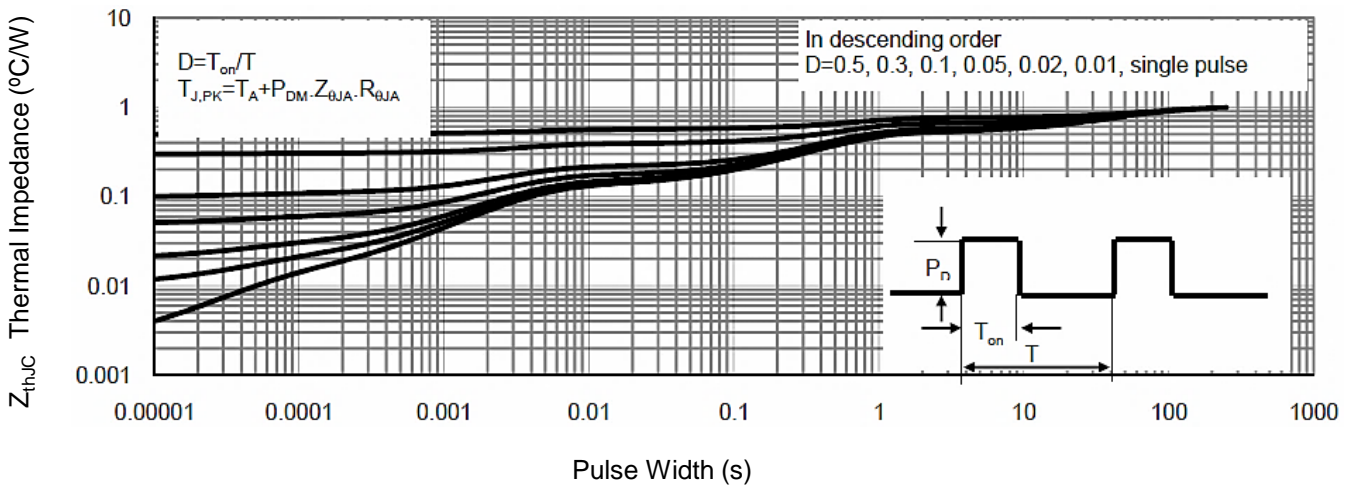
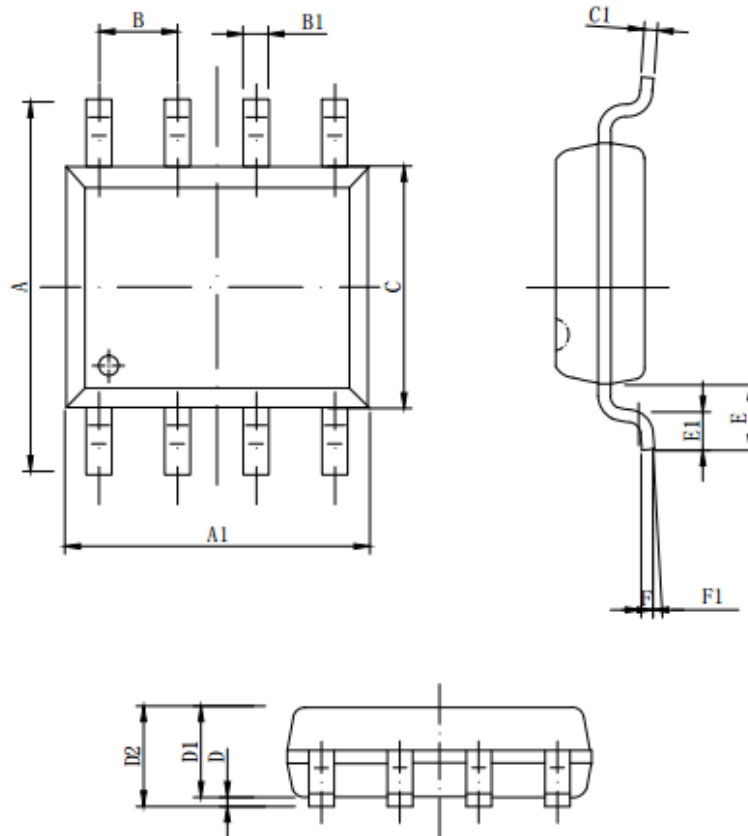


Figure 9. Normalized Maximum Transient Thermal Impedance



SOP-8 Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	5.800	6.000	6.200
A1	4.800	4.900	5.000
B	1.270BSC		
B1	0.35 ^{8x}	0.40 ^{8x}	0.45 ^{8x}
C	3.780	3.880	3.980
C1	--	0.203	0.253
D	0.050	0.150	0.250
D1	1.350	1.450	1.550
D2	1.500	1.600	1.700
D2	1.500	1.600	1.700
E	1.060REF		
E1	0.400	0.700	0.100
F	0.250BSC		
F1	2°	4°	6°