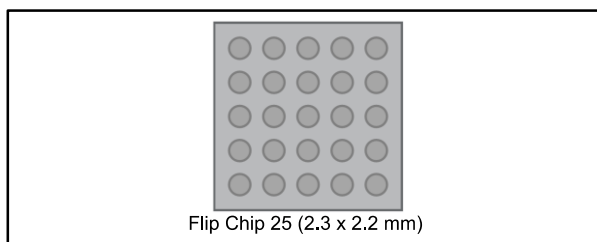


## Switch mode single cell Li+ battery charger with OTG boost, voltage mode fuel gauge and LDO

Datasheet - production data



- Interrupt output pin
- Flip Chip package, 25 bumps (2.3 x 2.2 mm)

### Applications

- Mobile phones
- Smart phones

### Description

The STBCFG01 is a switching battery charger integrating the necessary functions to charge single cell Li-Ion batteries, monitor the battery charge and generate 5 V to supply USB OTG bus powered devices.

The IC also integrates the LDO regulator to support system boot in dead battery conditions.

The battery charger features a smart input current limit: the maximum input current can be selected through I<sup>2</sup>C and if the input voltage drops below a programmable threshold, the input current is reduced even if the selected maximum current limit has not been reached yet. The dynamic input current limit can be disabled.

An automatic input pre-bias load makes the device suitable for applications using voltage sources with a minimum external load for the right regulation.

The STBCFG01 also integrates a voltage mode fuel gauge to provide the state of charge evaluation without the current sensing resistor.

### Features

- High efficiency switching battery charger
  - 2 MHz or 3 MHz switching frequency
  - 1.2 A max. charging current
  - 20 V tolerant input with OVP
  - Programmable input current limitation and dynamic input current limit
  - Battery overvoltage protection
  - Auto-recharge
  - Integrated current sensing resistor
  - USB compatible
- Voltage mode fuel gauge
  - External sensing resistor is not needed
  - Battery swap detection through ID resistor
  - Low battery voltage and low SOC programmable alarms
- 50 mA LDO for system boot in dead battery condition
- USB OTG V<sub>BUS</sub> generation (500 mA)
  - USB overvoltage protection
  - Programmable battery overcurrent protection
- Automatic 60 mA input pre-bias
- I<sup>2</sup>C compatible control interface

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# 1 Application schematic

Figure 1: STBCFG01 application schematic

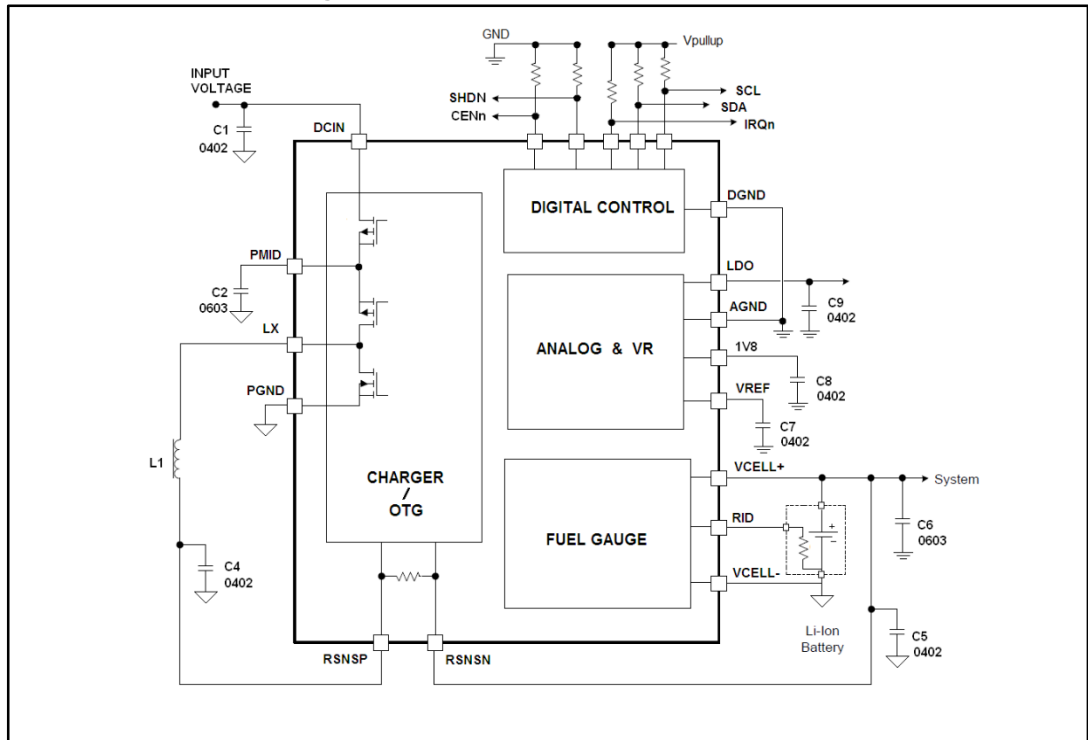


Table 1: Typical bill of material (BOM)

Component name	Size	Value	Supplier	Part number
C1	0603	10 $\mu$ F, 16 V	MURATA	GRM188R61C106MA73D
C2	0603	4.7 $\mu$ F, 25 V	TDK	C1608X5R1E475K080AC
C3	0402	1 $\mu$ F, 16 V	MURATA	GRM155R61C105KA12D
C4	0603	4.7 $\mu$ F, 25 V	TDK	C1608X5R1E475K080AC
C5	0603	1 $\mu$ F, 16 V	MURATA	GRM185R61C105KE44
C6	0603	10 $\mu$ F, 16 V	MURATA	GRM188R61C106MA73D
C7	0603	100 nF, 25 V	MURATA	GRM188R71H104KA93
C8	0603	1 $\mu$ F, 16 V	MURATA	GRM185R61C105KE44
C9	0603	1 $\mu$ F, 16 V	MURATA	GRM185R61C105KE44
L1	2.5 x 2.2 mm	1 $\mu$ H, 2.2 A	TDK	VLS252012ET-1R0N

## 2 Pin configuration

Figure 2: Pin connections (top view)

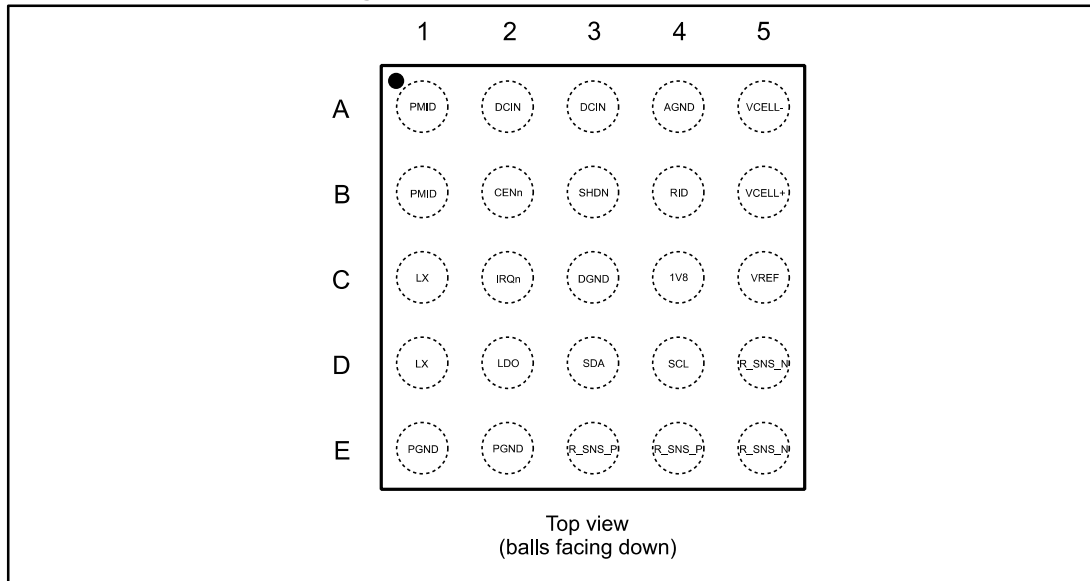


Table 2: Pin description

Symbol	Ball	Pin function	Description
PMID	A1, B1	Power I/O	Reverse blocking MOSFET to high-side connection node
DCIN	A2, A3	Power I/O	Input supply voltage/OTG output
AGND	A4	Analog ground	Analog ground
VCELL-	A5	Analog input	Battery pack negative terminal sense input
CENn	B2	Digital input	Charger enable, active low. Internal 200 kΩ pull-down to GND
SHDN	B3	Digital input	Shutdown input, active high. Internal 200 kΩ pull-down to GND
RID	B4	Analog input	Battery identification resistor connection (for battery detection). An external bias has to be applied
VCELL+	B5	Analog input	Battery pack positive terminal sense input
LX	C1, D1	Power I/O	Switch mode, inductor connection
IRQn	C2	Digital input	Open drain interrupt output, active low
DGND	C3	Digital ground	Digital ground
1V8	C4	Analog out	1.8 V internal regulator bypass pin. Bypass this pin to GND with a capacitor of 220 nF. Do not connect any load
VREF	C5	Analog out	Reference voltage bypass pin. Do not connect any load
LDO	D2	Analog out	4.85 V LDO output
SDA	D3	Digital I/O	I <sup>2</sup> C data pin to the baseband, I <sup>2</sup> C master peripheral
SCL	D4	Digital input	I <sup>2</sup> C clock pin to the baseband, I <sup>2</sup> C master peripheral
R_SNS_N	D5, E5	Power I/O	Internal sense resistor, negative terminal

Symbol	Ball	Pin function	Description
PGND	E1, E2	Power ground	Power ground
R_SNS_P	E3, E4	Power I/O	Internal sense resistor, positive terminal

### 3 Maximum ratings

**Table 3: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DCIN}$ , $V_{PMID}$	Charger input voltage	-1.5 to +20	V
$V_{LX}$	Switch mode voltage	-0.3 to +8	V
$V_{CELL+}$ , $R_{SNS\_N}$ , $R_{SNS\_P}$	Battery pin	-0.3 to +6	V
$V_{VREF}$ , $V_{V1V8}$ , $V_{CENn}$ , $V_{SHDN}$	Low voltage pins	-0.3 to +2.1	V
$V_{AMR}$	All other input voltage pins	-0.3 to +5.5	V
ESD	Human body model	$\pm 2000$	V
	Charged device model	$\pm 250$	V
$T_{AMB}$	Operating ambient temperature	-30 to +85	°C
$T_J$	Maximum junction temperature	+125	°C
$T_{STG}$	Storage temperature	-65 to +150	°C



Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

**Table 4: Thermal data**

Symbol	Parameter	Value	Unit
$R_{th(JC)}$	Thermal resistance junction-case	TBD	°C/W
$R_{th(JA)}$	Thermal resistance junction-ambient	TBD	°C/W



## 4 Electrical characteristics

$T_J = -30\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ,  $V_{BAT} = 3.6\text{ V}$ ,  $V_{DCIN} = 5\text{ V}$  unless otherwise specified.

**Table 5: Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
<b>General information</b>						
V <sub>IN</sub>	DCIN input voltage range		3.78		5.95	V
f <sub>sw</sub>	Switching frequency	FSW bit = 0		2		MHz
		FSW bit = 1		3		
T <sub>SD</sub>	Thermal shutdown threshold			165		°C
	Hysteresis			20		
t <sub>TSD</sub>	Thermal shutdown deglitch time			50		µs
<b>Battery charger</b>						
I <sub>IN</sub>	Current consumption from DCIN	Charger enabled, switching, V <sub>BUS_CON</sub> = 5 V		14		mA
		Shutdown, LDO disabled		290	400	µA
		Shutdown, LDO enabled		500	800	µA
I <sub>BAT</sub>	Current consumption from BAT(including fuel gauge)	On battery power V <sub>BUS_CON</sub> = 0 V GG_RUN = 0		10	25	µA
		On battery power V <sub>BUS_CON</sub> = 0 V GG_RUN = 1		32	100	µA
V <sub>INOVP</sub>	DCIN overvoltage protection	V <sub>DCIN</sub> rising	6.05	6.3	6.62	V
		V <sub>DCIN</sub> falling	5.95	6.2	6.51	
V <sub>INOVP_PB</sub>	Pre-bias overvoltage protection	V <sub>DCIN</sub> rising		7.0		V
		V <sub>DCIN</sub> falling		6.9		V
	Pre-bias OVP accuracy		-5		+5	%
V <sub>INUVLO</sub>	DCIN undervoltage lockout	V <sub>DCIN</sub> rising		3.6		V
		V <sub>DCIN</sub> falling		3.5		
	DCIN UVLO accuracy		-5		+5	%
I <sub>PREB</sub>	Pre-bias current			60		mA
t <sub>PBD</sub>	Pre-bias current enable deglitch time	V <sub>DCIN</sub> rising over V <sub>INOVP</sub> but below V <sub>INOVP_PB</sub>		5		ms
t <sub>HDO</sub>	Hold-off time	Valid DCIN connection to charging start		200		ms

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>ASD</sub>	Automatic shutdown threshold	V <sub>ASD</sub> = V <sub>DCIN</sub> -V <sub>BAT</sub> , V <sub>DCIN</sub> rising		130		mV
		V <sub>ASD</sub> = V <sub>DCIN</sub> -V <sub>BAT</sub> , V <sub>DCIN</sub> falling	0	36		mV
t <sub>ASD</sub>	Automatic shutdown threshold deglitch time			50		μs
I <sub>INLIM</sub>	D <sub>CIN</sub> current limit	I <sub>LIM</sub> configurable by I <sup>2</sup> C		90		mA
				476		
				760		
				1140		
V <sub>DICL</sub>	Dynamic input current limit threshold	DICL configurable by I <sup>2</sup> C (4.0 V, 4.25 V, 4.5 V, 4.75 V)	4.0		4.75	V
	DICL accuracy		-3		+3	%
t <sub>DICL</sub>	DICL activation deglitch time			100		ms
V <sub>FLOAT</sub>	CV regulation voltage	V <sub>BUS_CON</sub> = 5 V	3.52		4.78	V
	CV regulation voltage accuracy	V <sub>BUS_CON</sub> = 5 V	-1		+1	%
V <sub>FLD</sub>	CC to CV threshold deglitch time			170		ms
V <sub>RCHG</sub>	Auto-recharge threshold voltage	ARCHG bit = 1		V <sub>FLOAT</sub> -0.12		V
	Auto-recharge threshold accuracy	ARCHG bit = 1	-17		+17	%
t <sub>RCHG</sub>	Auto-recharge threshold deglitch time	ARCHG bit = 1		170		ms
V <sub>BATOVP</sub>	Battery overvoltage protection	This is got by increasing the battery voltage until BATOVP status register turns on		V <sub>FLOAT</sub> +0.1		V
	Battery OVP accuracy		-10		+10	%
t <sub>BOVP</sub>	Battery OVP deglitch time			170		ms
I <sub>TRK</sub>	Trickle charge current	V <sub>BAT</sub> <V <sub>TRK</sub>		45		mA
	Trickle charge current accuracy		-20		+20	%
I <sub>PRE</sub>	Pre-charge current	V <sub>TRK</sub> < V <sub>BAT</sub> <V <sub>PRE</sub>		450		mA
	Pre-charge current accuracy		-10		+10	%
I <sub>FAST</sub>	Fast charge current	V <sub>BAT</sub> > V <sub>PRE</sub>	550		1250	mA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
	Fast charge current accuracy		-10		10	%
I <sub>TERM</sub>	Termination current		50		300	mA
	Termination current accuracy		-30		30	%
t <sub>TERM</sub>	Charge termination deglitch time			170		ms
V <sub>TRK</sub>	Trickle charge to pre-charge battery voltage threshold			2		V
	V <sub>TRK</sub> accuracy		-5		+5	%
t <sub>TPD</sub>	Trickle charge to pre-charge threshold deglitch time			100		ms
V <sub>PRE</sub>	Pre-charge to fast charge battery voltage threshold			3		V
	V <sub>PRE</sub> accuracy		-5		+5	%
t <sub>FPD</sub>	Pre-charge to fast charge threshold deglitch time			170		ms
V <sub>DETH</sub>	Battery detection high threshold			3		V
V <sub>DETL</sub>	Battery detection low threshold			2		V
I <sub>DETSNK</sub>	Sink detection current			-5		mA
t <sub>DETSRC</sub>	Current source detection time			340		ms
t <sub>DETSNK</sub>	Current sink detection time			200		ms
R <sub>ON_HI</sub>	High-side MOSFET on- resistance (including reverse blocking MOFET)			300		mΩ
R <sub>ON_LOW</sub>	Low-side MOSFET on- resistance			125		mΩ
R <sub>SNS</sub>	Internal sensing resistor			35	68	mΩ
t <sub>MAXPRE</sub>	Maximum pre-charge time	Including trickle charge		45		min.
t <sub>MAXCHG</sub>	Maximum fast charge time	Including taper charge		360		min.
<b>OTG boost regulator</b>						
I <sub>BQ</sub>	Boost quiescent current	V <sub>BAT</sub> = 3.7 V, no load		4		mA

Electrical characteristics

STBCFG01

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>BUS</sub>	Output voltage at V <sub>BUS_CON</sub>		4.75	5	5.25	V
I <sub>VBUS</sub>	Output current capability	V <sub>BUS</sub> ≥ 4.75 V	500			mA
V <sub>BATUVLO</sub>	Battery undervoltage lockout	Falling edge		3		V
	Accuracy		-5		+5	%
V <sub>BUSOVP</sub>	Output overvoltage protection			6		V
	Accuracy		-5		+5	%
t <sub>VBUSOVP</sub>	V <sub>BUSOVP</sub> deglitch time			30		ms
I <sub>BATLIM</sub>	Battery average current limitation		350		950	mA
	Accuracy		-10		+10	%
I <sub>LMAX</sub>	Cycle-by-cycle limitation			1.2		A
Z <sub>0</sub>	Output impedance in OFF mode		100			kΩ
<b>LDO output</b>						
V <sub>LDO</sub>	LDO output voltage	I <sub>LDO</sub> = 50 mA, V <sub>DCIN</sub> - V <sub>LDO</sub> > 300 mV		4.85		V
	Accuracy		-4		+4	%
I <sub>LDO</sub>	LDO output current	V <sub>DCIN</sub> - V <sub>LDO</sub> > 300 mV	50			mA
I <sub>SC</sub>	LDO short-circuit current	V <sub>LDO</sub> ≤ 4 V		75		mA
	Accuracy		-27		+27	%
V <sub>DO</sub>	LDO dropout voltage	I <sub>LDO</sub> = 50 mA		150	300	mV
V <sub>INMIN</sub>	LDO input undervoltage lockout	V <sub>DCIN</sub> rising		3.6		V
		V <sub>DCIN</sub> falling		3.5		V
	V <sub>INMIN</sub> accuracy		-5		+5	%
V <sub>INMAX</sub>	LDO input overvoltage lockout	V <sub>DCIN</sub> rising		6.3		V
		V <sub>DCIN</sub> falling		6.2		V
	V <sub>INMAX</sub> accuracy		-5		+5	%
<b>Fuel gauge</b>						
I <sub>FGQ</sub>	Fuel gauge quiescent current	GG_RUN = 1		25		μA
		GG_RUN = 0		2		
UVLO	Fuel gauge undervoltage lockout	Rising edge	2.0	2.6	2.7	V
	Hysteresis			100		mV
f <sub>OSC</sub>	Internal time base frequency			512		kHz
	Time base accuracy			1		%



Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>STRB</sub>	ADC conversion strobe			4		s
t <sub>SWAP</sub>	Battery swap deglitch time			1		s
V <sub>BATERR</sub>	V <sub>BAT</sub> measurement error		-0.5		+0.5	%
V <sub>BATRES</sub>	V <sub>BAT</sub> measurement resolution	OCV reading		2.69		mV
V <sub>BATRNG</sub>	V <sub>BAT</sub> measurement range		2.5		5.5	V
V <sub>RIDTH</sub>	RID threshold		1.2	1.25	1.3	V
	Hysteresis			0.130		V
<b>I<sup>2</sup>C compatible interface</b>						
V <sub>IH</sub>	High level input voltage		1.3			V
V <sub>IL</sub>	Low level input voltage				0.6	V
V <sub>OL</sub>	Low level output voltage at 10 mA sink current for open drain I/O				0.3	V
C <sub>IO</sub>	I/O pin capacitance				10	pF
f <sub>SCL</sub>	SCL clock frequency				400	kHz
t <sub>LOW</sub>	Minimum clock low period		1.3			μs
t <sub>HIGH</sub>	Minimum clock high period		600			ns
t <sub>F</sub>	SDA and SCL fall time				300	ns
t <sub>HOLD_STA</sub>	Start condition hold time		600			ns
t <sub>SU_STA</sub>	Start condition set-up time		600			ns
t <sub>SU_DAT</sub>	Data set-up time		100			ns
t <sub>HOLD_DAT</sub>	Data hold time		0			μs
t <sub>SU_STO</sub>	Stop condition set-up time		600			ns
t <sub>BUF</sub>	Minimum delay between operations		1.3			μs
<b>Digital interface</b>						
V <sub>IH</sub>	Input high threshold		1.3			V
V <sub>IL</sub>	Input low threshold				0.6	V
V <sub>OL</sub>	Output low threshold				0.3	V

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I <sub>IN_IO</sub>	I/O pin input current		-10		+10	μA



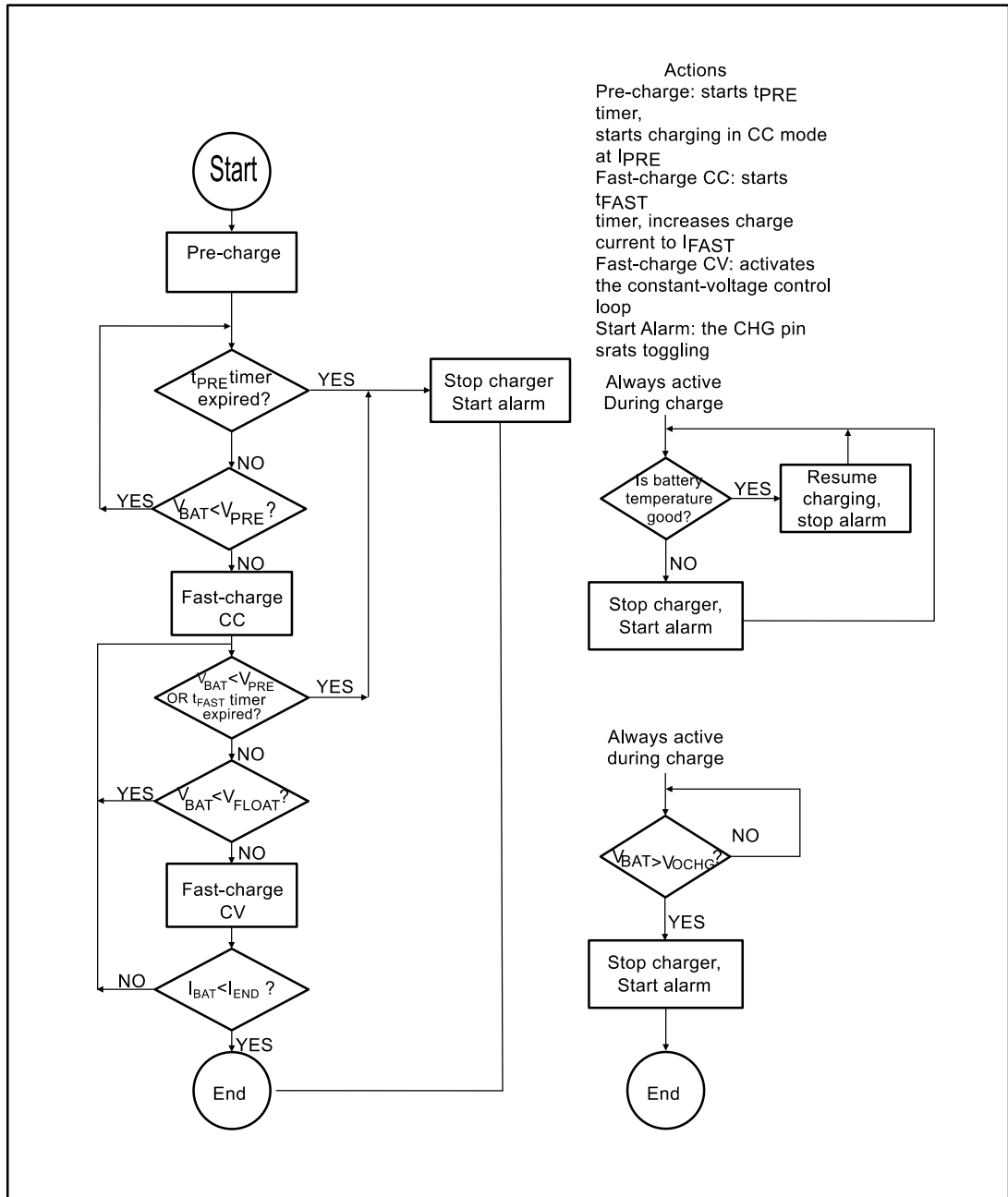
Dropout voltage is the input-to-output voltage difference at which the output voltage is 100 mV below its nominal value.

## 5 Operation description

### 5.1 Battery charger

The STBCFG01 integrates a high efficiency battery charger of 1.2 A implementing the CC/CV charging algorithm for single cell Li-Ion battery powered applications. The switching frequency can be either 2 MHz or 3 MHz, according to platform noise requirements, and the inductor value is 1  $\mu$ H. The charging current sensing resistor is integrated.

Figure 3: Simplified charger architecture



When the battery is deeply discharged ( $V_{CELL+} < V_{TRK}$ ,  $V_{TRK} = 2\text{ V}$ ) the device is in trickle charge mode and charges the battery in linear mode with a low current ( $I_{TRK} = 45\text{ mA}$ ) up to the trickle charge threshold.

As soon as the battery voltage enters the pre-charge range ( $V_{TRK} < V_{CELL+} < V_{PRE}$ ,  $V_{PRE} = 3\text{ V}$ ) the device starts the switch mode charging and increases the charging current up to the pre-charge current level ( $I_{PRE}$ ) to make the system voltage rise quickly up to a level which allows the system to wake up.

The typical value for the pre-charge current is 450 mA but this value can be decreased to 100 mA through the I<sup>2</sup>C compatible interface.

A 45 minute (typ.) safety timer is active during both trickle charge and pre-charge.

When the battery voltage is above the pre-charge threshold, the STBCFG01 enters fast charge mode and increases the charging current up to  $I_{FAST}$  value. The fast charge current can be programmed through the I<sup>2</sup>C compatible interface between 550 mA and 1.2 A in 100 mA steps.

A soft-start function makes the battery current increase smoothly when the charging current changes.

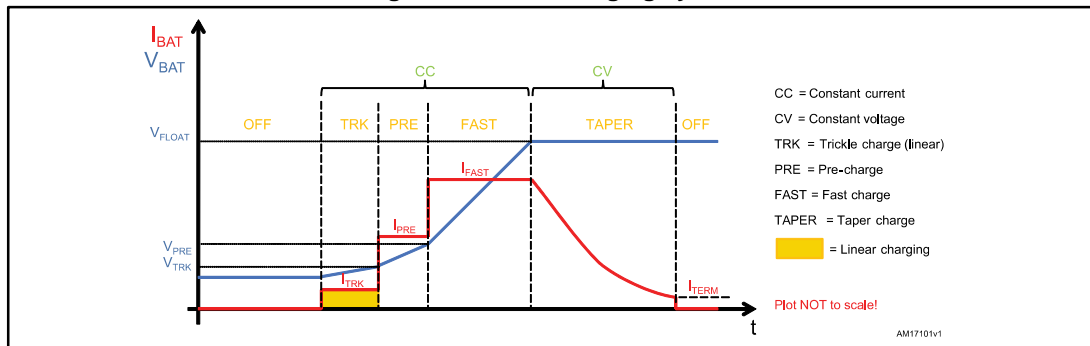
The constant voltage mode enters when the battery voltage reaches the programmable floating voltage threshold ( $V_{FLOAT}$ , 3.60 V to 4.70 V in 20 mV steps).

In constant voltage mode, the charging current tapers down the termination current threshold and then the charging process stops. The termination current is programmable from 50 mA to 300 mA in 25 mA steps.

A 360 minute (typ.) safety timer is active when the fast charge starts.

The charger can be disabled pulling high the charger enable input (CENn) and is automatically stopped in automatic shutdown conditions (ASD,  $V_{DCIN} - V_{BAT} < V_{ASD}$ ).

Figure 4: CC/CV charging cycle



### 5.1.1 Input current limit

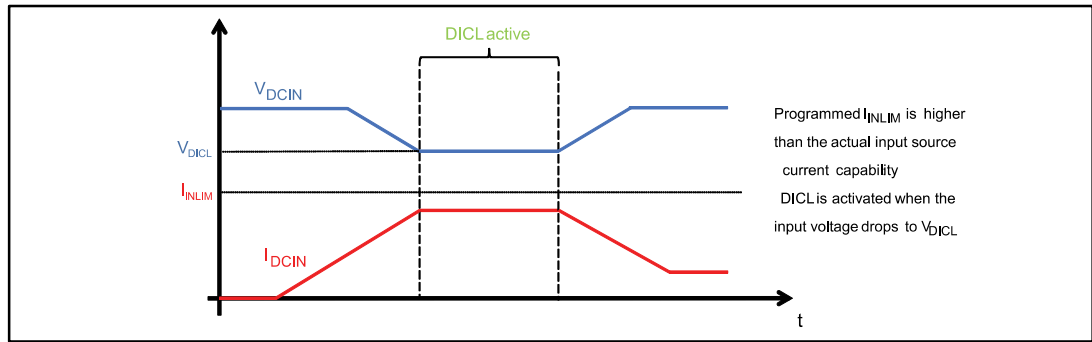
The STBCFG01 implements a programmable input current limitation to prevent the battery charger from exceeding DCIN voltage source current capability. The current limit can be programmed through I<sup>2</sup>C to the following maximum values: 100 mA, 500 mA, 800 mA, 1.2 A. A “no limit” option is also available.

### 5.1.2 Dynamic input current limit (DICL)

Independently from the chosen input current limit, a dynamic input current limit loop can also be enabled through the I<sup>2</sup>C compatible interface (DICL\_en bit). When DICL is active, an analog loop limits the input current when the input voltage drops to a programmable threshold ( $V_{DICL} = 4.0\text{ V}$  to 4.75 V in 250 mV steps).

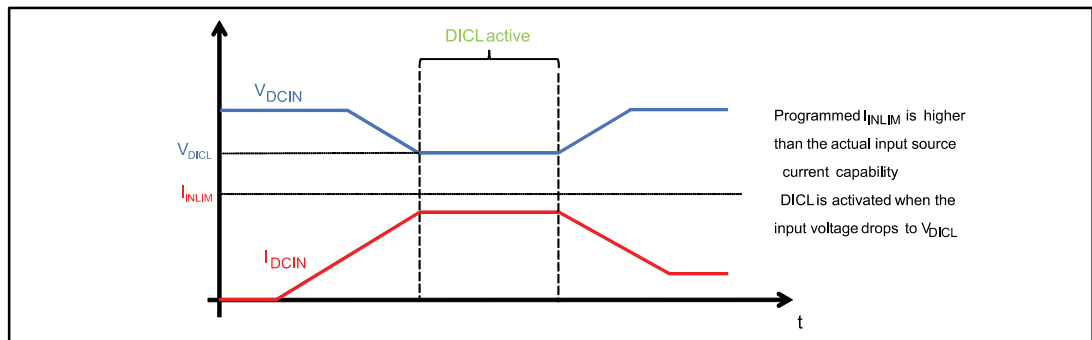


Figure 5: DICL activation



When a valid input source is connected to DCIN, DICL is enabled only if the input voltage is higher than  $V_{DICL}$  for a deglitch time ( $t_{DICL} = 100$  ms). The user can check the enabling status of DICL function reading DICL status bit. Once DICL is enabled it can be disabled through DICL\_en bit.

Figure 6: DICL enable strategy



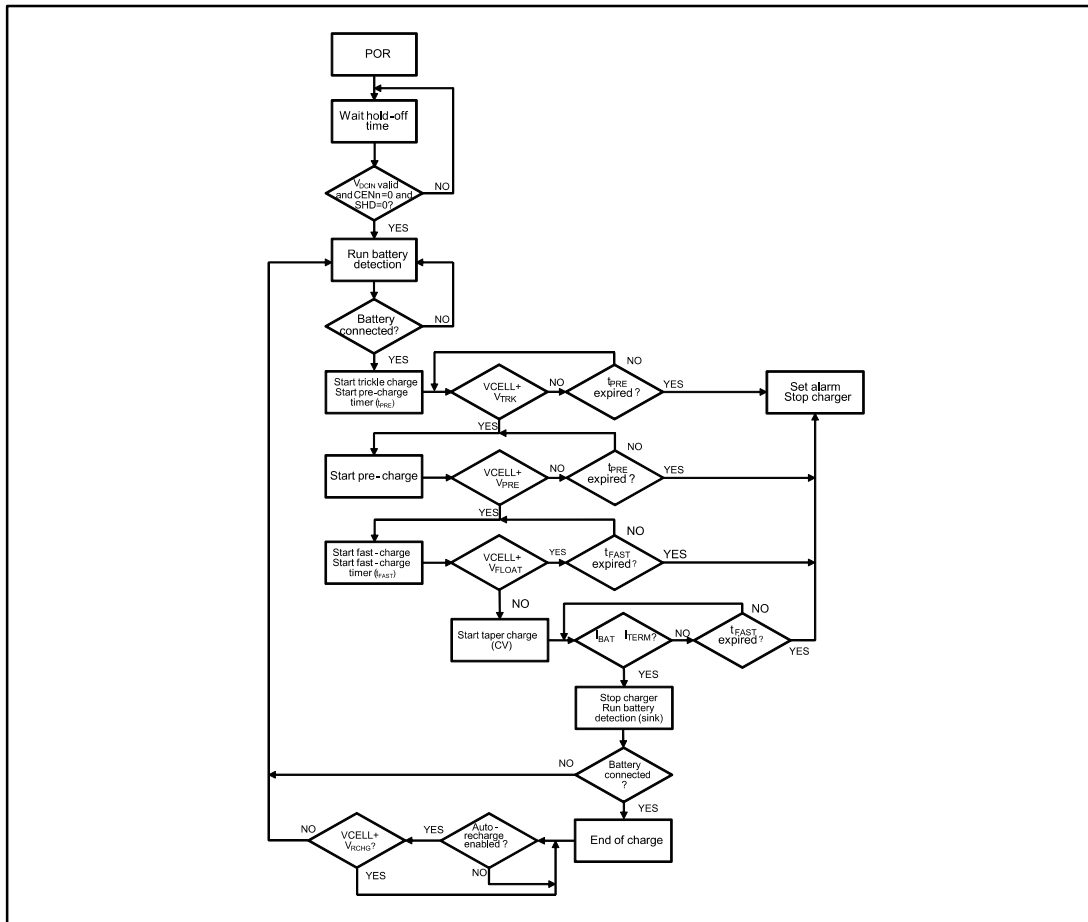
### 5.1.3 Automatic recharge

When the charging cycle is over, the device keeps monitoring the battery voltage: if the voltage drops below the auto-recharge threshold ( $V_{RCHG} = V_{FLOAT} - 120$  mV), a new charging cycle starts to keep the battery at maximum capacity. The automatic recharge function can be disabled through I<sup>2</sup>C.

### 5.1.4 Battery detection

The battery charger IC features a battery detection function to check if a battery is inserted before starting the charging cycle and to make sure that charging termination is not triggered because of a battery disconnection. If the battery is not detected when the input voltage is valid, the device keeps running the detection sequence until a battery is inserted. The battery detection result is reported by DET\_ok bit. If the battery detection function or RID comparator detects a battery disconnection, BAT\_Fail interrupt is generated. See the battery detection algorithm flowchart for more details.

Figure 7: Battery charger flowchart



### 5.1.5 Battery overvoltage protection

If the battery voltage exceeds the battery overvoltage protection threshold ( $V_{BATOVP} = V_{FLOAT} + 100\text{ mV}$ ) for more than  $t_{BOVP}$ , the charging cycle stops and an alarm is generated. The battery overvoltage protection is active only when the charger is enabled. The charger automatically restarts when the battery voltage falls below the battery overvoltage protection threshold.

### 5.2 OTG boost

The STBCFG01's internal bridge can be used in boost configuration to generate USB OTG  $V_{BUS}$  voltage (5 V, 500 mA).

OTG boost generator can be enabled setting the dedicated I<sup>2</sup>C enable bit (OTG\_en) according to the following conditions:

- $V_{DCIN} < V_{INUVLO}$
- CENn = high
- $V_{CELL+} > V_{BATUVLO}$

OTG boost operation is automatically stopped if the battery voltage falls below  $V_{BATUVLO}$  or if CENn is pulled low during operation.

The device also features an output overvoltage protection which turns off OTG boost if the output voltage rises above  $V_{BUSOVLP}$ . If the overvoltage lasts for more than  $t_{VBUSOVLP}$ , OTG boost is disabled and an alarm is generated.

Together with the standard cycle-by-cycle current limit for the inductor peak current, the STBCFG01 also implements an average battery current limitation to avoid excessive battery voltage drop during peaks in system current consumption. When the average boost input current reaches the programmed limit ( $I_{BATLIM} = 350\text{ mA}, 450\text{ mA}, 550\text{ mA}, 950\text{ mA}$ ), OTG boost is disabled and an alarm is generated.

### 5.3 LDO regulator

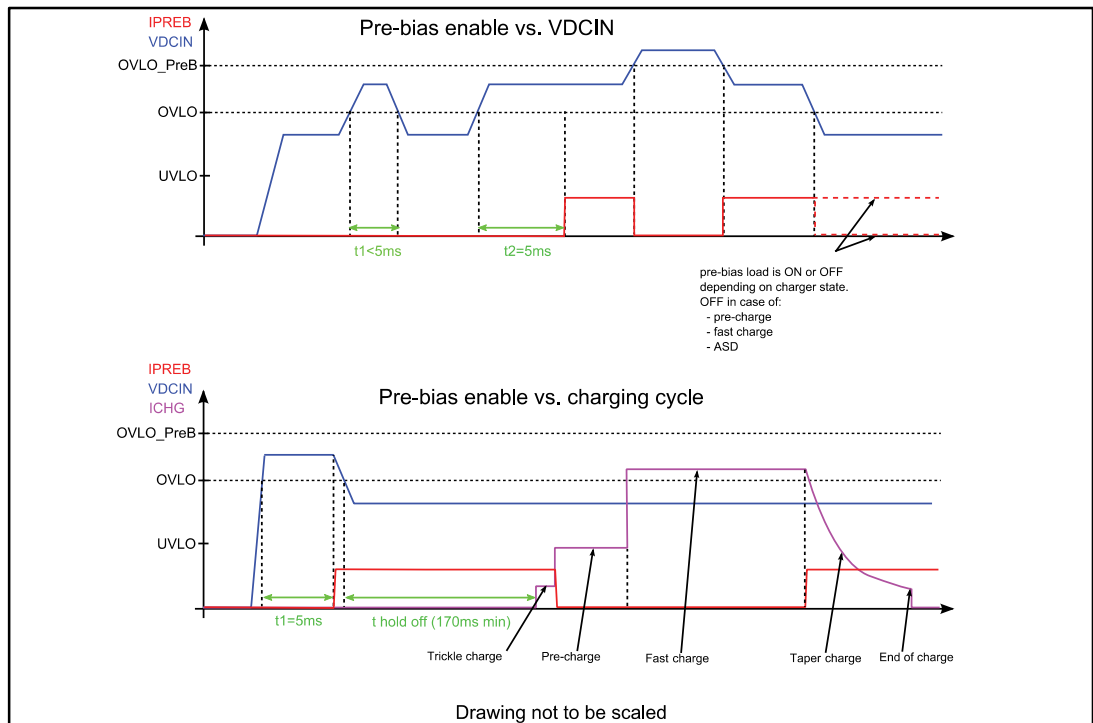
The STBCFG01 integrates a 4.85 V, 50 mA LDO regulator which is active when DCIN voltage is higher than  $V_{INMIN}$  and lower than  $V_{INMAX}$ . LDO is also active when the battery is not connected and in OTG mode, while it is turned off in automatic shutdown conditions ( $V_{DCIN} - V_{CELL+} < V_{ASD}$ ). LDO function can be disabled through I<sup>2</sup>C and its output is protected against short-circuit.

### 5.4 Pre-bias

In order to allow proper functionality with input sources not integrating the necessary minimum load to provide a valid voltage, the STBCFG01 integrates an automatic pre-bias circuit: if the input voltage ( $V_{DCIN}$ ) is above the input OVP threshold but lower than the pre-bias OVP threshold ( $V_{INOVP} < V_{DCIN} < V_{INOVP\_PB}$ ) a pre-bias current is applied to DCIN to attempt reducing the input voltage down to a valid level. During the charging cycle, if the pre-bias current has been activated, it is kept on only during trickle charge and taper charge. The pre-bias current is also turned off in automatic shutdown conditions (ASD).

The pre-bias current is active only if the input voltage is in the activation range for at least  $t_{PBD}$  (5 ms typ.). The pre-bias function can be disabled through I<sup>2</sup>C.

Figure 8: Pre-bias enable strategy



## 5.5 Fuel gauge

The voltage mode fuel gauge provides the accurate information about the state of the Lithium-Ion battery. Battery voltage is constantly monitored to evaluate the state of charge of battery and open circuit voltage.

At power-up, the fuel gauge algorithm uses the voltage reading to provide a first evaluation of SOC based on battery modeling data. The evolution of voltage is then used to track the changes of SOC of battery while cycling. The external software driver performs the temperature compensation.

Initial accuracy depends on the state of the battery. When the fuel gauge is active the battery is supposed to be in fully relaxed state. If the battery is not fully relaxed the initial error in the evaluation of the state of charge is high but converges to lower values while the battery is being used.

The fuel gauge block can be adapted to different batteries. Programmable parameters are used to tailor the algorithm to each battery model.

In order to keep the optimal performance and avoid losing information learned during battery cycling, the user is supposed to save data contained in the device's volatile memory when power is removed. The same data has to be restored at power-up.

The STBCFG01 also provides programmable alarms to notify low battery voltage and low SOC conditions.

### 5.5.1 Operating mode

At start-up and when the battery voltage is below UVLO threshold, the fuel gauge is in standby mode. This block is active when the battery voltage is above UVLO and GG\_RUN bit has been set through I<sup>2</sup>C. When the fuel gauge is in standby mode, all register values are frozen and the algorithm does not run. In active mode, a voltage reading is acquired every 4 seconds ( $t_{STRB}$ ).

### 5.5.2 Battery connection

When a battery is connected, the device wakes up and attempts reading the battery voltage before high current loads can change the open circuit voltage. The charging process is inhibited until the battery voltage reading is completed. If the battery voltage is too low, the charger is not inhibited to allow the battery to be charged up to a stable voltage and avoid oscillations.

### 5.5.3 Low battery alarm

The voltage mode fuel gauge provides low SOC and low battery voltage alarms, which are notified to the host through the active low open drain interrupt register (IRQn). Both of alarms can be disabled clearing ALRM\_en bit in FG\_Mode register.

Low battery voltage threshold and low SOC threshold can be changed writing ALARM\_Voltage and ALARM\_SOC registers. The default thresholds are 3.00 V battery voltage and 1% SOC.

When a low battery voltage condition or a low SOC condition is detected and alarms are enabled, the corresponding bit in FG\_CTRL register is set (ALRM\_VBAT or ALRM\_SOC) and IRQn output is pulled low.

ALRM\_VBAT and ALRM\_SOC bits have to be cleared by the host to release the interrupt pin (if no other interrupt is active in the device).

If the alarm is cleared while the alarm condition is still true, the device does not generate another interrupt: the alarm condition has to disappear and be detected again in order to generate another interrupt.

At power-up or when the fuel gauge is reset, fuel gauge alarms are enabled and alarms are generated after the first OCV reading and SOC estimation (if the alarm condition is true).

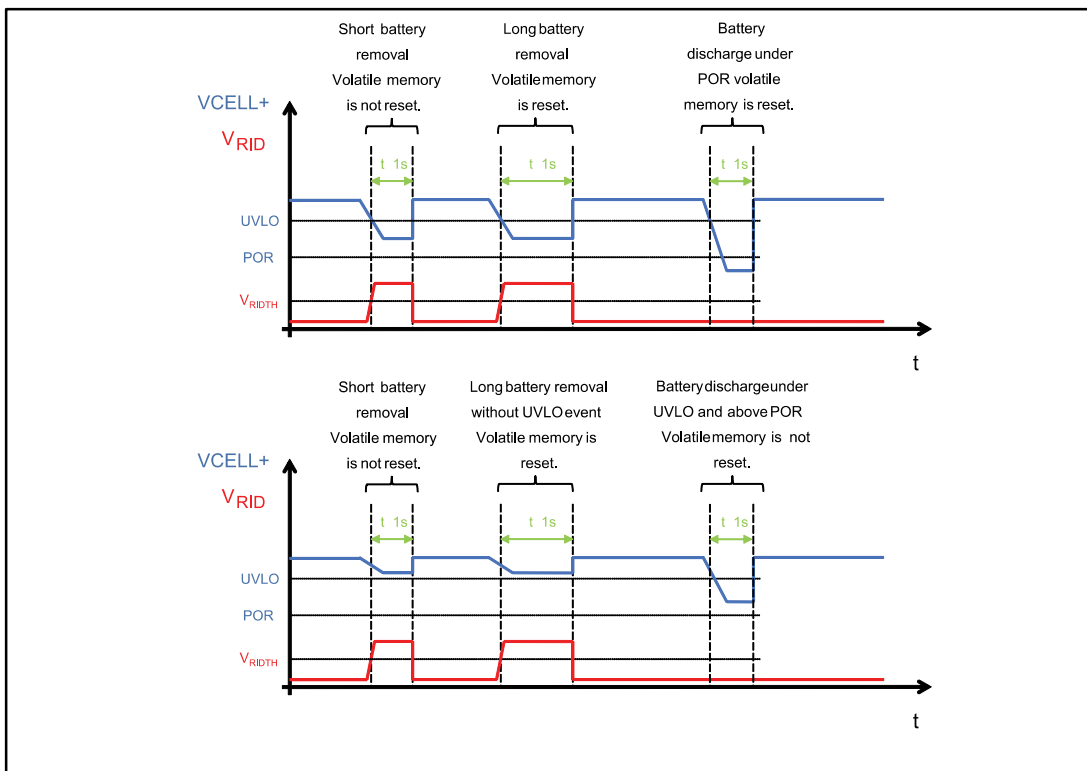
### 5.5.4 Battery swap

When the battery is removed from the system, the fuel gauge is reset to avoid providing wrong battery information if a different battery is inserted.

In order to detect battery disconnection, the STBCFG01 monitors both the battery voltage (VCELL+) and the voltage on RID pin connected to the battery identification resistor.

All volatile memory information is always lost when the battery voltage falls below POR threshold.

Figure 9: Battery swap detection



### 5.6 Thermal shutdown

In any working condition, if the die temperature reaches the thermal shutdown threshold ( $T_{SD} = 165\text{ °C typ.}$ ) the device enters shutdown mode: the bridge and LDO output turn off. The fuel gauge keeps working normally. The operation is automatically restored when the temperature falls back into the valid range. Safety timers are reset when a thermal shutdown is triggered.

## 5.7 Shutdown mode

When SHDN pin is tied high the device enters shutdown mode. In this mode, the switching converter turns off and it cannot be used neither in charging mode nor OTG boost mode. LDO and fuel gauge functionality are not affected by SHDN pin.

## 5.8 Watchdog

A watchdog timer function can be enabled to reset the programmable register values to power-on reset values if no I<sup>2</sup>C acknowledgments are generated for more than 45 seconds. This function is normally disabled.

## 5.9 Alarms

The STBCFG01 provides an open drain active low interrupt output (IRQn) to notify the application processor about abnormal operating conditions or generic events. The following register types check the status of alarms and control the device:

- Interrupt enable
- Interrupt latch

The interrupt enable registers enable the propagation of alarms to the interrupt pin (IRQn). The interrupt is generated (IRQn pulled low) on a rising edge of the interrupt latch bits (assuming that the corresponding enable bit has been set).

The interrupt latch registers show the alarm conditions, which generate the interrupt. Although the alarm condition is no longer active, once each latch register bit is set, it stays high until the register is updated. Interrupt latch registers are updated by writing 0 to their bits: if the alarm condition is still active the bit is kept to 1 (new interrupt is not generated); if the alarm condition is no more active the bit is cleared. This update method assures that no further rising edge on the latch bit is generated for alarms which have already been signaled before the update operation. In order to release IRQn line after an interrupt generated by the charger/OTG, the host processor has to write 0 to IRQ\_CLR bit in CHG\_Cfg2 register and then back 1. The fuel gauge generated alarms share the same enable bit (ALRM\_en).

The following conditions generate an interrupt signal:

- DCIN UVLO
- DCIN OVP
- ASD condition
- Pre-charge timer expiration
- Fast charge timer expiration
- Watchdog timer expiration
- Battery overvoltage protection (charger)
- End of charge
- Battery undervoltage lockout (OTG boost)
- V<sub>BUS</sub> overvoltage protection (OTG boost)
- Average current limit reached (OTG boost, I<sub>BATLIM</sub>)
- OTG output short-circuit; thermal shutdown
- Low battery voltage (fuel gauge)
- Low SOC (fuel gauge)

## 6 I<sup>2</sup>C compatible interface registers

The STBCFG01 can be monitored and controlled using the I<sup>2</sup>C compatible communication interface. The 7-bit device slave address is 1110001<sub>BIN</sub>. The table below shows the register map.

**Table 6: Register map**

Name	Address	POR value	R/W
<b>Fuel gauge</b>			
FG_Mode	00h	19h	R/W
FG_CTRL	01h	15h	R/W
SOC	02h-03h	0000h	R/W
VBAT	08h-09h	0000h	R
OCV	0Dh-0Eh	0000h	R
VM_CNF	11h-12h	0141h	R/W
ALARM_SOC	13h	02h	R/W
ALARM_Voltage	14h	AAh	R/W
REG_ID	18h	14h	R
RAM0...RAM15	20h...2Fh	-	R/W
OCV_ADJ	30h...3Fh	-	R/W
LUT	5Dh...8Ch	-	R/W
<b>Charger/OTG</b>			
CHG_Cfg1	90h	00h	R/W
CHG_Cfg2	91h	62h	R/W
CHG_Cfg3	92h	61h	R/W
CHG_Cfg4	93h	4Fh	R/W
CHG_Cfg5_OTG_Status	94h	06h	R/W
CHG_Status1	95h	00h	R
CHG_Status2	96h	C0h	R
Int_Enable_1	97h	00h	R/W
Int_Enable_2	98h	00h	R/W
Int_Latch_1	99h	00h	R/W
Int_Latch_2	9Ah	00h	R/W

## 6.1 Fuel gauge registers

**Table 7: Fuel gauge mode register (address: 00h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
-	OTG_en	LPM_dis	GG_RUN	ALRM_en	-	-	-	19h	R/W

ALRM\_en: fuel gauge alarm enable

- 0: disabled
- 1: enabled (default)

GG\_RUN: fuel gauge operative mode

- 0: standby (default). Registers are frozen, fuel gauge in standby
- 1: running

LPM\_dis: low power mode disable (set this bit to program battery charger/OTG configuration registers and enable OTG function when USB input is not plugged and GG\_RUN = 0)

- 0: low power mode enabled (default)
- 1: low power mode disabled

OTG\_en: OTG boost enable bit

- 0: disabled (default)
- 1: enabled

**Table 8: FG\_CTRL register (address: 01h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
-	ALRM_VBAT	ALRM_SOC	POR_Det	BAT_Fail	-		IODATA	15h	R/W

IODATA: IRQn pin status

Read:

- 0: IRQn pin is low
- 1: IRQn pin is high

Write:

- 0: forces IRQn pin low
- 1: IRQn pin is driven by interrupt logic

BAT\_Fail: battery removal or battery UVLO detection bit. Write 0 to clear

- 0: battery connected
- 1: battery removed or UVLO

POR\_Det: power-on reset detection bit. Write 1 to force a soft reset (self-clearing)

- 0: no POR event occurred
- 1: POR event occurred

ALRM\_SOC: low SOC alarm

- 0: SOC OK
- 1: low SOC





Write this bit to 0 to clear the alarm. If the alarm condition is still active a new alarm is triggered only on the following rising edge of the alarm condition (the alarm condition has to disappear and then appear again).

ALRM\_VBAT: low battery voltage alarm

- 0: battery voltage above threshold
- 1: low battery voltage



Write this bit to 0 to clear the alarm. If the alarm condition is still active a new alarm is triggered only on the following rising edge of the alarm condition (the alarm condition has to disappear and then appear again).

**Table 9: SOC register LSB (register address: 02h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
SOC[7:0]								00h	R/W

**Table 10: SOC register MSB (register address: 03h)**

b15	B14	b13	b12	b11	b10	b9	b8	POR	R/W
SOC[15:8]								00h	R/W

SOC register LSb: 1/512% SOC

**Table 11: VBAT register LSB (register address: 08h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
VBAT[7:0]								00h	R

**Table 12: VBAT register MSB (register address: 09h)**

b15	B14	b13	b12	b11	b10	b9	b8	POR	R/W
Reserved					VBAT[10:8]			00h	R

VBAT register LSb: 2.69 mV

**Table 13: OCV register LSB (register address: 0Dh)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
OCV[7:0]								00h	R

**Table 14: OCV register MSB (register address: 0Eh)**

b15	B14	b13	b12	b11	b10	b9	b8	POR	R/W
Reserved			OCV[12:8]					00h	R

OCV register LSb: 0.67 mV

**Table 15: VM\_CNF register LSB (register address: 11h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
VM_CNF[7:0]								41h	R/W

**Table 16: ALARM\_SOC register (address: 13h)**

b15	B14	b13	b12	b11	b10	b9	b8	POR	R/W
VM_CNF[15:8]								01h	R

ALARM\_SOC register LSb: 0.5%

**Table 17: ALARM\_Voltage register (address: 14h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
ALARM_Voltage								AAh	R/W

ALARM\_Voltage register LSb: 21.49 mV

## 6.2 Charger/OTG/LDO registers

**Table 18: CHG\_Cfg1 register**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
ITERM				IPRE	ifast			40h	R/W

IFAST: fast charge current

- Offset: 550 mA
- LSb: 100 mA
- Range: 550 mA to 1250 mA
- Default: 550 mA (000)

IPRE: pre-charge current

- 0: 450 mA (default)
- 1: 100 mA

ITERM: termination current

- Offset: 50 mA
- LSb: 25 mA

Range: 50 mA to 300 mA

- Default: 150 mA (0100)
- Values 1011 through 1111: reserved

**Table 19: CHG\_Cfg2 register (address: 91h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
IRQ_CLR	ARCHG	VFLOAT						C0h	R/W

VFLOAT: floating voltage

- Offset: 3.52 V
- LSb: 20 mV
- Range: 3.52 V to 4.78 V

- Default: 3.52 V (000000)
- ARCHG: automatic recharge enable
- 0: disabled
  - 1: enabled (default)
- IRQ\_CLR: clear interrupt latch
- 0: clear interrupt latch
  - 1: propagate interrupt (default)

Table 20: CHG\_Cfg3 register (address: 92h)

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
IBATLIM		VDICL		DICL_en		lin_lim		61h	R/W

lin\_lim: input current limit (DCIN)

- 000: max.100 mA
- 001: max.
- 500 mA (default)
- 010: max. 800 mA
- 011: max. 1.2 A
- 100: no limit
- Values 101 through 111: reserved

DICL\_en: dynamic input current limit enable

- 0: disabled (default)
- 1: enabled

VDICL: dynamic input current limit threshold

- 00: 4.00 V
- 01: 4.25 V
- 10: 4.50 V (default)
- 11: 4.75 V

IBATLIM: OTG average battery current limit

- 00: 350 mA
- 01: 450 mA (default)
- 10: 550 mA
- 11: 950 mA

**Table 21: CHG\_Cfg4 register format (register address: 93h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
RID_STAT	LDO_en	LDO_UVLO_th	WD	PreB_en	THRML	TFAST	TPRE	4Fh	R/W

TPRE: pre-charge timer enable

- 0: disabled
- 1: enabled (default)

TFAST: fast charge timer enable

- 0: disabled
- 1: enabled (default)

THRML: thermal loop enable (this bit can be masked through OTP)

- 0: disabled
- 1: enabled (default)

PreB\_en: pre-bias function enable

- 0: disabled
- 1: enabled (default)

WD: watchdog timer function enable

- 0: disabled (default)
- 1: enabled

LDO\_UVLO\_th: LDO UVLO threshold

- 0: 3.6 V rising, 3.5 V falling (default)
- 1: 4.75 V rising, 4.65 V falling

LDO\_en: LDO output enable

- 0: LDO output disabled
- 1: LDO output enabled (default)

RID\_STAT: RID status (read only)

- 0: RID connected
- 1: RID disconnected

**Table 22: CHG\_Cfg5\_OTG\_Status register format (register address: 94h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
BST_SH	BST_status			-	DICHG_adj	FSW	CHG_rst	06h	R/W



b0, b1, b2 are R/W; b4, b5, b6, b7 are read status bit only.

CHG\_rst: charger reset, all charger registers to POR value. Self-clearing.

- 0: no action (default)
- 1: reset charger

FSW: switching frequency. The switching frequency can be changed only when the device doesn't switch. SHDN input should be pulled high before modifying this setting.

- 0: 2 MHz
- 1: 3 MHz (default)

DICHG\_adj: dynamic charging current adjustment enable (for soft-current transitions)

- 0: disabled
- 1: enabled (default)

BST\_status: OTG boost status

- 000: idle
- 001: wait soft-start
- 010: linear soft-start
- 011: switching soft-start
- 100: frequency ramp-up
- 101: OTG\_run
- 110: PMOS-off
- 111: shutdown

BST\_SH: OTG boost output short at beginning

- 0: no short detected (default)
- 1: short detected

**Table 23: CHG\_Status1 register format (register address: 95h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
CHG_status					PreB_st	PreB	Alarm	00h	R

Alarm: alarm state

- 0: no alarm is active
- 1: alarm condition detected

PreB: pre-bias current activation

- 0: pre-bias current has not been activated
- 1: pre-bias current has been activated ( $V_{INOVP} < V_{DCIN} < V_{INOVP\_PB}$  for more than  $t_{PB D}$ )

PreB\_st: pre-bias current sink status

- 0: pre-bias current sink is currently off
- 1: pre-bias current sink is currently on

CHG\_status: charger status

- 00000: idle
- 00001: trickle charge
- 00010: pre-charge
- 00011: fast charge
- 00100: taper charge (constant voltage)
- 00101: charge done (termination)
- 00110: boost on
- 00111: shutdown
- 01000: battery detection running

**Table 24: CHG\_Status2 register format (register address: 96h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
-	-	-	-	-	DET_ok	DET_run	DICL	C0h	R

DICL: dynamic input current limit activation

- 0: not active
- 1: active

DET\_run: charger battery detection status

- 0: battery detection does not run
- 1: battery detection runs

DET\_Fail: charger battery detection result

- 0: battery connected
- 1: battery not connected

**Table 25: Int\_Enable\_1 register format (register address: 97h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
EOC	Bat_OVP	WD	Fast_TMR	Pre_TMR	ASD	IN_OVP	IN_UVLO	00h	R

For all bits

- Write 1 to propagate the event to IRQn
- Write 0 to mask the event (default)

IN\_UVLO: charger input voltage UVLO

IN\_OVP: charger input voltage OVP

ASD: automatic shutdown condition

Pre\_TMR: pre-charge timer expiration

Fast\_TMR: fast charge timer expiration

WD: watchdog timer expiration

Bat\_OVP: battery overvoltage protection

EOC: end-of-charge (termination current reached)

**Table 26: Int\_Enable\_2 register format (register address: 98h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
BAT_Fail	CHG_ON	-	OTG_short	Ibat_Lim	VBus_OVP	TSHDN	Bat_UVLO	00h	R/W

For all bits:

- Write 1 to propagate the event to IRQn
- Write 0 to mask the event (default)

Bat\_UVLO: battery UVLO (OTG)

TSHDN: thermal shutdown

VBus\_OVP: OTG boost output OVP

Ibat\_Lim: OTG battery average current limit

OTG\_short: OTG output short-circuit

CHG\_ON: charging started

BAT\_Fail: battery fail

**Table 27: Int\_Latch\_1 register format (register address: 99h)**

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
EOC	Bat_OVP	WD	Fast_TMR	Pre_TMR	ASD	IN_OVP	IN_UVLO	00h	R/W



This register is cleared upon read operation.

IN\_UVLO: charger input voltage UVLO

- 0: charger input voltage is above UVLO
- 1: charger input voltage is below UVLO

IN\_OVP: charger input voltage OVP

- 0: charger input voltage is below OVP
- 1: charger input voltage is above OVP

ASD: automatic shutdown condition

- 0: charger input voltage above the automatic shutdown threshold
- 1: charger input voltage below the automatic shutdown threshold

Pre\_TMR: pre-charge timer expiration (has to be cleared by the host)

- 0: pre-charge timer running
- 1: pre-charge timer expired

Fast\_TMR: fast charge timer expiration (has to be cleared by the host)

- 0: fast charge timer running
- 1: fast charge timer expired

WD: watchdog timer expiration (has to be cleared by the host)

- 0: watchdog timer running
- 1: watchdog timer expired

Bat\_OVP: battery overvoltage protection

- 0: battery voltage below OVP threshold during charging
- 1: battery voltage above OVP threshold during charging

EOC: end-of-charge (termination current reached)

- 0: termination current not reached
- 1: termination current reached

Table 28: Int\_Latch\_2 register format (register address: 9Ah)

b7	b6	b5	b4	b3	b2	b1	b0	POR	R/W
BAT_Fail	CHG_ON	TSHDN_LDO	OTG_short	lbat_Lim	VBus_OVP	TSHDN	Bat_UVLO	00h	R/W



Write 0 to update these register bits.

Bat\_UVLO: battery UVLO (OTG)

- 0: battery voltage above UVLO threshold during boost operation
- 1: battery voltage below UVLO threshold during boost operation

TSHDN: thermal shutdown

- 0: device in normal operation conditions
- 1: device in thermal shutdown

VBus\_OVP: OTG boost output OVP

- 0: OTG boost output voltage below OVP threshold
- 1: OTG boost output voltage above OVP threshold

lbat\_Lim: OTG battery average current limit (has to be cleared by the host)

- 0: average battery current limit not reached during OTG boost operation
- 1: average battery current limit reached during OTG boost operation

OTG\_short: OTG output short-circuit

- 0: OTG output short-circuit condition not detected
- 1: OTG output short-circuit condition detected

TSHDN\_LDO: LDO thermal shutdown

- 0: LDO in normal operation conditions
- 1: LDO in thermal shutdown

CHG\_ON: charger cycle start

- 0: charging cycle not active
- 1: charging cycle started

BAT\_Fail: battery status (from state machine or RID)

- 0: battery connected/good battery
- 1: battery disconnected/not good



## 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 7.1 Flip Chip 25 (2.3x2.2 mm) option H package information

Figure 10: Flip Chip 25 (2.3x2.2 mm) option H package outline

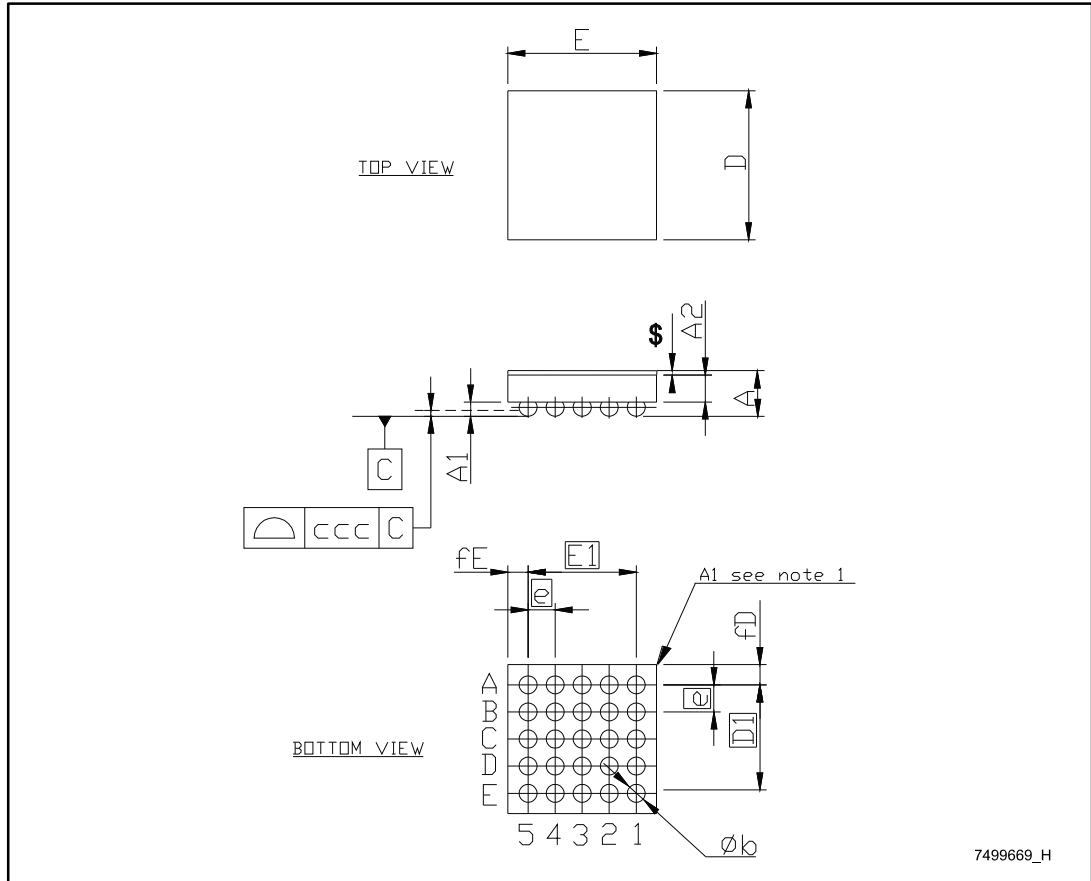
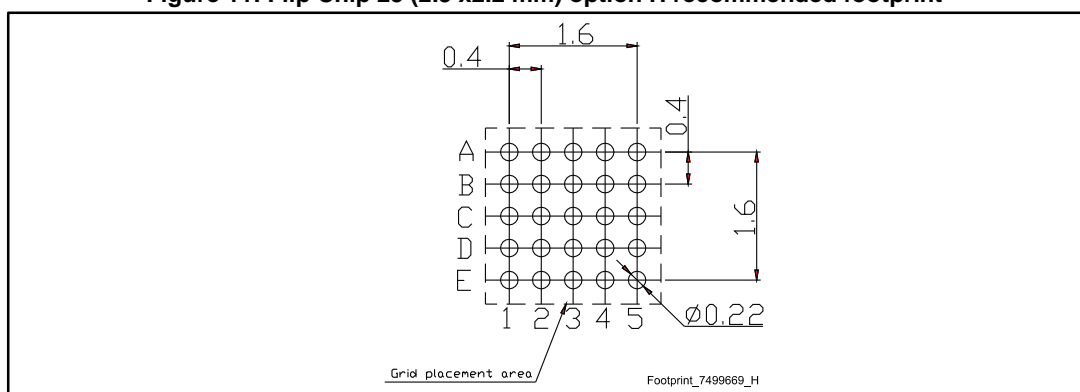


Table 29: Flip Chip 25 (2.3 x 2.2 mm) option H package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.495	0.55	0.605
A1	0.17	0.20	0.23
A2	0.275	0.30	0.325
b	0.23	0.26	0.29
D	2.25	2.28	2.31
D1		1.6	
E	2.16	2.19	2.22
E1		1.6	
e		0.4	
fD	0.33	0.34	0.35
fE	0.285	0.295	0.305
ccc		0.075	
\$		0.05	

Figure 11: Flip Chip 25 (2.3 x 2.2 mm) option H recommended footprint



## 8 Ordering information

**Table 30: Ordering information**

Order code	Package	Packing
STBCFG01JR	Flip Chip 25 (2.3 x 2.2 mm)	Tape and reel

## 9 Revision history

Table 31: Document revision history

Date	Revision	Changes
10-Jun-2014	1	Initial release.
09-Dec-2014	2	Added the table titled "Typical external components".
28-Apr-2016	3	Modified <a href="#">Table 10: "SOC register MSB (register address: 03h)"</a> .

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