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U_A-Headers
A-Headers.SchDoc



U_Analog
Analog.SchDoc



U_DDR3-RAM
DDR3-RAM.SchDoc



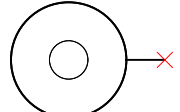
U_USB-PHY
USB-PHY.SchDoc



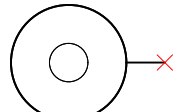
U_PowerSupply
PowerSupply.SchDoc



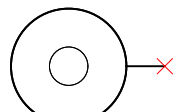
U_FTDI
FTDI.SchDoc



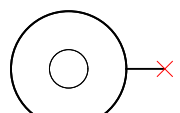
Mount.Hole 3.2mm (unplated)



Mount.Hole 3.2mm (unplated)



Mount.Hole 3.2mm (unplated)



Mount.Hole 3.2mm (unplated)

A

A

B

B

U_FPGA_B34
FPGA_B34.SchDoc



U_FPGA_B35
FPGA_B35.SchDoc



U_FPGA_MIO
FPGA_MIO.SchDoc



U_FPGA_RAM
FPGA_RAM.SchDoc

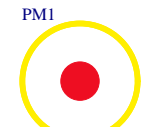


U_FPGA_PWR
FPGA_PWR.SchDoc



C

C



FIDU-DOT - small



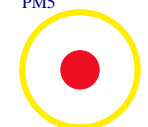
FIDU-DOT - small



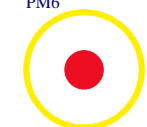
FIDU-DOT - small



FIDU-DOT - small



FIDU-DOT - small



FIDU-DOT - small

D

D

LOGO1
TE Logo PRINT Layer

LOGO PRINT

Serial
Serial
Serialnumber 6,3 x 6.3mm



S/N
Serialnumber



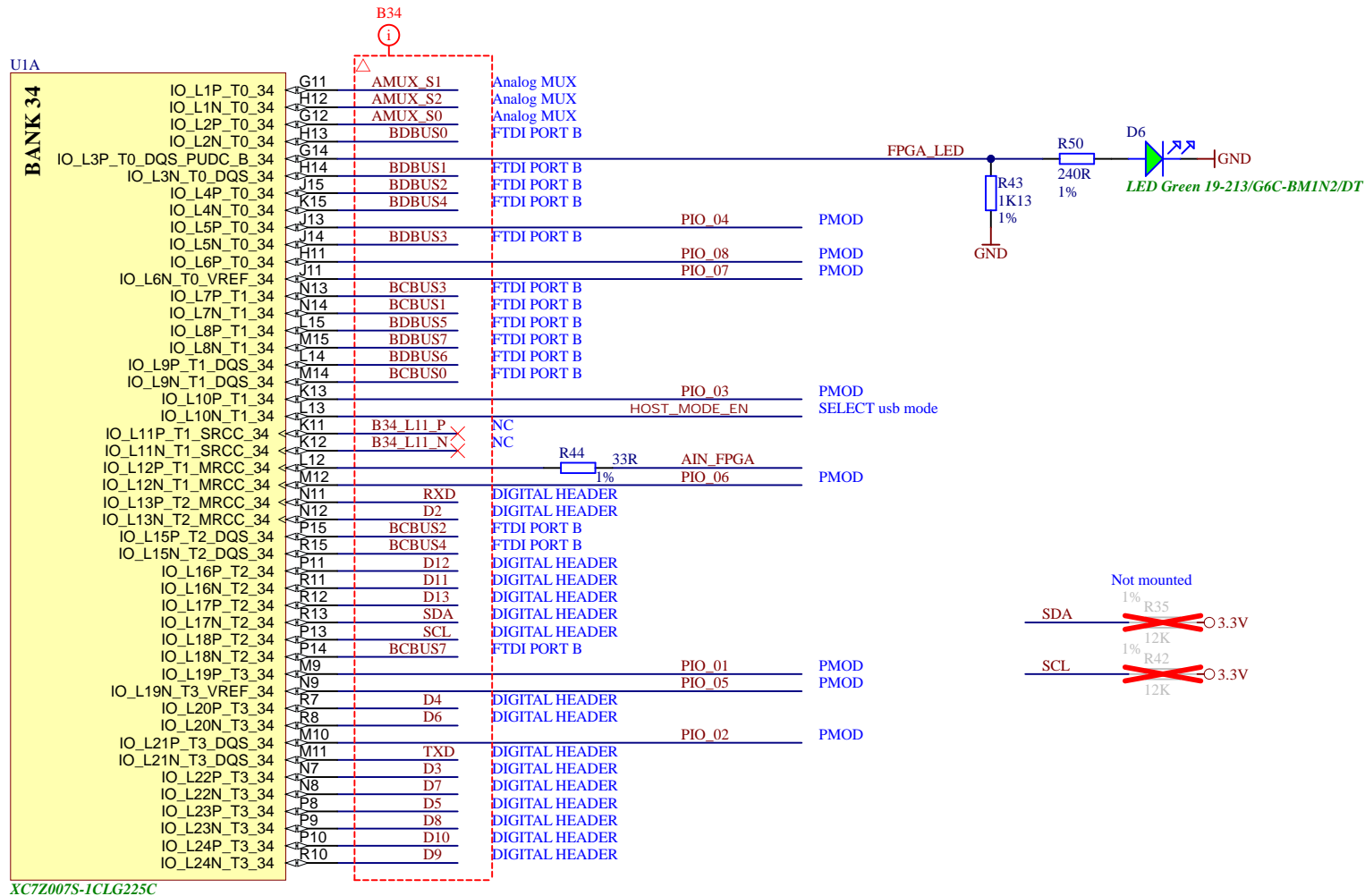

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A4	Number: TE0723 11C64-A	Rev. 03
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Filename: TE0723.SchDoc		

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Title: TE0723 - FPGA B34		
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Filename: FPGA_B34.SchDoc		

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A

A

B

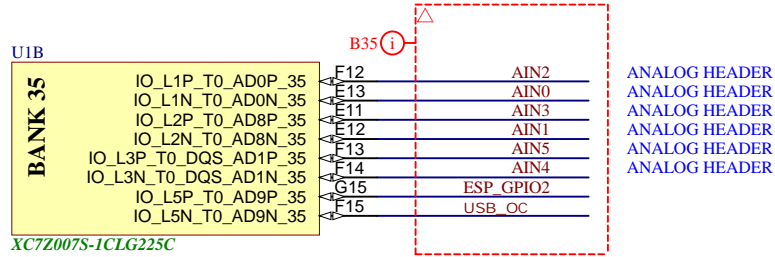
B


C

C

D

D



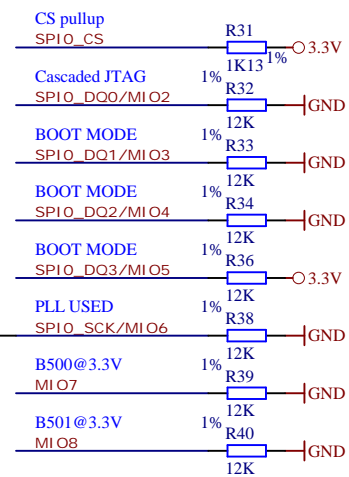
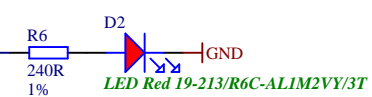
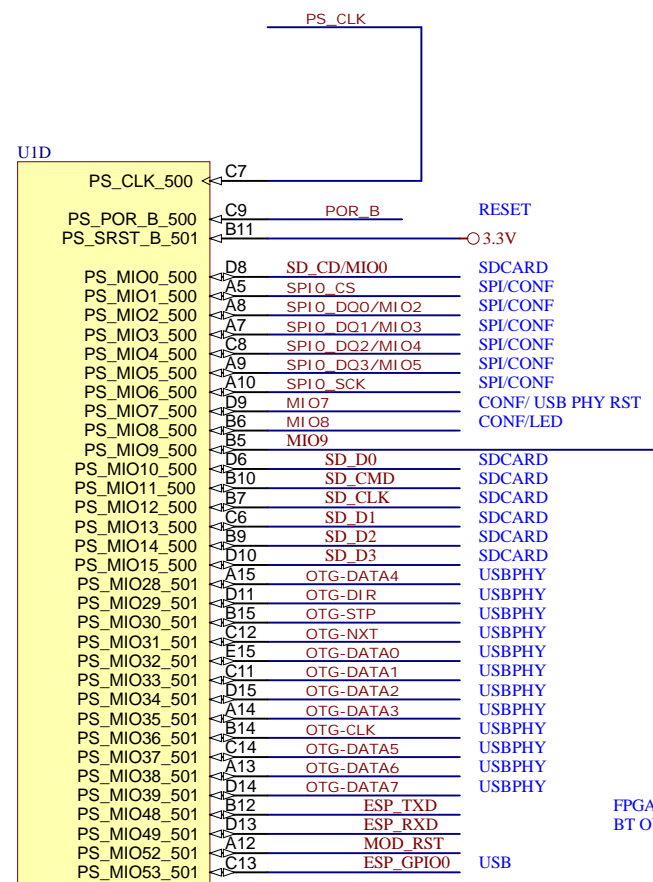
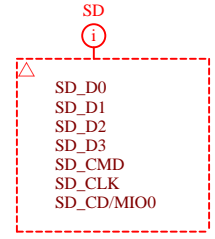
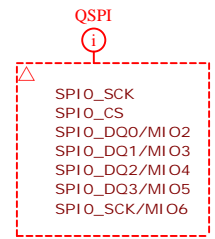
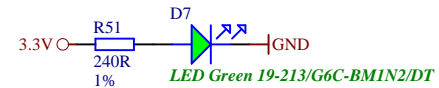
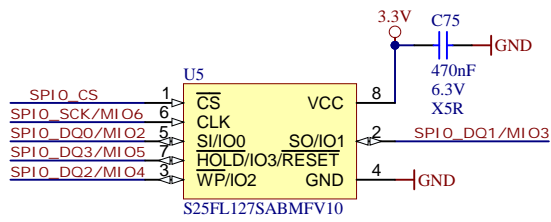
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	A4	Number: TE0723 11C64-A	Rev. 03
	Date: 2016-07-15	Copyright: Trenz Electronic GmbH	Page 3 of 13
	Filename: FPGA_B35.SchDoc		

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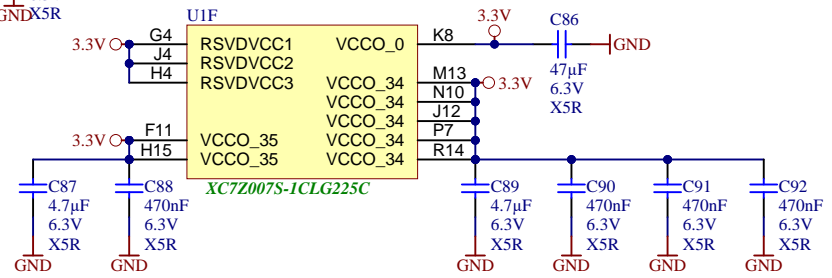
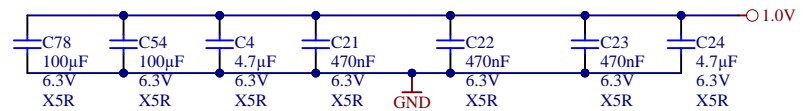
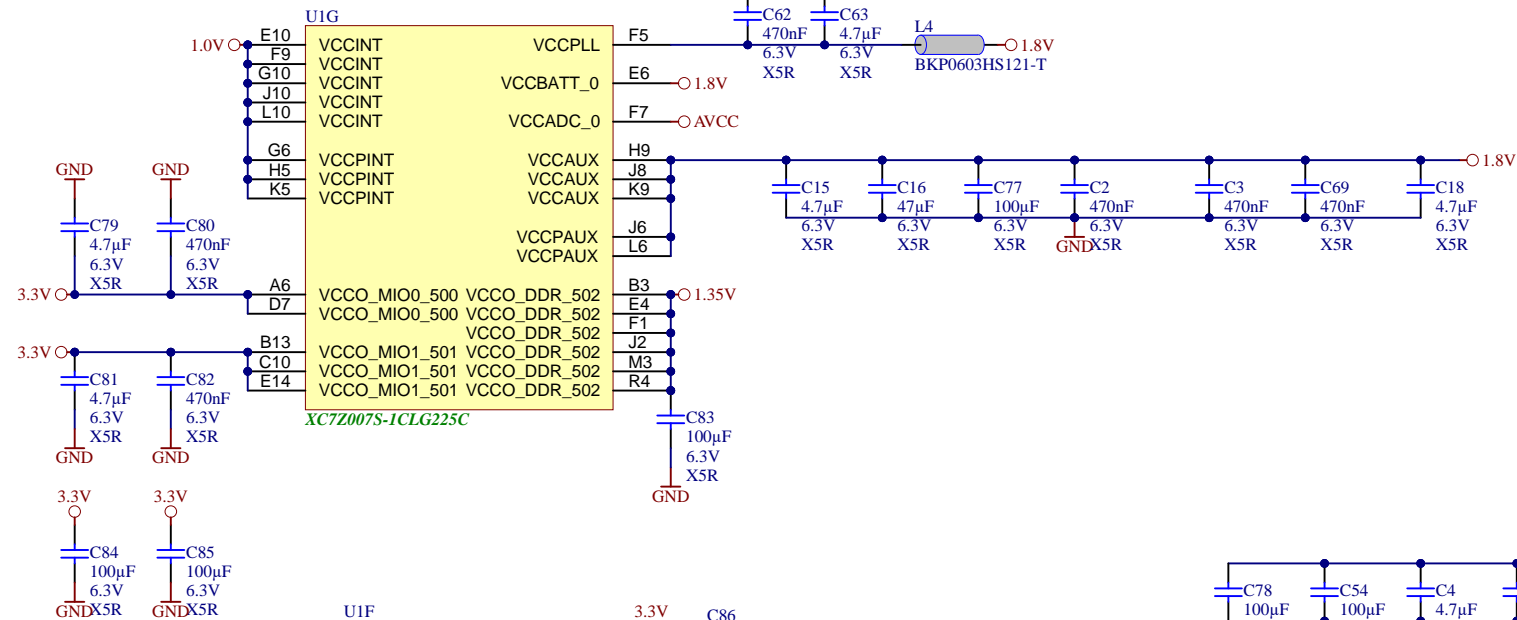
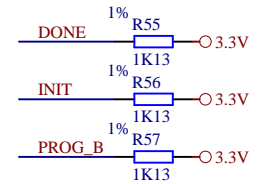
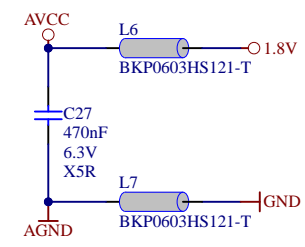
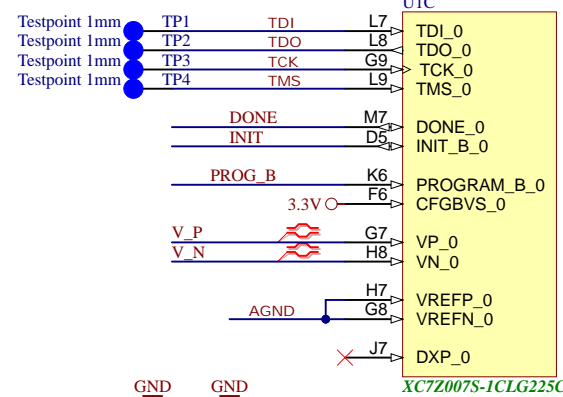
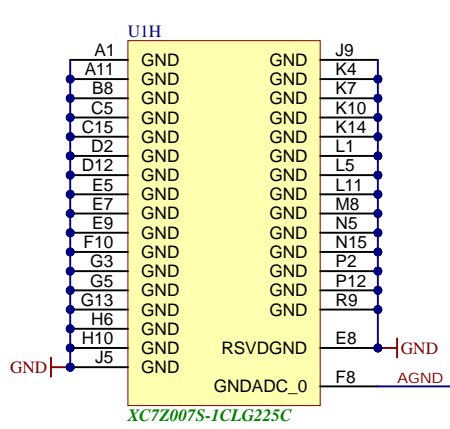


FPGA OUT -> BT IN
BT OUT -> FPGA IN

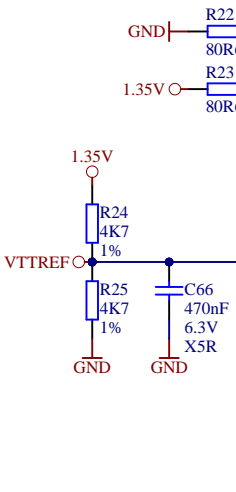
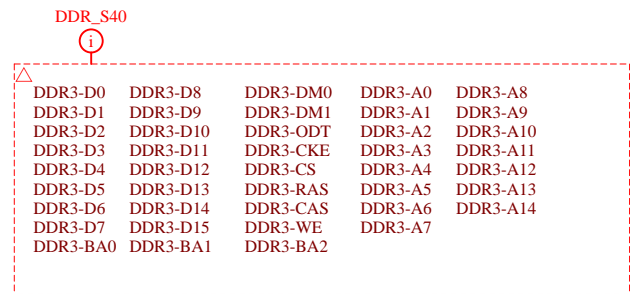
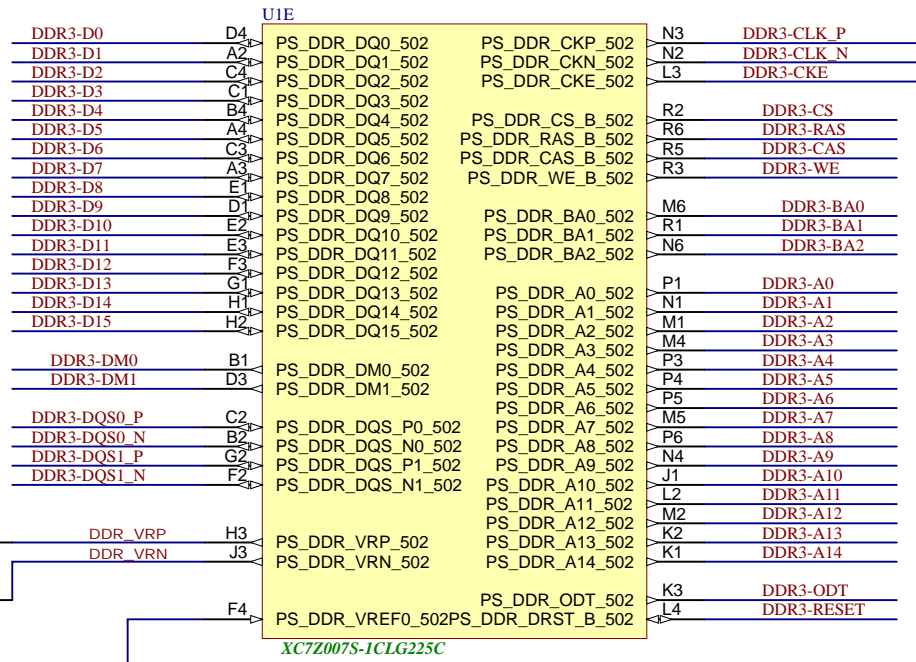


Title: TE0723 - FPGA MIO		
A4	Number: TE0723 11C64-A	Rev. 03
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Filename: FPGA_MIO.SchDoc		

XC7Z007S-1CLG225C



Title: TE0723 - FPGA PWR		
A4	Number: TE0723 11C64-A	Rev. 03
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Filename: FPGA_PWR.SchDoc		

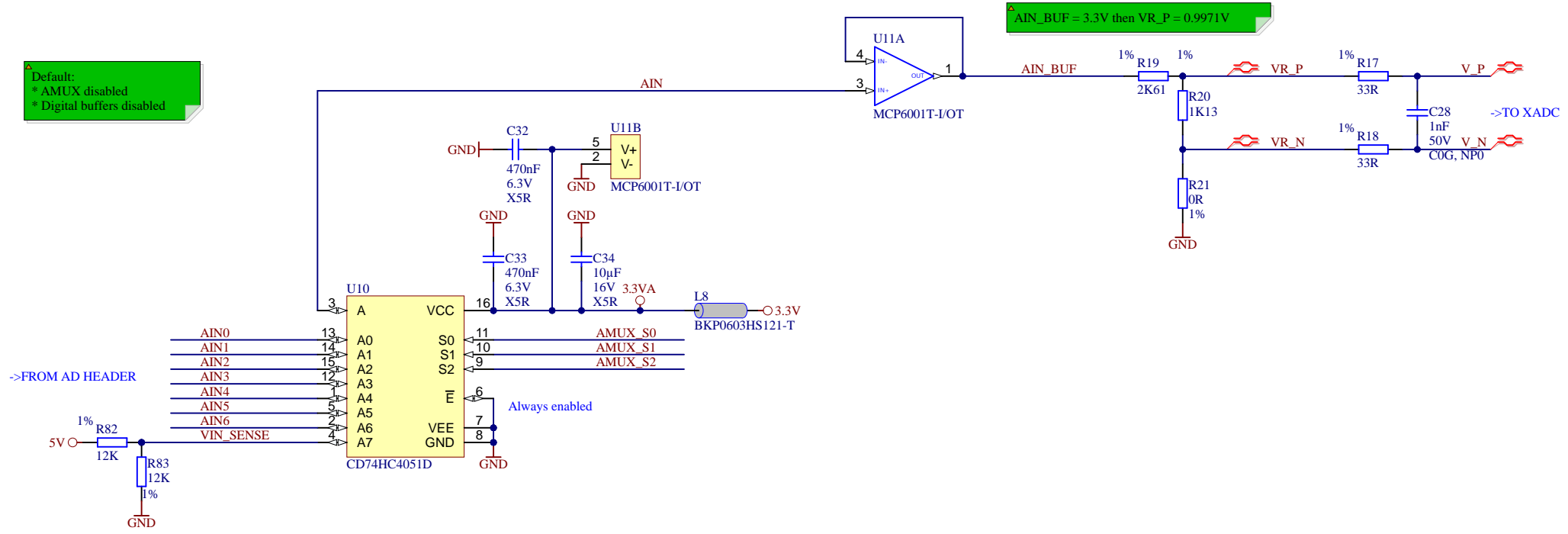


		Title: TE0723 - FPGA RAM	
		A4	Number: TE0723 11C64-A
Date: 2016-07-15		Copyright: Trenz Electronic GmbH	
Filename: FPGA_RAM.SchDoc		Page 6 of 13	

Default:
 * AMUX disabled
 * Digital buffers disabled

AIN_BUF = 3.3V then VR_P = 0.9971V

->FROM AD HEADER



	Title: TE0723 - Analog Input		
	A4	Number: TE0723 11C64-A	Rev. 03
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	Filename: Analog.SchDoc		

A

A

B

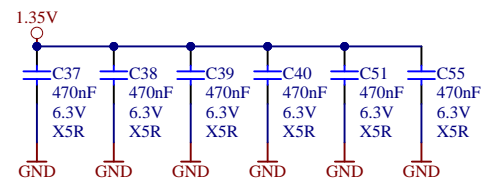
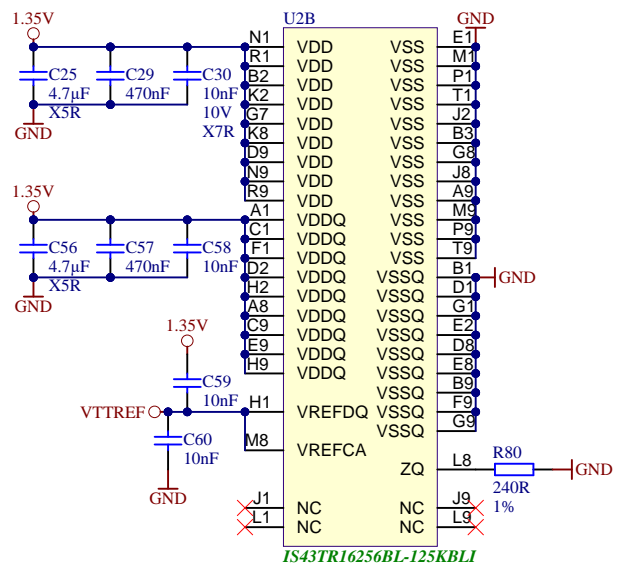
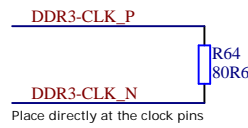
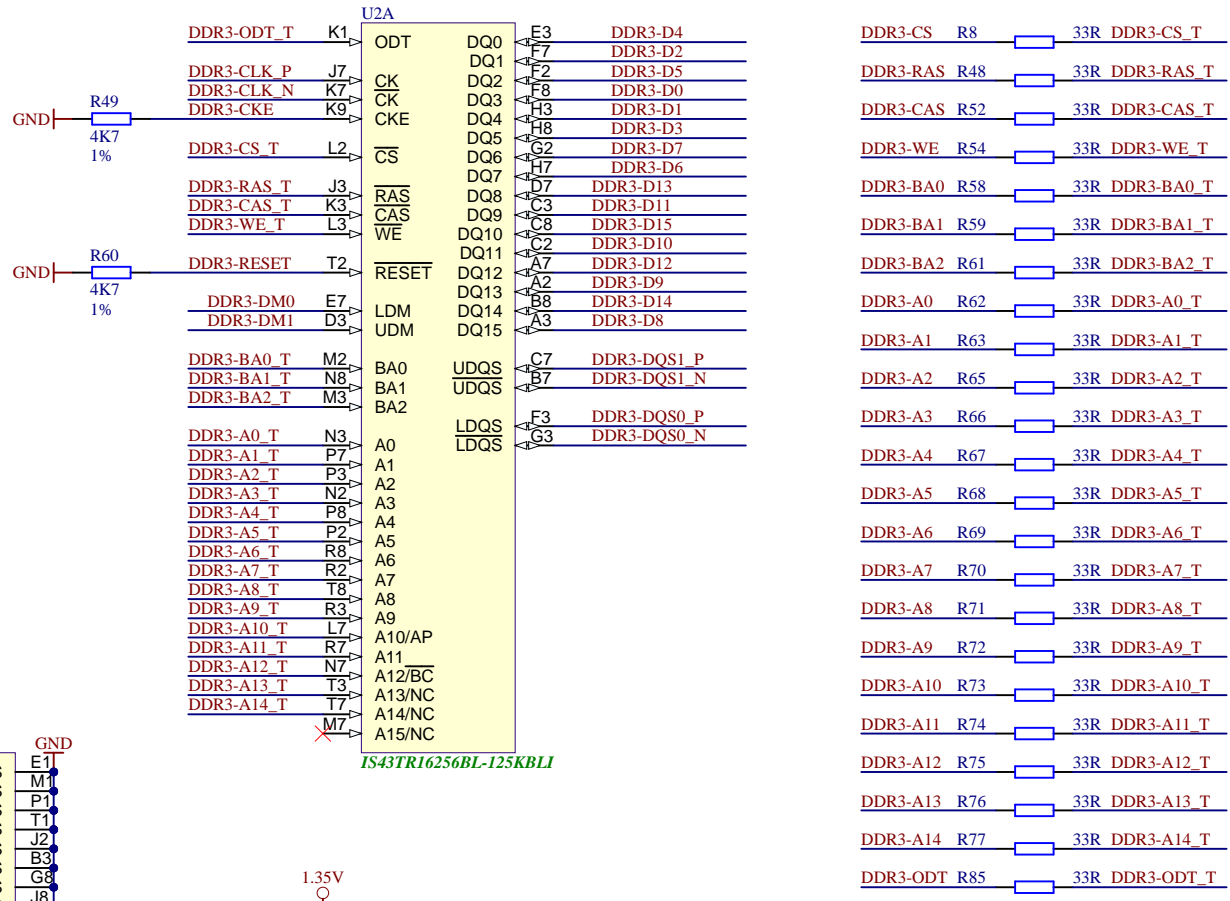
B

C

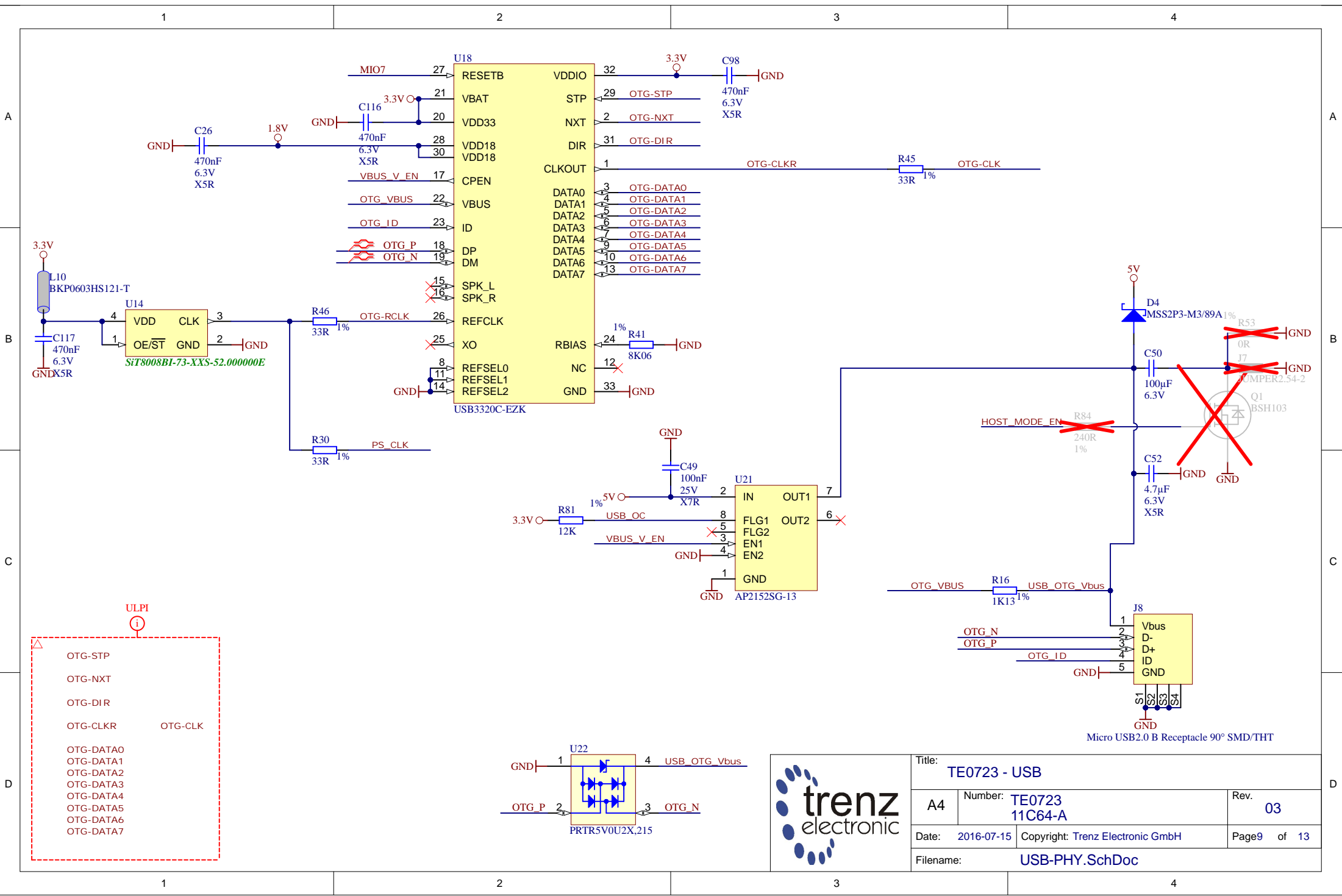
C

D

D



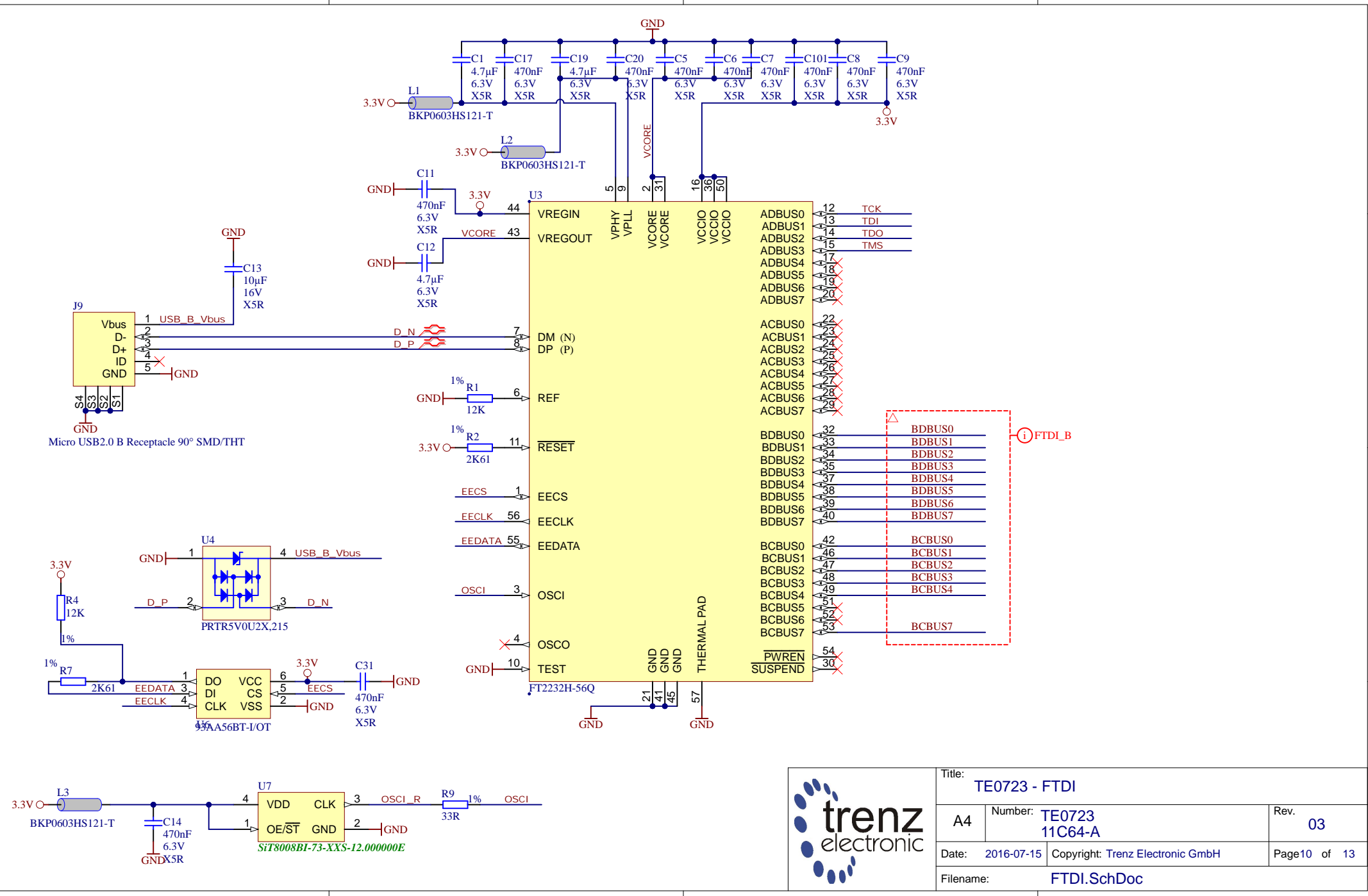
Title: TE0723 - DDR Memory		
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Date: 2016-07-15	Copyright: Trenz Electronic GmbH	Page8 of 13
Filename: DDR3-RAM.SchDoc		



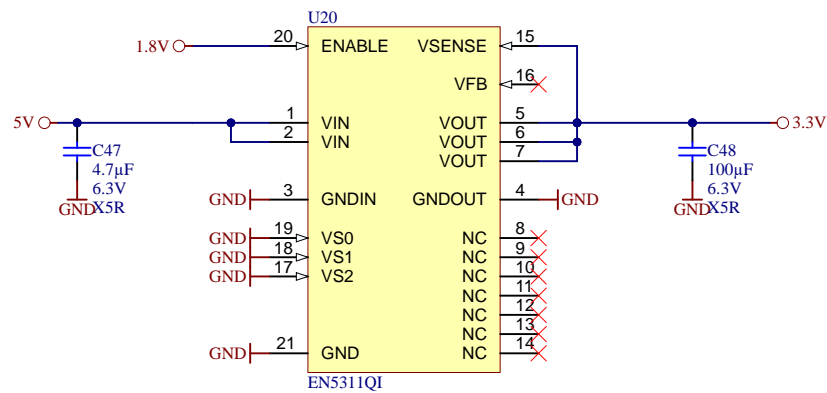
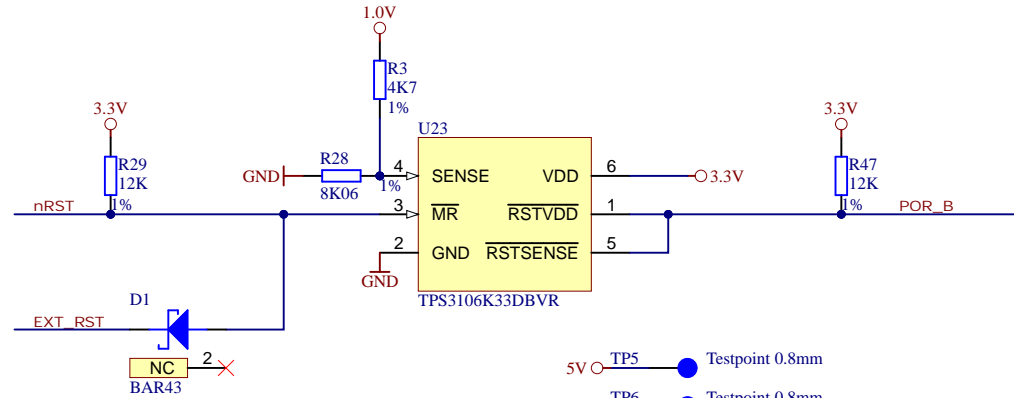
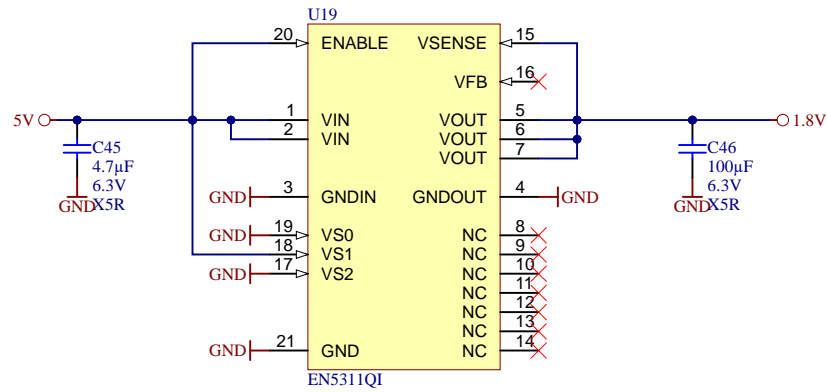
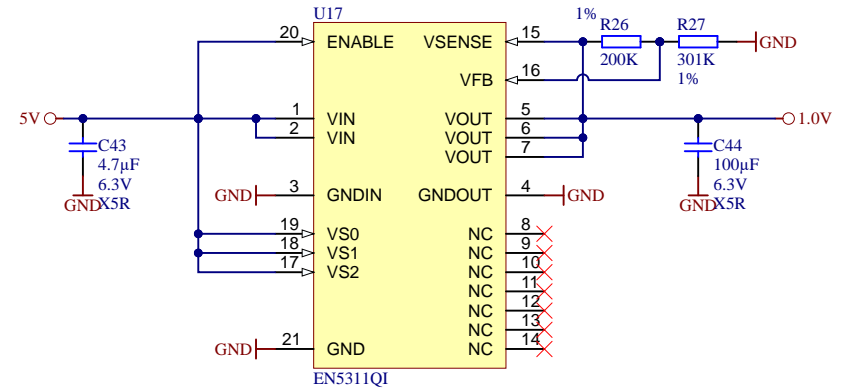
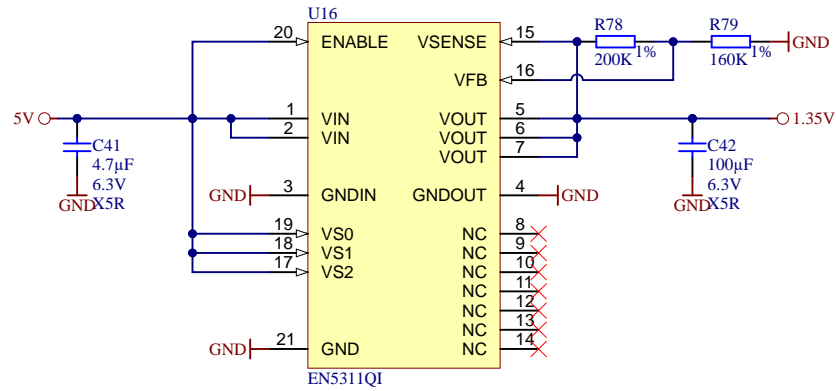
- ULPI
- OTG-STP
 - OTG-NXT
 - OTG-DIR
 - OTG-CLKR
 - OTG-CLK
 - OTG-DATA0
 - OTG-DATA1
 - OTG-DATA2
 - OTG-DATA3
 - OTG-DATA4
 - OTG-DATA5
 - OTG-DATA6
 - OTG-DATA7



Title: TE0723 - USB		
A4	Number: TE0723 11C64-A	Rev. 03
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Filename: USB-PHY.SchDoc		



Title: TE0723 - FTDI		
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Filename: FTDI.SchDoc		



- 5V ○ TP5 ● Testpoint 0.8mm
- 3.3V ○ TP6 ● Testpoint 0.8mm
- 1.8V ○ TP7 ● Testpoint 0.8mm
- 1.35V ○ TP8 ● Testpoint 0.8mm
- 1.0V ○ TP9 ● Testpoint 0.8mm
- GND | TP10 ● Testpoint 0.8mm
- GND | TP11 ● Testpoint 0.8mm
- GND | TP12 ● Testpoint 0.8mm
- GND | TP13 ● Testpoint 0.8mm

			Title: TE0723 - PowerSupply	
			A4	Number: TE0723 11C64-A
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CHANGES REV02 to REV03

- 1) changed FTDI-chip on 56pins package
- 2) changed micro-USB connectors
- 3) optimized BOM
- 4) update footprints, full update lib
- 5) added serial number (traceability pad)

A

A

B


B

C

C

D

D

	Title: TE0723 - Changes list		
	A4	Number: TE0723 11C64-A	Rev. 03
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	Filename: Revision_Changes.SchDoc		

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