

## Replacing 8024 Devices with the Teridian 73S8014R/RN

### 1 Introduction

This document describes the differences between the Teridian 73S8014R/RN (73S8014) and the industry standard 8024 Smart Card Interface ICs, including the Teridian 73S8024RN (73S8024R/RN). The 73S8014 is a single Smart Card Interface IC that provides the necessary input and output signal interfaces and power supply to the smart card.

The 73S8014 IC is available in an SO20 package and is not a pin-compatible drop-in replacement for the 73S8024 and 73S8024R/RN devices.

- The 73S8014 employs an on-chip Low Drop Out (LDO) regulator for the smart card power supply ( $V_{CC}$ ). The LDO regulator does not generate switching noise and offers improved performance and lower component count over 8024 devices using DC/DC converter regulators. The 73S8014 requires analog power-supply input ( $V_{PC}$ ) to be 5V typical (4.85V Min for NDS; 4.75V Min for EMV 4.0) to ensure compliance with applicable standards when using 5V smart cards.
- The 73S8014 does not support the 73S8024 and 73S8024R/RN auxiliary data signals C4 and C8.
- The control and status signals for both the 8024 and 73S8024RN devices and the 73S8014 are functionally identical.
- The control signals consist of:
  - The  $3V/5V$  select,
  - $\overline{CMDVCC}$  and
  - $\overline{RSTIN}$ .
- The status signal is the  $\overline{OFF}$  signal.
- Dependent upon the type of 8024 device being used, some differences in the timing between the 8024 and 73S8014R/RN may be observed. See [Section 3](#) for details.

## 2 Replacement Considerations

This section describes the various considerations that need to be made by an implementer when substituting the 73S8014 for either the industry standard 80124 or the Teridian 73S8024R/RN.

### 2.1 Replacement of Converter-Based 8024 Devices with 73S8014

Following the recommendations below allows the 73S8014 to eliminate or replace components in applications that utilize a converter type 8024 devices.

#### 2.1.1 Required Changes

The 220nF low ESR Vcc capacitor located close to the card connector (connected to pin 17), used with the 8024 parts must be replaced by a 1 $\mu$ F low ESR cap when using the 8014RN/R part in ISO7816 or NDS environments. The Vcc output on the 73S8014R/RN is pin 18. Its placement should also be close to the card connector.

#### 2.1.2 BOM Cost Reduction Changes

Capacitors between pins 5 and 6 (the 100nF low ESR charge pump capacitor of the 8024 parts), and the capacitor connected to pin 8 (100nF low ESR) can be removed.

The 100nF capacitor between pins 17 and 14 can be removed also (goes in parallel to the 1 $\mu$ F).

#### 2.1.3 Use of VDD Fault Input (Pin 18, SO28 Package)

Some 8024 applications may implement the optional resistor bridge connection to pin 18. This allows matching of the operating voltage range of the smart card interface IC (VDD digital power supply IN) to the supply voltage range of the system controller. In other words, when the power supply of the system drops, the card interface is deactivated at the same time (or eventually before) the system controller. In the *73S8014R/RN Data Sheet*, this feature is called "VDD Fault Adjust".

To meet the exact voltage range (or V<sub>DD</sub> fault value), the R1 and R3 resistor values in [Figure 1](#) must be slightly modified. Refer to the respective data sheets for exact calculation of these resistors. The VDDF\_ADJ pin on the 73S8014 is pin 12.

### 2.2 Replacement of Teridian 73S8024RN with 73S8014

The 73S8014 devices are feature reduced versions of the 73S8024RN and have the following differences:

- The 73S8014 does not use the smart card C4 and C8 auxiliary data as supported on the 8024. This removes the pins; AUX1, AUX2, AUX1UC and AUX2UC.
- The 73S8014 does not support the clock stop and clock stop output level functions that are supported on the 8024. The CLKSTOP and CLKLVL pins are not available.
- The 73S8014 does not use the  $\overline{\text{PRES}}$  pin. The PRES pin is still supported. If a design uses the  $\overline{\text{PRES}}$  pin, then the card switch logic must be inverted so the PRES pin can be used.
- The clock divider on the 73S8014RN is different from the 73S8014R and the 73S8024RN. This is the only functional difference between the 73S8014R and 73S8014RN. The 73S8014RN supports divisor rates of 1, 2, 4 and 6 where as the 73S8014R and 73S8024RN supports divisor rates of 1, 2, 4 and 8. The impact of this difference on the design must be considered by the implementer.
- The 73S8014 removes the sequencer logic present in the 8024. See [Section 3](#) for more details.
- All other pin functions are identical.

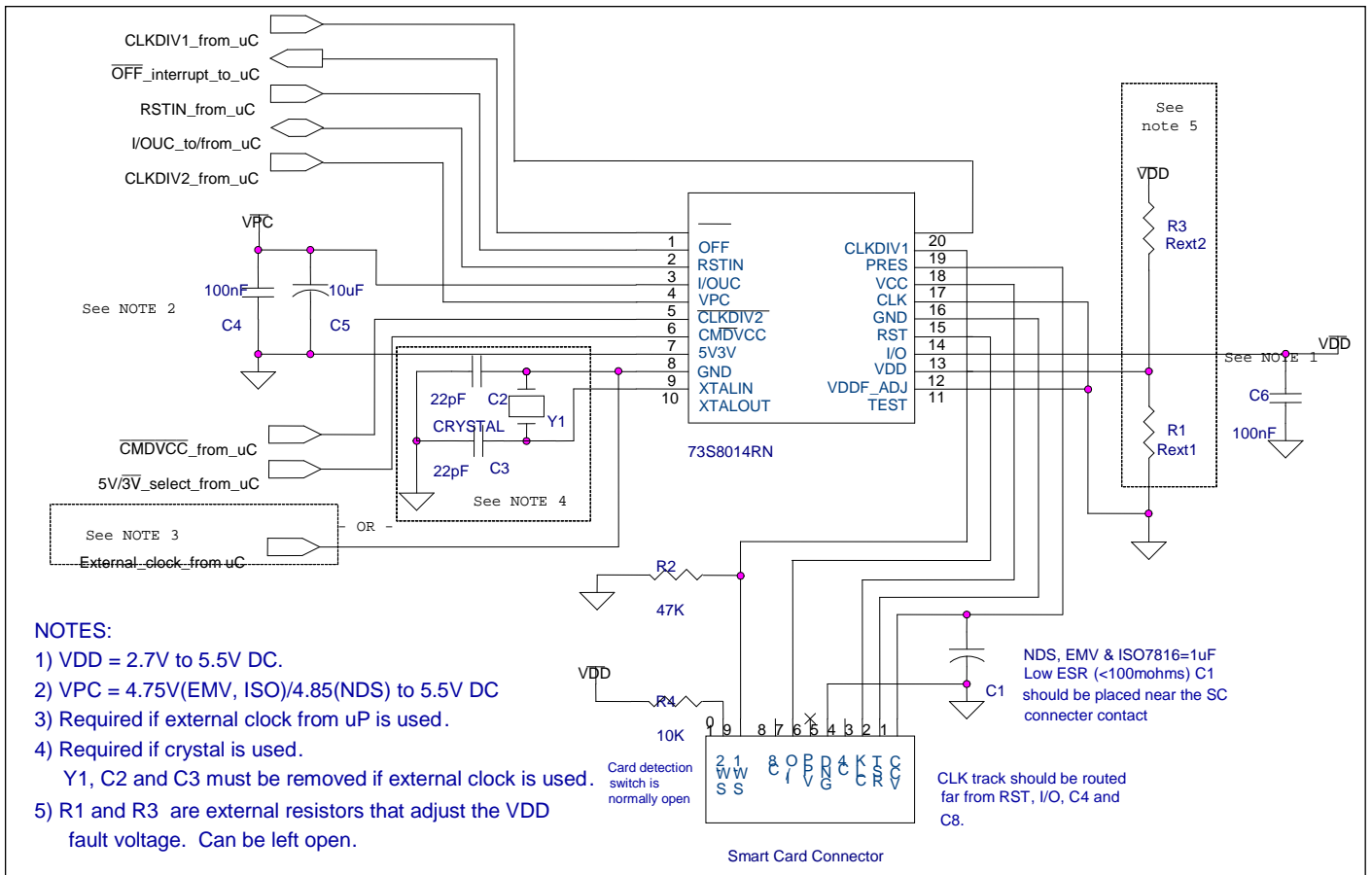


Figure 1: Teridian 73S8014RN Application Schematic

### 3 Timing Differences

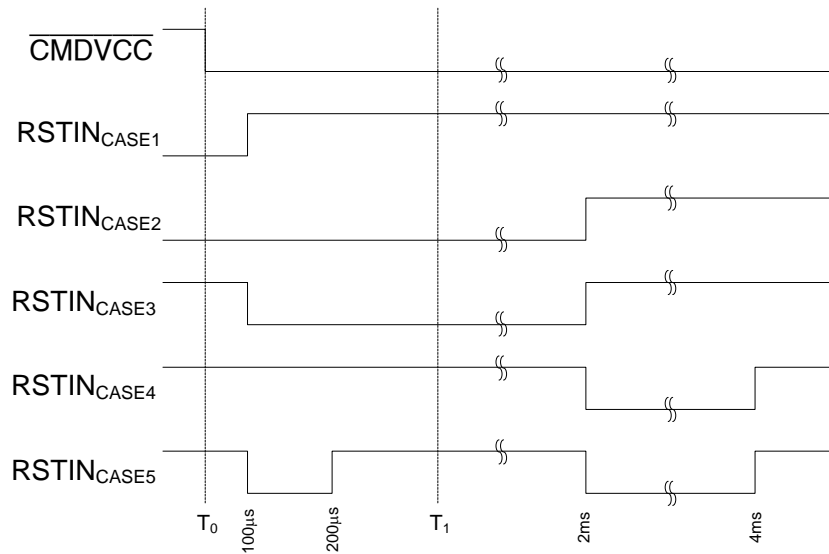
The following section provides detail on the differences in the timing operation of the 73S8014 and the 8024 and 8024R/RN. The implementer needs to understand these differences and make the determination if or what kind of changes to the host firmware need to be made when switching to the 73S8014.

#### 3.1 Teridian 73S8024RN

Unlike the other converter-based 8024 devices, the 73S8024RN internally generates the EMV 4.0 compliant CLK to RST delay at activation. The related timing differences between 73S8024RN and 73S8014R/RN are:

- The 73S8024RN automatically asserts 42,000 CLK cycles of RST delay at activation. RSTIN is ignored and RST is held high during this time period. The 73S8014R/RN does not provide any delay; RSTIN control of RST is active immediately after the CLK starts.
- The 73S8024RN will delay both the CLK and I/O output when the RSTIN is high at time T1 (approximately 500-520 $\mu$ s after  $\overline{\text{CMDVCC}}$  goes low). The I/O will go high and CLK will start on the falling edge of RSTIN. The 73S8014R/RN will set I/O high and delay CLK at time T1. The CLK will start upon the falling edge of RSTIN. Note: this difference in operation should have no effect on smart card operation.
- Activation is invoked by negating  $\overline{\text{CMDVCC}}$  at time T0. The Vcc output is deemed stable at time T1. CLK, I/O and RST output timing depends on RSTIN input timing. Five example cases for RSTIN starts are illustrated in [Figure 2](#).
- Case 1: RSTIN is low before T0 and goes high before T1. See [Figure 8](#) through [Figure 12](#).
- 73S8024RN – I/O goes high at T1, CLK starts at least 500ns after I/O goes high and RST goes high 42000 clock cycles after the CLK starts.
- 73S8014R/RN – CLK starts at T1, CLK starts at least 500ns after I/O goes high and RST goes high shortly after the CLK starts.
- Case 2: RSTIN is low before T0 and goes high after T1. See [Figure 14](#) through [Figure 16](#).
- 73S8024RN – I/O goes high at T1, CLK starts at least 500ns after I/O goes high and RST goes high 42000 clock cycles after the CLK starts.
- 73S8014R/RN – CLK starts at T1, CLK starts at least 500ns after I/O goes high and RST goes high shortly after the CLK starts.
- Case 3: RSTIN is high before T0, goes low before T1 and goes high after T1. See [Figure 18](#) through [Figure 20](#).
- Both devices behave the same as Case 2.
- Case 4: RSTIN is high before T0, goes low after T1 and goes high sometime later. See [Figure 22](#) through [Figure 24](#).
- 73S8024RN – I/O, RST and CLK are held low until RSTIN is set low (after T1). I/O goes high, CLK starts at least 500ns after I/O and RST goes high 42000 clock cycles after the CLK starts.
- 73S8014R/RN - I/O goes high at T1, CLK and RST remain low. The CLK starts after RSTIN goes low. RST goes high shortly after the CLK starts.
- Case 5: RSTIN is high before T0, goes low and then high before T1, goes low after T1 and goes high sometime later. See [Figure 26](#) through [Figure 28](#).
- Both devices behave the same as Case 4.
- RST de-assertion (RST rising)
- 73S8024RN – RST is de-asserted at 42,000 CLK cycles (T2) after CLK start if RSTIN becomes high before T2. If RSTIN goes high after T2, RST is de-asserted at RSTIN rising. In this manner, the 42,000 clock-cycle delay, as per EMV 4.0 and ISO7816-3 is ensured by the 73S8024RN. The CLK to RST delay can lengthen beyond the 42000 CLK cycles by the system controller.
- 73S8014R/RN – After CLK has started, RST will track RSTIN.

**Note: The 73S8014R/RN activation sequence and its controlling host firmware are fully compatible with the 73S8024RN (as long as the RSTIN line is asserted and de-asserted by the host after time  $T_2$ ).**



**Figure 2: Activation Sequence Cases**

### 3.1.1 Reset Signal Precautions

Due to activation sequence timing differences between the Teridian 73S8014R/RN and the Teridian 73S8024RN, there is a possibility of missing an ATR response or violating some minimum number of clock cycles on CLK before de-asserting RST with the 73S8014R/RN when it replaces the 8024RN in an application. Since the deactivation of RST could occur 42000 cycles earlier, the host may not be configured to read the ATR this much earlier. If the host is able to accept the ATR at this earlier time, then there should not be any changes required for the firmware in this respect when used on the 73S8014R/RN. If the existing 73S8024RN firmware meets the associated ATR timeout specifications, then deactivating the RST earlier can mask a real ATR timeout error. This potential error can be eliminated by simply by extending the RSTIN deactivation signal by an amount that exceeds the 42000 CLK cycle delay of the 73S8024RN sequencer. This extension is legal under EMV, ISO and NDS specifications.

Figure 3 shows the differences on RST between the 73S8014R/RN and the 73S8024RN. All timing is referenced against the falling edge of  $\overline{\text{CMDVCC}}$ . The second line shows the range of RSTIN control that will cause different timing results between the two device types. After the 73S8024RN RST sequencer expires, the devices will operate the same. This time is shown as  $T_i$ . The third line shows that RST on the 73S8024RN will remain active (low) until time  $T_i$ . The fourth line shows the RST on the 73S8014R/RN will follow RSTIN between  $T_1$  and  $T_i$ . The fifth line shows an example of where an ISO-7816 violation could occur if the RSTIN is de-asserted before 400 CLK cycles. The sixth line shows an example of where an NDS violation could occur if the RSTIN is not deactivated before 40000 CLK cycles. These examples would not be a violation when using the 73S8024RN as RST is always held active until time  $T_i$ .

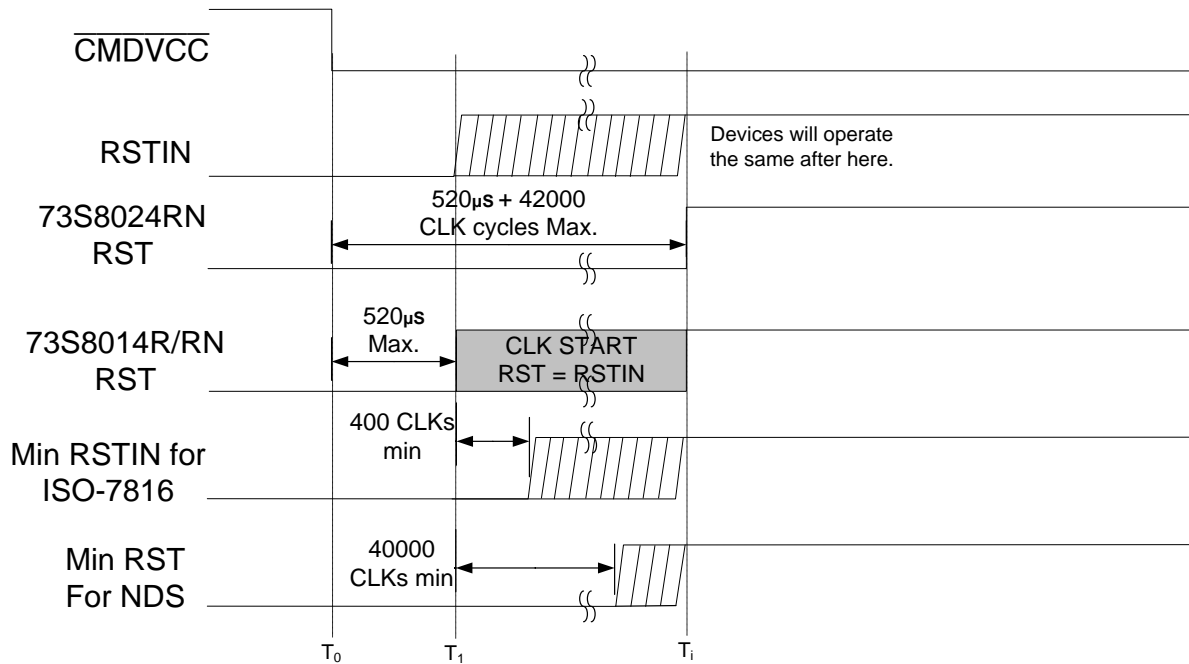


Figure 3: 73S8014R/RN and 73S8024RN RST Timing Differences

### 3.2 Converter-Based 8024 Devices

The converter-based 8024 devices and the Teridian 73S8014R/RN contain a rudimentary sequencer that controls the timing of the smart card signals upon activation. Upon the falling edge of CMDVCC the activation sequence is initiated and the smart card power is turned on (V<sub>cc</sub>). The converter based 8024 devices take less time for the V<sub>cc</sub> to activate than the Teridian 73S8014R/RN. The Teridian 73S8014R/RN and Teridian 73S8024RN devices use the same activation logic with regard to when the V<sub>cc</sub> supply is deemed stable (time T<sub>1</sub> from above). As a result, there can be some problem when transitioning to a Teridian device. These differences are described below.

#### 3.2.1 Clock Start Timing Differences

The converter-based 8024 will start the card CLK between 50 and 200µs after the falling edge of CMDVCC, whereas the Teridian devices will start the CLK around 520µs after. The specification for the Teridian 73S8024RN is 1ms maximum. As a result, the Teridian 73S8024RN CLK signal can start as much as 1ms – 50µs = 950µs (worst case maximum) after the converter based 8024s.

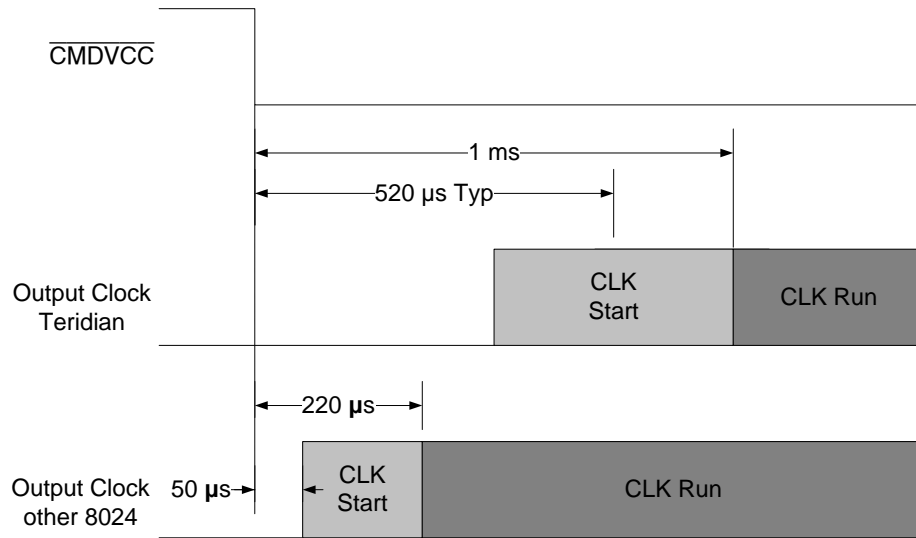


Figure 4: Clock Start Timing Differences

### 3.2.2 RST Timing Differences

The converter based 8024s and the Teridian 73S8014R/RN do not have any built-in RST out delay with respect to CLK. On both types of devices, the RST output is controlled by the RSTIN after the clock starts. Since the CLK starts up to 950 $\mu\text{s}$  earlier in the converter based 8024 devices, the RSTIN signal can control the RST output to the card that much earlier.

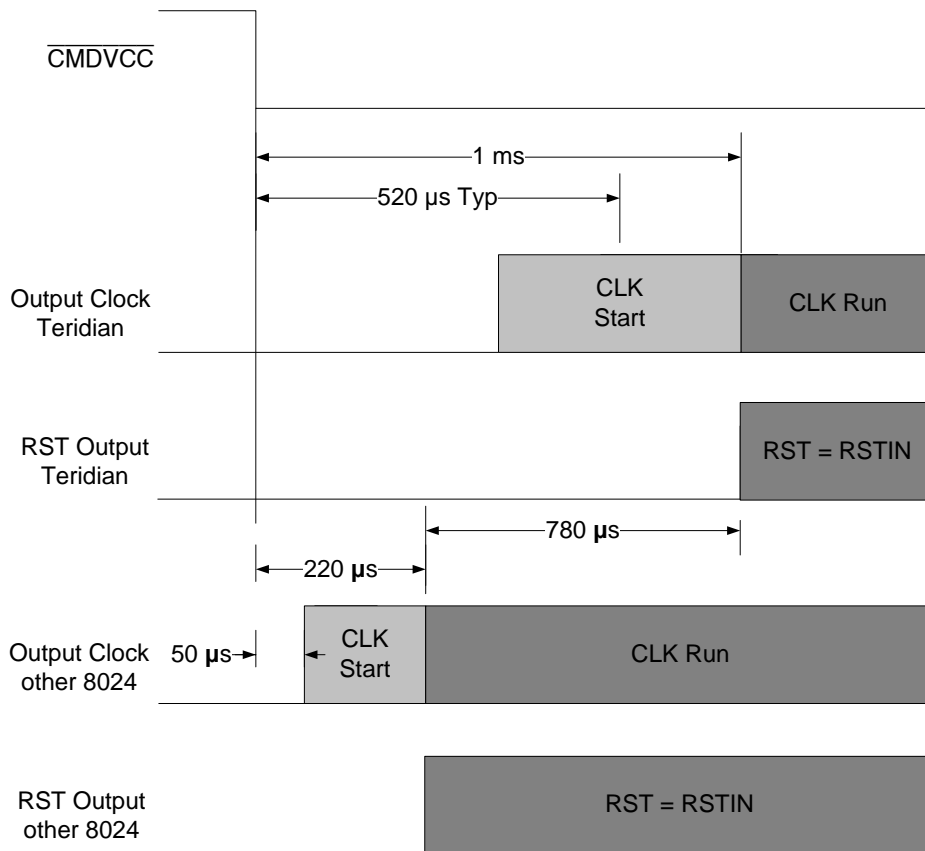


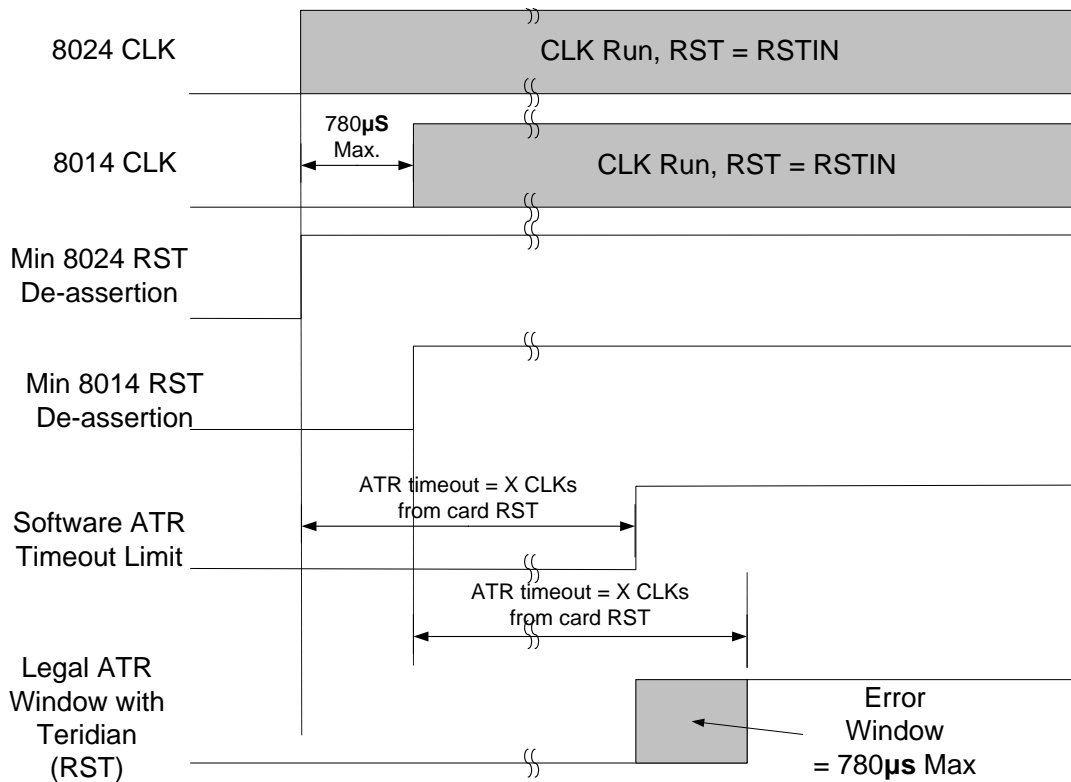
Figure 5: RST Timing Differences

Once card RST is de-asserted, the system controller expects an ATR response from the card within a certain window of time. If the ATR is not properly received before the end of this window an ATR timeout error will occur.



**Figure 6: ATR Timeout Error**

With the converter based 8024s, this timeout starts at the rising edge of RSTIN. If the system controller de-asserts RSTIN 220µs (worst case CLK start time) and 1ms after de-asserting  $\overline{CMDVCC}$ , the card RST signal timing will be different between the converter based 8024s and the Teridian 73S8014R/RN.



**Figure 7: RST Timing Differences**

Due to the timing difference between the devices in the case of RSTIN being de-asserted between 220µs and 1ms after de-assertion of  $\overline{CMDVCC}$ , there is a delay between RSTIN and card RST on the Teridian 73S8014R/RN up to 780 µs. This means that a card can respond with a valid ATR response (with respect to card RST) and still generate an ATR timeout error (with respect to RSTIN).



This maximum 950 $\mu$ s clock start timing differential need to be added to the ATR timeout to insure the ATR timeout error will not be generated when the card responds with a valid ATR response.

### 3.3 Firmware Precautions

#### 3.3.1 $\overline{\text{CMDVCC}}$ Activation Control

The Teridian 73S8014/RRN must use  $\overline{\text{CMDVCC}}$  to start activation. The converter based 8024s can use the card detect signals (PRES and  $\overline{\text{PRES}}$ ) to start activation if the  $\overline{\text{CMDVCC}}$  signal is held low when the card insertion is detected. The Teridian 73S8014R/RN will only start activation upon the falling edge of  $\overline{\text{CMDVCC}}$  when a card is present.

#### 3.3.2 $\overline{\text{OFF}}$ Debounce

The converter-based 8024s contain a debounce circuit on the card detect inputs (PRES and  $\overline{\text{PRES}}$ ). This can prevent any bouncing on the  $\overline{\text{OFF}}$  signal going to the controller device. The Teridian 73S8014R/RN does not have any debounce on the card detect input pins. If debounce on the  $\overline{\text{OFF}}$  signal is necessary, there are two methods to debounce the  $\overline{\text{OFF}}$  signal. The hardware can implement an RC network on the card detect signal to prevent bouncing. The second method is to implement a firmware-based debounce of the  $\overline{\text{OFF}}$  input signal.

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## Appendix A

The following set of scope captures show the timing of the smart card signals based on the five activation sequence cases described above. The signals are defined as follows:

### Legend A

CH:	Color	Signal
4	Blue	RSTIN
2	Green	$\overline{\text{CMDVCC}}$
3	Red	RST
1	Black	I/O

### Legend B

CH:	Color	Signal
4	Blue	CLK
2	Green	$\overline{\text{CMDVCC}}$
3	Red	RST
1	Black	I/O

Note: the timebases may be different between devices to show all the signals.

### Case 1 Captures:

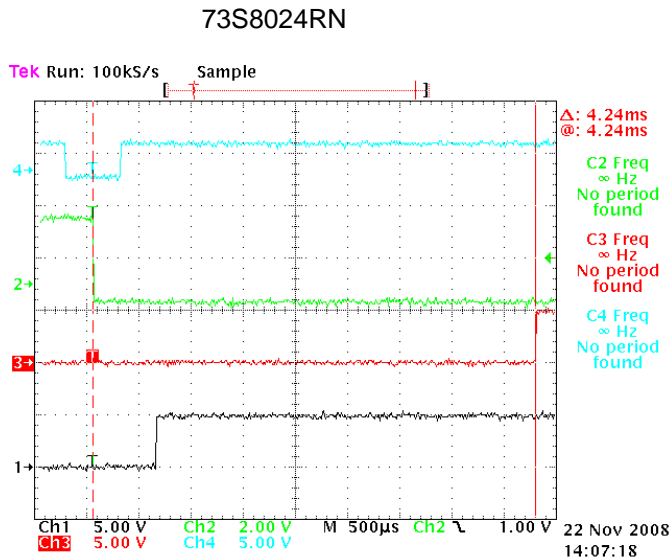


Figure 8: 73S8024RN, Case 1, Legend A

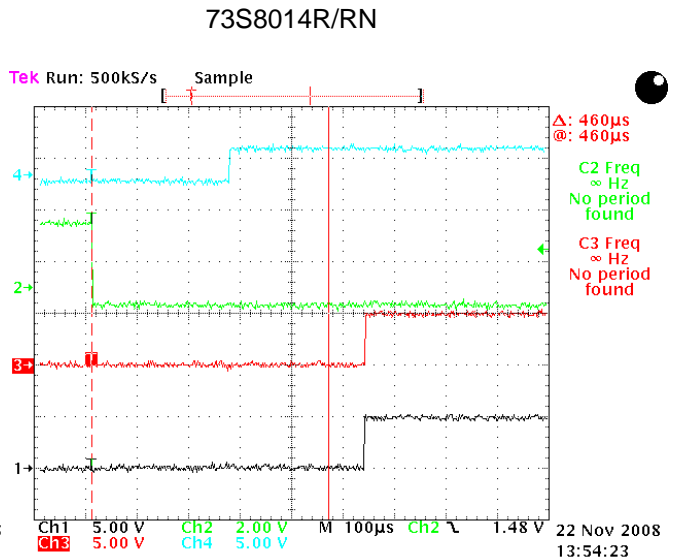


Figure 9: 73S8014R/RN, Case 1, Legend A

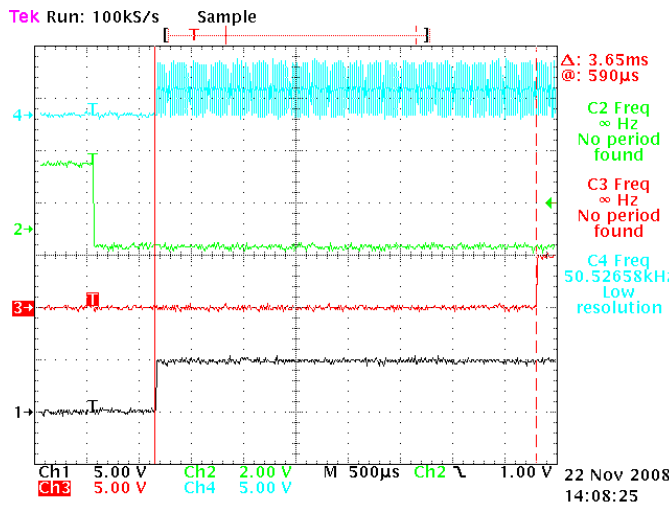


Figure 10: 73S8024RN, Case 1, Legend B

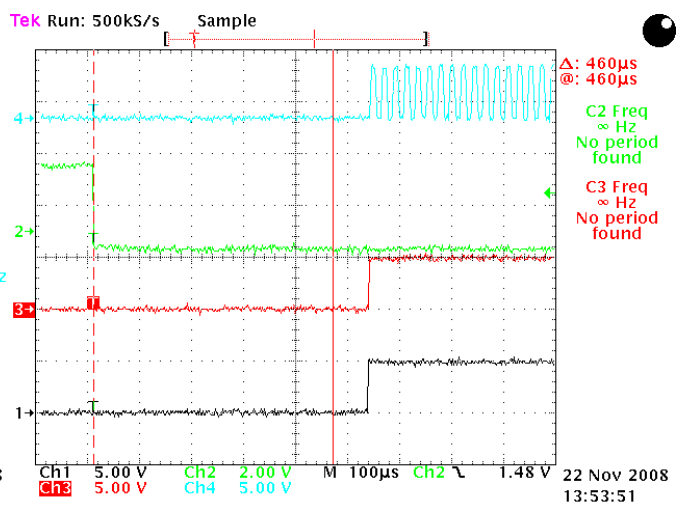


Figure 11: 73S8014R/RN, Case 1, Legend B

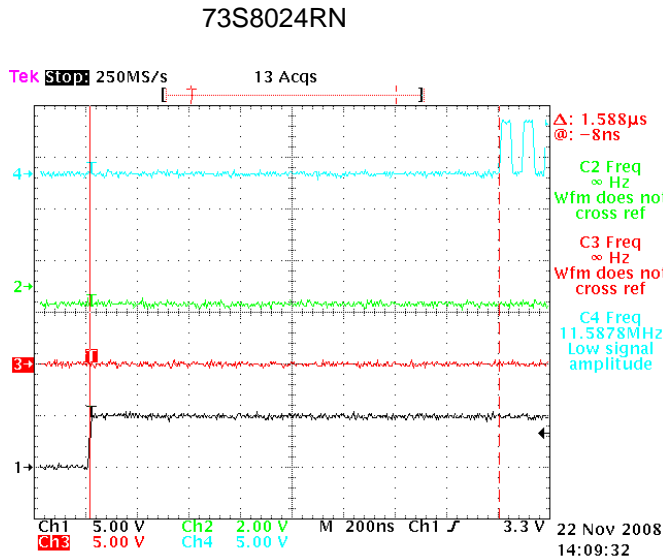


Figure 12: 73S8024RN, Case 1, Legend B Zoom

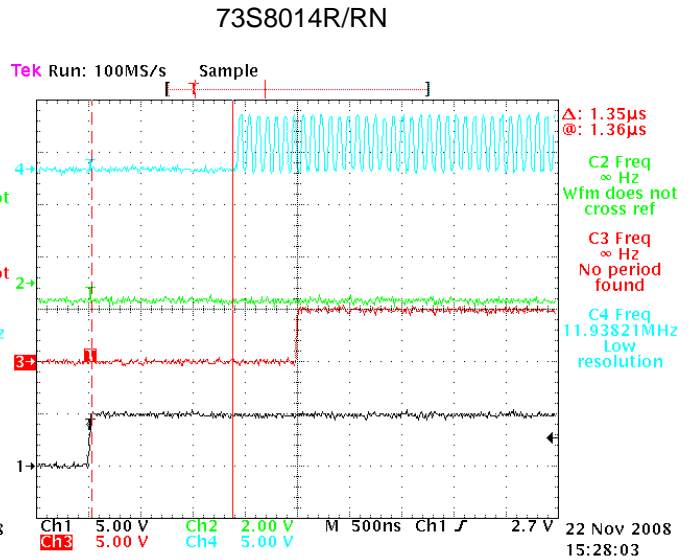


Figure 13: 73S8014R/RN, Case 1, Legend B Zoom

Case 2 Captures:

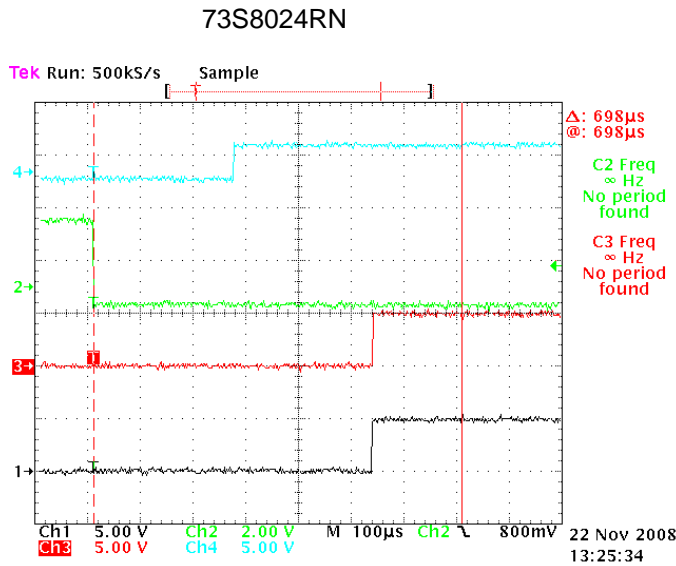


Figure 14: 73S8024RN, Case 2, Legend A

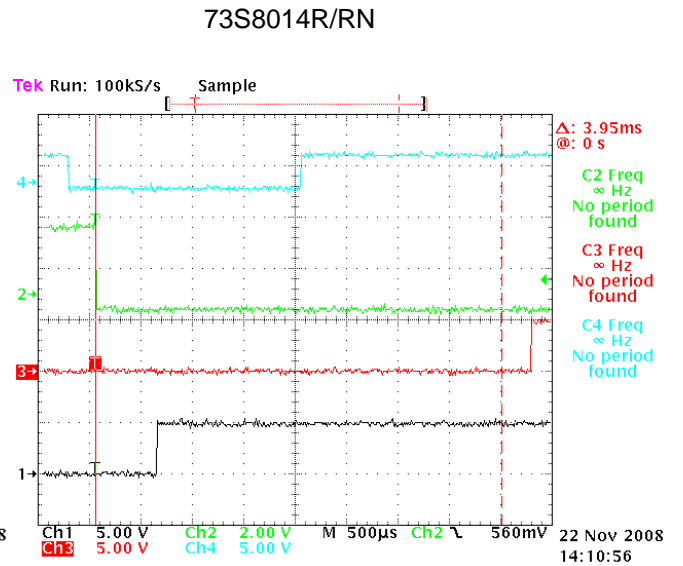


Figure 15: 73S8014R/RN, Case 2, Legend A

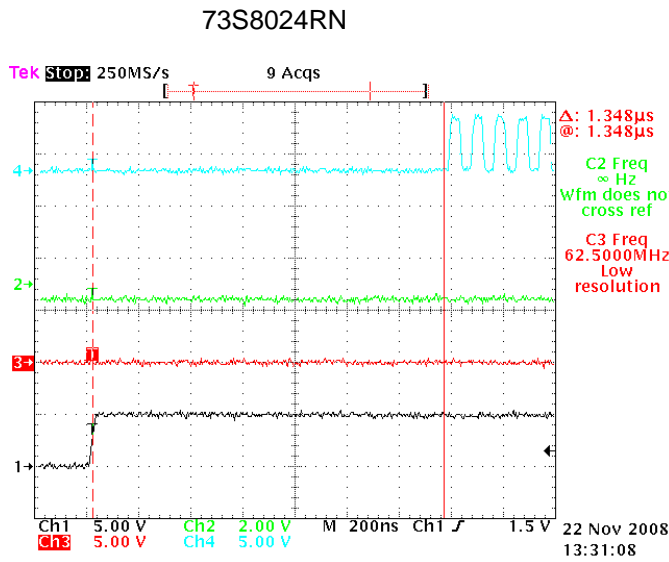


Figure 16: 73S8024RN, Case 2, Legend B

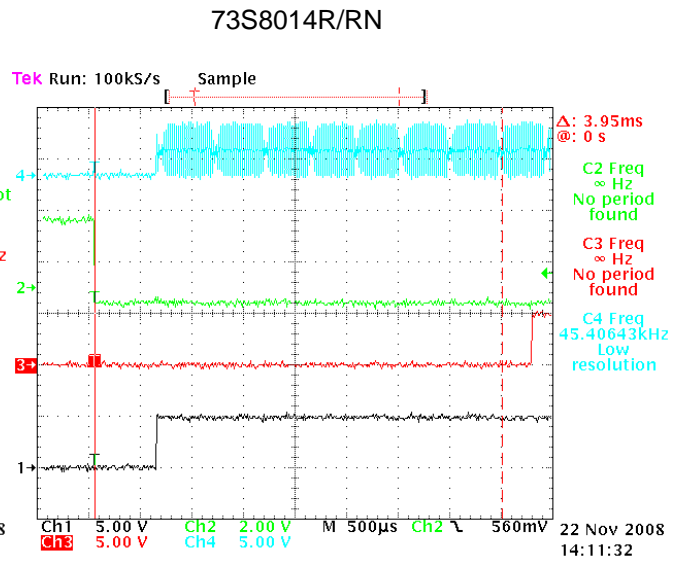


Figure 17: 73S8014R/RN, Case 2, Legend B

Case 3 Captures:

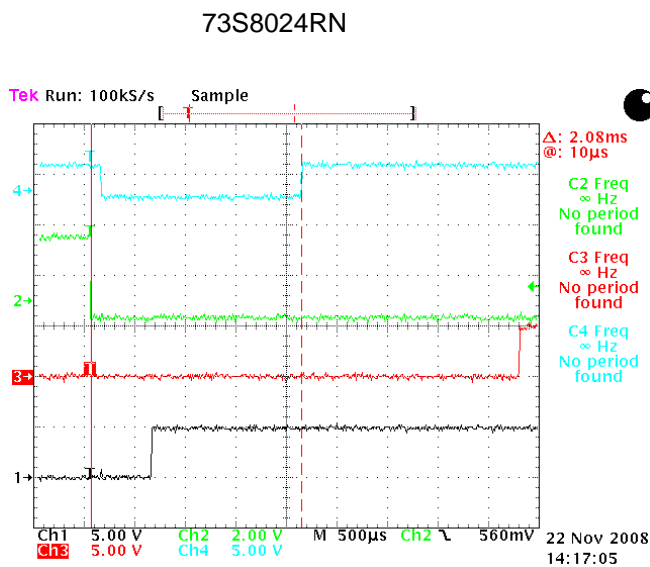


Figure 18: 73S8024RN, Case 3, Legend A

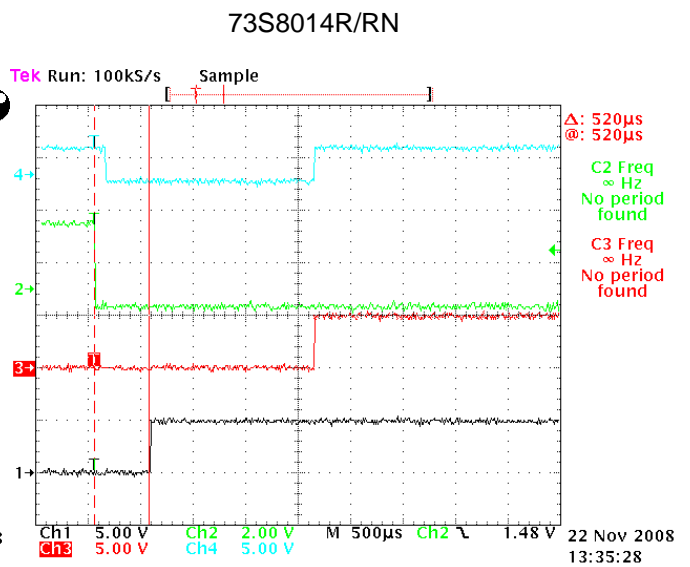


Figure 19: 73S8014R/RN, Case 3, Legend A

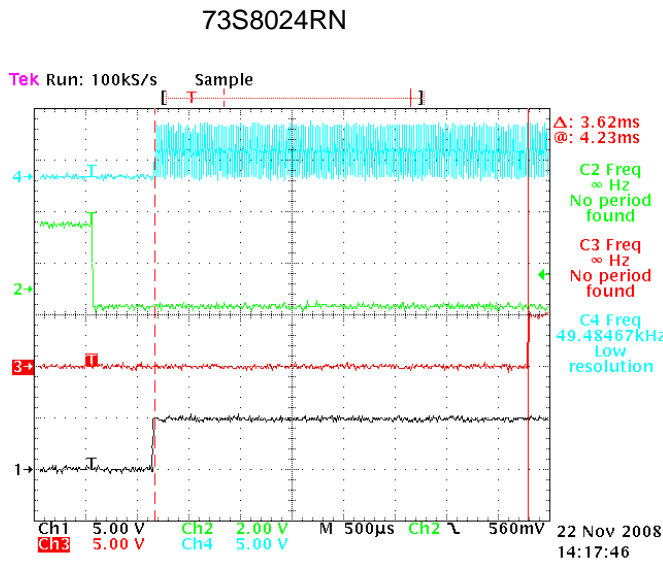


Figure 20: 73S8024RN, Case 3, Legend B

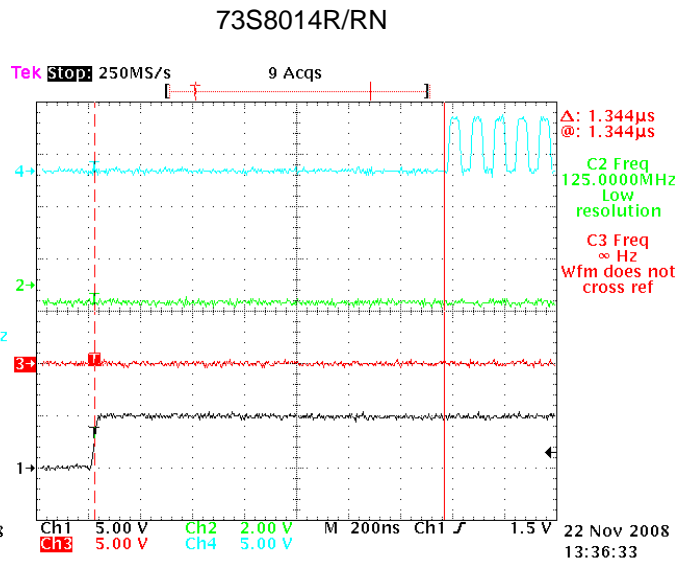


Figure 21: 73S8014R/RN, Case 3, Legend B

Case 4 Captures:

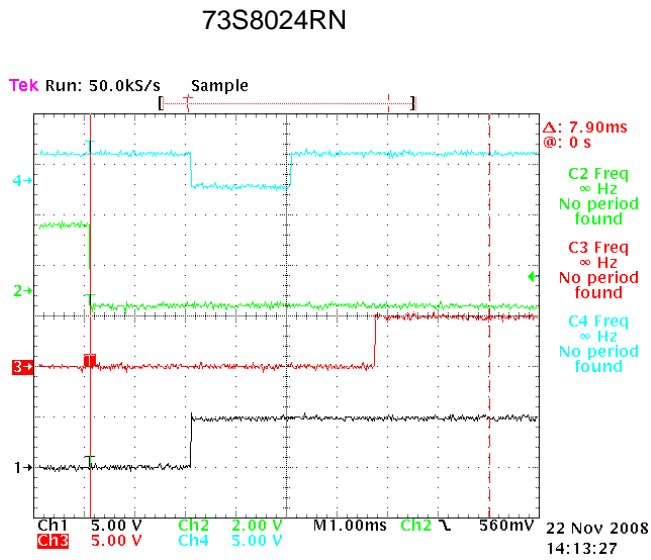


Figure 22: 73S8024RN, Case 4, Legend A

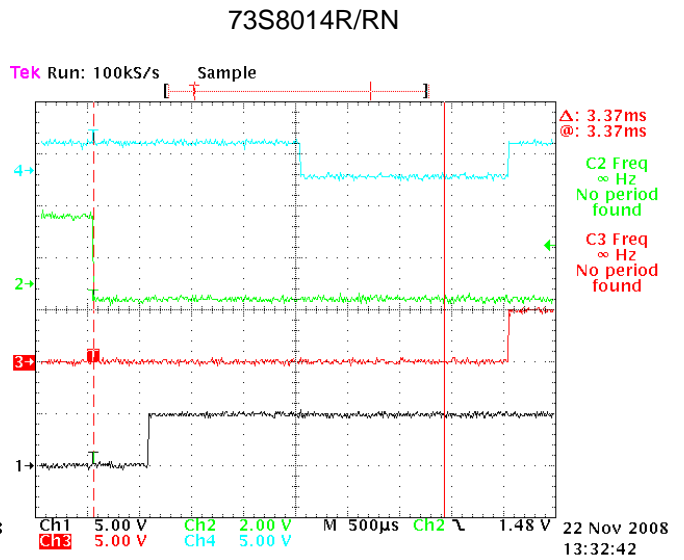


Figure 23: 73S8014R/RN, Case 4, Legend A

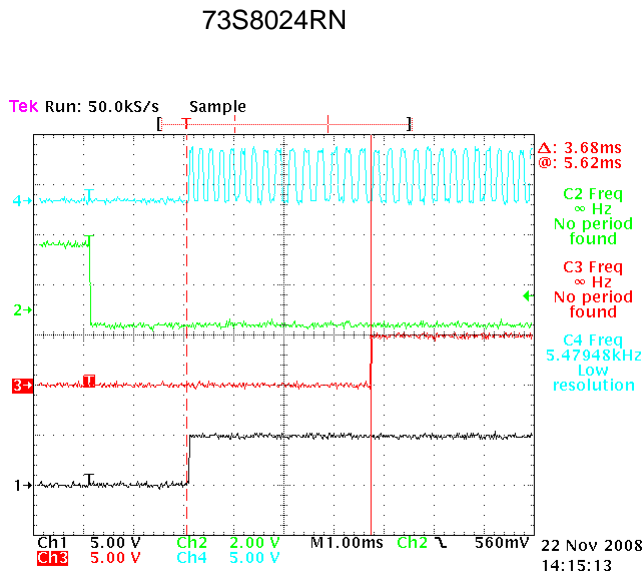


Figure 24: 73S8024RN, Case 4, legend B.

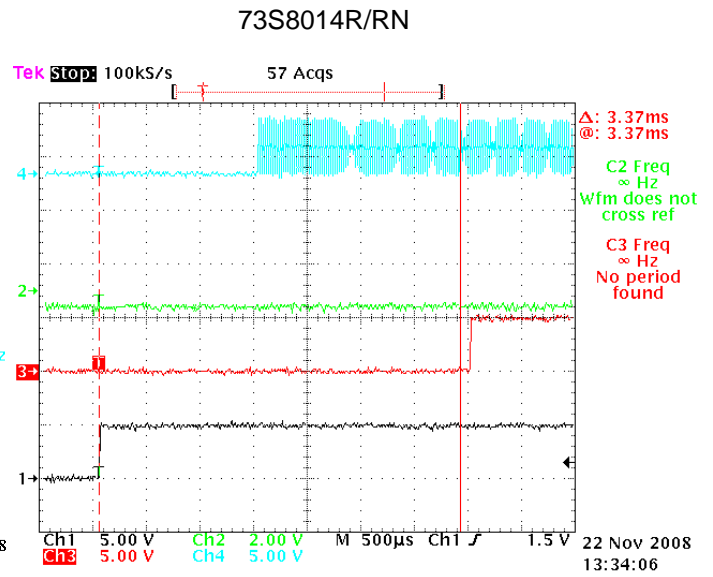


Figure 25: 73S8014R/RN, Case 4, legend B.

Case 4 Captures:

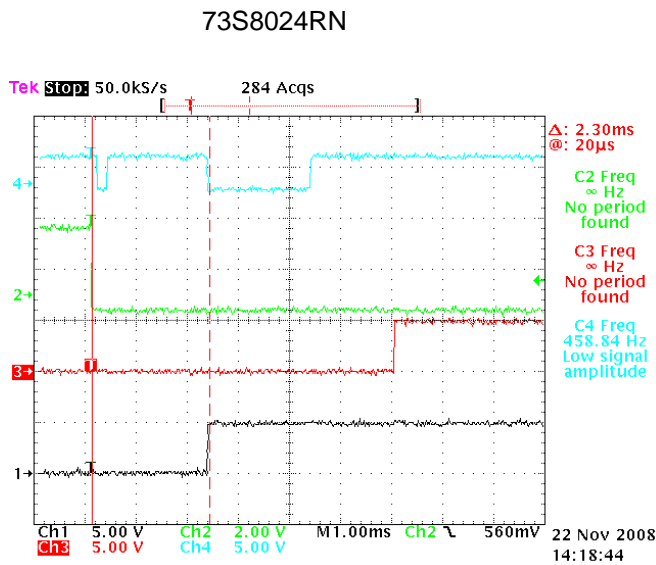


Figure 26: 73S8024RN, Case 5, Legend A

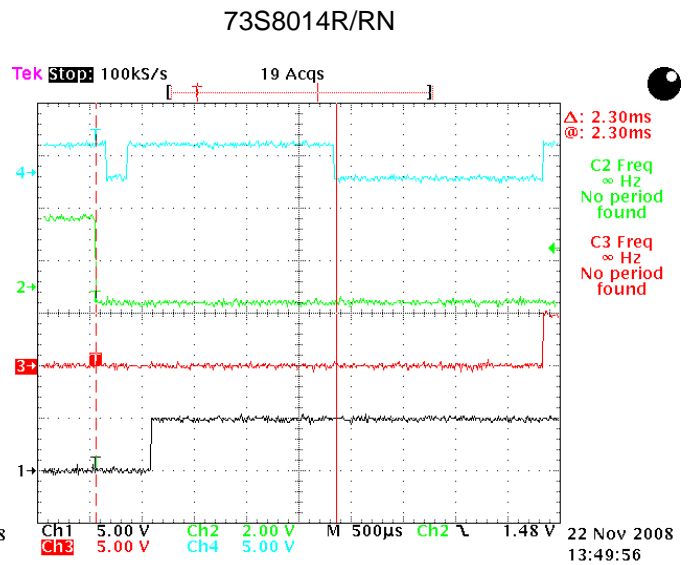


Figure 27: 73S8014R/RN, Case 5, Legend A

73S8024RN

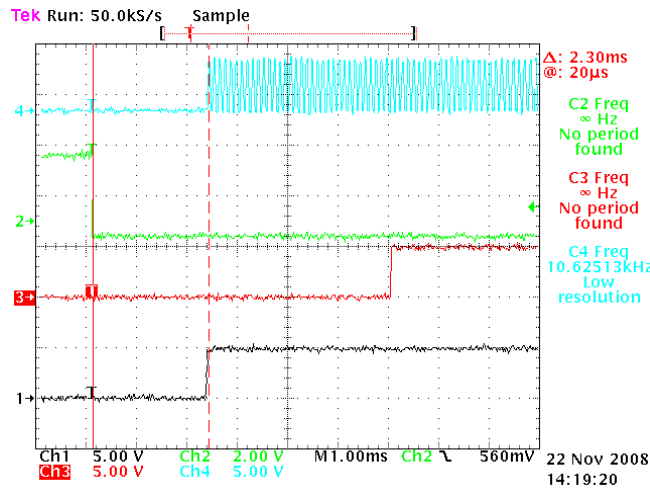


Figure 28: 73S8024RN, Case 5, Legend B

73S8014R/RN

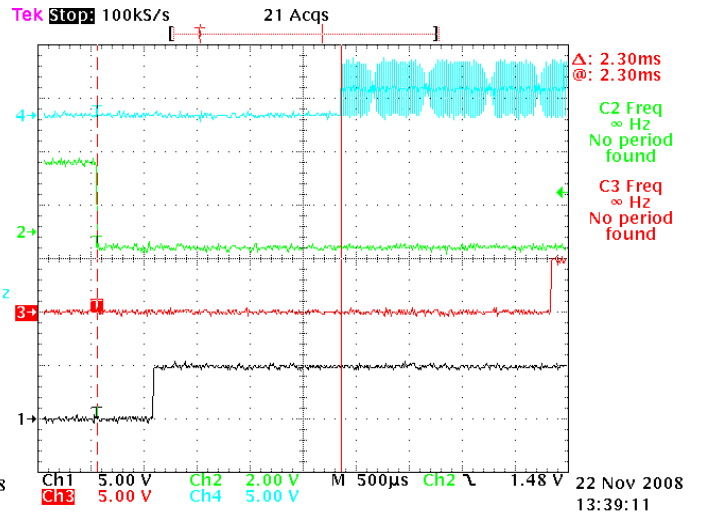


Figure 29: 73S8014R/RN, Case 5, Legend B

**Revision History**

<b>Revision</b>	<b>Date</b>	<b>Description</b>
1.0	1/5/2009	First publication.
1.1	1/23/2009	Replaced <a href="#">Figure 2: Activation Sequence Cases</a> .