
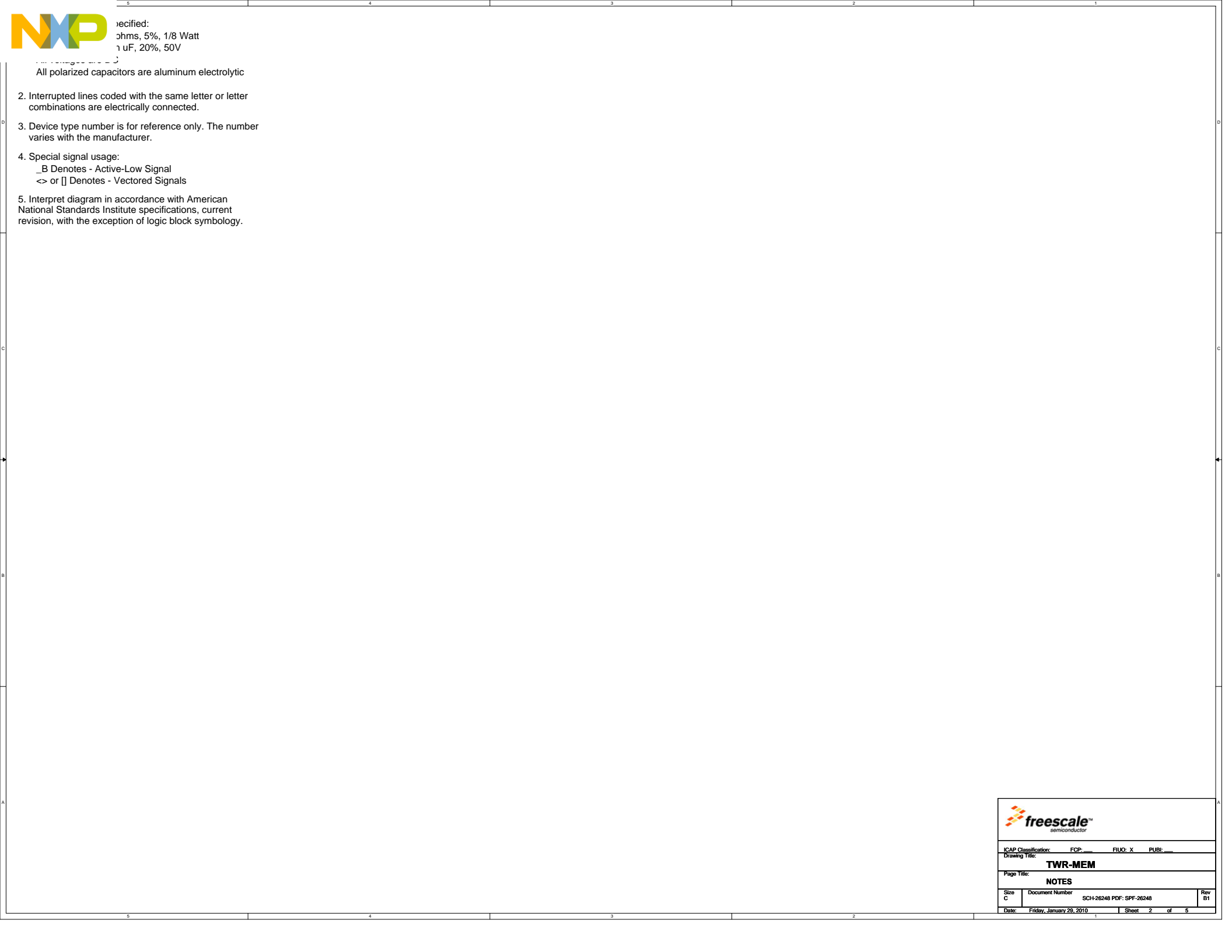


5	Contents
4	
3	
2	
1	
	FLASH
	CONT

Revisions			
Rev	Description	Date	Approved
X10	Convert into FSL template	9/8/09	DESIGNER
X11	All parts FCL	9/14/09	Michael N
X12	Replaced U5 with the correct part	9/15/09	Michael N
X14	Replaced some components with similar per Micetek suggestion	9/22/09	Michael N
X15	Added a Jumper on SD WR per BU request	9/25/09	Michael N
X16	Replaced SC part with shorter one	9/28/09	Michael N
X17	Replaced SD/MMC connector	10/09/09	Michael N
A	Released to Fab	10/15/09	Michael N
B	Add J15, J16 and J17 per customer req Released to fab	10/15/09	Michael N
B1	Replace with alternate part LEDs	1/29/10	Michael N

		Microcontroller Solutions Group 6501 William Cannon Drive West Austin, TX 78755-5598	
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Designer: Rodolfo G		ICAP Classification: FCP: FLUQ: X PUB:	
Drawing Title: TWR-MEM			
Drawn by: Rodolfo G		Page Title: Table of contents	
Approved: Michael N		Document Number: SCH-26248 PDF: SPF-26248	
Size: C		Rev: B1	
Date: Friday, January 29, 2010		Sheet 1 of 5	

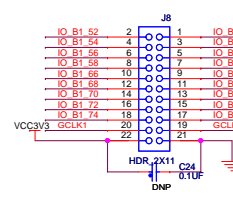
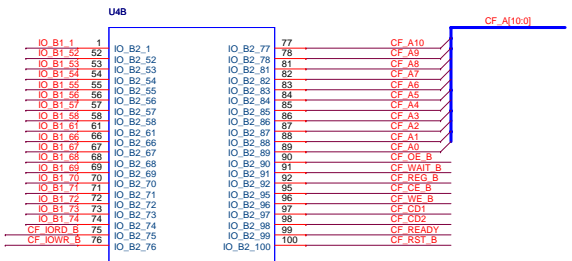
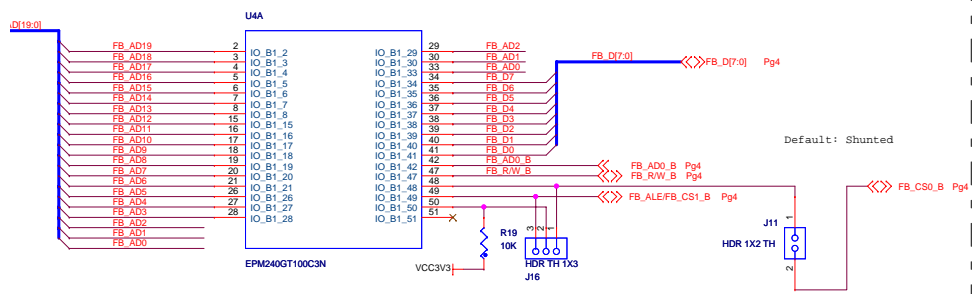


pecified:
 ohms, 5%, 1/8 Watt
 uF, 20%, 50V

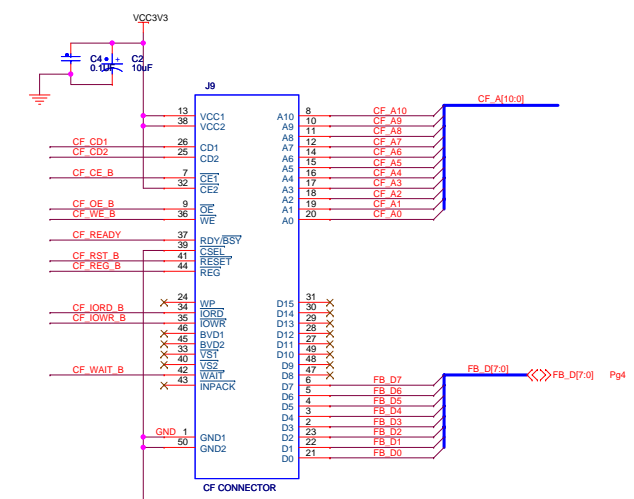
All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.
3. Device type number is for reference only. The number varies with the manufacturer.
4. Special signal usage:
 _B Denotes - Active-Low Signal
 <> or [] Denotes - Vectored Signals
5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

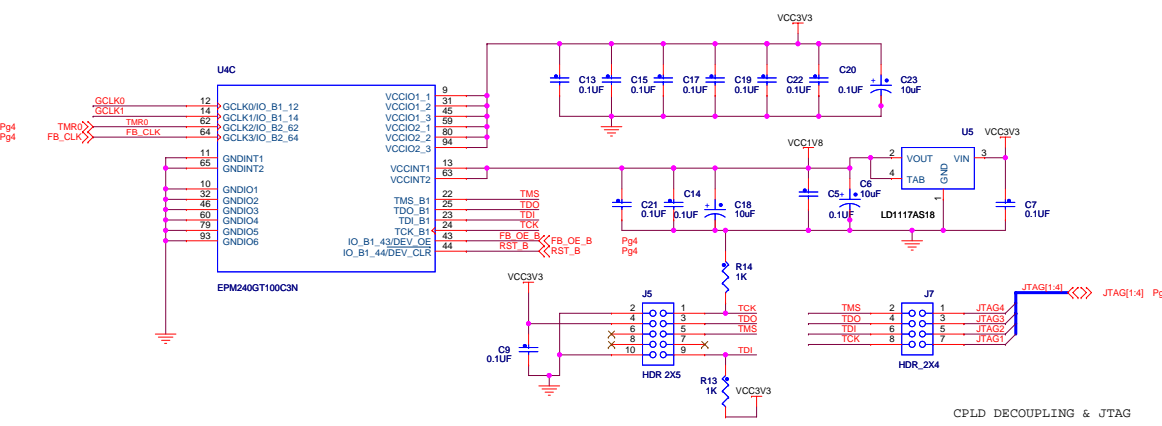
ICAP Classification: FCP: _____ FIUC: X PUBI: _____		
Drawing Title: TWR-MEM		
Page Title: NOTES		
Size C	Document Number SCH-26248 PDF: SPF-26248	Rev B1
Date: Friday, January 29, 2010	Sheet 2	of 5



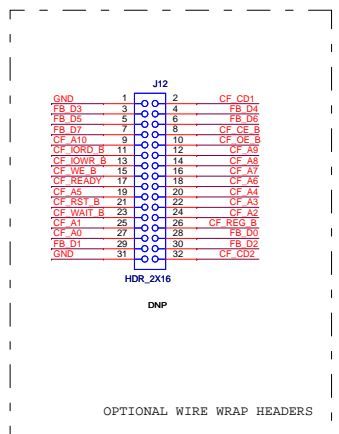
CPLD CONNECTIONS



CF HEADER



CPLD DECOUPLING & JTAG



OPTIONAL WIRE WRAP HEADERS

freescale
semiconductor

ICAP Classification: FCP: _____ FIUC: X PUBL: _____
Drawing Title: **TWR-MEM**

Page Title: **CF & CPLD**

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J5008			
GND	D1	5V_3	C1
	D2	GND_17	C2
	D3	3.3V_8	C3
GND	D4	ELF_PS_SENSE_2	C4
	D5	GND_18	C5
GND	D6	GND_18	C6
	D7	GND_19	C7
X	D8	SPI2_CLK	C8
X	D9	SPI2_CS1_B	C9
X	D10	SPI2_CS3_B	C10
X	D11	SPI2_MOSI	C11
X	D12	SPI2_MISO	C12
X	D13	ETH_COL_2	C13
X	D14	ETH_RXER_2	C14
X	D15	ETH_TXCLK_2	C15
X	D16	ETH_TXEN_2	C16
X	D17	GPIO18	C17
X	D18	GPIO19SDHC_D4	C18
X	D19	GPIO20SDHC_D5	C19
X	D20	ETH_TXD1_2	C20
X	D21	ETH_TXD0_2	C21
X	D22	ULPI_NEXTAUSB1_DM	C22
X	D23	ULPI_DIRAUSB1_DP	C23
X	D24	ULPI_DATA6USB2_DM	C24
X	D25	ULPI_DATA6USB2_DP	C25
X	D26	ULPI_DATA7	C26
GND	D27	GND_20	C27
X	D28	LCD_HSYNC_LCD_P24	C28
X	D29	LCD_VSYNC_LCD_P25	C29
X	D30	AN13	C30
GND	D31	AN12	C31
X	D32	LCD_CLK_LCD_P26	C32
X	D33	TMR11	C33
X	D34	TMR10	C34
X	D35	GPIO21	C35
X	D36	3.3V_9	C36
X	D37	PWM15	C37
X	D38	PWM14	C38
X	D39	PWM13	C39
X	D40	PWM12	C40
X	D41	CANRX1	C41
X	D42	CANTX1	C42
X	D43	LCD_DE_LCD_P27	C43
X	D44	LCD_D0_LCD_P0	C44
X	D45	LCD_D1_LCD_P1	C45
X	D46	LCD_D2_LCD_P2	C46
X	D47	LCD_D3_LCD_P3	C47
X	D48	GND_22	C48
GND	D49	GPIO23	C49
X	D50	GPIO24	C50
X	D51	LCD_D4_LCD_P4	C51
X	D52	LCD_D5_LCD_P5	C52
X	D53	LCD_D6_LCD_P6	C53
X	D54	LCD_D7_LCD_P7	C54
X	D55	LCD_D8_LCD_P8	C55
X	D56	LCD_D9_LCD_P9	C56
X	D57	LCD_D10_LCD_P10	C57
X	D58	LCD_D11_LCD_P11	C58
X	D59	IRQ_M	C59
X	D60	IRQ_L	C60
X	D61	IRQ_K	C61
X	D62	IRQ_J	C62
X	D63	LCD_D15_LCD_P15	C63
X	D64	LCD_D16_LCD_P16	C64
GND	D65	LCD_D17_LCD_P17	C65
X	D66	GND_23	C66
X	D67	EBI_AD20_LCD_P42	C67
X	D68	EBI_AD21_LCD_P43	C68
X	D69	EBI_AD22_LCD_P44	C69
X	D70	EBI_AD23_LCD_P45	C70
X	D71	EBI_AD24_LCD_P46	C71
X	D72	EBI_AD25_LCD_P47	C72
X	D73	EBI_AD26_LCD_P48	C73
X	D74	EBI_AD27_LCD_P49	C74
X	D75	EBI_AD28_LCD_P50	C75
X	D76	EBI_AD29_LCD_P51	C76
X	D77	EBI_AD30_LCD_P52	C77
X	D78	EBI_AD31_LCD_P53	C78
X	D79	LCD_D20_LCD_P20	C79
X	D80	LCD_D21_LCD_P21	C80
GND	D81	LCD_D22_LCD_P22	C81
GND	D82	GND_24	C82
		3.3V_10	C83



PCI EXPRESS X 16
SECONDARY PORT

freescale
semiconductor

ICAP Classification: FCP: FUC: X PUB: _____
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Page Title: **OPTIONAL PORT**

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