DLP650NE 0.65 1080p S600 DMD

1 Features

- 0.65-Inch Micromirror Array Diagonal
  - 1080p (1920 x 1080)
  - 7.56 Micron Micromirror Pitch
  - ± 12° Micromirror Tilt Angle (Relative to Flat State)
  - Corner Illumination
- 2x LVDS Input Data Bus
- Dedicated DLPC4422 Display Controller, DLPA100 Power Management IC and Motor Driver for reliable operation

2 Applications

- Full HD (1080p) Display
- Laser TV
- Mobile Smart TV
- Digital Signage
- Gaming
- Home Cinema

3 Description

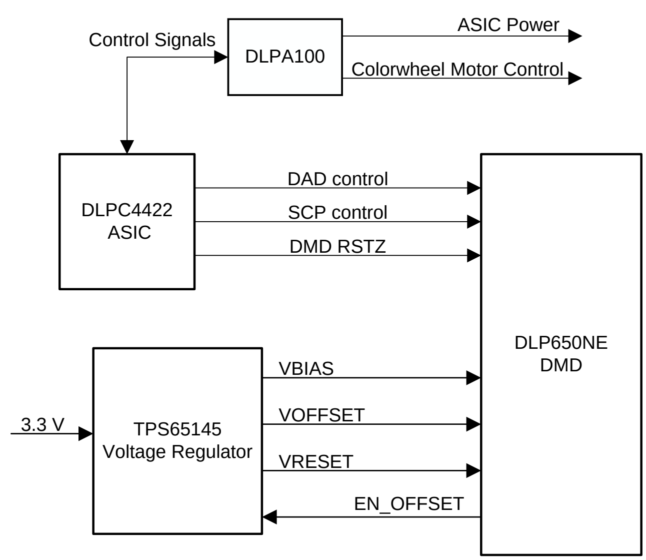
The TI DLP650NE digital micromirror device (DMD) is a digitally controlled micro-opto-electromechanical system (MEMS) spatial light light modulator (SLM) that enables bright, affordable DLP® 0.65 1080p display solutions. The DLP650NE DMD, together with the DLPC4422 display controller and DLPA100 power and motor driver, comprise the DLP 0.65 1080p chipset. The solution is a great fit for display systems that require high resolution, high brightness and system simplicity.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLP650NE	FYE (350)	35.0 mm × 32.2 mm × 5.1 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

DLP650NE 0.65 1080P DMD



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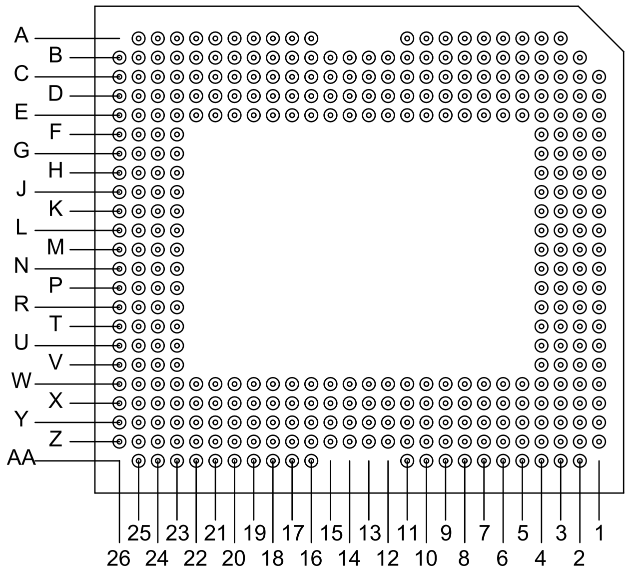
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2017	*	Initial release.

5 Pin Configuration and Functions

FYE Package
350-Pin CPGA
Top View



Pin Functions

PIN (1)		TYPE (2)	SIGNAL	DATA RATE (3)	INTERNAL TERM (4)	DESCRIPTION	TRACE (mils) (5)
NAME	NO.						
DATA BUS A							
D_AN(0)	B14	I	LVDS	DDR	Differential	Data, negative	494.88
D_AN(1)	B15	I	LVDS	DDR	Differential	Data, negative	486.18
D_AN(2)	C16	I	LVDS	DDR	Differential	Data, negative	495.16
D_AN(3)	K24	I	LVDS	DDR	Differential	Data, negative	485.67
D_AN(4)	B18	I	LVDS	DDR	Differential	Data, negative	494.76
D_AN(5)	L24	I	LVDS	DDR	Differential	Data, negative	490.63
D_AN(6)	C19	I	LVDS	DDR	Differential	Data, negative	495.16
D_AN(7)	H24	I	LVDS	DDR	Differential	Data, negative	485.55
D_AN(8)	H23	I	LVDS	DDR	Differential	Data, negative	495.16
D_AN(9)	B25	I	LVDS	DDR	Differential	Data, negative	485.59
D_AN(10)	D24	I	LVDS	DDR	Differential	Data, negative	495.16
D_AN(11)	E25	I	LVDS	DDR	Differential	Data, negative	495.16
D_AN(12)	F25	I	LVDS	DDR	Differential	Data, negative	490.04
D_AN(13)	H25	I	LVDS	DDR	Differential	Data, negative	485.91
D_AN(14)	L25	I	LVDS	DDR	Differential	Data, negative	495.16
D_AN(15)	G24	I	LVDS	DDR	Differential	Data, negative	495.16
D_AP(0)	C14	I	LVDS	DDR	Differential	Data, positive	494.84
D_AP(1)	B16	I	LVDS	DDR	Differential	Data, positive	486.22
D_AP(2)	C17	I	LVDS	DDR	Differential	Data, positive	494.65

(1) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.
(2) I = Input, O = Output, G = Ground
(3) DDR = Double Data Rate. SDR = Single Data Rate. Refer to the Timing Requirements for specifications and relationships.
(4) Internal term - CMOS level internal termination. Refer to Recommended Operating Conditions for differential termination specification.
(5) Dielectric Constant for the DMD S600 ceramic package is approximately 9.6. For the package trace lengths shown: Propagation Speed = 11.8 / sqrt(9.6) = 3.808 in/ns. Propagation Delay = 0.262 ns/in = 262 ps/in = 10.315 ps/mm.

Pin Functions (continued)

PIN[1]		TYPE [2]	SIGNAL	DATA RATE[3]	INTERNAL TERM [4]	DESCRIPTION	TRACE (mils)[5]
NAME	NO.						
D_AP(3)	K23	I	LVDS	DDR	Differential	Data, positive	488.42
D_AP(4)	B19	I	LVDS	DDR	Differential	Data, positive	495.16
D_AP(5)	L23	I	LVDS	DDR	Differential	Data, positive	490.67
D_AP(6)	C20	I	LVDS	DDR	Differential	Data, positive	498.11
D_AP(7)	J24	I	LVDS	DDR	Differential	Data, positive	486.22
D_AP(8)	J23	I	LVDS	DDR	Differential	Data, positive	495.47
D_AP(9)	C25	I	LVDS	DDR	Differential	Data, positive	485.94
D_AP(10)	E24	I	LVDS	DDR	Differential	Data, positive	495.16
D_AP(11)	D25	I	LVDS	DDR	Differential	Data, positive	494.13
D_AP(12)	G25	I	LVDS	DDR	Differential	Data, positive	488.98
D_AP(13)	J25	I	LVDS	DDR	Differential	Data, positive	492.56
D_AP(14)	K25	I	LVDS	DDR	Differential	Data, positive	495.16
D_AP(15)	F24	I	LVDS	DDR	Differential	Data, positive	495.16
DATA BUS B							
D_BN(0)	Z14	I	LVDS	DDR	Differential	Data, negative	494.92
D_BN(1)	Z15	I		DDR	Differential	Data, negative	486.18
D_BN(2)	Y16	I		DDR	Differential	Data, negative	496.46
D_BN(3)	P24	I		DDR	Differential	Data, negative	493.74
D_BN(4)	Z18	I		DDR	Differential	Data, negative	494.76
D_BN(5)	N24	I		DDR	Differential	Data, negative	495.16
D_BN(6)	Y19	I		DDR	Differential	Data, negative	492.16
D_BN(7)	T24	I		DDR	Differential	Data, negative	492.68
D_BN(8)	T23	I		DDR	Differential	Data, negative	484.45
D_BN(9)	Z25	I		DDR	Differential	Data, negative	492.09
D_BN(10)	X24	I		DDR	Differential	Data, negative	497.72
D_BN(11)	W25	I		DDR	Differential	Data, negative	495.16
D_BN(12)	V25	I		DDR	Differential	Data, negative	484.17
D_BN(13)	T25	I		DDR	Differential	Data, negative	481.42
D_BN(14)	N25	I		DDR	Differential	Data, negative	495.16
D_BN(15)	U24	I		DDR	Differential	Data, negative	489.8
D_BP(0)	Y14	I	LVDS	DDR	Differential	Data, positive	494.88
D_BP(1)	Z16	I		DDR	Differential	Data, positive	486.26
D_BP(2)	Y17	I		DDR	Differential	Data, positive	495.16
D_BP(3)	P23	I		DDR	Differential	Data, positive	492.48
D_BP(4)	Z19	I		DDR	Differential	Data, positive	495.16
D_BP(5)	N23	I		DDR	Differential	Data, positive	497.99
D_BP(6)	Y20	I		DDR	Differential	Data, positive	495.16
D_BP(7)	R24	I		DDR	Differential	Data, positive	492.05
D_BP(8)	R23	I		DDR	Differential	Data, positive	484.45
D_BP(9)	Y25	I		DDR	Differential	Data, positive	492.24
D_BP(10)	W24	I		DDR	Differential	Data, positive	495.16
D_BP(11)	X25	I		DDR	Differential	Data, positive	494.72
D_BP(12)	U25	I		DDR	Differential	Data, positive	483.78
D_BP(13)	R25	I		DDR	Differential	Data, positive	489.13
D_BP(14)	P25	I		DDR	Differential	Data, positive	499.53
D_BP(15)	V24	I		DDR	Differential	Data, positive	488.66

Pin Functions (continued)

PIN[(1)] NAME	NO.	TYPE [(2)]	SIGNAL	DATA RATE[(3)]	INTERNAL TERM [(4)]	DESCRIPTION	TRACE (mils)[(5)]
SERIAL CONTROL							
SCTRL_AN	C23	I	LVDS	DDR	Differential	Serial control, negative	492.95
SCTRL_BN	Y23	I	LVDS	DDR	Differential	Serial control, negative	493.78
SCTRL_AP	C24	I	LVDS	DDR	Differential	Serial control, negative	493.78
SCTRL_BP	Y24	I	LVDS	DDR	Differential	Serial control, negative	493.11
CLOCKS							
DCLK_AN	B23	I	LVDS		Differential	Clock, negative	480.35
DCLK_BN	Z23	I	LVDS		Differential	Clock, negative	486.22
DCLK_AP	B22	I	LVDS		Differential	Clock, negative	485.83
DCLK_BP	Z22	I	LVDS		Differential	Clock, negative	491.93
SERIAL COMMUNICATIONS PORT (SCP)							
SCP_DO	B8	O	LVCMOS	SDR		Serial communications port output	
SCP_DI	B7	I	LVCMOS	SDR	Pull-Down	Serial communication port data I	
SCP_CLK	B6	I	LVCMOS		Pull-Down	Serial communications port clock	
SCP_ENZ	C8	I	LVCMOS		Pull-Down	Active-low serial communications port enable	
MICROMIRROR RESET CONTROL							
RESET_ADDR(0)	X9	I	LVCMOS		Pull-Down	Reset driver address select	
RESET_ADDR(1)	X8	I	LVCMOS		Pull-Down	Reset driver address select	
RESET_ADDR(2)	Z8	I	LVCMOS		Pull-Down	Reset driver address select	
RESET_ADDR(3)	Z7	I	LVCMOS		Pull-Down	Reset driver address select	
RESET_MODE(0)	W11	I	LVCMOS		Pull-Down	Reset driver mode select	
RESET_MODE(1)	Z10	I	LVCMOS		Pull-Down	Reset driver mode select	
RESET_SEL(0)	Y10	I	LVCMOS		Pull-Down	Reset driver level select	
RESET_SEL(1)	Y9	I	LVCMOS		Pull-Down	Reset driver level select	
RESET_STROBE	Y7	I	LVCMOS		Pull-Down	Reset address, mode, and level latched on rising-edge	
ENABLES & INTERRUPTS							
PWRDNZ	D2	I	LVCMOS		Pull-Down	Active-low device reset	
RESET_OEZ	W7	I	LVCMOS		Pull-Down	Active-low output enable for DMD reset driver circuits	
RESETZ	Z6	I	LVCMOS		Pull-Down	Active-low sets reset circuits in known VOFFSET state	
RESET_IRQZ	Z5	O	LVCMOS			Active-low, output interrupt to ASIC	
VOLTAGE REGULATOR MONITORING							
PG_BIAS	E11	I	LVCMOS		Pull-Up	Active-low fault from external VBIAS regulator	
PG_OFFSET	B10	I	LVCMOS		Pull-Up	Active-low fault from external VOFFSET regulator	
PG_RESET	D11	I	LVCMOS		Pull-Up	Active-low from external VRESET regulator	
EN_BIAS	D9	O	LVCMOS			Active-high enable for external VBIAS regulator	
EN_OFFSET	C9	O	LVCMOS			Active-high enable for external VOFFSET regulator	
EN_RESET	E9	O	LVCMOS			Active-high enable for external VRESET regulator	

Pin Functions (continued)

PIN[1] NAME	NO.	TYPE[2]	SIGNAL	DATA RATE[3]	INTERNAL TERM[4]	DESCRIPTION	TRACE (mils)[5]
LEAVE PIN UNCONNECTED							
MBRST(0)	C2	O	Analog		Pull-Down	For proper DMD operation, do not connect	
MBRST(1)	C3	O					
MBRST(2)	C5	O					
MBRST(3)	C4	O					
MBRST(4)	E5	O					
MBRST(5)	E4	O					
MBRST(6)	E3	O					
MBRST(7)	G4	O					
MBRST(8)	G3	O					
MBRST(9)	G2	O					
MBRST(10)	J4	O					
MBRST(11)	J3	O					
MBRST(12)	J2	O					
MBRST(13)	L4	O					
MBRST(14)	L3	O					
MBRST(15)	L2	O					
LEAVE PIN UNCONNECTED							
RESERVED_PFE	E7	I	LVCMOS		Pull-Down	For proper DMD operation, do not connect	
RESERVED_TM	D13	I					
RESERVED_XI1	E13	I					
RESERVED_TP0	W12	I	Analog				
RESERVED_TP1	Y11	I					
RESERVED_TP2	X11	I					
LEAVE PIN UNCONNECTED							
RESERVED_BA	Y12	O	LVCMOS			For proper DMD operation, do not connect	
RESERVED_BB	C12	O					
RESERVED_TS	D5	O					
LEAVE PIN UNCONNECTED							
NO CONNECT	B11					For proper DMD operation, do not connect	
NO CONNECT	C11						
NO CONNECT	C13						
NO CONNECT	E12						
NO CONNECT	E14						
NO CONNECT	E23						
NO CONNECT	H4					For proper DMD operation, do not connect	
NO CONNECT	N2						
NO CONNECT	N3						
NO CONNECT	N4						
NO CONNECT	R2						
NO CONNECT	R3						
NO CONNECT	R4						
NO CONNECT	T4						

Pin Functions (continued)

PIN[1]		TYPE[2]	SIGNAL	DATA RATE[3]	INTERNAL TERM [4]	DESCRIPTION	TRACE (mils)[5]
NAME	NO.						
NO CONNECT	U2					For proper DMD operation, do not connect	
NO CONNECT	U3						
NO CONNECT	U4						
NO CONNECT	W3						
NO CONNECT	W4						
NO CONNECT	W5						
NO CONNECT	W13						
NO CONNECT	W14						
NO CONNECT	W23						
NO CONNECT	X4					For proper DMD operation, do not connect	
NO CONNECT	X5						
NO CONNECT	X13						
NO CONNECT	Y2						
NO CONNECT	Y3						
NO CONNECT	Y4						
NO CONNECT	Y5						
NO CONNECT	Z11						

Power Pin Functions

PIN		TYPE (I/O/P) (1)	SIGNAL	DESCRIPTION
NAME (2)	NO.			
VBIAS	A6, A7, A8, AA6, AA7, AA8	P	Analog	Supply voltage for positive Bias level of Micromirror reset signal
VOFFSET	A3, A4, A25		Analog	Supply voltage for HVCMOS logic
	B26, L26, M26		Analog	Supply voltage for stepped high voltage at Micromirror address electrodes
	N26, Z26, AA3, AA4		Analog	Supply voltage for positive Offest level of Micromirror reset signal.
VRESET	G1, H1, J1, R1, T1, U1		Analog	Supply voltage for negative Reset level of Micromirror reset signal.
VCC	A9, B3, B5, B12, C1, C6, C10, D4, D6, D8, E1, E2, E10, E15, E16, E17, F3, H2, K1, K3, M4, P1, P3, T2, V3, W1, W2, W6, W9, W10, W15, W16, W17, X3, X6, Y1, Y8, Y13, Z1, Z3, Z12, AA2, AA9, AA10		Analog	Supply voltage for LVCMOS core logic. Supply voltage for normal high level at Micromirror address electrodes. Supply voltage for positive Offset level of Micromirror reset signal during Power Down sequence.
VCCI	A16, A17, A18, A20, A21, A23, AA16, AA17, AA18, AA20, AA21, AA23		Analog	Supply voltage for LVDS receivers.
VSS	A5, A10, A11, A19, A22, A24, B2, B4, B9, B13, B17, B20, B21, B24, C7, C15, C18, C21, C22, C26, D1, D3, D7, D10, D12, D14, D15, D16, D17, D18, D19, D20, D21, D22, D23, D26, E6, E8, E18, E19, E20, E21, E22, E26, F1, F2, F4, F23, F26, G23, G26, H3, H26, J26, K2, K4, K26, L1, M1, M2, M3, M23, M24, M25, N1, P2, P4, P26, R26, T3, T26, U23, U26, V1, V2, V4, V23, V26, W8, W18, W19, W20, W21, W22, W26, X1, X2, X7, X10, X12, X14, X15, X16, X17, X18, X19, X20, X21, X22, X23, X26, Y6, Y15, Y18, Y21, Y22, Y26, Z2, Z4, Z9, Z13, Z17, Z20, Z21, Z24, AA5, AA11, AA19, AA22, AA24		Analog	Device ground. Common return for all power.

(1) P = Power
(2) The following power supplies are required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
SUPPLY VOLTAGES				
VCC	Supply voltage for LVCMOS core logic (2)	–0.5	4	V
VCCI	Supply voltage for LVDS receivers(2)	–0.5	4	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrode (2) (3)	–0.5	9	V
VBIAS	Supply voltage for micromirror electrode (2)	–0.5	17	V
VRESET	Supply voltage for micromirror electrode (2)	–11	0.5	V
| VCC – VCCI |	Supply voltage change (absolute value) (4)		0.3	V
| VBIAS – VOFFSET |	Supply voltage change (absolute value) (5)		8.75	V
INPUT VOLTAGES				
	Input voltage for all other LVCMOS input pins (2)	–0.5	VCC + 0.15	V
	Input voltage for all other LVDS input pins (2) (6)	–0.5	VCCI + 0.15	V
| V_{ID} |	Input differential voltage (absolute value) (7)		700	mV
I_{ID}	Input differential current (7)		7	mA
CLOCKS				
f_{clock}	Clock frequency for LVDS interface, DCLK (all channels)		460	MHz
ENVIRONMENTAL				
T_{ARRAY} and T_{WINDOW}	Temperature: operational : Reference Locations TP2 and TP3(8) (9)	10	90	ºC
	Temperature: operational : Reference Locations TP1(8) (9)	10	70	ºC
	Temperature: non–operational (9)	–40	80	ºC
T_{DP}	Dew Point temperature, operating and non-operating (non-condensing)		81	ºC

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(3) VOFFSET supply transients must fall within specified voltages.
(4) To prevent excess current, the supply voltage change |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage change |VBIAS – VOFFSET| must be less than specified limit. Refer to Power Supply Requirements for additional information.
(6) This maximum LVDS input voltage rating applies when each input of a differential pair is at the same voltage potential.
(7) LVDS differential inputs must not exceed the specified limit or damage may result to the internal termination resistors
(8) Exposure of the DMD simultaneously to any combination of the maximum operating conditions for case temperature, differential temperature, or illumination power density reduces the device lifetime.
(9) The highest temperature of the active array (as calculated by the Micromirror Array Temperature Calculation) or of any point along the Window Edge as defined in Figure 15. The locations of thermal test points TP2, TP3, TP4 and TP5 in Figure 15 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, add a test point to that location.

6.2 Storage Conditions

applicable before the DMD is installed in the final product

		MIN	MAX	UNIT
T_{DMD}	DMD storage temperature	–40	80	°C
T_{DP-AVG}	Average dew point temperature (non-condensing) (1)		28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) (2)	28	36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range		24	Months

(1) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(2) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.

6.3 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY VOLTAGES[1] [2]					
VCC	Supply voltage for LVCMOS core logic	3.15	3.3	3.45	V
VCCI	Supply voltage for LVDS receivers	3.15	3.3	3.45	V
VOFFSET	Supply voltage for HVCMOS and micromirror electrodes[2]	8.25	8.5	8.75	V
VBIAS	Supply voltage for micromirror electrodes	15.5	16	16.5	V
VRESET	Supply voltage for micromirror electrodes	–9.5	–10	–10.5	V
|VCCI–VCC|	Supply voltage change (absolute value) [3]		0	0.3	V
|VBIAS–VOFFSET|	Supply voltage change (absolute value)[4]			8.75	V
LVCMOS PINS					
V_{IH}	High level Input voltage [5]	1.7	2.5	VCC + 0.15	V
V_{IL}	Low level Input voltage[5]	– 0.3		0.7	V
I_{OH}	High level output current at V_{OH} = 2.4 V			–20	mA
I_{OL}	Low level output current at V_{OL} = 0.4 V			15	mA
T_{PWRDNZ}	PWRDNZ pulse width[6]	10			ns
SCP INTERFACE[7]					
f_{clock}	SCP clock frequency[8]			500	kHz
t_{SCP_SKEW}	Time between valid SCPDI and rising edge of SCPCLK[9]	–800		800	ns
t_{SCP_DELAY}	Time between valid SCPDO and rising edge of SCPCLK[9]			700	ns
$t_{SCP\_BYTE\_INTERVAL}$	Time between consecutive bytes	1			µs
$t_{SCP\_NEG\_ENZ}$	Time between falling edge of SCPENZ and the first rising edge of SCPCLK	30			ns
$t_{SCP\_PW\_ENZ}$	SCPENZ inactive pulse width (high level)	1			µs
$t_{SCP\_OUT\_EN}$	Time required for SCP output buffer to recover after SCPENZ (from tri-state)			1.5	ns
f_{clock}	SCP circuit clock oscillator frequency [10]	9.6		11.1	MHz

(1) Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) VOFFSET supply transients must fall within specified max voltages.
(3) To prevent excess current, the supply voltage change |VCCI – VCC| must be less than specified limit.
(4) To prevent excess current, the supply voltage change |VBIAS – VOFFSET| must be less than specified limit. Refer to the *Power Supply Requirements* section for additional information.
(5) Tester conditions for V_{IH} and V_{IL}:
Frequency = 60 MHz. Maximum Rise Time = 2.5 ns at (20% to 80%)
Frequency = 60 MHz. Maximum Fall Time = 2.5 ns at (80% to 20%)
(6) PWRDNZ input pin resets the SCP and disables the LVDS receivers. PWRDNZ input pin overrides SCPENZ input pin and tri-states the SCPDO output pin.
(7) For all Serial Communications Port (SCP) operations, DCLK_A and DCLK_B are required.
(8) The SCP clock is a gated clock. Duty cycle shall be 50% ± 10%. SCP parameter is related to the frequency of DCLK.
(9) Refer to Figure 2.
(10) SCP internal oscillator is specified to operate all SCP registers. For all SCP operations, DCLK is required.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
LVDS INTERFACE					
f_{clock}	Clock frequency for LVDS interface, DCLK (all channels)			400	MHz
$\|V_{ID}\|$	Input differential voltage (absolute value)[11]	100	400	600	mV
V_{CM}	Common mode [11]		1200		mV
V_{LVDS}	LVDS voltage[11]	0		2000	mV
t_{LVDS_RSTZ}	Time required for LVDS receivers to recover from PWRDNZ			10	ns
Z_{IN}	Internal differential termination resistance	95		105	Ω
Z_{LINE}	Line differential impedance (PWB/trace)	90	100	110	Ω
ENVIRONMENTAL [12]					
T_{ARRAY}	Array temperature – operational, long-term [13] [14] [15]	10		40 to 70[16]	°C
	Array temperature – operational, short-term [13] [14] [17]	0		10	
T_{WINDOW}	Window temperature – operational[18]			85	°C
$T_{\|DELTA\|}$	Absolute temperature change between any point on the window edge and the ceramic test point TP1. [19]			26	°C
T_{DP-AVG}	Average dew point temperature (non-condensing) [20]			28	°C
T_{DP-ELR}	Elevated dew point temperature range (non-condensing) [21]	28		36	°C
CT_{ELR}	Cumulative time in elevated dew point temperature range			24	Months
ILL_{UV}	Illumination, wavelength < 395 nm [21]		0.68	2.0	mW/cm^2
ILL_{VIS}	Illumination, wavelength between 395 nm and 800 nm			Thermally Limited	
ILL_{IR}	Illumination, wavelength > 800 nm			10	mW/cm^2

(11) Refer to Figure 3, Figure 4, and Figure 5.
(12) Optimal, long-term performance and optical efficiency of the Digital Micromirror Device (DMD) can be affected by various application parameters, including illumination spectrum, illumination power density, micromirror landed duty-cycle, ambient temperature (storage and operating), DMD temperature, ambient humidity (storage and operating), and power on or off duty cycle. TI recommends that application-specific effects be considered as early as possible in the design cycle.
(13) Simultaneous exposure of the DMD to the maximum *Recommended Operating Conditions* for temperature and UV illumination reduces device lifetime.
(14) The array temperature cannot be measured directly and must be computed analytically from the temperature measured at test point 1 (TP1) shown in Figure 15 and the package thermal resistance in *Thermal Information* using *Micromirror Array Temperature Calculation*.
(15) Long-term is defined as the average over the usable life.
(16) Per Figure 1, base the maximum operational case temperature derating on the micromirror landed duty cycle that the DMD experiences in the end application. Refer to *Micromirror Landed-on or Landed-Off Duty Cycle* for a definition of micromirror landed duty cycle.
(17) Array temperatures beyond the specified long-term operational DMD temperature are recommended for short-term conditions only (for example, power-up). Short-term is defined as cumulative time over the usable life of the device and is less than 500 hours.
(18) The locations of thermal test points TP2, TP3, TP4 and TP5 in Figure 15 are intended to measure the highest window edge temperature. If a particular application causes another point on the window edge to be at a higher temperature, add a test point to that location. This ensures that the window bond temperature does not exceed the limits in *Absolute Maximum Ratings*
(19) Temperature change is the highest difference between the ceramic test point 1 (TP1) and anywhere on the window edge as shown in Figure 15 The window test points TP2, TP3, TP4 and TP5 shown in Figure 15 are intended to result in the worst-case temperature change. If a particular application causes another point on the window edge to result in a larger temperature change, use that point.
(20) The average over time (including storage and operating) that the device is not in the 'elevated dew point temperature range'.
(21) Limit exposure to dew point temperatures in the elevated range during storage and operation to less than a total cumulative time of CT_{ELR}.

6.5 Thermal Information

THERMAL METRIC(1)		DLP650NE FYE (CPGA) 350 PINS	UNIT
$R_{ARRAY\text{–}TO\text{–}CERAMIC}$	Active Area-to-Case Ceramic Thermal resistance (2)	0.6	°C/W

(1) The DMD is designed to conduct absorbed and dissipated heat to the back of the package where it can be removed by an appropriate heat sink. The heat sink and cooling system must be capable of maintaining the package within the temperature range specified in the *Recommended Operating Conditions* table. The total heat load on the DMD is largely driven by the incident light absorbed by the active area; although other contributions include light energy absorbed by the window aperture and electrical power dissipation of the array. Design optical systems to minimize the light energy falling outside the window clear aperture because any additional thermal load in this area can significantly degrade the reliability of the device.
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

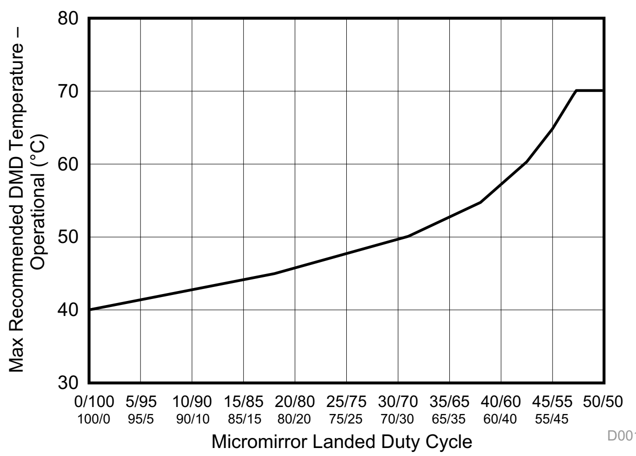


Figure 1. Recommended Maximum DMD Temperature – Derating Curve

6.6 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	VCC = 3.3 V, I_{OH} = –20 mA	2.4			V
V_{OL}	Low -level output voltage	VCC = 3.45 V, I_{OL} = 15 mA			0.4	V
I_{IH}	High-level input current[2] [3]	VCC = 3.45 V , V_I = VCC			250	µA
I_{IL}	Low-level input current	VCC = 3.45 V, V_I = 0	–250			µA
I_{OZ}	High–impedance output current	VCC = 3.45 V			10	µA
CURRENT						
I_{CC}	Supply current [4]	VCC = 3.45 V			1100	mA
I_{CCI}		VCCI = 3.45 V			500	
I_{OFFSET}	Supply current [5]	VOFFSET = 8.75 V			25	mA
I_{BIAS}		VBIAS = 16.5 V			14	
I_{RESET}	Supply current	VRESET = –10.5 V			11	mA
I_{TOTAL}		Total Sum			1650	
CAPACITANCE						
C_I	Input capacitance	f = 1 MHz			10	pF
C_O	Output capacitance	f = 1 MHz			10	pF
C_M	Reset group capacitance MBRST(14:0)	f = 1 MHz all inputs interconnected, (1920 x 1080) array	330		390	pF

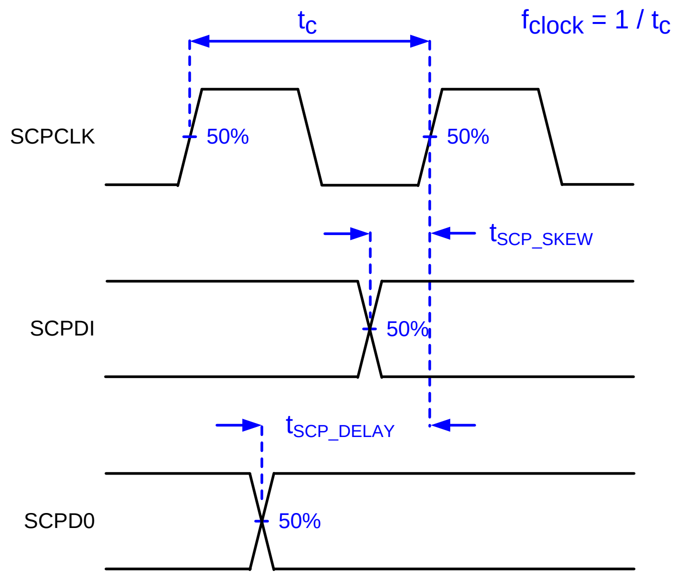
(1) All voltages are referenced to common ground VSS. Supply voltages VCC, VCCI, VOFFSET, VBIAS, and VRESET are all required for proper DMD operation. VSS must also be connected.
(2) Applies to LVCMOS input pins only. Does not apply to LVDS pins and MBRST pins.
(3) LVCMOS input pins utilize an internal 18000 Ω passive resistor for pull-up and pull-down configurations. Refer to *Pin Configuration and Functions* to determine pull-up or pull-down configuration used.
(4) To prevent excess current, the supply voltage change |VCCI – VCC| must be less than specified limit.
(5) To prevent excess current, the supply voltage change |VBIAS – VOFFSET| must be less than specified limit.

6.7 Timing Requirements

Over *Recommended Operating Conditions* unless otherwise noted.(1)

		DESCRIPTION(2)		MIN	TYP	MAX	UNIT
SCP INTERFACE(3)							
t_r	Rise time	20% to 80%				200	ns
t_f	Fall time	80% to 20%				200	ns
LVDS INTERFACE(3)							
t_r	Rise time	20% to 80%		100		400	ps
t_f	Fall time	80% to 20%		100		400	ps
LVDS CLOCKS(4)							
t_c	Cycle time	DCLK_A, 50% to 50%		2.5			ns
		DCLK_B, 50% to 50%		2.5			
t_w	Pulse duration	DCLK_A, 50% to 50%		1.19	1.25		ns
		DCLK_B, 50% to 50%		1.19	1.25		
LVDS INTERFACE(4)							
t_{su}	Setup time	D_A(15:0) before rising or falling edge of DCLK_A		0.1			ns
		D_B(15:0) before rising or falling edge of DCLK_B		0.1			
t_{su}	Setup time	SCTRL_A before rising or falling edge of DCLK_A		0.1			ns
		SCTRL_B before rising or falling edge of DCLK_B		0.1			
t_h	Hold time	D_A(15:0) after rising or falling edge of DCLK_A		0.4			ns
		D_B(15:0) after rising or falling edge of DCLK_B		0.4			
t_h	Hold time	SCTRL_A after rising or falling edge of DCLK_A		0.3			ns
		SCTRL_B after rising or falling edge of DCLK_B		0.3			
LVDS INTERFACE(5)							
t_{skew}	Skew time	Channel B relative to Channel A (5)	Channel A includes the following LVDS pairs: DCLK_AP and DCLK_AN SCTRL_AP and SCTRL_AN D_AP(15:0) and D_AN(15:0)	–1.25		1.25	ns
			Channel B includes the following LVDS pairs: DCLK_BP and DCLK_BN SCTRL_BP and SCTRL_BN D_BP(15:0) and D_BN(15:0)				

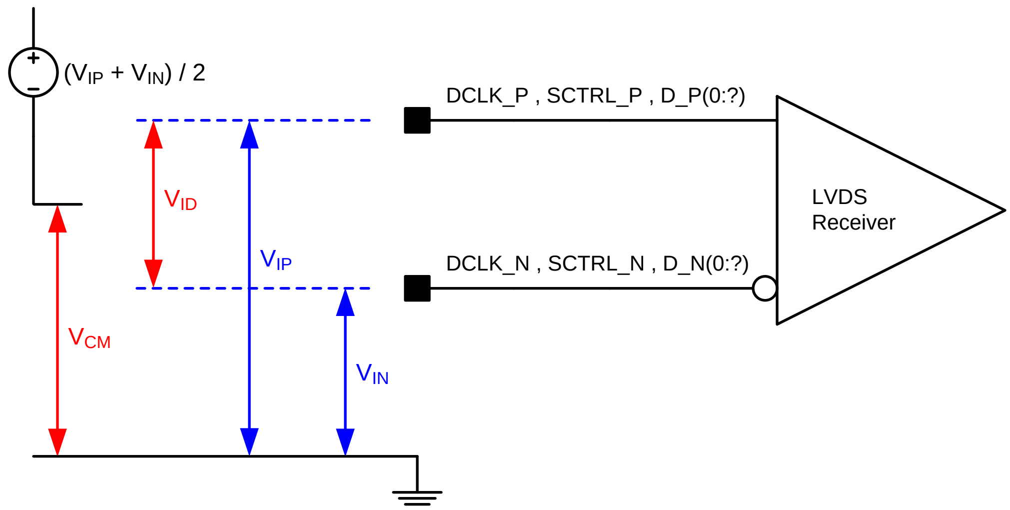
(1) Tested at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account
(2) Refer to *Pin Configuration and Functions* for pin details.
(3) Refer to Figure 6.
(4) Refer to Figure 7.
(5) Refer to Figure 8.



Not to scale.

Refer to SCP Interface section of the Recommended Operating Conditions table.

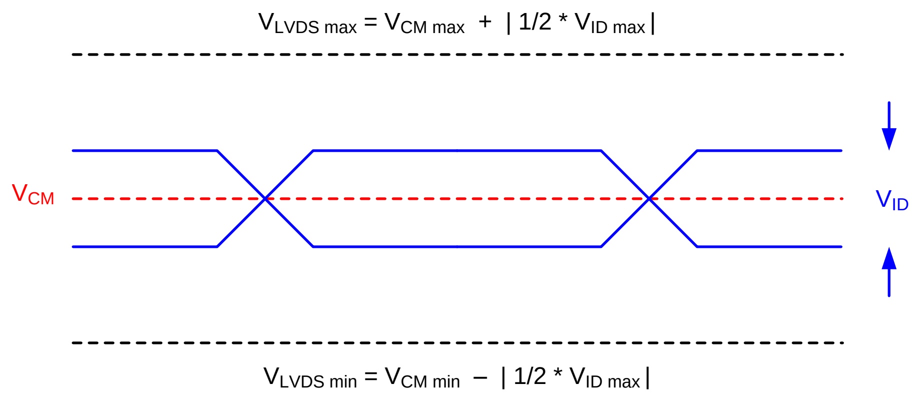
Figure 2. SCP Timing Parameters



Refer to LVDS Interface section of the Recommended Operating Conditions table.

Refer to Pin Configuration and Functions for list of LVDS pins.

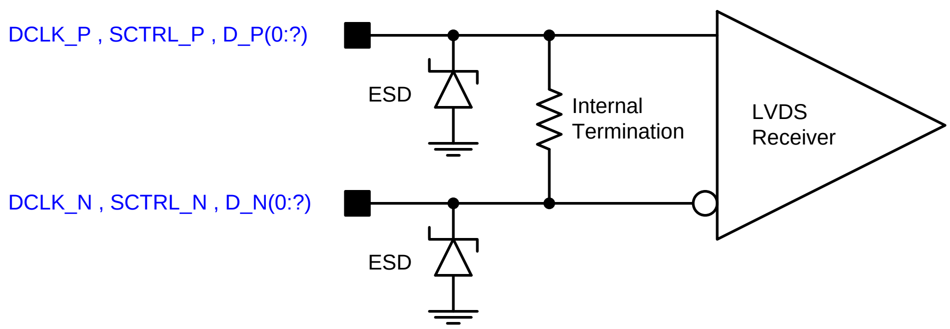
Figure 3. LVDS Voltage Definitions (References)



Not to scale.

Refer to LVDS Interface section of the Recommended Operating Conditions table.

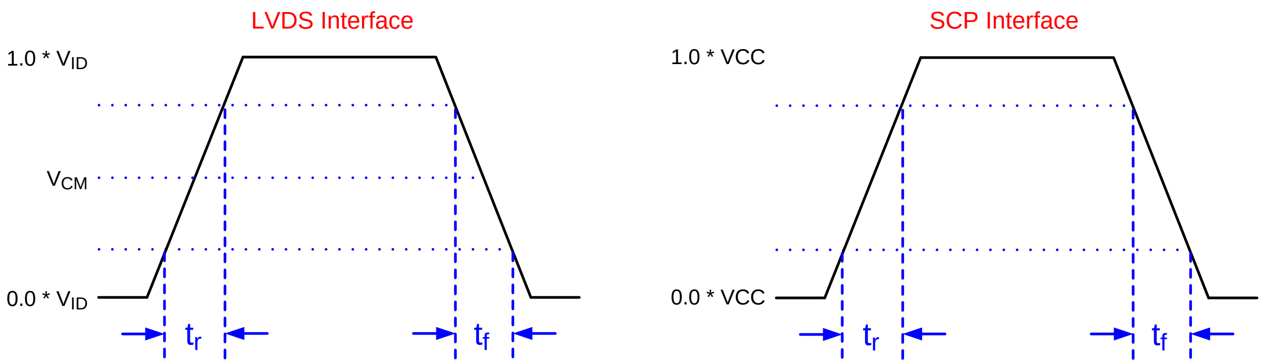
Figure 4. LVDS Voltage Parameters



Refer to LVDS Interface section of the *Recommended Operating Conditions* table.

Refer to for list of LVDS pins.

Figure 5. LVDS Equivalent Input Circuit

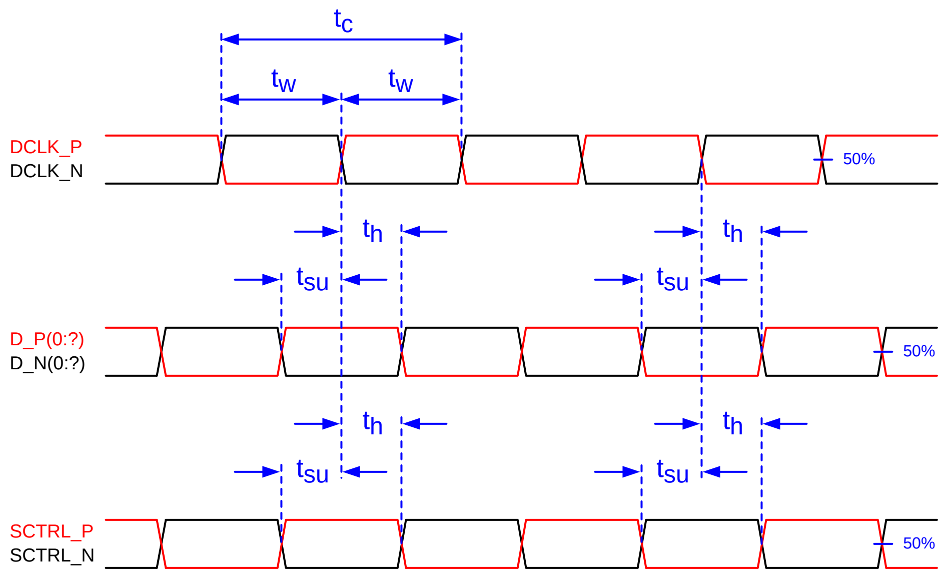


Not to scale.

Refer to the *Timing Requirements*

Refer to in for list of LVDS pins and SCP pins.

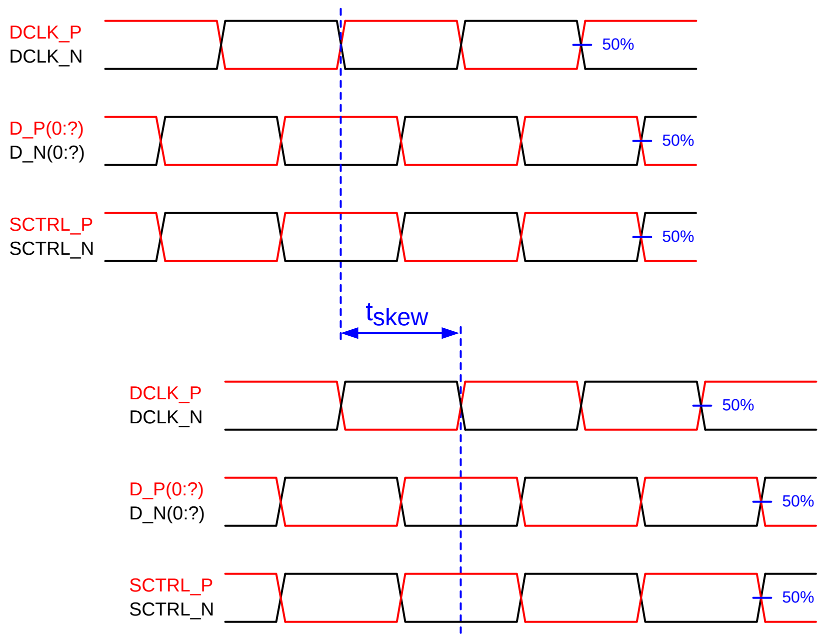
Figure 6. Rise Time and Fall Time



Not to scale.

Refer to LVDS INTERFACE section in the *Timing Requirements* table.

Figure 7. Timing Requirement Parameter Definitions



Not to scale.

Refer to LVDS INTERFACE section in the *Timing Requirements* table.

Figure 8. LVDS Interface Channel Skew Definition

6.8 System Mounting Interface Loads[(1)(2)]

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Maximum system mounting interface load[(3)]	Thermal interface area			11.30	kg
	Electrical Interface areas			11.30	
Maximum load applied [(4)]	Thermal interface area			0	kg
	Electrical interface areas			22.60	

(1) See Figure 9
(2) Combined loads of the thermal and electrical interface areas in excess of Datum "A" load shall be evenly distributed outside the Datum "A" area (300 + 35 – Datum "A").
(3) Evenly distributed within each area
(4) Unevenly distributed within each area.

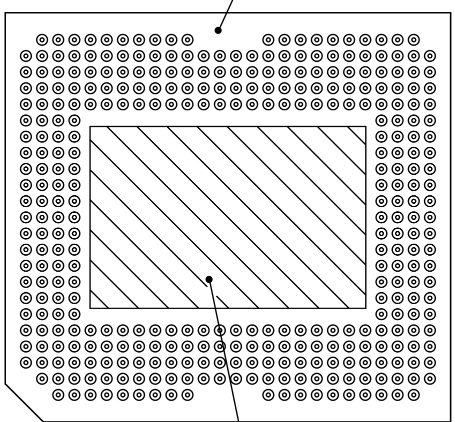
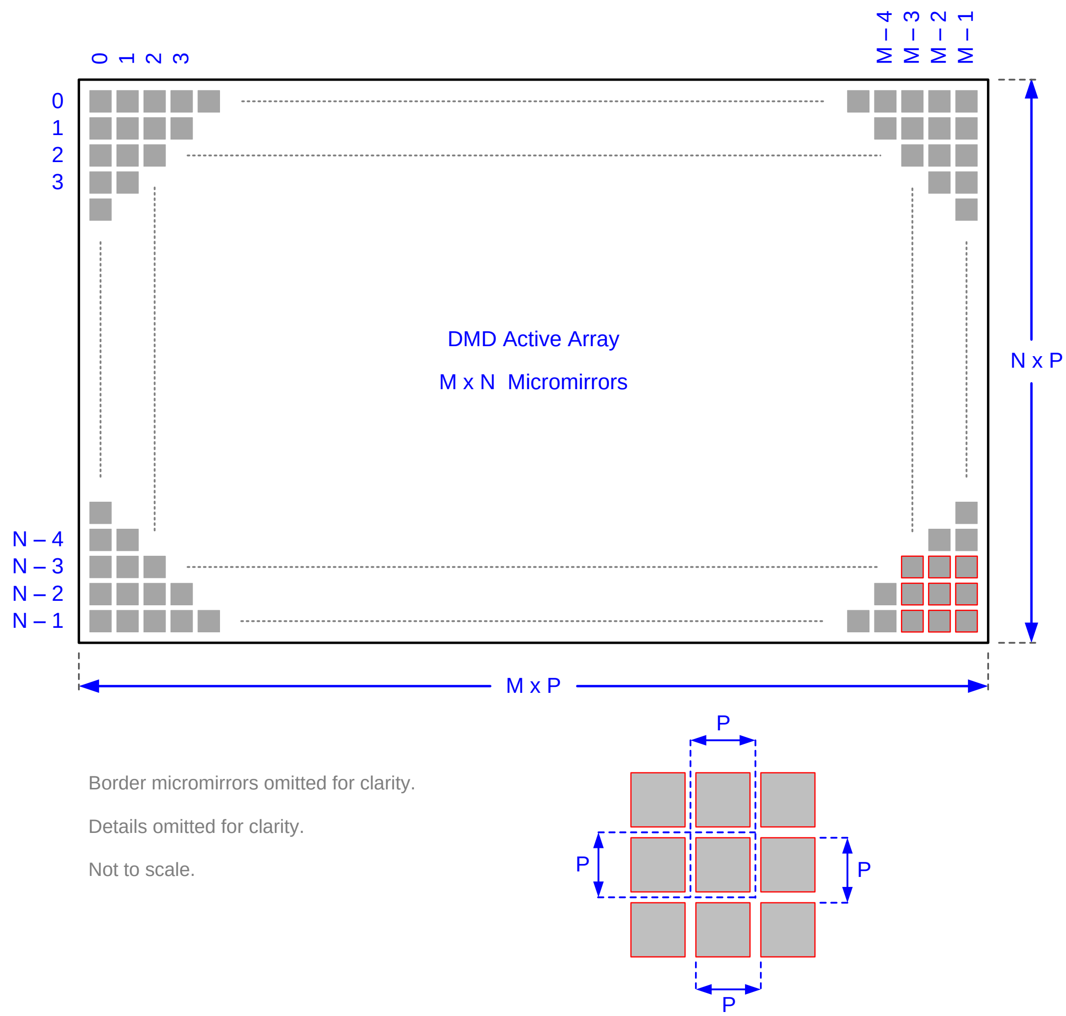


Figure 9. System Mounting Interface Loads

6.9 Micromirror Array Physical Characteristics

				VALUE	UNIT
M	Number of active columns		See Figure 10	1920	micromirrors
N	Number of active rows			1080	micromirrors
P	Micromirror (pixel) pitch			7.56	µm
	Micromirror active array width	M × P		14.5152	mm
	Micromirror active array height	N × P		8.1648	mm
	Micromirror active border	Pond of micromirrors (POM)[(1)]		14	micromirrors /side

(1) The structure and qualities of the border around the active array includes a band of partially functional micromirrors (POM). These micromirrors are structurally and/or electrically prevented from tilting toward the bright or ON state, but still require an electrical bias to tilt toward OFF.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 10. Micromirror Array Physical Characteristics

6.10 Micromirror Array Optical Characteristics

See *Optical Interface and System Image Quality* for important information

	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
α	Micromirror tilt angle	DMD landed state (1)		12		°
β	Micromirror tilt angle tolerance (1) (2) (3) (4) (5)		–1		1	°
	Micromirror tilt direction (5) (6) (7)		44	45	46	°

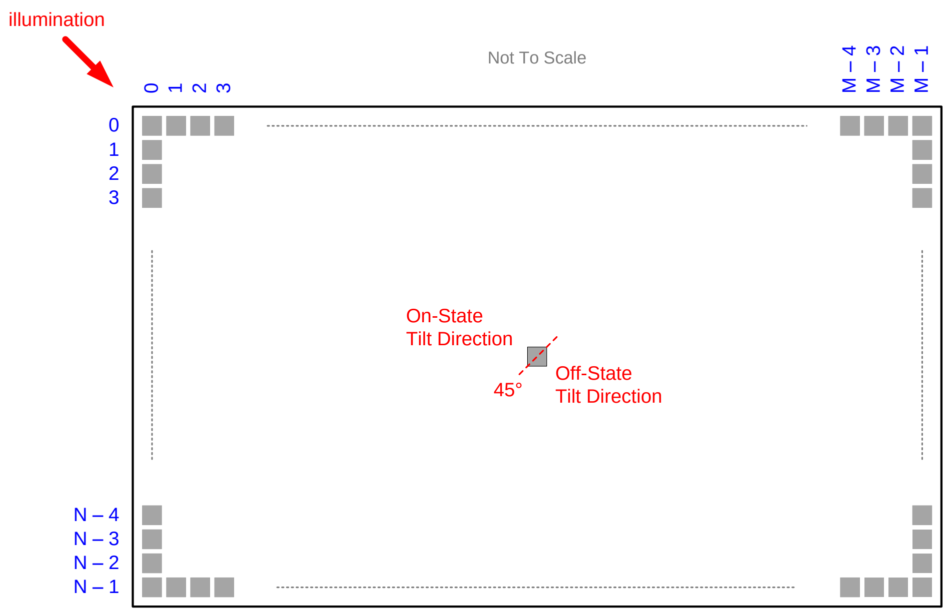
(1) Measured relative to the plane formed by the overall micromirror array. For more information please refer to Figure 14
(2) Additional variation exists between the micromirror array and the package datums.
(3) Represents the landed tilt angle variation relative to the nominal landed tilt angle.
(4) Represents the variation that can occur between any two individual micromirrors, located on the same device or located on different devices.
(5) For some applications, it is critical to account for the micromirror tilt angle variation in the overall system optical design. With some system optical designs, the micromirror tilt angle variation within a device may result in perceivable non-uniformities in the light field reflected from the micromirror array. With some system optical designs, the micromirror tilt angle variation between devices may result in colorimetry variations, system efficiency variations or system contrast variations.
(6) When the micromirror array is landed (not parked), the tilt direction of each individual micromirror is dictated by the binary contents of the CMOS memory cell associated with each individual micromirror. A binary value of 1 results in a micromirror landing in the ON State direction. A binary value of 0 results in a micromirror landing in the OFF State direction.
(7) Refer to Figure 11.

Micromirror Array Optical Characteristics (continued)

See *Optical Interface and System Image Quality* for important information

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Number of out-of-specification micromirrors (8)	Adjacent micromirrors			0	micromirrors
	Non-adjacent micromirrors			10	
Micromirror crossover time (9) (10)	Typical performance		2.5		µs
Mirror Metal Specular Reflectivity within the wavelength range 420nm – 700nm			89.4%		
DMD photopic efficiency within the wavelength range 420 nm to 700 nm (11)			66%		

(8) An out-of-specification micromirror is defined as a micromirror that is unable to transition between the two landed states within the specified Micromirror Switching Time.
(9) Micromirror crossover time is primarily a function of the natural response time of the micromirrors.
(10) Performance as measured at the start of life.
(11) Efficiency numbers assume 24-degree illumination angle, F/2.4 illumination and collection cones, uniform source spectrum, and uniform pupil illumination. Efficiency numbers assume 100% electronic mirror duty cycle and do not include optical overfill loss. Note that this number is specified under conditions described above and deviations from the specified conditions could result in decreased efficiency.



Refer to section *Micromirror Array Physical Characteristics* table for M, N, and P specifications.

Figure 11. Micromirror Landed Orientation and Tilt

6.11 Window Characteristics

PARAMETER (1)	CONDITIONS	MIN	NOM	MAX	UNIT
Window material designation S600	Corning Eagle XG				
Window refractive index	at wavelength 546.1 nm		1.5119		
Window aperture	See (2)				
Illumination overfill	Refer to *Illumination Overfill*				

(1) See *Window Characteristics and Optics* for more information.
(2) For details regarding the size and location of the window aperture, see the package mechanical characteristics listed in the Mechanical ICD in the Mechanical, Packaging, and Orderable Information section.

Window Characteristics (continued)

PARAMETER[1]	CONDITIONS	MIN	NOM	MAX	UNIT
Window transmittance, single–pass through both surfaces and glass [3]	Minimum window transmittance T_{MIN} measured at all angles between 0 AOI and 30 AOI (single pass) over the wavelength range (between 420 nm and 680 nm)	97%			
	Average Window Transmittance Tave measured at all angles 0 – 30 AOI (single pass) over the wavelength range (420 nm – 680 nm)[4]	99%			
	Average Window Transmittance Tave measured at all angles 30 – 45 AOI (single pass) over the wavelength range (420nm – 680nm)	97%			

(3) See the TI application report *Wavelength Transmittance Considerations for DLP® DMD Window*, .
(4) Angle of incidence 0° to 45° at 420 nm to 680 nm. Double pass system. Two AR coating surfaces at 0.5% reflectivity per AR coating up to 30° AOI.

6.12 Chipset Component Usage Specification

The DLP650NE is a component of one or more DLP chipsets. Reliable function and operation of the DLP650NE requires that it be used in conjunction with the other components of the applicable DLP chipset, including those components that contain or implement TI DMD control technology. TI DMD control technology are the TI technology and devices for operating or controlling a DLP DMD.

7 Parameter Measurement Information

Figure 12 shows an equivalent test load circuit for the output under test. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. Use IBIS or other simulation tools to correlate the timing reference load to a system environment. Refer to the *Application and Implementation* section.

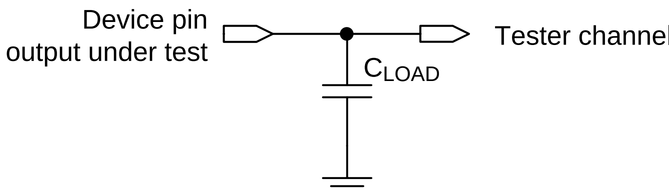


Figure 12. Test Load Circuit

8 Detailed Description

8.1 Overview

DLP650NE is a 0.65 inch diagonal spatial light modulator which consists of an array of highly reflective aluminum micromirrors. Pixel array size and square grid pixel arrangement are shown in Figure 10.

The DMD is an electrical input, optical output micro-electrical-mechanical system (MEMS). The electrical interface is Low Voltage Differential Signaling (LVDS), Double Data Rate (DDR).

DLP650NE DMD consists of a two-dimensional array of 1-bit CMOS memory cells. The array is organized in a grid of *M* memory cell columns by *N* memory cell rows. Refer to the *Functional Block Diagram*.

The positive or negative deflection angle of the micromirrors can be individually controlled by changing the address voltage of underlying CMOS addressing circuitry and micromirror reset signals (MBRST).

Each cell of the $M \times N$ memory array drives its true and complement (‘Q’ and ‘QB’) data to two electrodes underlying one micromirror, one electrode on each side of the diagonal axis of rotation. Refer to *Micromirror Array Optical Characteristics*. The micromirrors are electrically tied to the micromirror reset signals (MBRST) and the micromirror array is divided into reset groups.

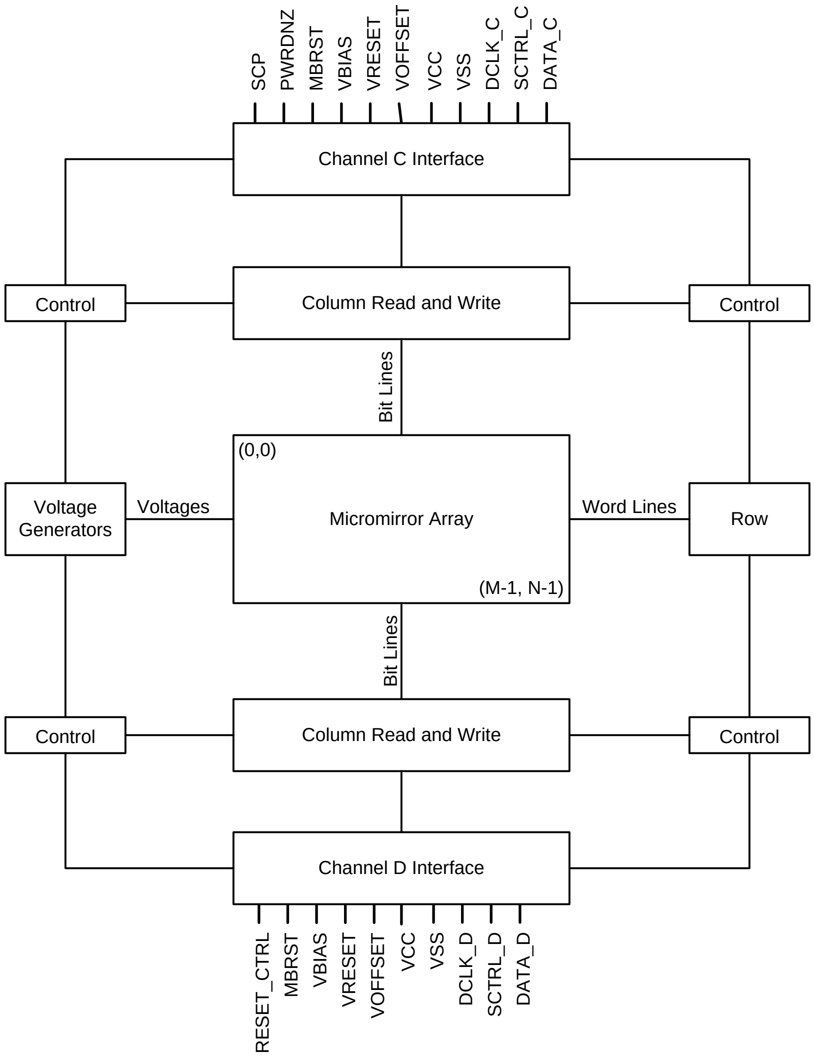
Electrostatic potentials between a micromirror and its memory data electrodes cause the micromirror to tilt toward the illumination source in a DLP projection system or away from it, thus reflecting its incident light into or out of an optical collection aperture. The positive (+) tilt angle state corresponds to an 'on' pixel, and the negative (–) tilt angle state corresponds to an 'off' pixel.

Refer to *Micromirror Array Optical Characteristics* for the ± tilt angle specifications. Refer to *Pin Configuration and Functions* for more information on micromirror reset control.

8.2 Functional Block Diagram

The main LVDS lines going to the DMD are connected via channel A and B. However, the LVDS lines come from channel C and D off the DLPC4422. Please refer to the DLPC4422 datasheet for more information.

Functional Block Diagram (continued)



For pin details on Channels A, B, C, and D, refer to *Pin Configuration and Functions* and LVDS Interface section of *Timing Requirements* .

8.3 Feature Description

8.3.1 Micromirrors

DLP650NE device consists of highly reflective, digitally switchable, micrometer-sized mirrors (micromirrors) organized in a two-dimensional orthogonal pixel array. Refer to Figure 10 and Figure 13.

Each aluminum micromirror is switchable between two discrete angular positions, $-\alpha$ and $+\alpha$. The angular positions are measured relative to the micromirror array plane, which is parallel to the silicon substrate. Refer to *Micromirror Array Optical Characteristics* and Figure 14.

The parked position of the micromirror is not a latched position and is therefore not necessarily perfectly parallel to the array plane. Individual micromirror flat state angular positions may vary. Tilt direction of the micromirror is perpendicular to the hinge-axis. The on-state landed position is directed toward the left-top edge of the package, as shown in Figure 13.

Each individual micromirror is positioned over a corresponding CMOS memory cell. The angular position of a specific micromirror is determined by the binary state (logic 0 or 1) of the corresponding CMOS memory cell contents, after the mirror *clocking pulse* is applied. The angular position ($-\alpha$ and $+\alpha$) of the individual micromirrors changes synchronously with a micromirror clocking pulse, rather than being coincident with the CMOS memory cell data update.

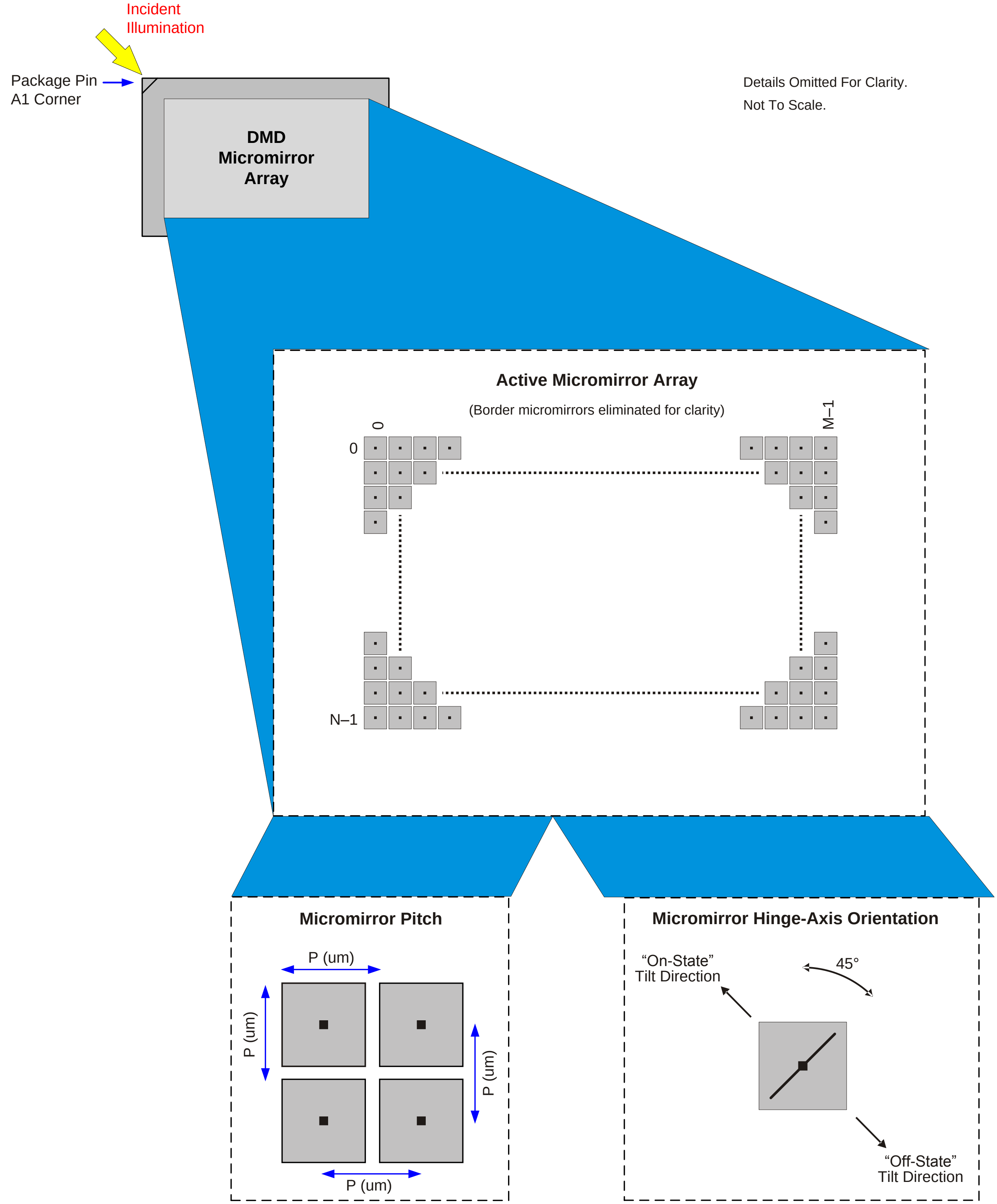
Writing logic 1 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a $+\alpha$ position. Writing logic 0 into a memory cell followed by a mirror clocking pulse results in the corresponding micromirror switching to a $-\alpha$ position.

Updating the angular position of the micromirror array consists of two steps:
- Update the contents of the CMOS memory.
- Apply a micromirror reset to all or a portion of the micromirror array (depending upon the configuration of the system).

Micromirror reset pulses are generated internally by the DLP650NE DMD, with application of the pulses being coordinated by the DLPC4422 display controller.

For more information, see the TI application report DLPA008A, *DMD101: Introduction to Digital Micromirror Device (DMD) Technology*.

Feature Description (continued)



Refer to *Micromirror Array Physical Characteristics*, Figure 10, and Figure 11

Figure 13. Micromirror Array, Pitch, Hinge Axis Orientation

Feature Description (continued)

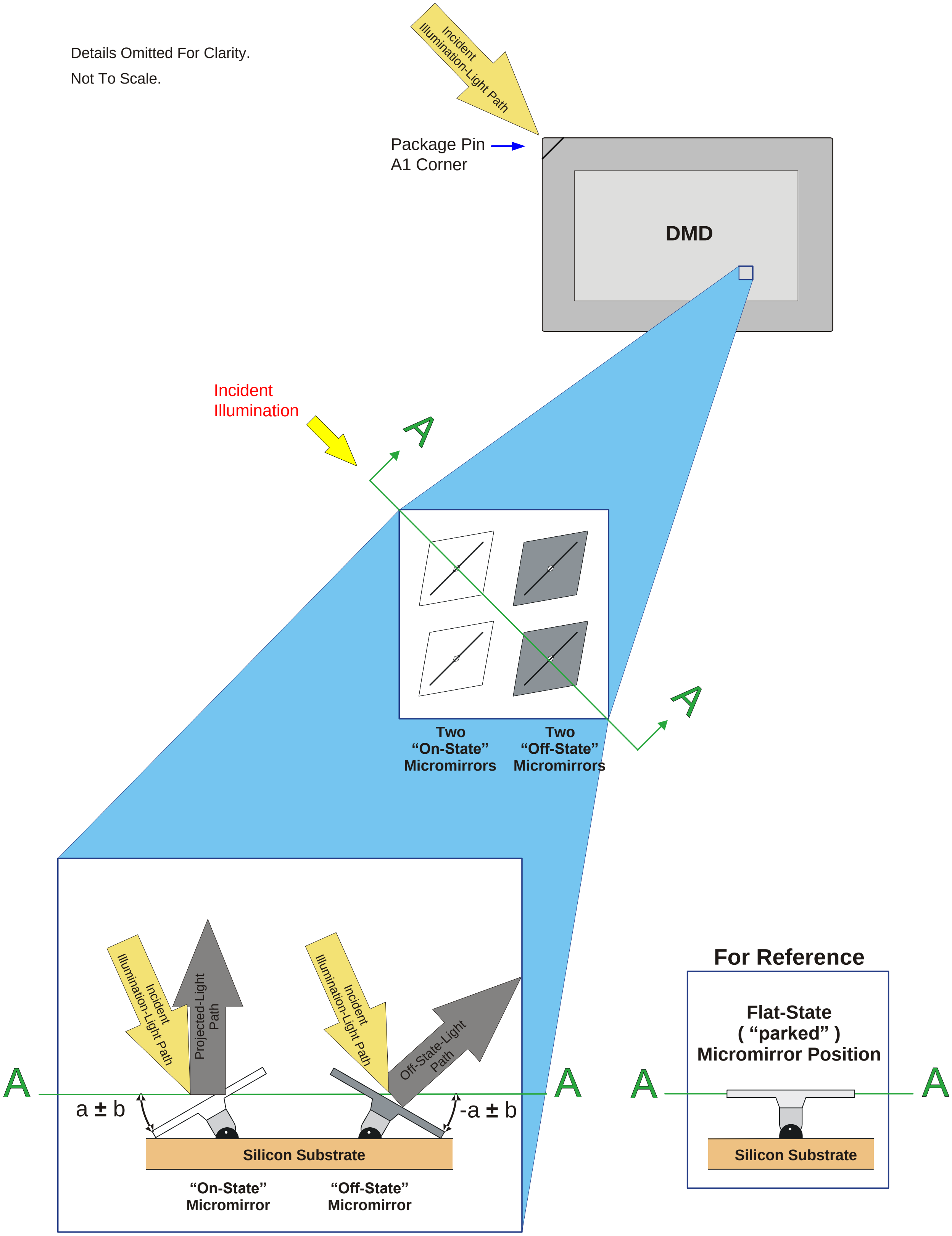


Figure 14. Micromirror States: On, Off, Flat

Feature Description (continued)

8.3.2 Timing

The data sheet provides timing analysis as measured at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. Figure 12 shows an equivalent test load circuit for the output under test. Timing reference loads are not intended as a precise representation of any particular system environment or depiction of the actual load presented by a production test. TI suggests that system designers use IBIS or other simulation tools to correlate the timing reference load to a system environment. The load capacitance value stated is only for characterization and measurement of AC timing signals. This load capacitance value does not indicate the maximum load the device is capable of driving.

8.3.3 Power Interface

The DMD requires five (5) DC voltage input signals.

- DMD_P3P3V
- DMD_P1P8V
- VOFFSET
- VRESET
- VBIAS

The DMD_P3P3V signal is created by the power and motor driver of the DLPA100 device. It is used on the DMD board to create the other four (4) DMD voltage inputs, as well as powering various peripherals (for example, TMP411, I^2C, and TI level translators). The DMD_P1P8V signal is created by the TI PMIC LP38513S and provides the VCC voltage required by the DMD. the other signals, (VOFFSET (8.5 V), VRESET (–10 V), and VBIAS(16.5 V)) are created by the TI PMIC TPS65145 device and are supplied to the DMD to control the micromirrors

8.3.4 Window Characteristics and Optics

CAUTION

TI assumes no responsibility for image quality artifacts or DMD failures caused by optical system operating conditions exceeding limits described previously.

8.3.4.1 Optical Interface and System Image Quality

TI assumes no responsibility for end-equipment optical performance. Achieving the desired end-equipment optical performance involves making trade-offs between numerous component and system design parameters. Optimizing system optical performance and image quality strongly relate to optical system design parameter trades. Although it is not possible to anticipate every conceivable application, projector image quality and optical performance is contingent on compliance to the optical system operating conditions described in the following sections.

8.3.4.2 Numerical Aperture and Stray Light Control

Ensure that the angle defined by the numerical aperture of the illumination and projection optics at the DMD optical area are the same. This angle must not exceed the nominal device mirror tilt angle unless appropriate apertures are added in the illumination and/or projection pupils to block out flat-state and stray light from the projection lens. The mirror tilt angle defines DMD capability to separate the "ON" optical path from any other light path, including undesirable flat-state specular reflections from the DMD window, DMD border structures, or other system surfaces near the DMD such as prism or lens surfaces. If the numerical aperture exceeds the mirror tilt angle, or if the projection numerical aperture angle is more than two degrees larger than the illumination numerical aperture angle, objectionable artifacts in the display's border and/or active area could occur.

Feature Description (continued)

8.3.4.3 Pupil Match

TI's optical and image quality specifications assume that the exit pupil of the illumination optics is nominally centered within 2° (two degrees) of the entrance pupil of the projection optics. Misalignment of pupils can create objectionable artifacts in the display's border and/or active area, which may require additional system apertures to control, especially if the numerical aperture of the system exceeds the pixel tilt angle.

8.3.4.4 Illumination Overfill

The active area of the device is surrounded by an aperture on the inside DMD window surface that masks structures of the DMD device assembly from normal view. The aperture is sized to anticipate several optical operating conditions. Overfill light illuminating the window aperture can create artifacts from the edge of the window aperture opening and other surface anomalies that may be visible on the screen. Design the illumination optical system to limit light flux incident anywhere on the window aperture from exceeding approximately 10% of the average flux level in the active area. Depending on the particular system's optical architecture, overfill light may have to be further reduced below the suggested 10% level in order to be acceptable.

8.3.5 Micromirror Array Temperature Calculation

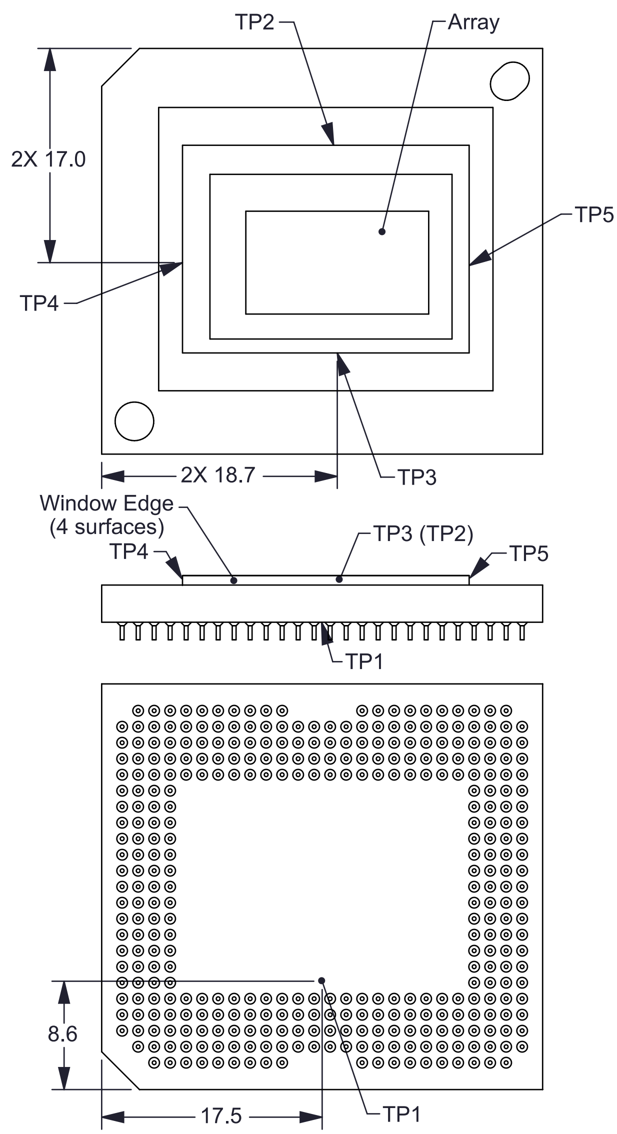


Figure 15. DMD Thermal Test Points

Feature Description (continued)

Micromirror array temperature can be computed analytically from measurement points on the outside of the package, the ceramic package thermal resistance, the electrical power dissipation, and the illumination heat load. The relationship between micromirror array temperature and the reference ceramic temperature is provided by the following equations:

$$T_{ARRAY} = T_{CERAMIC} + (Q_{ARRAY} \times R_{ARRAY\text{–}TO\text{–}CERAMIC}) \quad (1)$$

$$Q_{ARRAY} = Q_{ELECTRICAL} + Q_{ILLUMINATION} \quad (2)$$

$$Q_{ILLUMINATION} = (C_{L2W} \times SL)$$

where

- T_{ARRAY} = Computed micromirror array temperature (°C)
- $T_{CERAMIC}$ = Measured ceramic temperature (°C), TP1 location in Figure 15
- $R_{ARRAY\text{–}TO\text{–}CERAMIC}$ = DMD package thermal resistance from micromirror array to outside ceramic (°C/W) specified in *Thermal Information*
- Q_{ARRAY} = Total DMD power; electrical, specified in *Electrical Characteristics*, plus absorbed (calculated) (W)
- $Q_{ELECTRICAL}$ = Nominal DMD electrical power dissipation (W), specified in *Electrical Characteristics*
- C_{L2W} = Conversion constant for screen lumens to absorbed optical power on the DMD (W/lm) specified below
- SL = Measured ANSI screen lumens (lm) (3)

Electrical power dissipation of the DMD is variable and depends on the voltages, data rates and operating frequencies. The nominal electrical power dissipation to use when calculating array temperature is 2.9 W. Absorbed optical power from the illumination source is variable and depends on the operating state of the micromirrors and the intensity of the light source. Equations shown above are valid for a 1-chip DMD system with total projection efficiency through the projection lens from DMD to the screen of 87%.

The conversion constant CL2W is based on the DMD micromirror array characteristics. It assumes a spectral efficiency of 300 lm/W for the projected light and illumination distribution of 83.7% on the DMD active array, and 16.3% on the DMD array border and window aperture. The conversion constant is calculated to be 0.00293 W/lm.

Equation 4 through Equation 9 show sample calculations for a typical projection application.

$$T_{CERAMIC} = 55°C$$

where

- assumed system measurement
- see *Recommended Operating Conditions* for specific limits (4)

$$SL = 3000\ lm \quad (5)$$

$$Q_{ELECTRICAL} = 2.9\ W \quad (6)$$

For Equation 6, see the maximum power specifications in .

$$C_{L2W} = 0.00274\ W/lm \quad (7)$$

$$Q_{ARRAY} = 2.9\ W + (0.00274 \times 3000) = 11.12\ W \quad (8)$$

$$T_{ARRAY} = 55°C + (11.12\ W \times 0.6\ C/W) = 61.7°C \quad (9)$$

8.3.6 Micromirror Landed-on or Landed-Off Duty Cycle

8.3.6.1 Definition of Micromirror Landed-On or Landed-Off Duty Cycle

The micromirror landed-on or landed-off duty cycle (landed duty cycle) denotes the amount of time (as a percentage) that an individual micromirror is landed in the ON–state versus the amount of time the same micromirror is landed in the OFF–state.

As an example, a landed duty cycle of 100/0 indicates that the referenced pixel is in the ON–state 100% of the time (and in the OFF–state 0% of the time); whereas 0/100 would indicate that the pixel is in the OFF–state 100% of the time. Likewise, 50/50 indicates that the pixel is On 50% of the time and Off 50% of the time.

Note that when assessing landed duty cycle, the time spent switching from one state (ON or OFF) to the other state (OFF or ON) is considered negligible and is thus ignored.

Feature Description (continued)

Since a micromirror can only be landed in one state or the other (ON or OFF), the two numbers (percentages) always add to 100.

8.3.6.2 Landed Duty Cycle and Useful Life of the DMD

Knowing the long-term average landed duty cycle (of the end product or application) is important because subjecting all (or a portion) of the DMD's micromirror array (also called the active array) to an asymmetric landed duty cycle for a prolonged period of time can reduce the DMD's usable life.

Note that it is the symmetry/asymmetry of the landed duty cycle that is of relevance. The symmetry of the landed duty cycle is determined by how close the two numbers (percentages) are to being equal. For example, a landed duty cycle of 50/50 is perfectly symmetrical whereas a landed duty cycle of 100/0 or 0/100 is perfectly asymmetrical.

Individual DMD mirror duty cycles vary by application as well as the mirror location on the DMD within any specific application. DMD mirror useful life are maximized when every individual mirror within a DMD approaches 50/50 (or 1/1) duty cycle. Therefore, for the DLPC4422 and DLP650NE chipset, it is recommended that the DMD Idle Mode be enabled as often as possible. Examples are whenever the system is idle, the illumination is disabled, between sequential pattern exposures (if possible), or when the exposure pattern sequence is stopped for any reason. This software mode provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the on and off states. Refer to the DLPC4422 Software Programmer's Guide DLPU018 for a description of the DMD Idle Mode command. For the DLPC910 and DLP650NE chipset, it is recommended that the controlling applications processor provide a 50/50 pattern sequence to the DLPC910 for display on the DLP650NE as often as possible, similar to the above examples stated for the DLPC4422. The pattern provides a 50/50 duty cycle across the entire DMD mirror array, where the mirrors are continuously flipped between the ON and OFF states.

8.3.6.3 Landed Duty Cycle and Operational DMD Temperature

Operational DMD Temperature and Landed Duty Cycle interact to affect the DMD usable life, and this interaction can be exploited to reduce the impact that an asymmetrical Landed Duty Cycle has on the usable life of the DMD. This is quantified in the de-rating curve shown in Figure 1. The importance of this curve is that:

- All points along this curve represent the same usable life.
- All points above this curve represent lower usable life (and the further away from the curve, the lower the usable life).
- All points below this curve represent higher usable life (and the further away from the curve, the higher the usable life).

In practice, this curve specifies the maximum operating DMD temperature required for DMD operation at for a give long-term average Landed Duty Cycle.

8.3.6.4 Estimating the Long-Term Average Landed Duty Cycle of a Product or Application

During a given time period, the Landed Duty Cycle of a given pixel follows from the image content being displayed by that pixel.

For example, in the simplest case, when displaying pure-white on a given pixel for a given time period, that pixel operates under a 100/0 Landed Duty Cycle during that time period. Likewise, when displaying pure-black, the pixel operates under a 0/100 Landed Duty Cycle.

Between the two extremes (ignoring for the moment color and any image processing that may be applied to an incoming image), the Landed Duty Cycle tracks one-to-one with the gray scale value, as shown in Table 1.

Table 1. Grayscale Value and Landed Duty Cycle

GRAYSCALE VALUE	LANDED DUTY CYCLE
0%	0/100
10%	10/90
20%	20/80
30%	30/70

Table 1. Grayscale Value and Landed Duty Cycle (continued)

GRAYSCALE VALUE	LANDED DUTY CYCLE
40%	40/60
50%	50/50
60%	60/40
70%	70/30
80%	80/20
90%	90/10
100%	100/0

Accounting for color rendition (but still ignoring image processing) requires knowing both the color intensity (from 0% to 100%) for each constituent primary color (red, green, and/or blue) for the given pixel as well as the color cycle time for each primary color, where *color cycle time* is the total percentage of the frame time that a given primary must be displayed in order to achieve the desired white point.

During a given period of time, the landed duty cycle of a given pixel can be calculated in Equation 10.

Landed Duty Cycle = (Red_Cycle_% × Red_Scale_Value) + (Green_Cycle_% × Green_Scale_Value) + (Blue_Cycle_% × Blue_Scale_Value)

where

- Red_Cycle_% represents the percentage of the frame time that Red is displayed to achieve the desired white point
- Green_Cycle_% represents the percentage of the frame time that Green is displayed to achieve the desired white point
- Blue_Cycle_%, represents the percentage of the frame time that Blue is displayed to achieve the desired white point (10)

For example, assume that the red, green and blue color cycle times are 50%, 20%, and 30% respectively (in order to achieve the desired white point), then the Landed Duty Cycle for various combinations of red, green, blue color intensities would be as shown in Table 2.

Table 2. Example Landed Duty Cycle for Full-Color

CYCLE PERCENTAGE			Landed Duty Cycle
Red 50%	Green 20%	Blue 30%	
Red Scale Value	Green Scale Value	Blue Scale Value	
0%	0%	0%	0/100
100%	0%	0%	50/50
0%	100%	0%	20/80
0%	0%	100%	30/70
12%	0%	0%	6/94
0%	35%	0%	7/93
0%	0%	60%	18/82
100%	100%	0%	70/30
0%	100%	100%	50/50
100%	0%	100%	80/20
12%	35%	0%	13/87
0%	35%	60%	25/75
12%	0%	60%	24/76
100%	100%	100%	100/0

8.4 Device Functional Modes

When the DMD is controlled by the DLPC4422, the digital controller has four modes of operation.

- Video mode
- Video pattern mode
- Pre-stored pattern mode
- Pattern on-the-fly mode

DMD functional modes are controlled by the DLPC4422 display controller. See the DLPC4422 display controller data sheet or contact a TI applications engineer.

DMD functional modes are controlled by the DLPC4422 digital display controller. See the DLPC4422 data sheet. Contact a TI applications engineer for more information.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Texas Instruments DLP technology is a micro-electro-mechanical systems (MEMS) technology that modulates light using a digital micromirror device (DMD). The DMD is a spatial light modulator, which reflects incoming light from an illumination source to one of two directions, towards the projection optics or collection optics. The large micromirror array size and ceramic package provides great thermal performance for bright display applications. Typical applications using the DLP650NE include home theater, digital signage, interactive display, low-latency gaming display, portable smart displays.

9.2 Typical Application

The DLP650NE DMD combined with a DLPC4422 digital controller and DLPA100 power management device provides full HD resolution for bright, colorful display applications. A typical display system using the DLP650NE and additional system components can be seen in Figure 16.

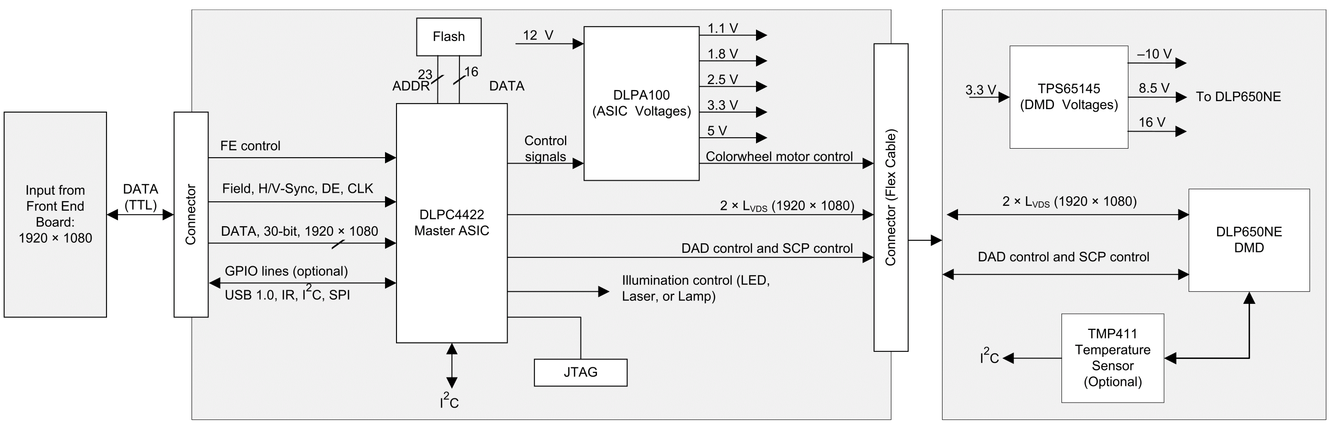


Figure 16. Typical DLPC4422 Application Schematic

9.2.1 Design Requirements

A DLP650NE projection system is created by using the DMD chipset, including the DLP650NE, DLPC4422, and DLPA100. The DLP650NE is used as the core imaging device in the display system and contains a 0.65-inch array of micromirrors. The DLPC4422 controller is the digital interface between the DMD and the rest of the system, taking digital input from front end receiver that converts the data from the source and using the converted data for driving the DMD over a LVDS interface. The DLPA100 power management device provides voltage regulators for the DMD, controller, and illumination functionality.

Other core components of the display system include an illumination source, an optical engine for the illumination and projection optics, other electrical and mechanical components, and software. The illumination source options include lamp, LED, laser or laser phosphor. The type of illumination used and desired brightness affects the overall system design and size.

9.2.2 Detailed Design Procedure

For a complete the DLP system, an optical module or light engine is required that contains the DLP650NE DMD, associated illumination sources, optical elements, and necessary mechanical components.

To ensure reliable operation, the DLP650NE DMD must always be used with the DLPC4422 display controllers and a DLPA100 PMIC driver.

10 Power Supply Requirements

10.1 DMD Power Supply Requirements

The following power supplies are all required to operate the DMD: VCC, VCCI, VOFFSET, VBIAS, and VRESET. VSS must also be connected. DMD power-up and power-down sequencing is strictly controlled by the DLPC4422 device.

CAUTION

For reliable operation of the DMD, the following power supply sequencing requirements must be followed. Failure to adhere to the prescribed power-up and power-down procedures may affect device reliability. VCC, VCCI, VOFFSET, VBIAS, and VRESET power supplies have to be coordinated during power-up and power-down operations. VSS must also be connected. Failure to meet any of the below requirements results in a significant reduction in the DMD's reliability and lifetime. Refer to Figure 17.

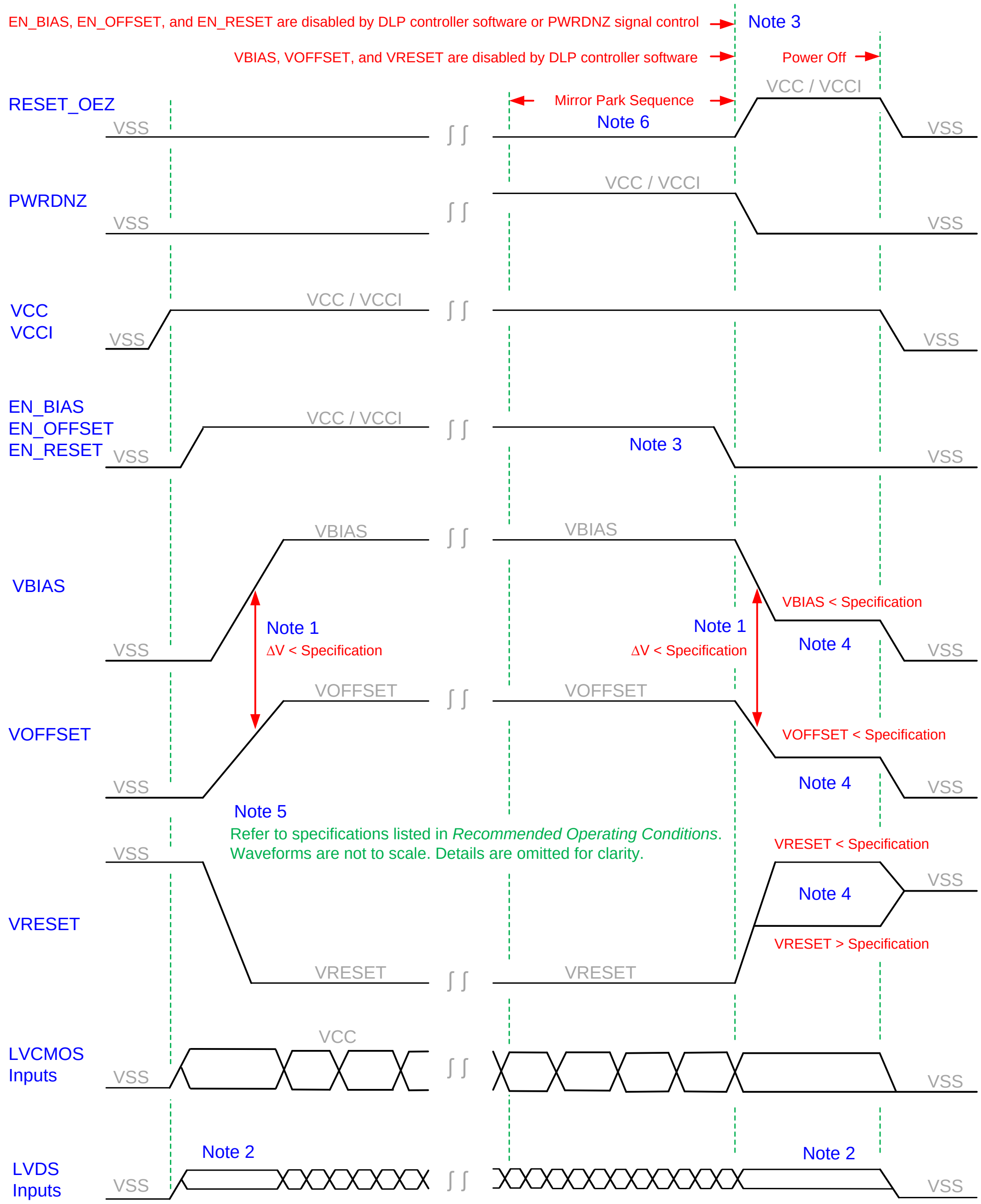
10.2 DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET, VBIAS, and VRESET voltages are applied to the DMD.
- During power-up, it is a strict requirement that the change between VBIAS and VOFFSET must be within the specified limit shown in *Recommended Operating Conditions*. During power-up, VBIAS does not have to start after VOFFSET.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements listed in the *Absolute Maximum Ratings* table, in the *Recommended Operating Conditions* table, and in the *DMD Power Supply Sequencing Requirements* section.
- During power-up, LVCMOS input pins must not be driven high until after VCC and VCCI have settled at operating voltages listed in *Recommended Operating Conditions* table.

10.3 DMD Power Supply Power-Down Procedure

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground. Refer to Table 3.
- During power-down, it is a strict requirement that the change between VBIAS and VOFFSET must be within the specified limit shown in the *Recommended Operating Conditions* table. During power-down, it is not mandatory to stop driving VBIAS prior to VOFFSET.
- During power-down, there is no requirement for the relative timing of VRESET with respect to VOFFSET and VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements listed in *Absolute Maximum Ratings*, in *Recommended Operating Conditions*, and in Figure 17.
- During power-down, LVCMOS input pins must be less than specified in the *Recommended Operating Conditions* table.

DMD Power Supply Power-Down Procedure (continued)



(1) To prevent excess current, the supply voltage change |VBIAS – VOFFSET| must be less than specified in the *Recommended Operating Conditions* table. OEMs may find that the most reliable way to ensure this is to power VOFFSET prior to VBIAS during power-up and to remove VBIAS prior to VOFFSET during power-down.

(2) LVDS signals are less than the input differential voltage (VID) maximum specified in the *Recommended Operating Conditions* table. During power-down, LVDS signals are less than the high level input voltage (VIH) maximum specified in the *Recommended Operating Conditions* table.

(3) When system power is interrupted, the DLP DLPC4422 initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET and VOFFSET after the micromirror park sequence. Software power-down disables VBIAS, VRESET, and VOFFSET after the micromirror park sequence through software control. For either case, enable signals EN_BIAS, EN_OFFSET, and EN_RESET are used to disable VBIAS, VOFFSET, and VRESET, respectfully.

(4) Refer to Table 3.

(5) Figure not to scale. Details have been omitted for clarity. Refer to the *Recommended Operating Conditions* table.

(6) EN_BIAS, EN_OFFSET, and EN_RESET are disabled by DLP controller software or PWRDNZ signal control.

DMD Power Supply Power-Down Procedure (continued)

(7) VBIAS, VOFFSET, and VRESET are disabled by DLP controller software

Figure 17. DMD Power Supply Sequencing Requirements

Table 3. DMD Power-Down Sequence Requirements

PARAMETER		MIN	MAX	UNIT
VBIAS	Supply voltage level during power–down sequence		4.0	V
VOFFSET			4.0	V
VRESET		–4.0	0.5	V

11 Layout

11.1 Layout Guidelines

The DLP650NE along with one DLPC4422 controller provides a solution for many applications including structured light and video projection. This section provides layout guidelines for the DLP650NE.

11.1.1 General PCB Recommendations

The PCB shall be designed to IPC2221 and IPC2222, Class 2, Type Z, at level B producibility and built to IPC6011 and IPC6012, class 2. The PCB board thickness to be 0.062 inches +/- 10%, using standard FR-4 material, and applies after all lamination and plating processes, measured from copper to copper.

Two-ounce copper planes are recommended in the PCB design in order to achieve needed thermal connectivity. Refer to Related Documents for the DLPC4422 Digital Controller Data Sheet for related information on the DMD Interface Considerations.

High-speed interface waveform quality and timing on the DLPC4422 controller (that is, the LVDS DMD interface) is dependent on the following factors:

- Total length of the interconnect system
- Spacing between traces
- Characteristic impedance
- Etch losses
- How well matched the lengths are across the interface

Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

- Setup Margin = (controller output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation)
- Hold-time Margin = (controller output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

The PCB SI degradation is the signal integrity degradation due to PCB affects which includes such things as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol-interference (ISI) noise.

The DLPC4422 Digital Controller data sheet reports the I/O timing parameters. Any PCB routing mismatches can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not as easy to determine.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines provide a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Deviation from these recommendations may allow the device to operate, but be sure to confirm system integrity with PCB analysis or lab measurements.

11.2 Layout Example

11.2.1 Board Stack and Impedance Requirements

Refer to Figure 18 for guidance on the parameters.

PCB design:

Configuration:	Asymmetric dual stripline
Etch thickness (T):	1.0-oz copper (1.2 mil)
Flex etch thickness (T):	0.5-oz copper (0.6 mil)
Single-ended signal impedance:	50 Ω (±10%)
Differential signal impedance:	100 Ω (±10%)

PCB stack-up:

Reference plane 1 is assumed to be a ground plane for proper return path.

Reference plane 2 is assumed to be the I/O power plane or ground.

Dielectric FR4, (Er):	4.2 (nominal)
Signal trace distance to reference plane 1 (H1):	5.0 mil (nominal)
Signal trace distance to reference plane 2 (H2):	34.2 mil (nominal)

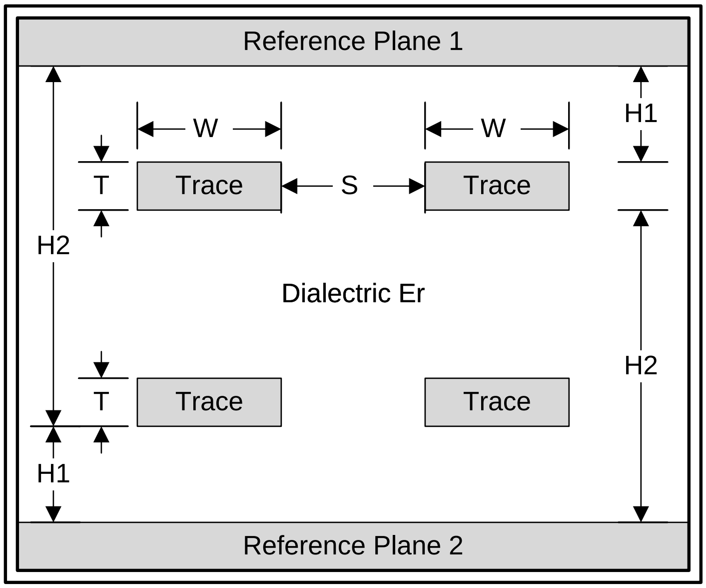


Figure 18. PCB Stack Geometries

Layout Example (continued)

Table 4. General PCB Routing(1)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Line width (W)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB etch clocks	7 (0.18)	4.25 (0.11)	mil (mm)
Differential signal pair spacing (S)	PCB etch data or control	N/A	5.75(2) –0.15	mil (mm)
	PCB etch clocks	N/A	5.75(2) –0.15	mil (mm)
Minimum differential pair-to-pair spacing (S)	PCB etch data or control	N/A	20 (0.51)	mil (mm)
	PCB etch clocks	N/A	20 (0.51)	mil (mm)
	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
Minimum line spacing to other signals (S)	PCB etch data or control	10 (0.25)	20 (0.51)	mil (mm)
	PCB etch clocks	20 (0.51)	20 (0.51)	mil (mm)
Maximum differential pair P-to-N length mismatch	Total data	N/A	12 0.3	mil (mm)

(1) Applies to all corresponding PCB signals
(2) Spacing may vary to maintain differential impedance requirements

Table 5. DMD Interface Specific Routing

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD (LVDS)	SCTRL_AN / SCTRL_AP D_AP(15:0)/ D_AN(15:0)	DCKA_P/ DCKA_N	± 150 (± 3.81)	mil (mm)
DMD (LVDS)	SCTRL_BN/ SCTRL_BP D_BP(15:0)/ D_BN(15:0)	DCKB_P/ DCKB_N	± 150 (± 3.81)	mil (mm)

Number of layer changes:
- Single-ended signals: Minimize
- Differential signals: If individual differential pairs are be routed on different layers, ensure the signals of a given pair do not change layers.

Table 6. DMD Signal Routing Length(1)

BUS	MIN	MAX	UNIT
DMD (LVDS)	50	375	mm

(1) Maximum signal routing length includes escape routing.

Stubs: Stubs, such as test points, must not be placed on a LVDS line.

Termination Requirements: DMD interface: None – The DMD receiver is differentially terminated to 100 Ω internally.

Connector (DMD-LVDS interface bus only):

High-speed connectors that meet the following requirements should be used:
- Differential crosstalk: < 5%
- Differential impedance: 75 Ω to 125 Ω

Routing requirements for right-angle connectors: When using right-angle connectors, P-N pairs should be routed in the same row to minimize delay mismatch. When using right-angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths. Voltage or low frequency signals should be routed on the outer layers. Signal trace corners shall be no sharper than 45 degrees. Adjacent signal layers shall have the predominant traces routed orthogonal to each other.

These guidelines produce a maximum PCB routing mismatch of 4.41 mm (0.174 inch) or approximately 30.4 ps, assuming 175 ps/inch FR4 propagation delay.

These PCB routing guidelines results in approximately 25-ps system setup margin and 25-ps system hold margin for the DMD interface after accounting for signal integrity degradation as well as routing mismatch.

Both the DLPC4422 output timing parameters and the DLP650NE DMD input timing parameters include timing budget to account for their respective internal package routing skew.

11.2.1.1 Power Planes

Signal routing is NOT allowed on the power and ground planes. Ensure that all device pin and via connections to this plane use a thermal relief with a minimum of four spokes. The power plane must clear the edge of the PCB by 0.2”.

Prior to routing, vias connecting all digital ground layers (GND) should be placed around the edge of the rigid PWB regions 0.025” from the board edges with a 0.100” spacing. It is also desirable to have all internal digital ground (GND) planes connected together in as many places as possible. If possible, all internal ground planes should be connected together with a minimum distance between connections of 0.5”. Extra vias are not required if there are sufficient ground vias due to normal ground connections of devices. NOTE: All signal routing and signal vias should be inside the perimeter ring of ground vias.

Power and Ground pins of each component shall be connected to the power and ground planes with one via for each pin. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100”). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. Ground plane slots are NOT allowed.

Route VOFFSET, VBIAS, and VRESET as a wide trace >20 mils (wider if space allows) with 20 mils spacing.

11.2.1.2 LVDS Signals

It is recommended that the LVDS signals should be routed first. Each pair of differential signals must be routed together at a constant separation such that constant differential impedance (as in section *Board Stack and Impedance Requirements*) is maintained throughout the length. Avoid sharp turns and layer switching while keeping lengths to a minimum. The distance from one pair of differential signals to another shall be at least 2 times the distance within the pair.

11.2.1.3 Critical Signals

The critical signals on the board must be hand routed in the order specified below. In case of length matching requirements, the longer signals should be routed in a serpentine fashion, keeping the number of turns to a minimum and the turn angles no sharper than 45 degrees. Avoid routing long trace all around the PCB.

Table 7. Timing Critical Signals

<table>
<tr><th>GROUP</th><th>SIGNAL</th><th>CONSTRAINTS</th><th>ROUTING LAYERS</th></tr>
<tr><td>1</td><td>D_AP(0:15), D_AN(0:15), DCLK_AP, DCLK_AN, SCTRL_AN, SCTRL_AP, D_BP(0:15), D_BN (0:15), DCLK_BP, DCLK_BN, SCTRL_BN, SCTRL_BP</td><td rowspan="3">Refer to Table 4 and Table 5</td><td>Internal signal layers. Avoid layer switching when routing these signals.</td></tr>
<tr><td>2</td><td>RESET_ADDR_(0:3),
RESET_MODE_(0:1),
RESET_OEZ,
RESET_SEL_(0:1)
RESET_STROBE,
RESET_IRQZ.</td><td>Internal signal layers. Top and bottom as required.</td></tr>
<tr><td>3</td><td>SCP_CLK, SCP_DO,
SCP_DI, SCP_DMD_CSZ.</td><td>Any</td></tr>
<tr><td>4</td><td>Others</td><td>No matching/length requirement</td><td>Any</td></tr>
</table>

11.2.1.4 Device Placement

Unless otherwise specified, all major components should be placed on top layer. Small components such as ceramic, non-polarized capacitors, resistors and resistor networks can be placed on bottom layer. All high frequency de-coupling capacitors for the ICs shall be placed near the parts. Distribute the capacitors evenly around the IC and locate them as close to the device’s power pins as possible (preferably with no vias). In the case where an IC has multiple de-coupling capacitors with different values, alternate the values of those that are side by side as much as possible and place the smaller value capacitor closer to the device.

11.2.1.5 Device Orientation

It is desirable to have all polarized capacitors oriented with their positive terminals in the same direction. If polarized capacitors are oriented both horizontally and vertically, then be sure to orient all horizontal capacitors and the positive terminal in the same direction and likewise for the vertically -oriented capacitors.

11.2.1.6 Fiducials

Follow these guidelines for fiducial placement for automatic component insertion on the board or on recommendation from manufacturer:

- Place fiducials for optical auto insertion alignment on three corners of both sides of the PWB.
- Place fiducials in the center of the land patterns for fine pitch components (lead spacing <0.05").
- Ensure fiducials are 0.050-inch copper with a 0.100-inch cutout (antipad).

12 Device Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

Table 8. Package Specific Information

PACKAGE TYPE	PINS	CONNECTOR
FYE	350	PGA

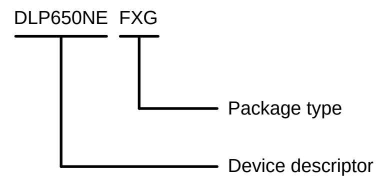


Figure 19. Device Number Description

12.1.2 Device Markings

The device marking will include both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 20. The 2-dimensional matrix code is an alpha-numeric character string that contains the DMD part number, Part 1 of Serial Number, and Part 2 of Serial Number. The first character of the DMD Serial Number (part 1) is the manufacturing year. The second character of the DMD Serial Number (part 1) is the manufacturing month. The last character of the DMD Serial Number (part 2) is the bias voltage bin letter.

Examples: *1910-6037E GHXXXXX LLLLLLM

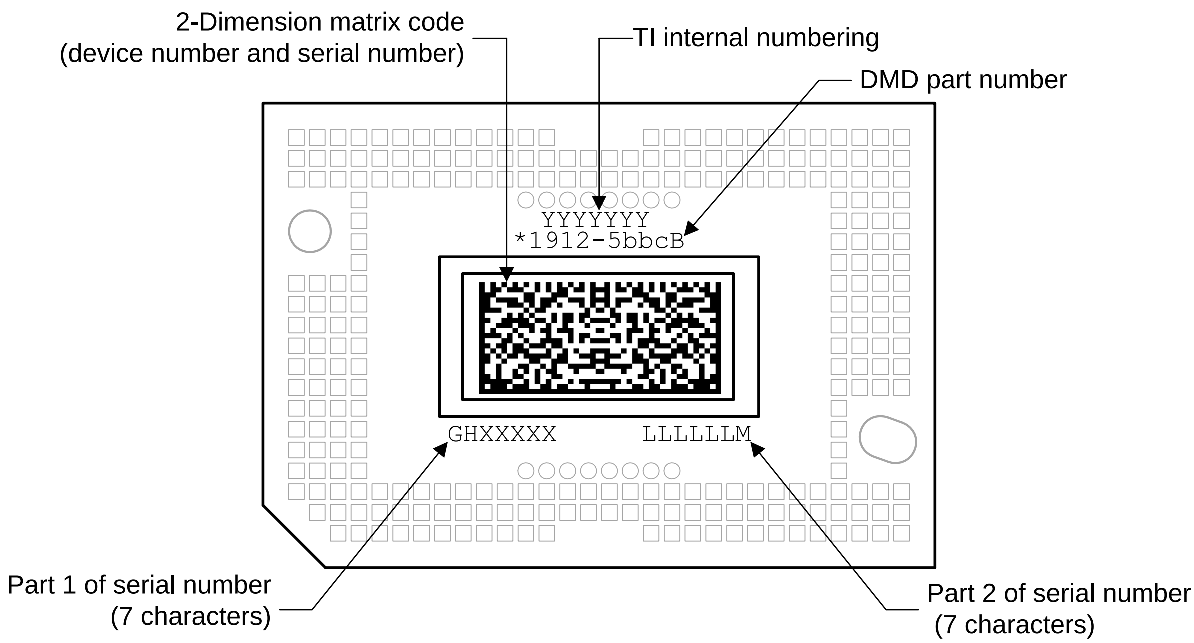


Figure 20. DMD Marking

12.2 Documentation Support

12.2.1 Related Documentation

The following documents contain additional information related to the use of the DLP650NE device.

Table 9. Related Documents

DOCUMENT	
DLPC4422 Digital Controller Data Sheet	DLPS074
TPS65145 Triple output LCD Supply With Linear Regulator and Power Good	SLVS497F
DLPA100 Power Management and Motor Driver	DLPS082
DMD101: Introduction to Digital Micromirror Device (DMD) Technology	DLPA008

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLP650NEFYE	ACTIVE	CPGA	FYE	350	21	RoHS & Green			10 to 90		Samples

[(1)] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[(2)] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[(3)] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[(4)] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[(5)] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[(6)] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

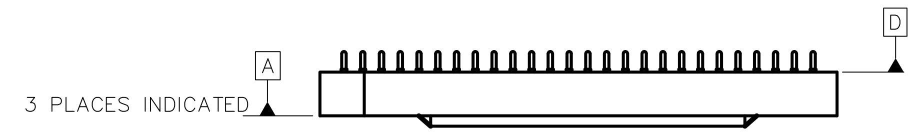
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

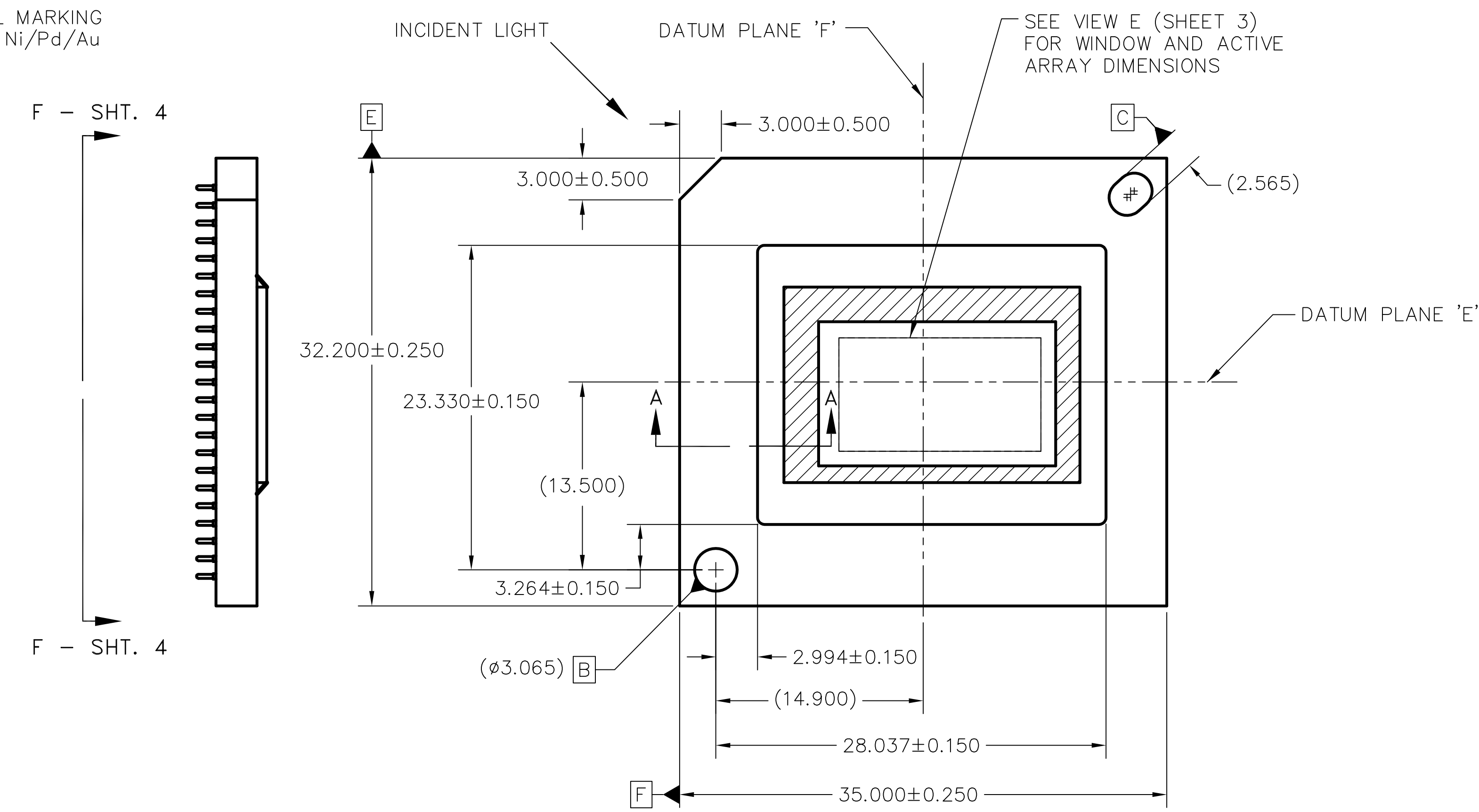
NOTES: UNLESS OTHERWISE SPECIFIED:

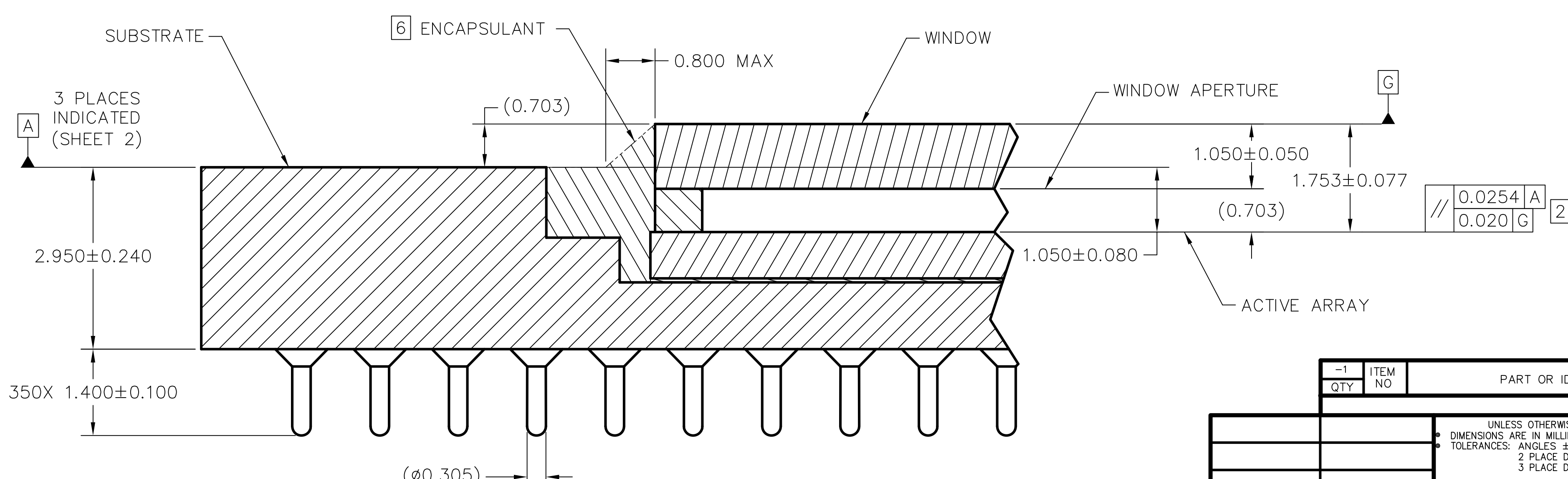
1. SUBSTRATE EDGE PERPENDICULARITY TOLERANCE APPLIES TO ENTIRE SURFACE
2. DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY
3. ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.8 DEGREES
4. SUBSTRATE SYMBOLIZATION PAD, AND PLATING AT BOTTOM OF DATUMS B AND C HOLES ARE ELECTRICALLY CONNECTED TO VSS PLANE WITHIN THE SUBSTRATE
5. BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE AREA
6. MAXIMUM ENCAPSULANT PROFILE SHOWN
7. ENCAPSULANT ALLOWED ON THE SURFACE OF THE CERAMIC IN THE AREA SHOWN IN VIEW B (SHEET 2). ENCAPSULANT SHALL NOT EXCEED 0.200 THICKNESS MAXIMUM.
8. SUBSTRATES PLATED WITH Ni/Au SHALL HAVE THE THREE-DIGIT NUMERICAL MARKING IN THE AREA ABOVE THE SYMBOLIZATION PAD. SUBSTRATES PLATED WITH Ni/Pd/Au SHALL HAVE THE MARKING IN THE AREA BELOW THE SYMBOLIZATION PAD.

REVISIONS

REV	DESCRIPTION	DATE	APPROVED
A	ECO 2111739, INITIAL RELEASE	11/04/2010	F. ARMSTRONG
B	ECO 2112602, CHANGE TOLERANCES ON OUTSIDE DIMENSIONS TO ±0.250; CHANGE DATUM B, BACK SIDE PINS, AND DATUM PLANES 'E' AND 'F' TO REFERENCE CENTERLINE OF PART	12/10/2010	F. ARMSTRONG
C	ECO 2135107, ADD NOTE 8 TO SHEETS 1 & 4	08/02/2013	F. ARMSTRONG
D	ECO 2139887, CHG GLASS SIZE UPPER TOL TO +0.050 TO MATCH PROCESS CAPABILITY	02/14/2014	F. ARMSTRONG
E	ECO 2179962, ADD PKG REF DESIGNATOR FYE TO TITLE BLOCK	03/04/2019	F. ARMSTRONG







SECTION A-A
SCALE 20/1

-1 QTY	ITEM NO	PART OR IDENTIFYING NUMBER	NOMENCLATURE OR DESCRIPTION	NOTES

PARTS LIST

UNLESS OTHERWISE SPECIFIED
- DIMENSIONS ARE IN MILLIMETERS
- TOLERANCES: ANGLES ± 1°
  2 PLACE DECIMALS ±0.25
  3 PLACE DECIMALS ±0.50
- REMOVE ALL BURRS AND SHARP EDGES
- INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5-1994
- DIMENSIONAL LIMITS APPLY BEFORE PROCESSES
- PARENTHETICAL INFO FOR REF ONLY

DWN	F. ARMSTRONG	DATE 11/02/2010
ENGR	F. ARMSTRONG	11/02/2010
QA	P. KONRAD	11/08/2010
CQE	M. DORAK	11/08/2010

THIRD ANGLE PROJECTION

NONE	0314DA
NEXT ASSY	USED ON
APPLICATION	

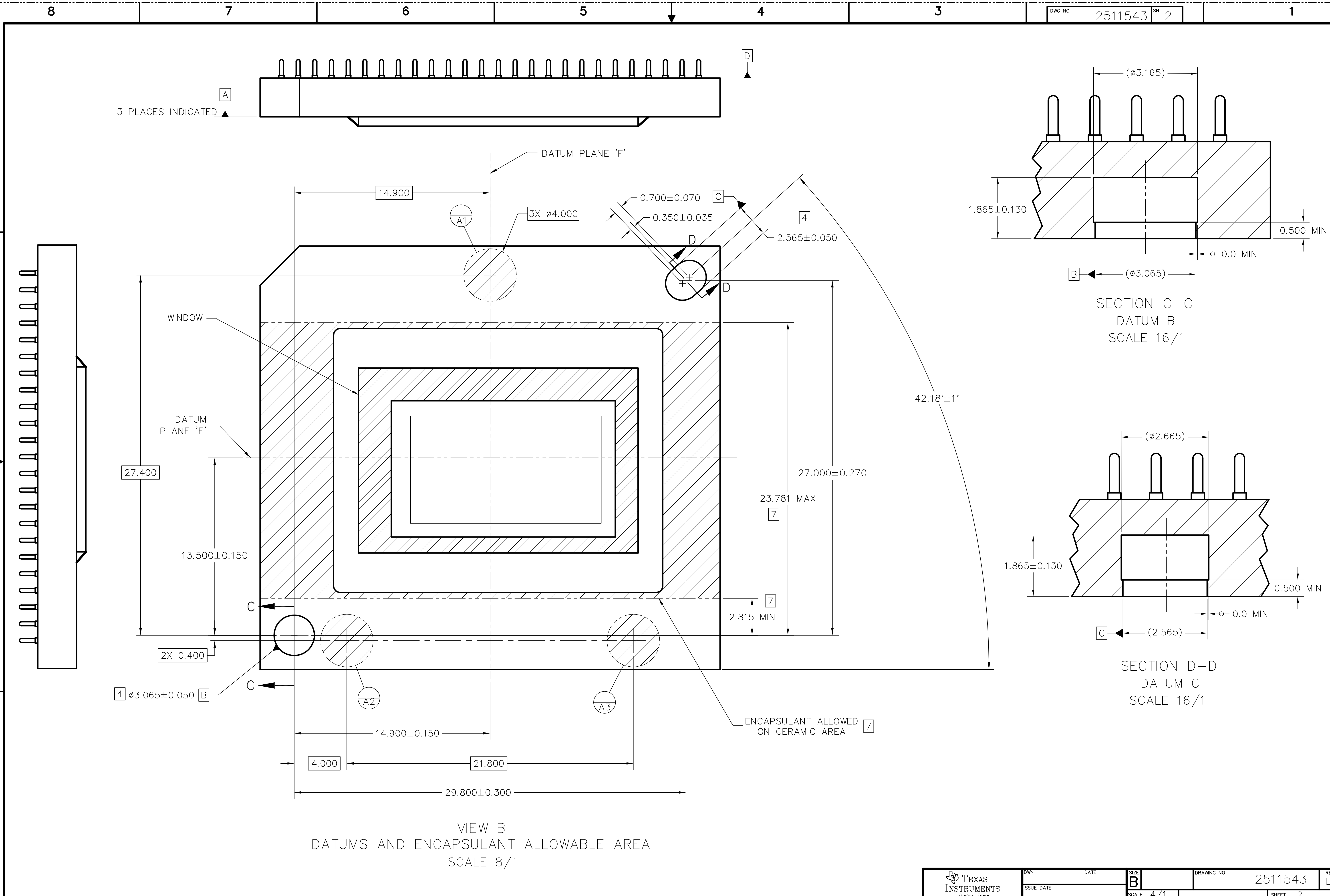
TEXAS INSTRUMENTS
Dallas, Texas

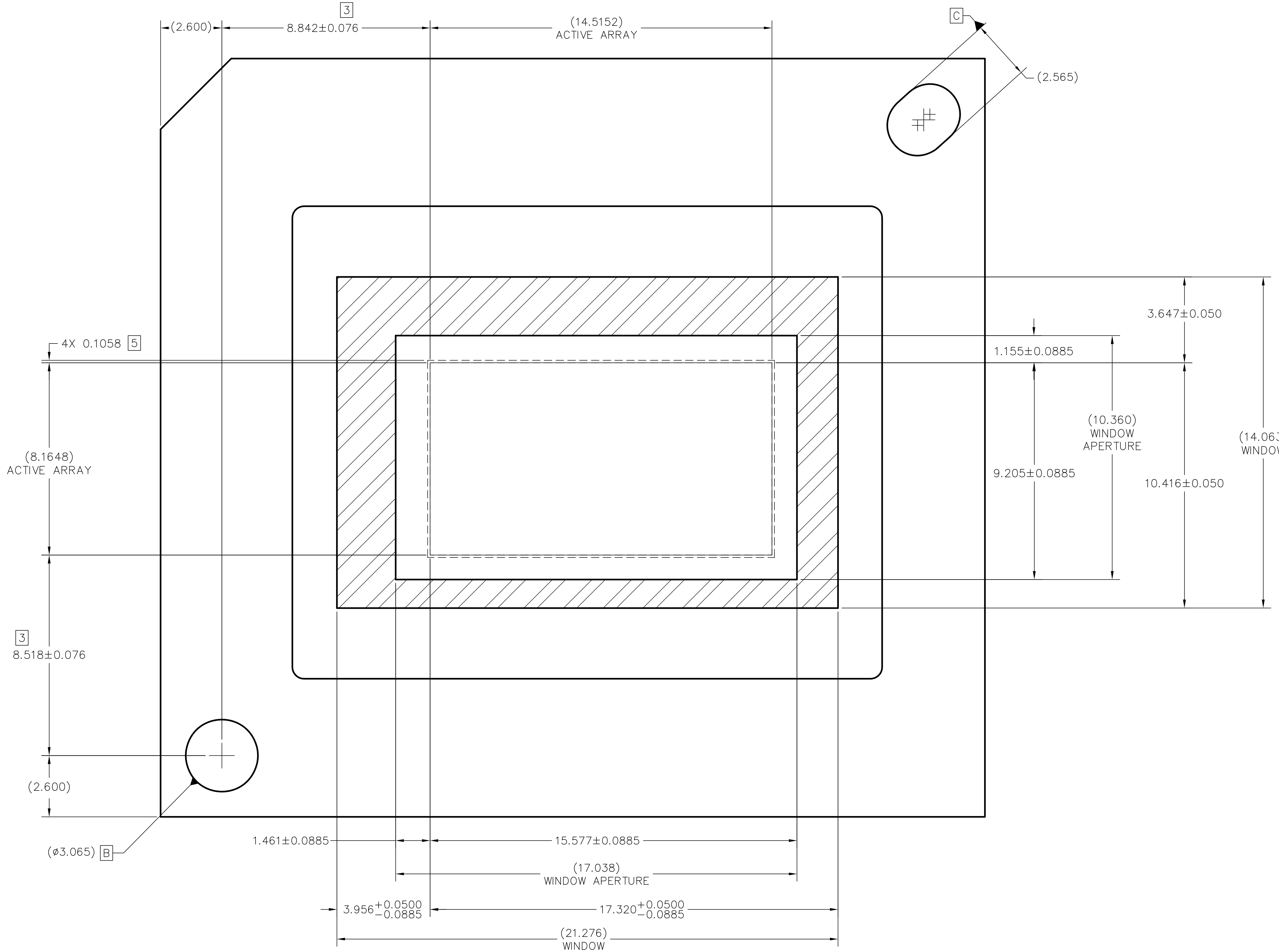
ICD, MECHANICAL, DMD
.65 1080p MVSP 2XLVDS
SERIES 600 (FYE PACKAGE)

SIZE	DRAWING NO	REV
B	2511543	E

SCALE 4/1 SHEET 1 OF 4

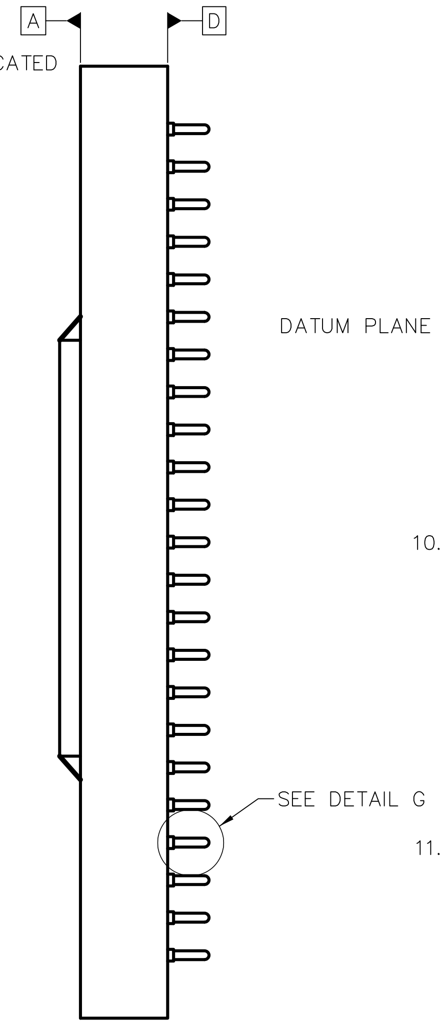
ACED1g

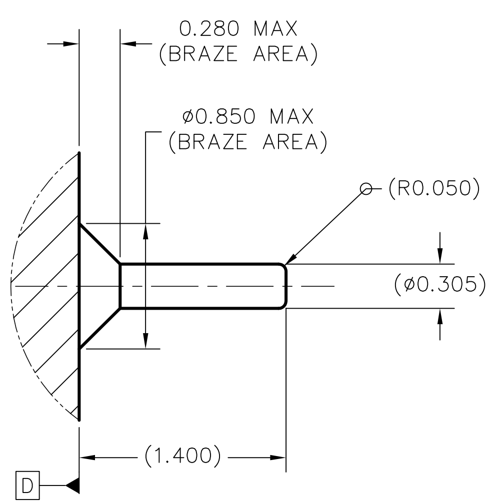

DWG NO 2511543 SH 2
3 PLACES INDICATED
A
D
DATUM PLANE 'F'
14.900
3X ø4.000
A1
0.700±0.070
0.350±0.035
C
4
2.565±0.050
D
D
WINDOW
DATUM PLANE 'E'
27.400
13.500±0.150
27.000±0.270
23.781 MAX
7
42.18°±1°
2.815 MIN
2X 0.400
4 ø3.065±0.050 B
C
C
A2
A3
ENCAPSULANT ALLOWED ON CERAMIC AREA 7
14.900±0.150
4.000
21.800
29.800±0.300
VIEW B
DATUMS AND ENCAPSULANT ALLOWABLE AREA
SCALE 8/1
(ø3.165)
1.865±0.130
0.500 MIN
0.0 MIN
B
(ø3.065)
SECTION C–C
DATUM B
SCALE 16/1
(ø2.665)
1.865±0.130
0.500 MIN
0.0 MIN
C
(2.565)
SECTION D–D
DATUM C
SCALE 16/1
TEXAS INSTRUMENTS
Dallas, Texas
DWN
DATE
ISSUE DATE
SIZE B
SCALE 4/1
DRAWING NO 2511543
REV E
SHEET 2
ACED2c



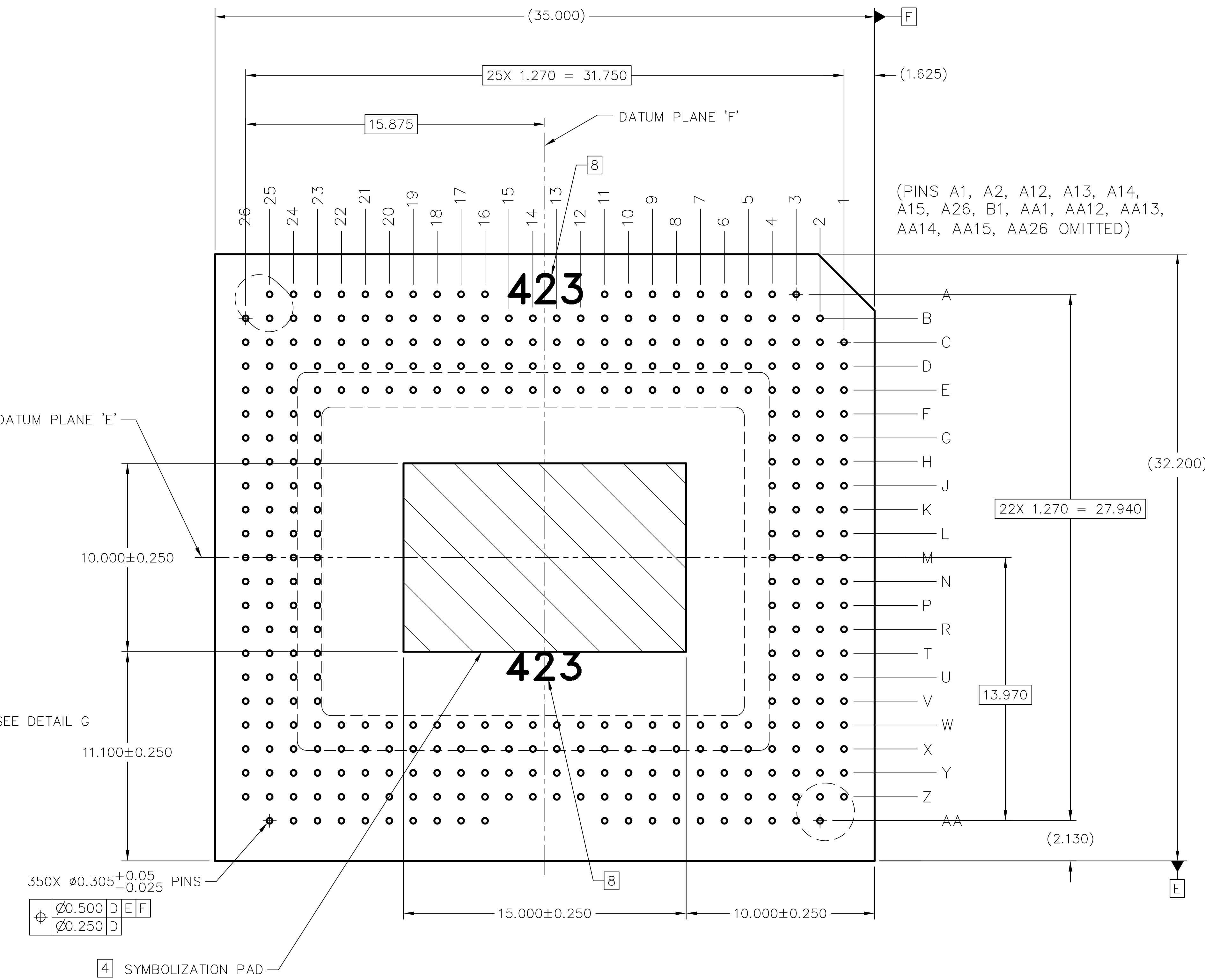
VIEW E (SHEET 1)
DMD WINDOW AND ACTIVE ARRAY
SCALE 12:1

TEXAS INSTRUMENTS Dallas, Texas	DWN DATE	SIZE B	DRAWING NO 2511543	REV E
	ISSUE DATE	SCALE 4/1		SHEET 3





DETAIL G (350 PLACES)
PIN & BRAZE DIMENSIONS
SCALE 40/1



VIEW F–F (SHEET 1)
PINS AND SYMBOLIZATION PAD
SCALE 8/1

TEXAS INSTRUMENTS Dallas, Texas	DWN / DATE / ISSUE DATE	SIZE B	DRAWING NO 2511543	REV E
		SCALE 4/1	SHEET 4	