User's Guide

TLV3605EVM User's Guide

ABSTRACT

The TLV3605EVM is an evaluation board designed to evaluate the high-speed TLV3605 comparator. The TLV3605EVM has layout options intended to make it simple to evaluate timing performance with different measurement tools. The output of the TLV3605 is designed for low-voltage differential signals (LVDS), that provide high-speed signals to interconnect devices such as FPGAs with minimal power dissipation.

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Trademarks

1 Introduction

The TLV3605EVM is an evaluation board designed to evaluate the high-speed TLV3605 comparator. The TLV3605EVM has layout options intended to make it simple to evaluate timing performance with different measurement tools. The output of the TLV3605 is designed for low-voltage differential signals (LVDS), which provide high-speed signals to interconnect devices such as FPGAs with minimal power dissipation.

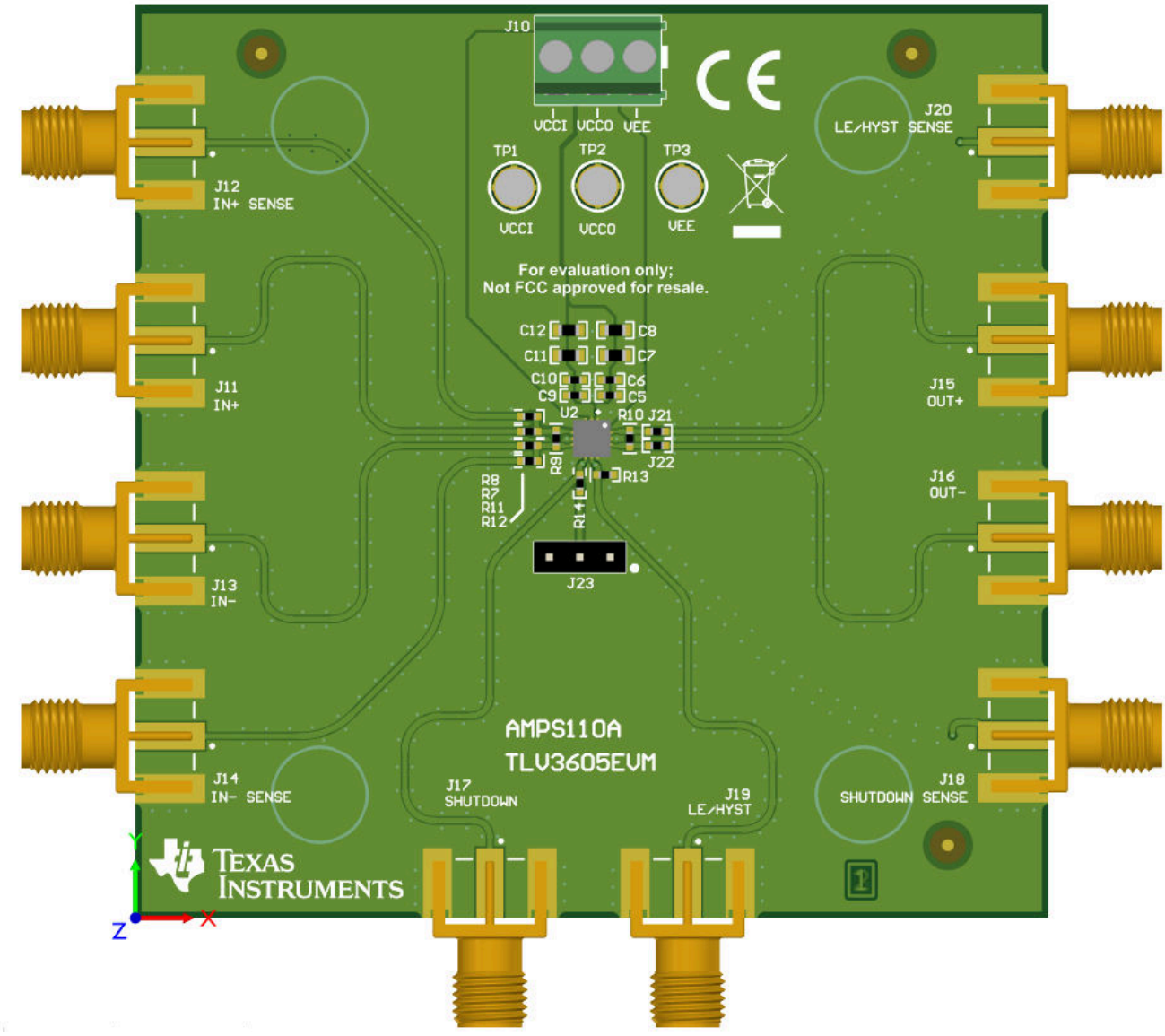

Figure 1-1. TLV3605EVM Board Top View

2 Features

- Low Propagation Delay: 800 ps
- Low Overdrive Dispersion: 450 ps
- High Toggle Frequency: 1.5 GHz/3.0 Gbps
- Narrow Pulse Width Detection Capability: 600ps
- LVDS Output
- Low Input Offset Voltage: +/-5mV
- RVK Package 12-Pin QFN

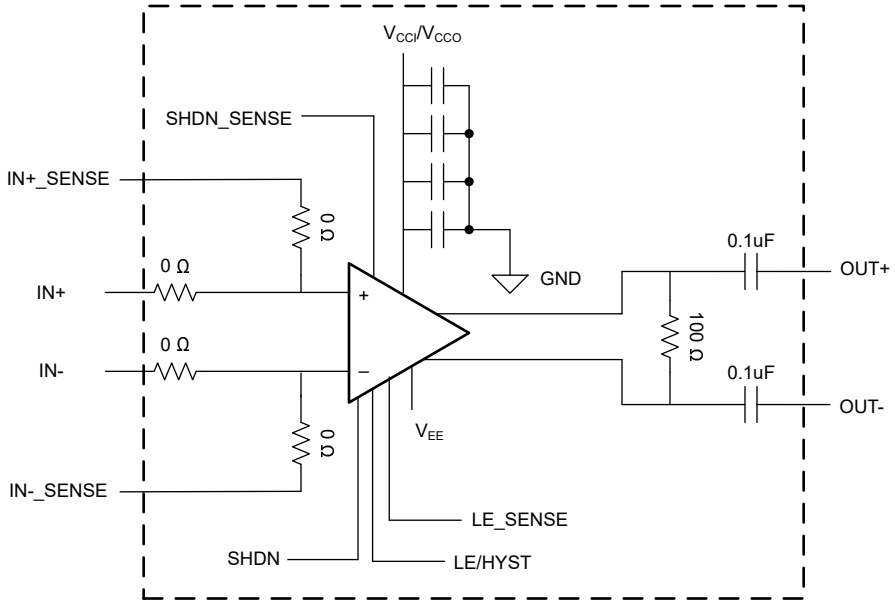

Figure 2-1. Block Diagram

3 EVM Specifications

- Supply Range: +2.4 V to +5.5 V (Single Supply Only)
- Input Common Mode Range: (Vee -200 mV) to (VCCI/VCCO + 200 mV)

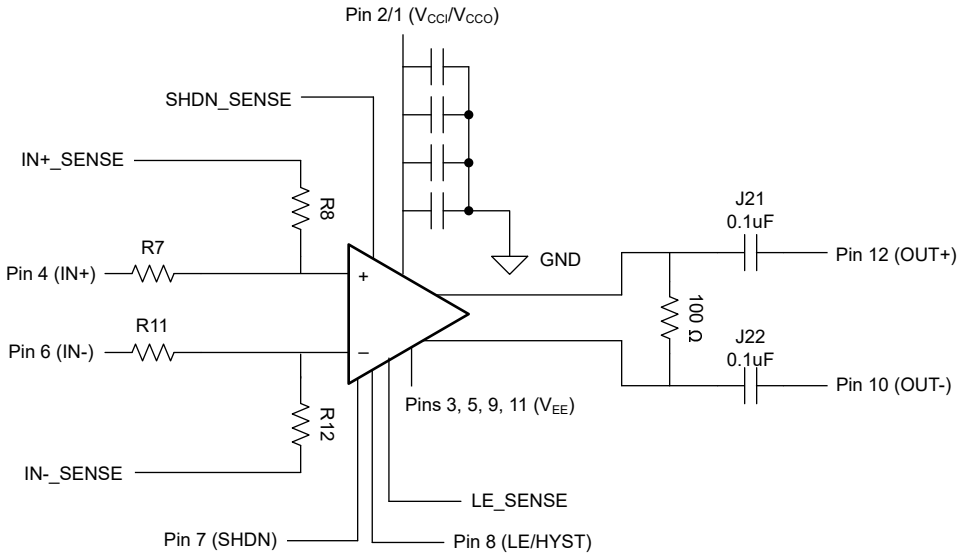

Figure 3-1. TLV3605EVM Pin Assignments

4 Recommended Equipment

- Power Supply
- High Speed Functional Generator with dual outputs
  - Fast rise/fall time recommended (≤ 500ps)
- High Speed Oscilloscope with 50Ω terminations
  - Differential probes with built in 100Ω terminations can be used to terminate the output properly
- SMA Cables/adapters
  - All forced input voltages and signals must have matched cable lengths.
    - IN+, IN-, SHUTDOWN, LE/HYST
  - All sensed voltages and signals
    - LE/HYST SENSE, IN+SENSE, IN-SENSE, SHUTDOWN SENSE, OUT+, and OUT-

5 How to Make a Propagation Delay Measurement With Latch

Note

Do not turn on power supply until all connections to the device are made to the board.

1. Set VCCI/VCCO Power Supply to 5.0 V and disable the power supply output
2. Since the same power supply is used for both VCCI and VCCO, connect positive terminal supply to TP1 and TP2, and negative terminal to TP3
3. Ensure that cables connecting to IN+, IN-, IN+SENSE, IN-SENSE, LE/HYST, LE/HYST SENSE, OUT+, and OUT- are matched length and impedance. Perform any deskewing if necessary. If IN- is a DC voltage reference, the cables used for IN- and IN- SENSE do not need to be matched.
   a. To make accurate measurements, match all forced input voltages (IN+, IN-, LE/HYST, SHDN) and match the cables for all sensed signals (IN+SENSE, IN-SENSE, LE/HYST SENSE, SHDN SENSE).
4. On one signal generator output, set the function generator to produce a square wave output with 100mVpp at 50MHz, with a DC offset of 0.300 V. On the other generator output, set the function generator to produce a square wave output with 5.0Vpp at 5MHz, with a DC offset of 0 V and 75% duty cycle. Disable the signal generator output. Connect the first output to IN+ and the second output to LE/HYST.
5. Set one of the outputs of the DC power supply to 300mV. Disable the power supply output. Connect the output to IN-.
6. Connect OUTP and OUTN to a 50Ω terminated scope. Alternatively, use a differential probe with a 100Ω termination and connect to the oscilloscope.
7. Connect IN+SENSE, IN-SENSE, and LE/HYST SENSE, to a 50Ω terminated scope channel.
8. Enable the VCCI/VCCO power supply.
9. Verify the supply current is < 17.5mA
10. Enable the IN- power supply.
11. Enable the signal generator.
12. Monitor and verify the inputs from IN+SENSE and IN-SENSE
13. Monitor and verify the outputs for OUT+ and OUT-

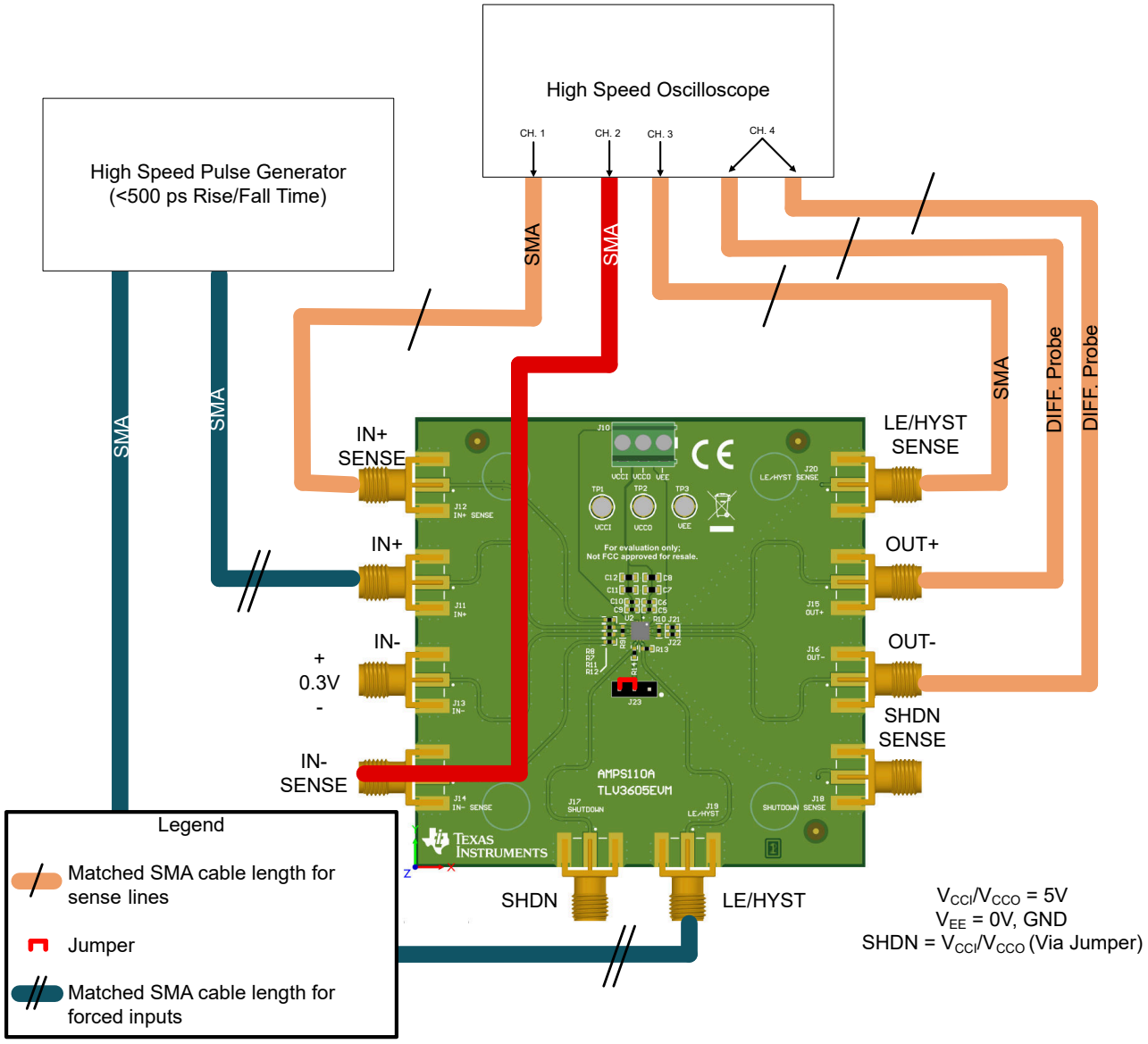

Figure 5-1. TLV3605 EVM Prop. Delay with Latch Setup

Next is a scope shot capture of the inputs and outputs described in the propagation delay procedure. This is defined as the time it takes for the output to respond when latch is disabled. Here, the propagation delay between LEB/HYST (LEB denotes active low) and the differential output is measured by taking the time delta between LEB/HYST 50% rising edge (disable latch), and when OUT (differential) reaches 50% of expected value (LOW). The propagation delay after latching was measured at 2.709ns with the setup described.

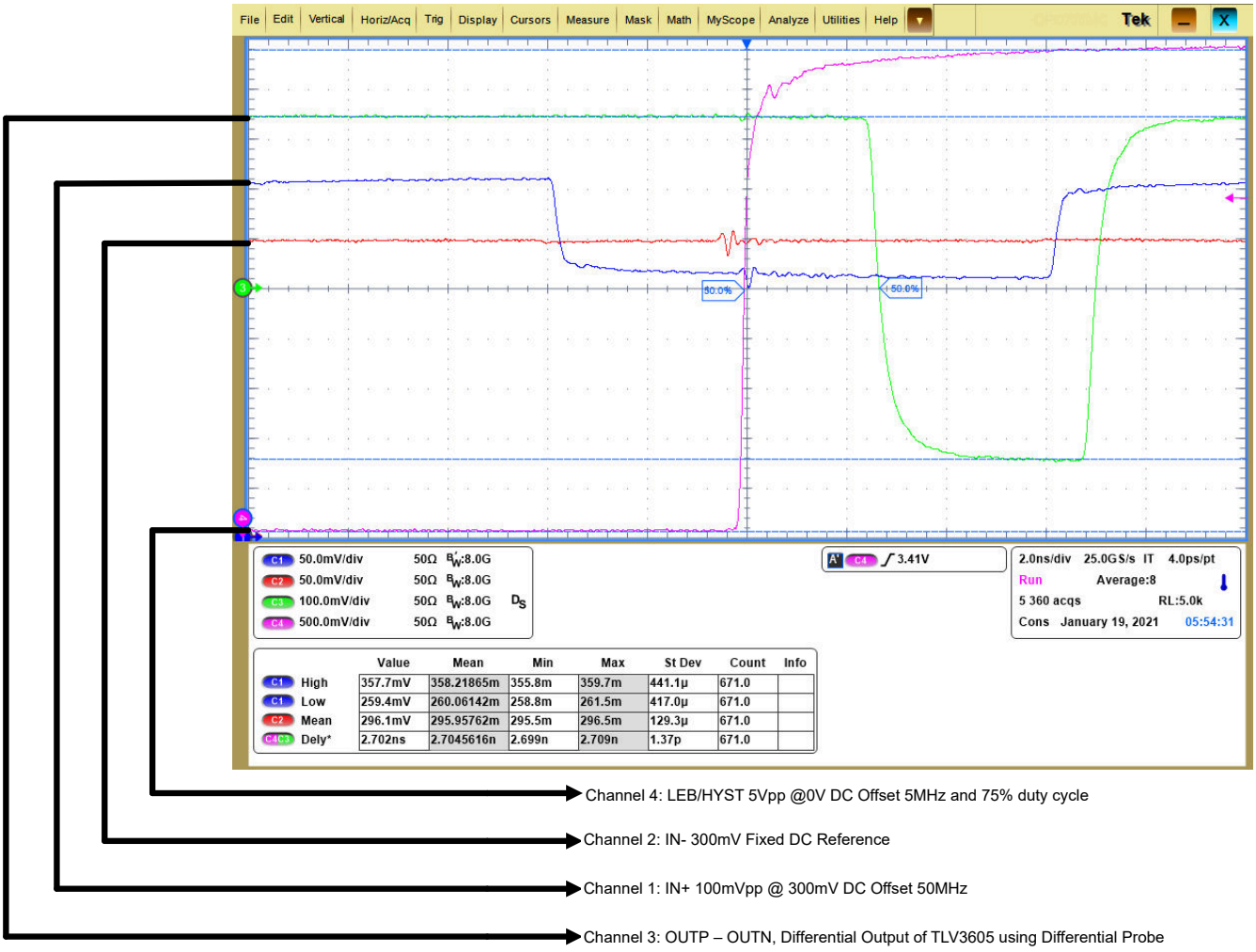

Figure 5-2. Quick Start Example

6 Board Setup

6.1 Supply Voltage

The TLV3605EVM operates from +2.4 V to +5.5 V. Connect VCCI and VEE using TP1 and TP3 respectively. Alternatively, J10 can also be used.

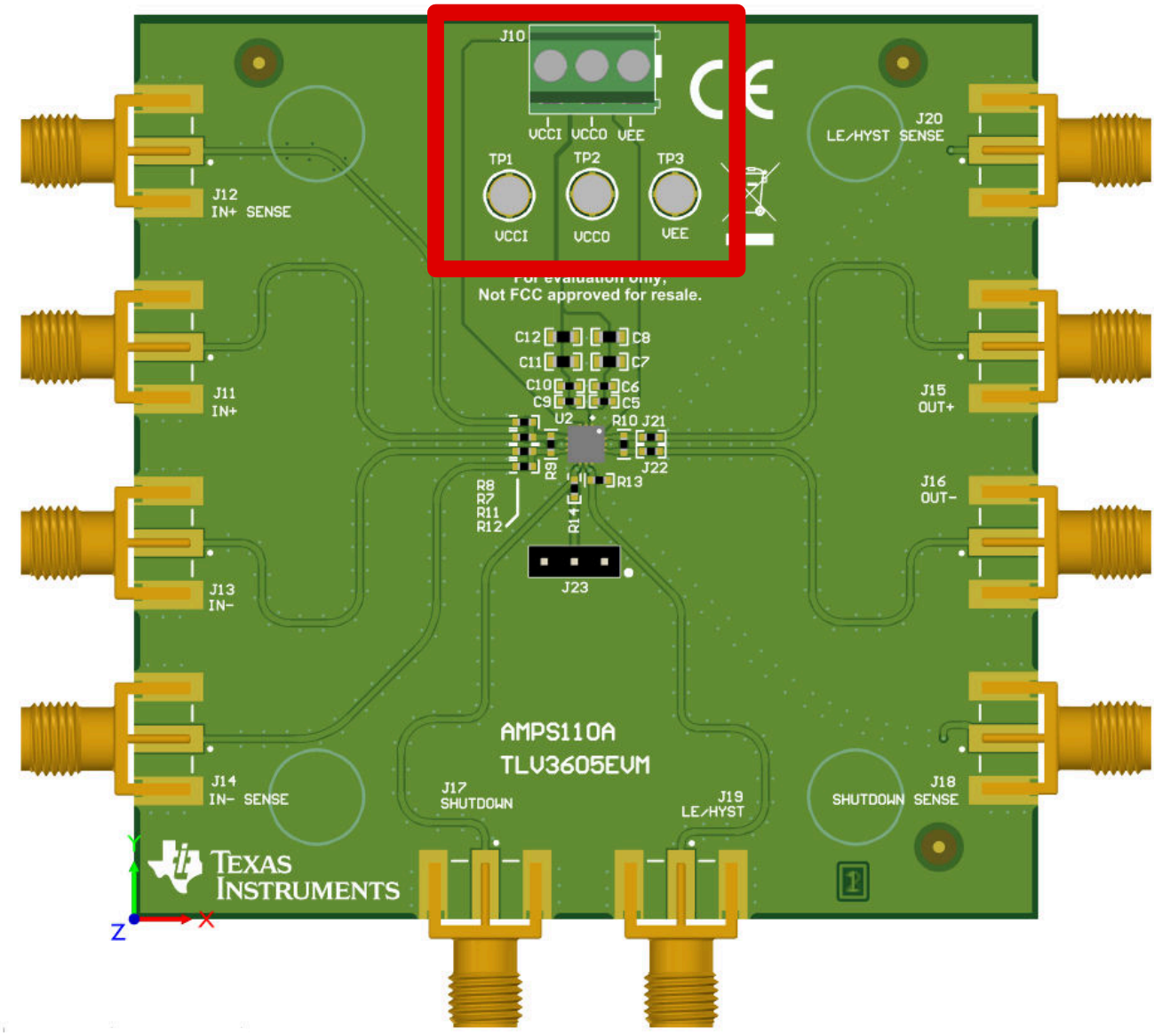

Figure 6-1. TLV3605EVM Supply Voltage Connection

6.2 Inputs

Resistors R8, R7, R11, and R12 are all 0 ohm resistors. The input terminals (IN+ and IN-) have corresponding sense lines so that the inputs to the device can be terminated on the lines with 50 ohms to an oscilloscope. This allows the input signals to be observed with minimal loading and distortion.

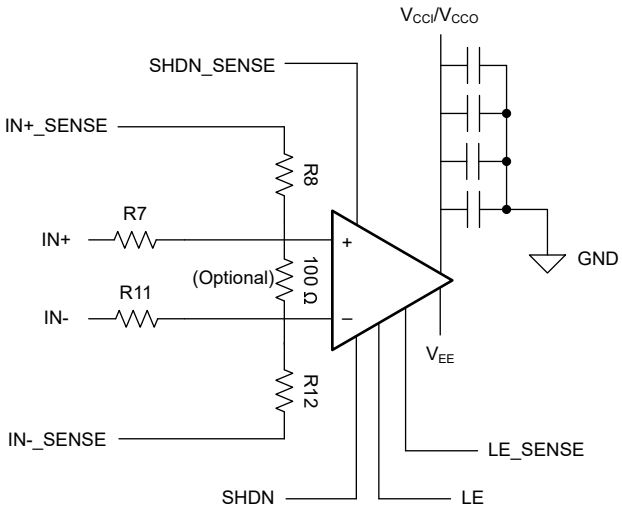

Figure 6-2. Input Side Schematic

The TLV3605EVM has an optional resistor pad between the device inputs meant for a 100 Ω resistor. This resistor is only needed if applying an unterminated LVDS signal to the board, otherwise it can be left uninstalled.

6.3 Outputs

R10 is only needed if it is preferred to measure the LVDS output directly across the component, or if the board is being used to feed directly to the inputs of another interconnect device such as an FPGA. Otherwise it can be left uninstalled.

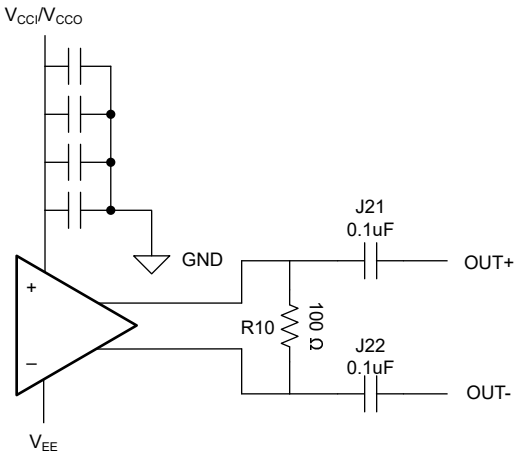

Figure 6-3. Output Side Schematic

J21 and J22 are installed with 0.1 uF capacitors. If probes are unavailable to measure the LVDS output across R10 or with a differential probe, these capacitors allow for the AC portion of the signal to be seen on a 50 Ω terminated scope. If equipment is available to measure the LVDS output with a respect to the 100 Ω resistor or with a differential probe, then J21 and J22 can be replaced with 0 Ω resistors to keep the DC integrity of the output signal.

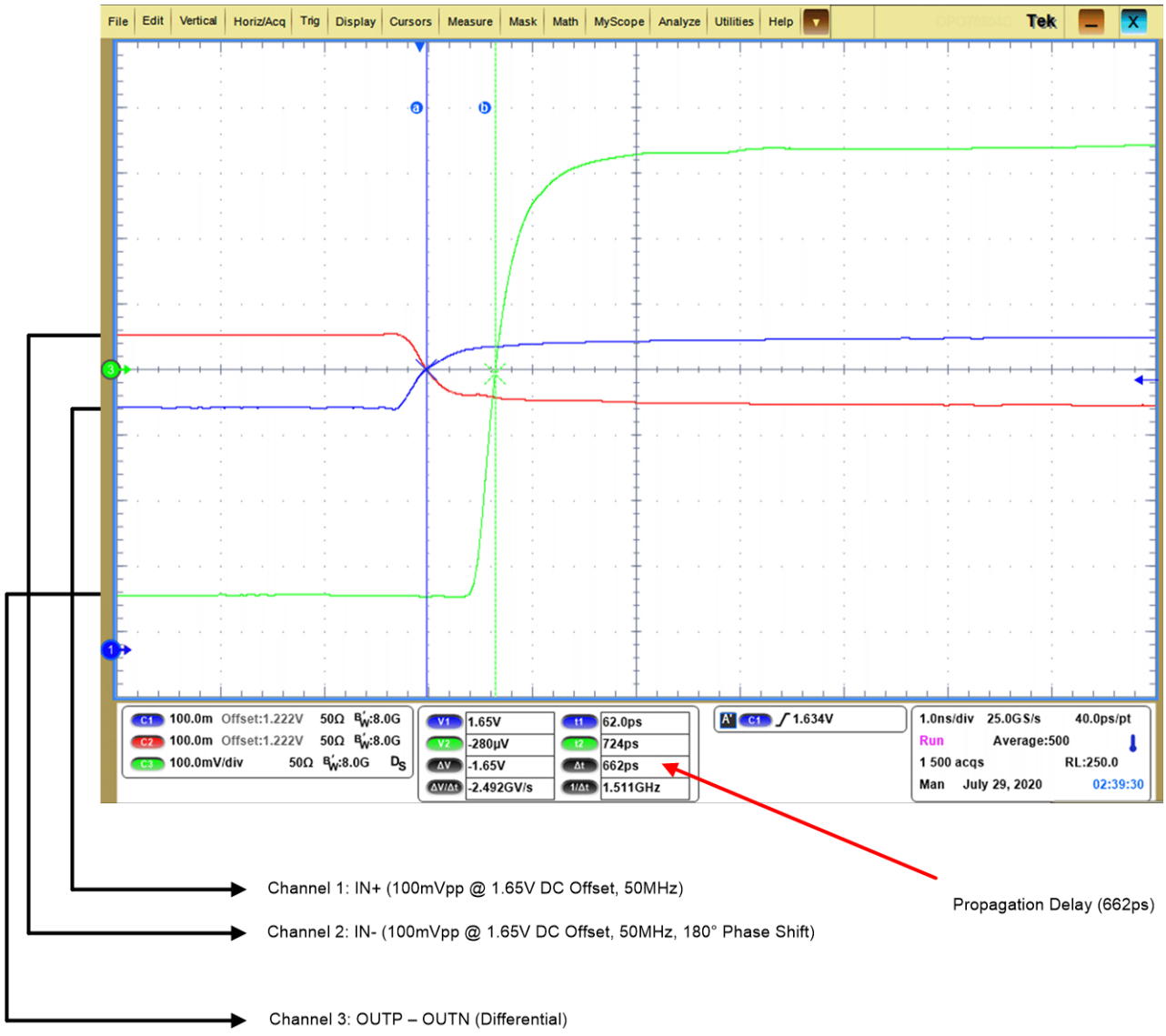

Figure 6-4. Differential Output of TLV3605EVM

7 Layout Guidelines

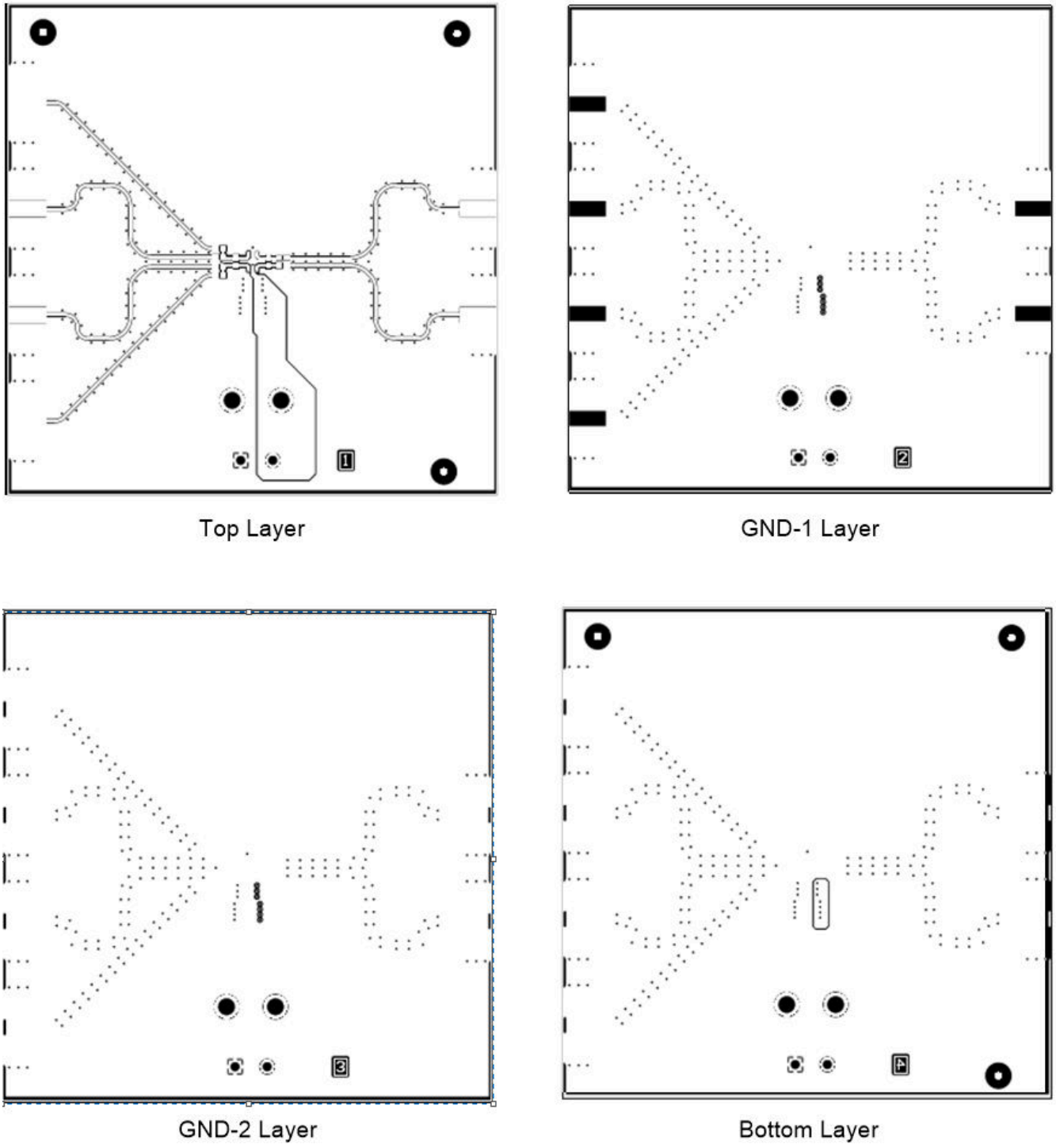

Figure 7-1. Layers

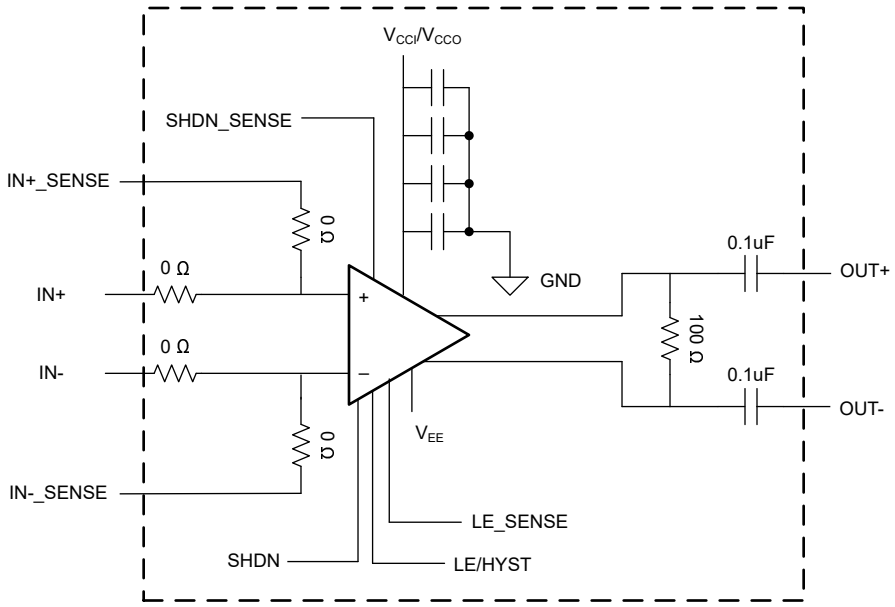

Figure 7-2. Block Diagram

8 Schematic

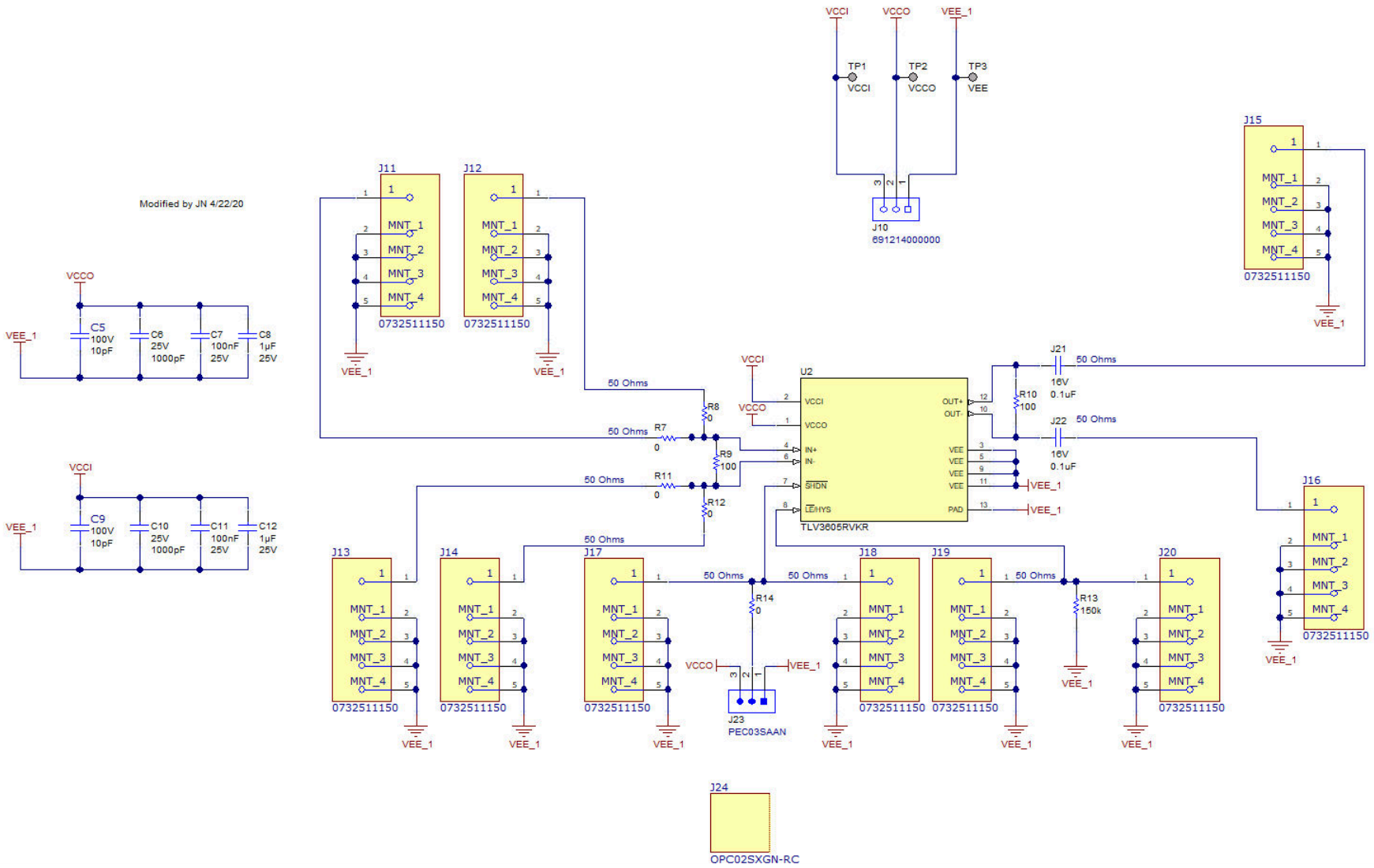

Figure 8-1. TLV3605 EVM Schematic

9 Bill of Materials

Table 9-1. BOM

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
C5, C9	2		CAP 0402 10pF 5% C0G 100V 30ppm	0402 (1005M)	GRT1555C2A100JA02D	Murata		
C6, C10	2	1000pF	CAP, CERM, 1000 pF, 25 V,+/- 5%, C0G/NP0, 0402	0402	C0402C102J3GACTU	Kemet		
C7, C11	2	0.1uF	CAP, CERM, 0.1 uF, 25 V, +/- 5%, X7R, 0603	0603	C0603C104J3RACTU	Kemet		
C8, C12	2	1uF	CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet		
FID1, FID2, FID3, FID4, FID5, FID6	6		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
H1, H2, H5, H6	4		Bumpon, Cylindrical, 0.312 X 0.200, Black	Black Bumpon	SJ61A1	3M		
J10	1		Terminal Block, 3.5mm, 3x1, Tin, TH	Terminal Block, 3.5mm, 3x1, Tin, TH	691214000000	Wurth Elektronik		
J11, J12, J13, J14, J15, J16, J17, J18, J19, J20	10		SMA Connector Receptacle, Female Socket 50Ohm Board Edge, End Launch Solder		0732511150	Molex Inc		
J21, J22	2	0.1uF	CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0402	0402	C0402C104K4RACAUTO	Kemet		
J23	1		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		
J24	1		CONN JUMPER S2 (1 x 2) Position Shunt Connector Black Open Top 0.100" (2.54mm) GoldHORTING .100 " GOLD	JUMPER	QPC02SXGN-RC	Sullins		
R7, R8, R11, R12, R14	5	0	RES, 0, 0%, 0.2 W, AEC-Q200 Grade 0, 0402	0402	CRCW04020000Z0EDHP	Vishay-Dale		

Table 9-1. BOM (continued)

Designator	Quantity	Value	Description	PackageReference	PartNumber	Manufacturer	Alternate PartNumber	Alternate Manufacturer
R13	1	150k	RES, 150 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF1503X	Panasonic		
TP1, TP2, TP3	3		Terminal, Turret, TH, Triple	Keystone1598-2	1598-2	Keystone		
U2	1		1ns High-Speed Comparator with LVDS Outputs, RVK0012A (QFN-12)	RVK0012A	TLV3605RVKR	Texas Instruments		Texas Instruments
R9, R10	0	100	RES, 100, 0.1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	MCS0402MD1000BE100	Vishay/Beyschlag		

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265