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U_J1
J1.SchDoc

U_J2
J2.SchDoc

U_J3
J3.SchDoc

U_J4
J4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_B64
B64.SchDoc

U_B65
B65.SchDoc

U_B66
B66.SchDoc

U_B_GT
B_GT.SchDoc

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B_PS_GT.SchDoc

U_PS_DDR
PS_DDR.SchDoc

U_B_MIO
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Clock.SchDoc

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CONFIG.SchDoc

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DDR4-RAM.SchDoc

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DDR4-RAM_4.SchDoc

U_DDR4-TERM
DDR4-TERM.SchDoc

U_ZU_POWER
ZU_POWER.SchDoc

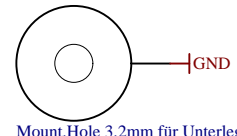
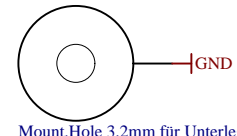
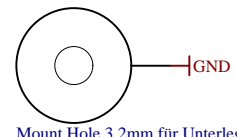
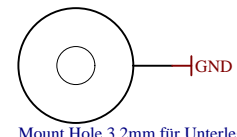
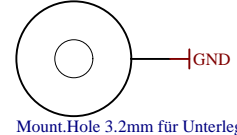
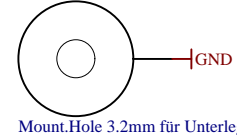
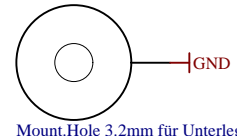
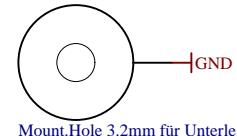
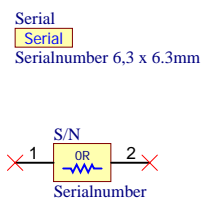
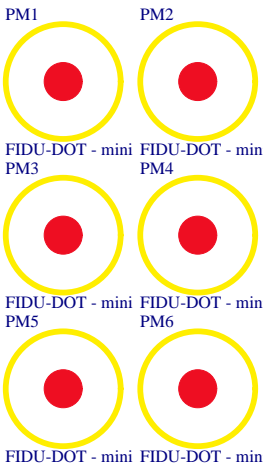
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ZU_PS_POWER.SchDoc

U_POWER
POWER.SchDoc

U_POWER_2
POWER_2.SchDoc

U_POWER_4
POWER_4.SchDoc

U_REV_CH
Revision_Changes.SchDoc



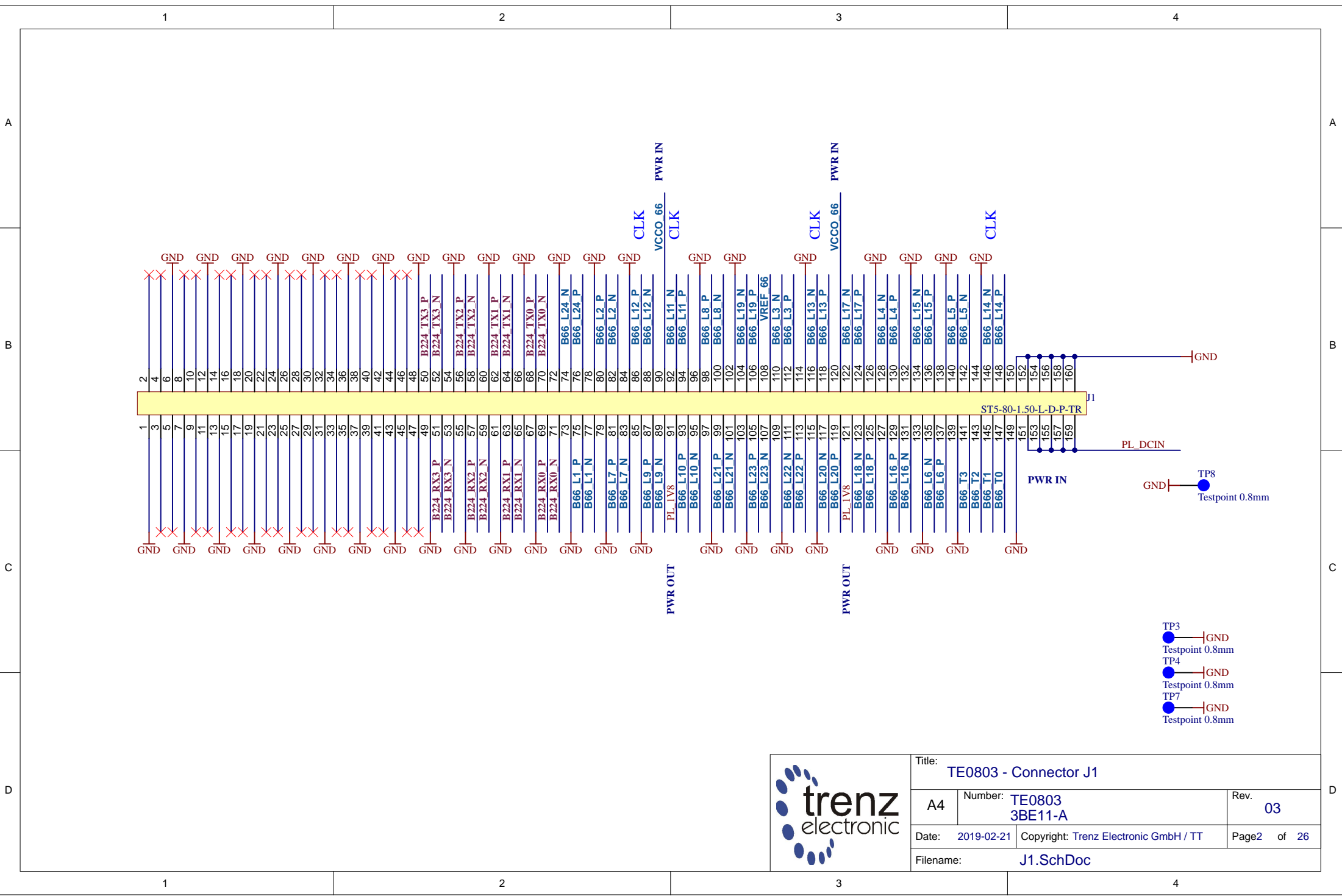
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A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page1 of 26
Filename: TE0803.SchDoc		

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Title: TE0803 - Connector J1		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page2 of 26
Filename: J1.SchDoc		

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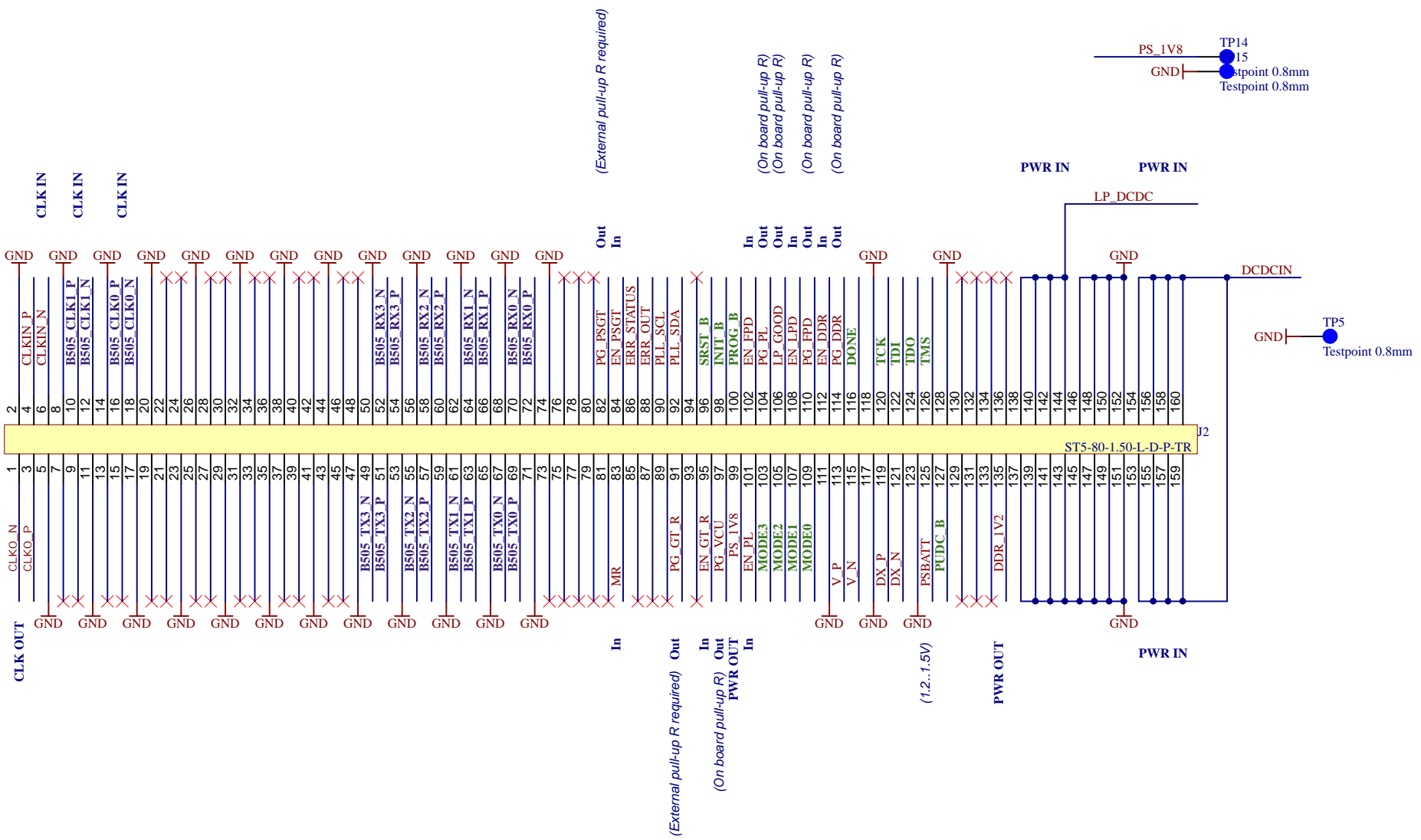
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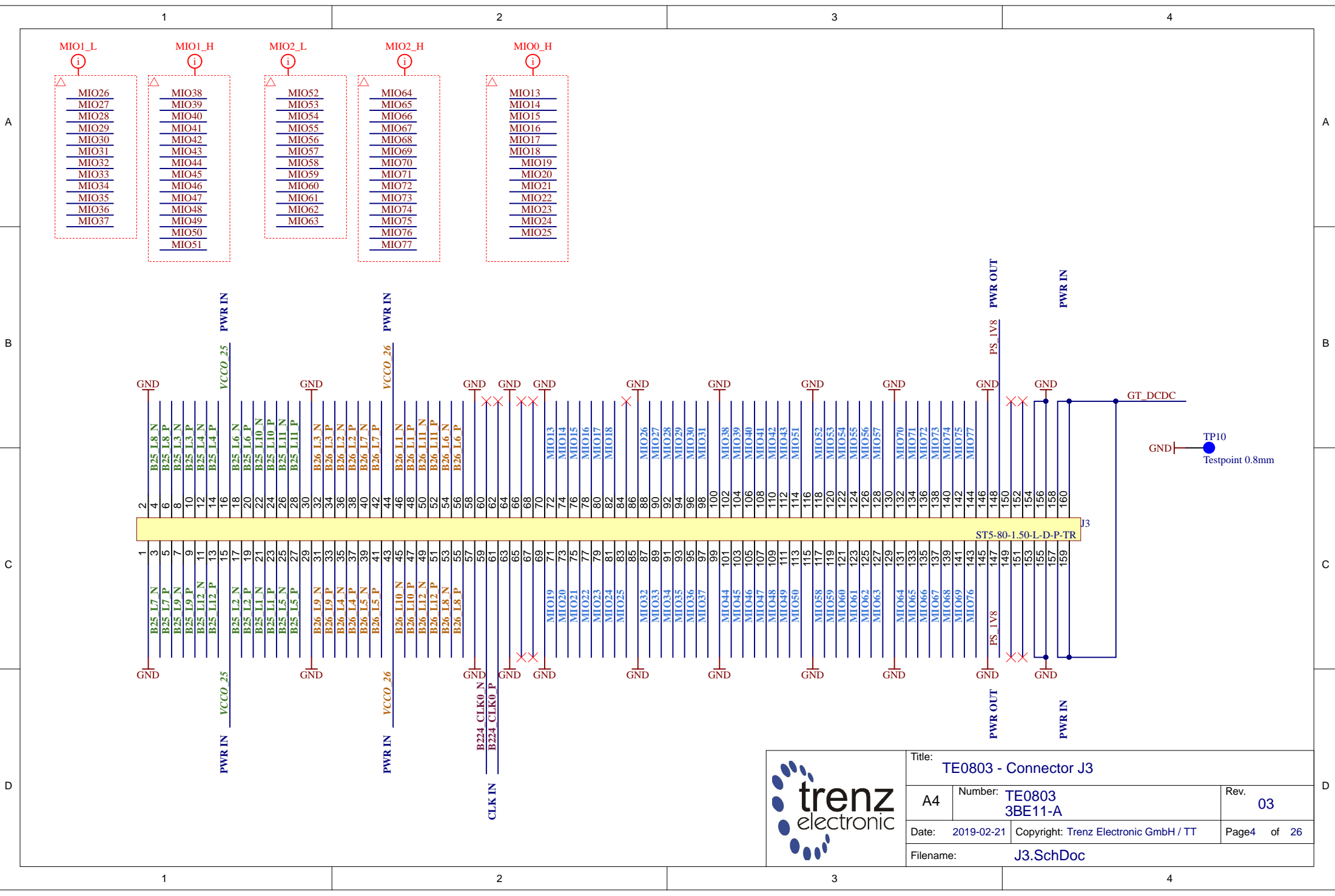
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Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT		Page3 of 26
Filename: J2.SchDoc				

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Title: TE0803 - Connector J3		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page4 of 26
Filename: J3.SchDoc		

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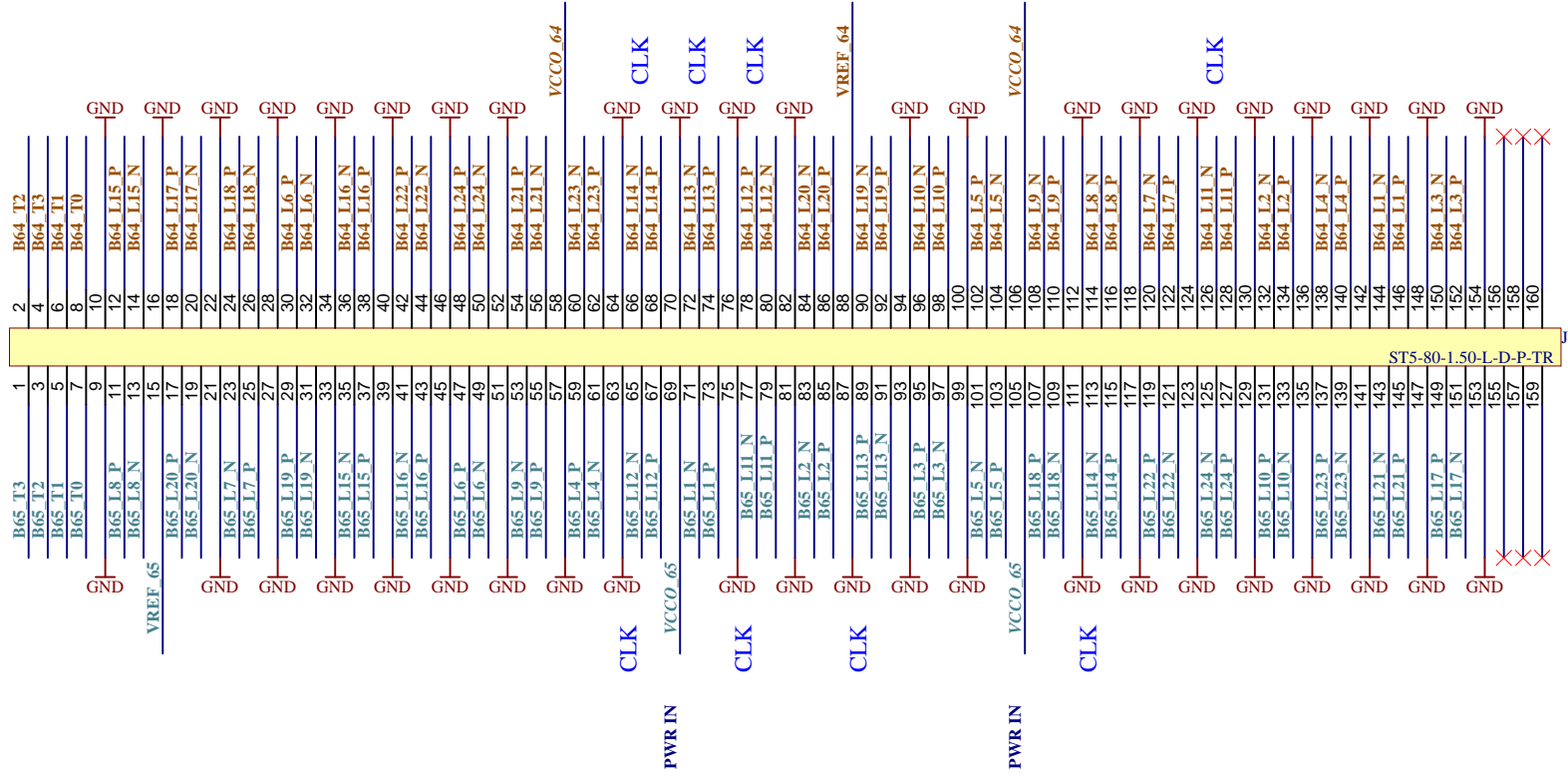
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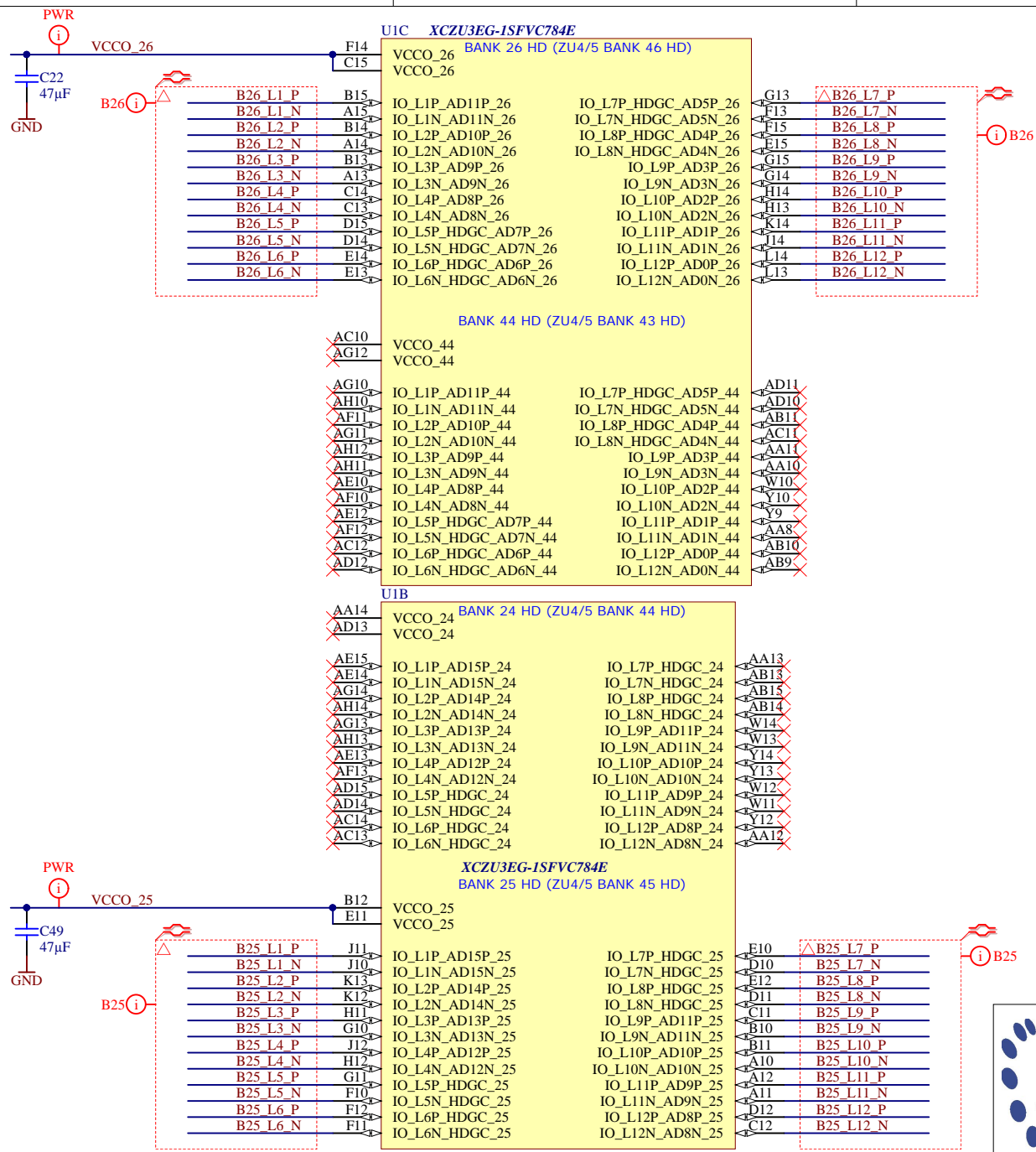
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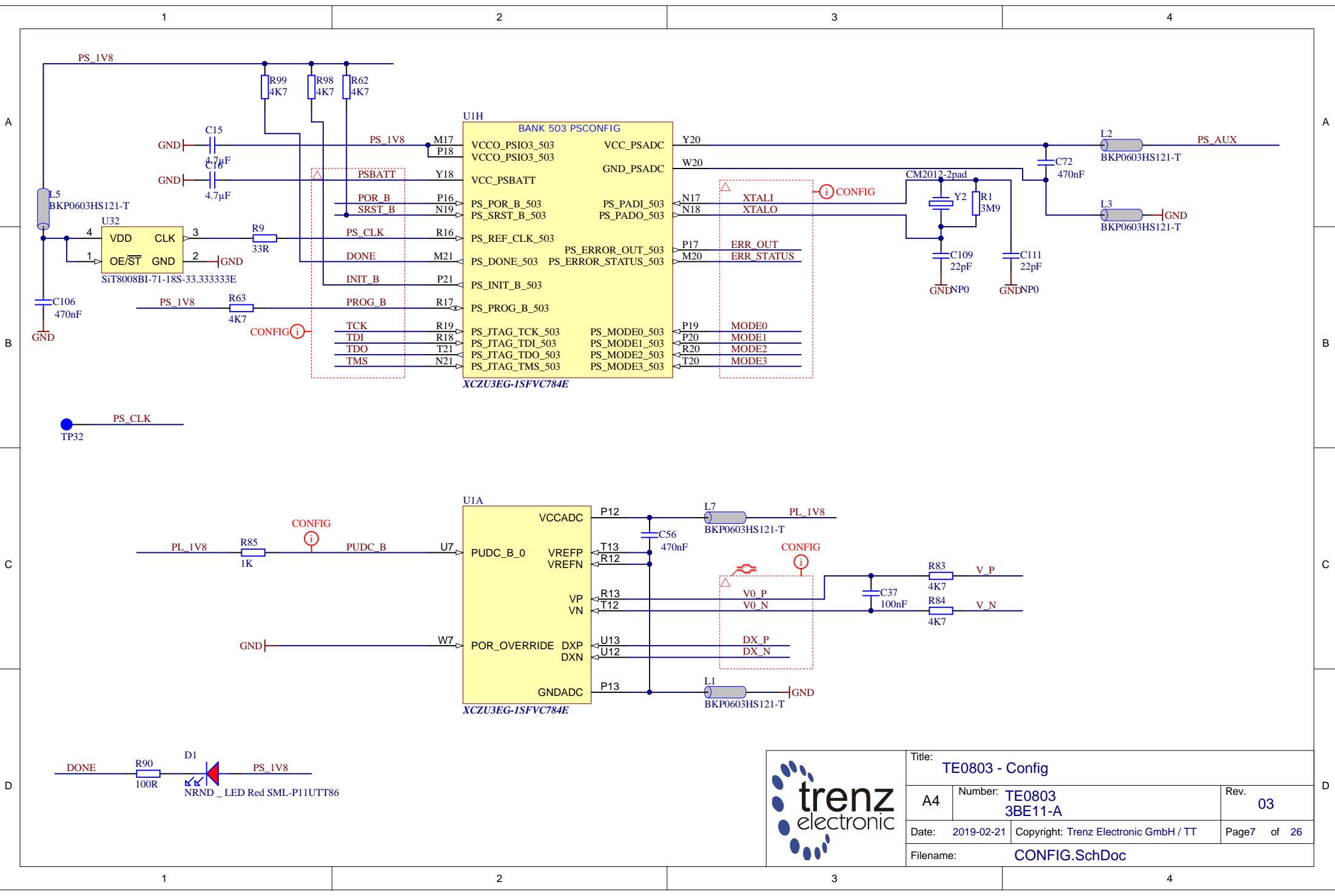
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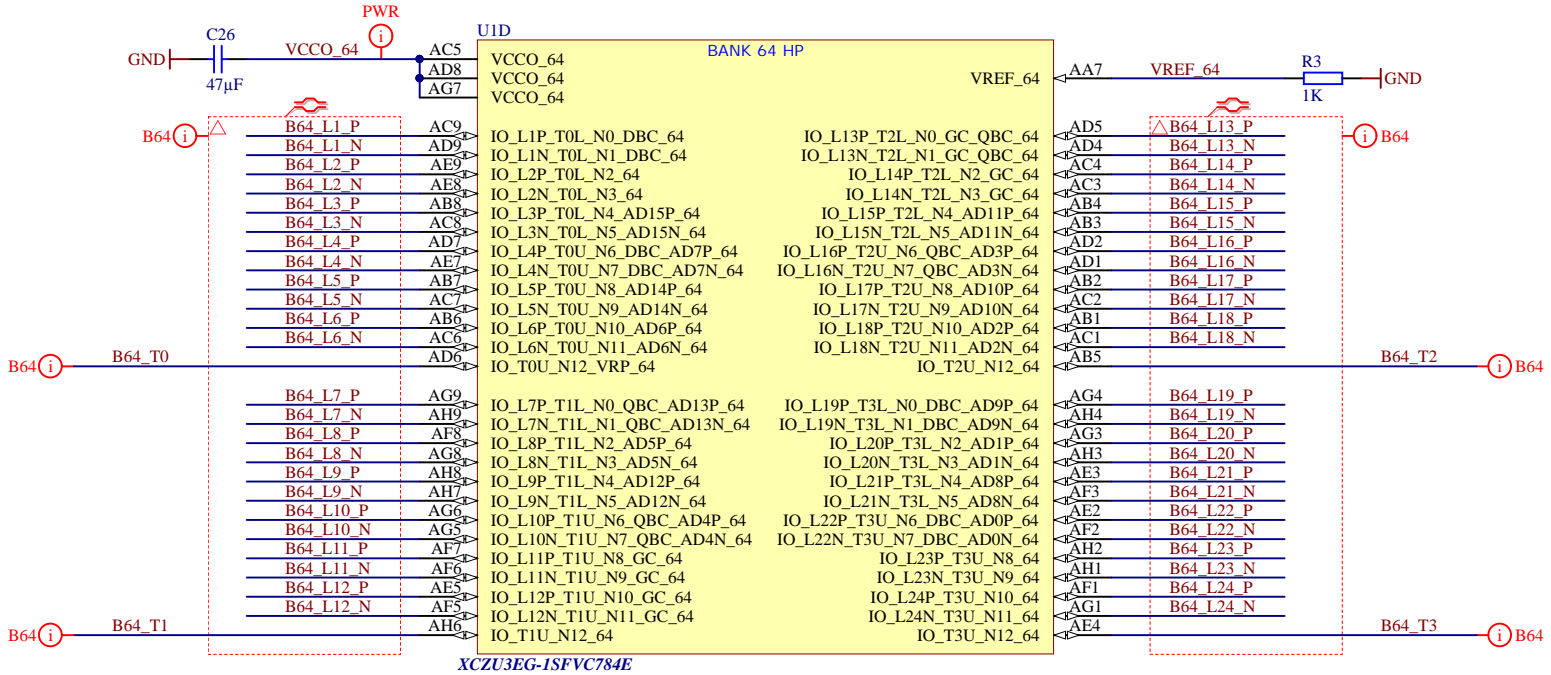
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page5 of 26
Filename: J4.SchDoc		



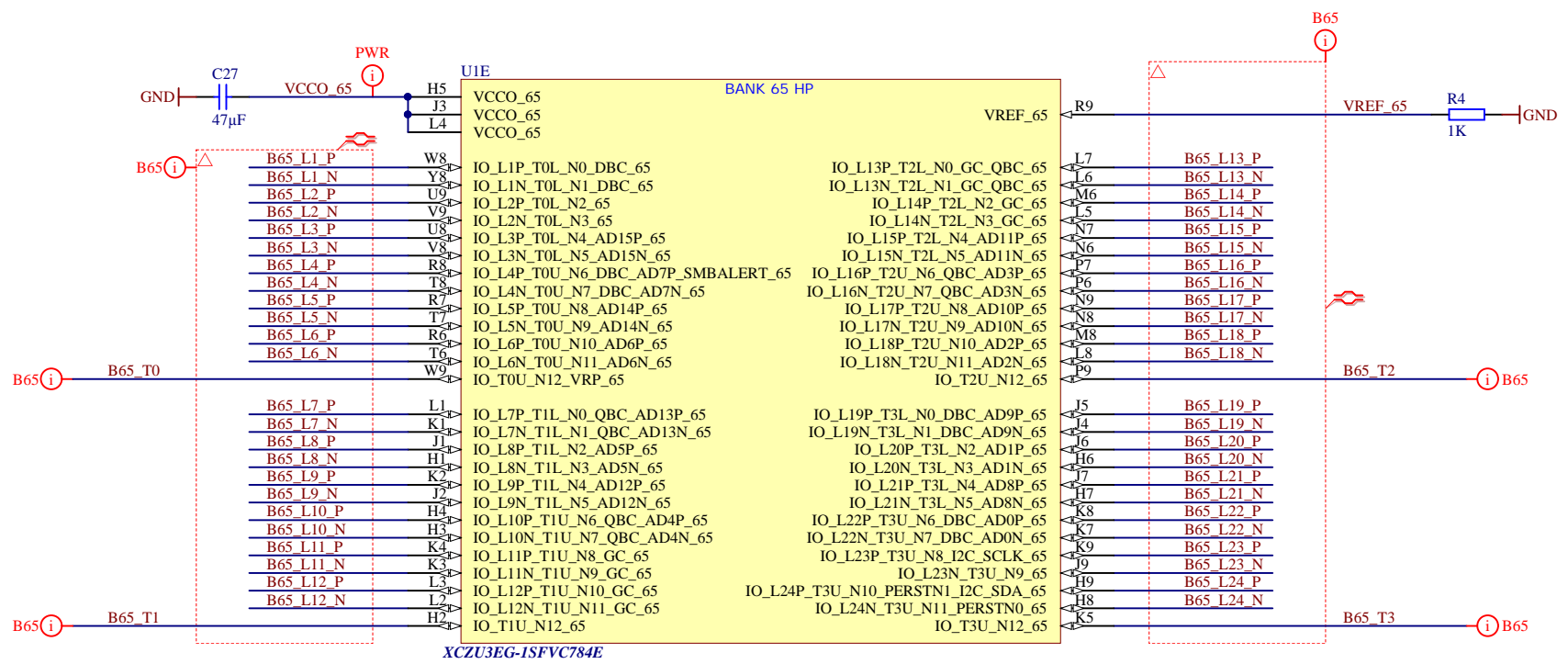
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 6 of 26
Filename: B_HD.SchDoc		



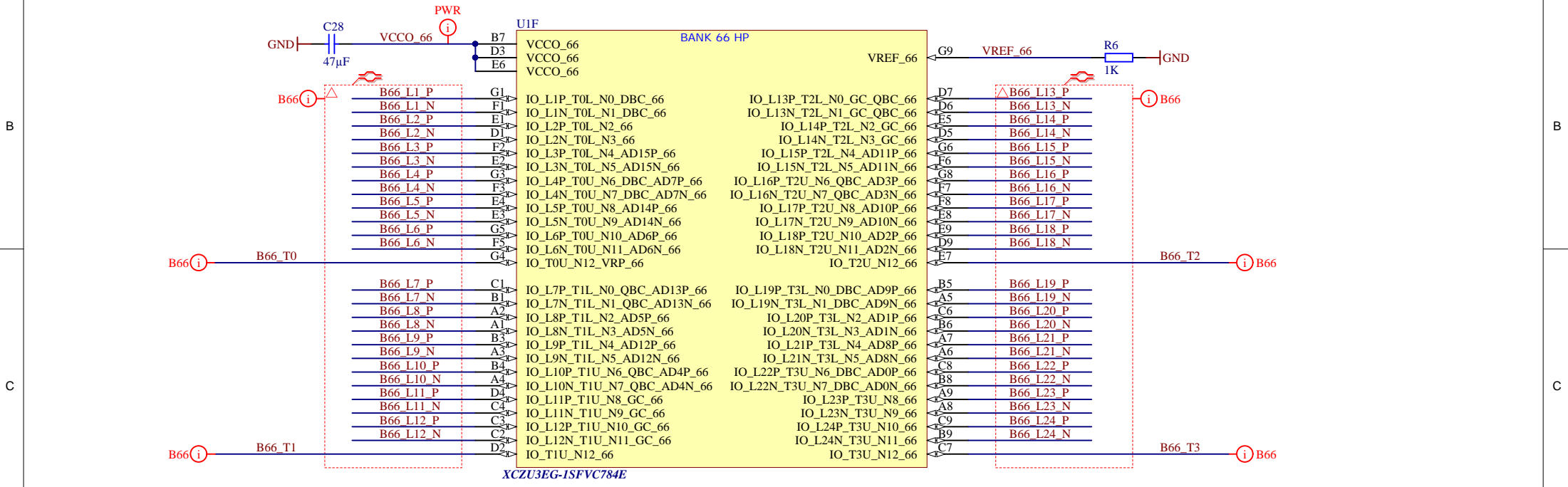
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 7 of 26
Filename: CONFIG.SchDoc		



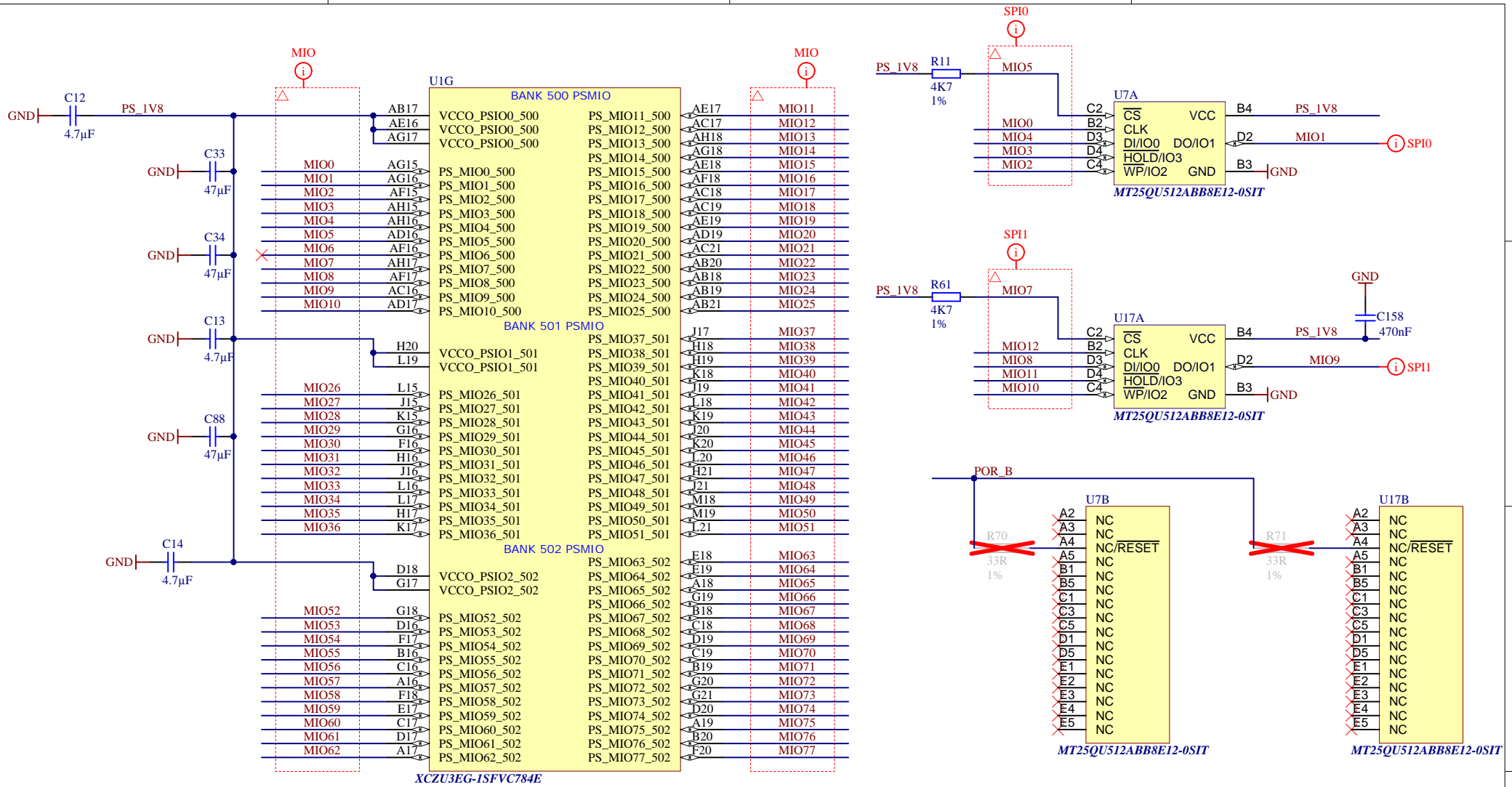
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 8 of 26
Filename: B64.SchDoc		



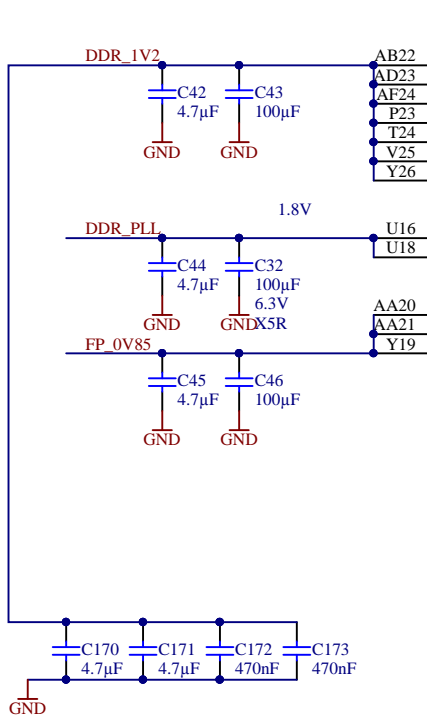
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A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page9 of 26
Filename: B65.SchDoc		



Title: TE0803 - B66		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 10 of 26
Filename: B66.SchDoc		



	Title: TE0803 - MIO Banks		
	A4	Number: TE0803 3BE11-A	Rev. 03
	Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	
	Page 11 of 26	Page 11 of 26	
Filename: B_MIO.SchDoc			



U1I		BANK 504 PSDDR	
V25	DDR4-CLK0 P	W25	DDR4-CLK0 P
W26	DDR4-CLK0 N	W26	DDR4-CLK0 N
V28	DDR4-CKE0	V28	DDR4-CKE0
Y24		Y24	
Y25		Y25	
V27		V27	
W28	DDR4-A0	W28	DDR4-A0
Y28	DDR4-A1	Y28	DDR4-A1
AB28	DDR4-A2	AB28	DDR4-A2
AA28	DDR4-A3	AA28	DDR4-A3
Y27	DDR4-A4	Y27	DDR4-A4
AA27	DDR4-A5	AA27	DDR4-A5
Y22	DDR4-A6	Y22	DDR4-A6
AA23	DDR4-A7	AA23	DDR4-A7
AA22	DDR4-A8	AA22	DDR4-A8
AB23	DDR4-A9	AB23	DDR4-A9
AA25	DDR4-A10	AA25	DDR4-A10
AA26	DDR4-A11	AA26	DDR4-A11
AB25	DDR4-A12	AB25	DDR4-A12
AB26	DDR4-A13	AB26	DDR4-A13
AB24	DDR4-A14	AB24	DDR4-A14
AC24	DDR4-A15	AC24	DDR4-A15
AC23	DDR4-A16	AC23	DDR4-A16
AC22	DDR4-A17	AC22	DDR4-A17
W27	DDR4-CS	W27	DDR4-CS
V26		V26	
V23	DDR4-BA0	V23	DDR4-BA0
W22	DDR4-BA1	W22	DDR4-BA1
W24	DDR4-BG0	W24	DDR4-BG0
V22	DDR4-BG1	V22	DDR4-BG1
V24	DDR4-PAR	V24	DDR4-PAR
U23	DDR4-RESET	U23	DDR4-RESET
Y23	DDR4-ACT	Y23	DDR4-ACT
U25	DDR4-ALERT	U25	DDR4-ALERT
U24		U24	
U28	DDR4-ODT0	U28	DDR4-ODT0
U26		U26	

XCZU3EG-1SFVC784E

U1J		BANK 504 PSDDR	
DQ0	AD21	PS_DDR_DQ0_504	PS_DDR_DQ32_504
DQ1	AE20	PS_DDR_DQ1_504	PS_DDR_DQ33_504
DQ2	AD20	PS_DDR_DQ2_504	PS_DDR_DQ34_504
DQ3	AF20	PS_DDR_DQ3_504	PS_DDR_DQ35_504
DQ4	AH21	PS_DDR_DQ4_504	PS_DDR_DQ36_504
DQ5	AH20	PS_DDR_DQ5_504	PS_DDR_DQ37_504
DQ6	AH19	PS_DDR_DQ6_504	PS_DDR_DQ38_504
DQ7	AG19	PS_DDR_DQ7_504	PS_DDR_DQ39_504
DQ8	AF22	PS_DDR_DQ8_504	PS_DDR_DQ40_504
DQ9	AH22	PS_DDR_DQ9_504	PS_DDR_DQ41_504
DQ10	AE22	PS_DDR_DQ10_504	PS_DDR_DQ42_504
DQ11	AD22	PS_DDR_DQ11_504	PS_DDR_DQ43_504
DQ12	AH23	PS_DDR_DQ12_504	PS_DDR_DQ44_504
DQ13	AH24	PS_DDR_DQ13_504	PS_DDR_DQ45_504
DQ14	AE24	PS_DDR_DQ14_504	PS_DDR_DQ46_504
DQ15	AG24	PS_DDR_DQ15_504	PS_DDR_DQ47_504
DQ16	AC26	PS_DDR_DQ16_504	PS_DDR_DQ48_504
DQ17	AD26	PS_DDR_DQ17_504	PS_DDR_DQ49_504
DQ18	AD25	PS_DDR_DQ18_504	PS_DDR_DQ50_504
DQ19	AD24	PS_DDR_DQ19_504	PS_DDR_DQ51_504
DQ20	AG26	PS_DDR_DQ20_504	PS_DDR_DQ52_504
DQ21	AH25	PS_DDR_DQ21_504	PS_DDR_DQ53_504
DQ22	AH26	PS_DDR_DQ22_504	PS_DDR_DQ54_504
DQ23	AG25	PS_DDR_DQ23_504	PS_DDR_DQ55_504
DQ24	AH27	PS_DDR_DQ24_504	PS_DDR_DQ56_504
DQ25	AH28	PS_DDR_DQ25_504	PS_DDR_DQ57_504
DQ26	AF28	PS_DDR_DQ26_504	PS_DDR_DQ58_504
DQ27	AG28	PS_DDR_DQ27_504	PS_DDR_DQ59_504
DQ28	AC27	PS_DDR_DQ28_504	PS_DDR_DQ60_504
DQ29	AD27	PS_DDR_DQ29_504	PS_DDR_DQ61_504
DQ30	AD28	PS_DDR_DQ30_504	PS_DDR_DQ62_504
DQ31	AC28	PS_DDR_DQ31_504	PS_DDR_DQ63_504
DDR4-DQS0 P	AF21	PS_DDR_DQS_P0_504	PS_DDR_DQ64_504
DDR4-DQS0 N	AG21	PS_DDR_DQS_N0_504	PS_DDR_DQ65_504
DDR4-DQS1 P	AF23	PS_DDR_DQS_P1_504	PS_DDR_DQ66_504
DDR4-DQS1 N	AG23	PS_DDR_DQS_N1_504	PS_DDR_DQ67_504
DDR4-DQS2 P	AF25	PS_DDR_DQS_P2_504	PS_DDR_DQ68_504
DDR4-DQS2 N	AF26	PS_DDR_DQS_N2_504	PS_DDR_DQ69_504
DDR4-DQS3 P	AE27	PS_DDR_DQS_P3_504	PS_DDR_DQ70_504
DDR4-DQS3 N	AF27	PS_DDR_DQS_N3_504	PS_DDR_DQ71_504
DDR4-DQS4 P	N23	PS_DDR_DQS_P4_504	PS_DDR_DM0_504
DDR4-DQS4 N	M23	PS_DDR_DQS_N4_504	PS_DDR_DM1_504
DDR4-DQS5 P	L23	PS_DDR_DQS_P5_504	PS_DDR_DM2_504
DDR4-DQS5 N	K23	PS_DDR_DQS_N5_504	PS_DDR_DM3_504
DDR4-DQS6 P	N26	PS_DDR_DQS_P6_504	PS_DDR_DM4_504
DDR4-DQS6 N	N27	PS_DDR_DQS_N6_504	PS_DDR_DM5_504
DDR4-DQS7 P	J26	PS_DDR_DQS_P7_504	PS_DDR_DM6_504
DDR4-DQS7 N	J27	PS_DDR_DQS_N7_504	PS_DDR_DM7_504
	R27	PS_DDR_DQS_P8_504	PS_DDR_DM8_504
	T27	PS_DDR_DQS_N8_504	

XCZU3EG-1SFVC784E



Title: TE0803 - PS_DDR		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 12 of 26
Filename: PS_DDR.SchDoc		

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A

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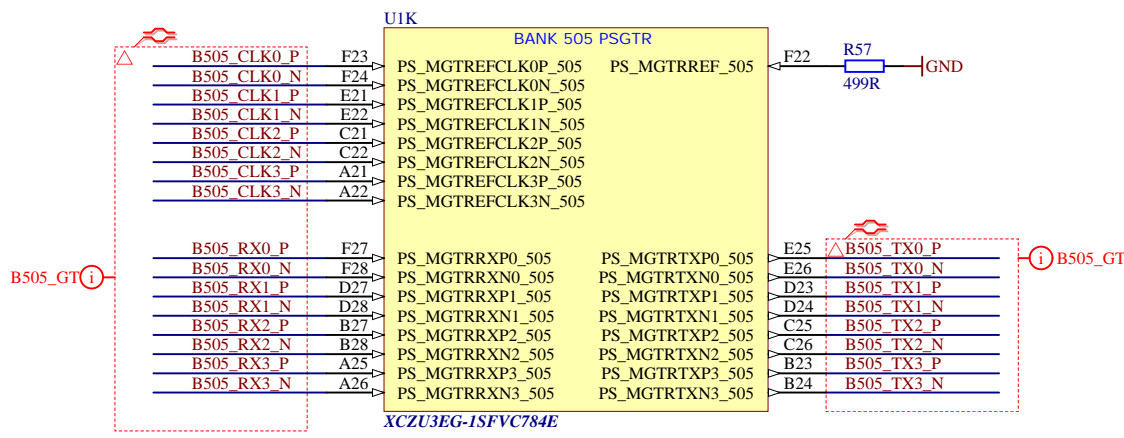
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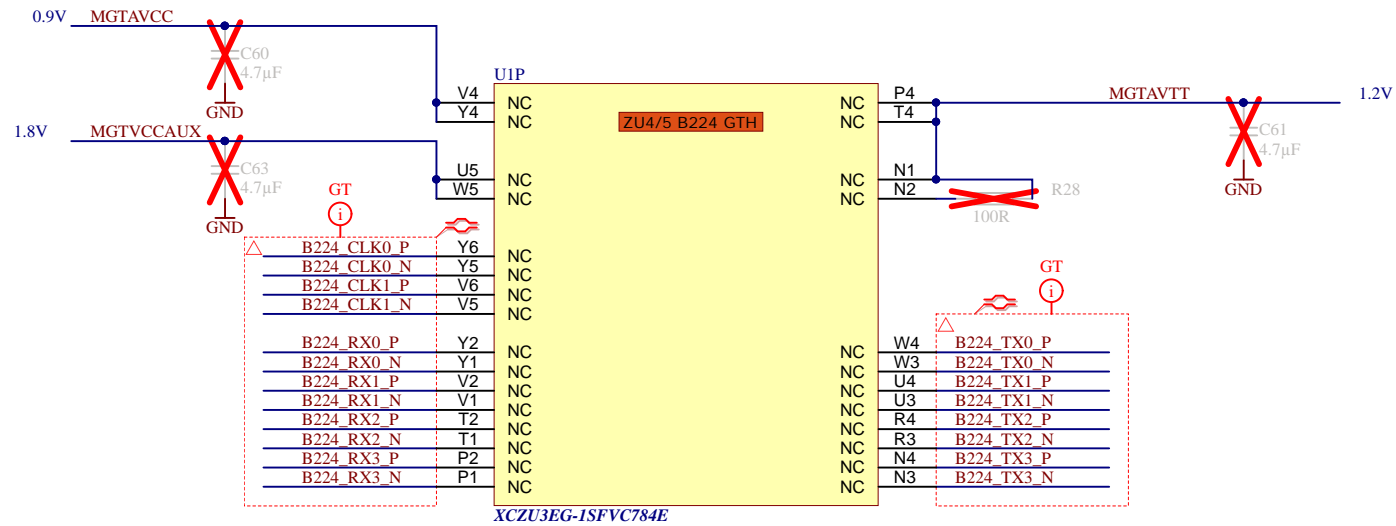

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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 13 of 26
Filename: B_PS_GT.SchDoc		

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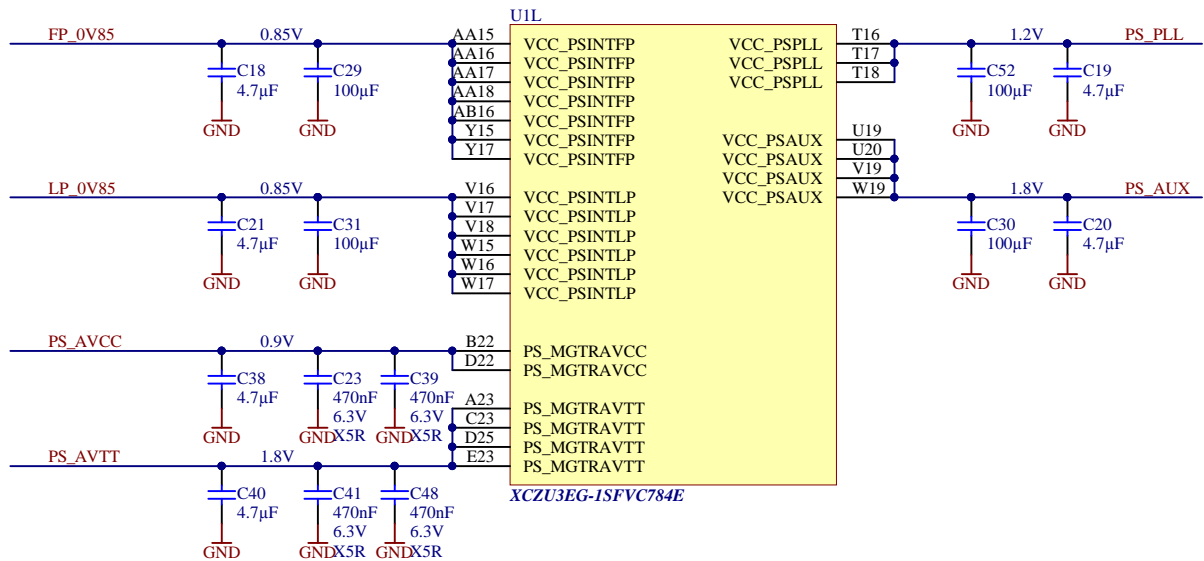
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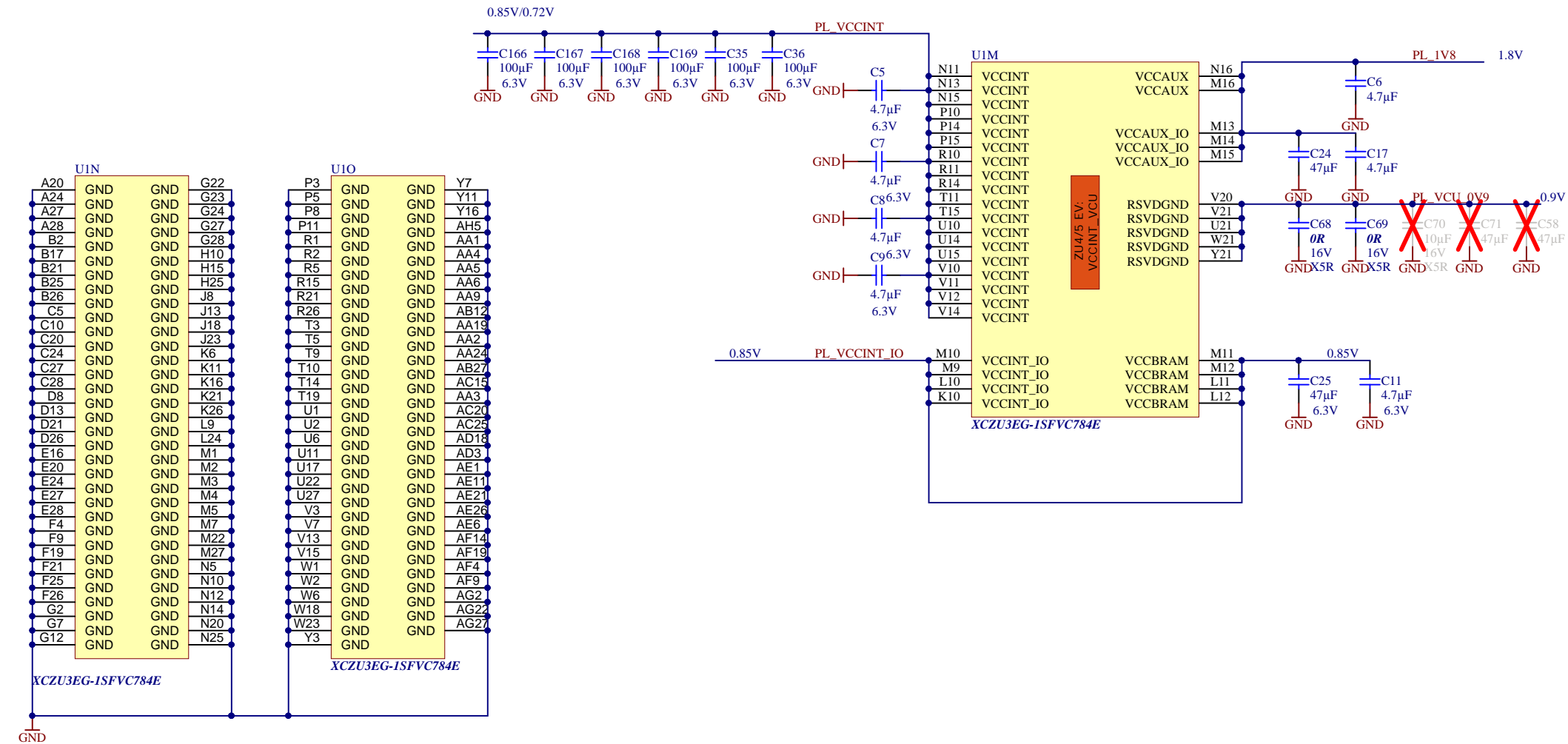
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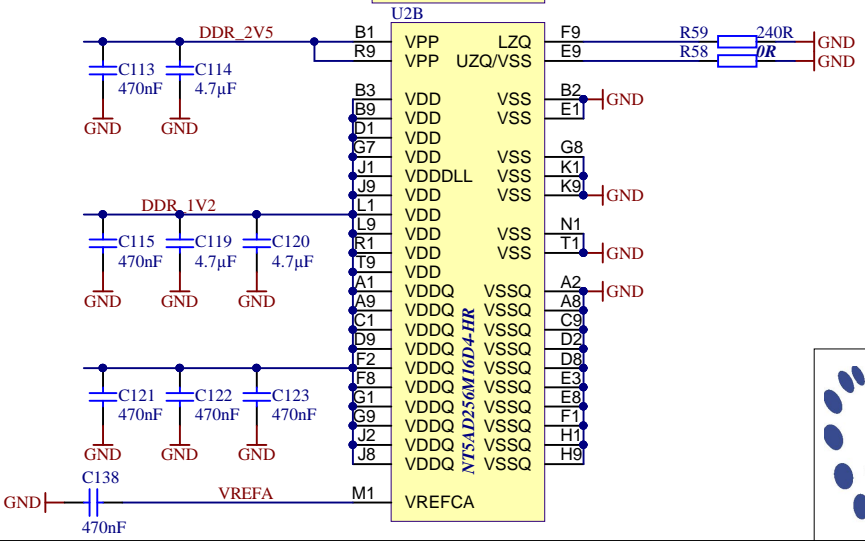
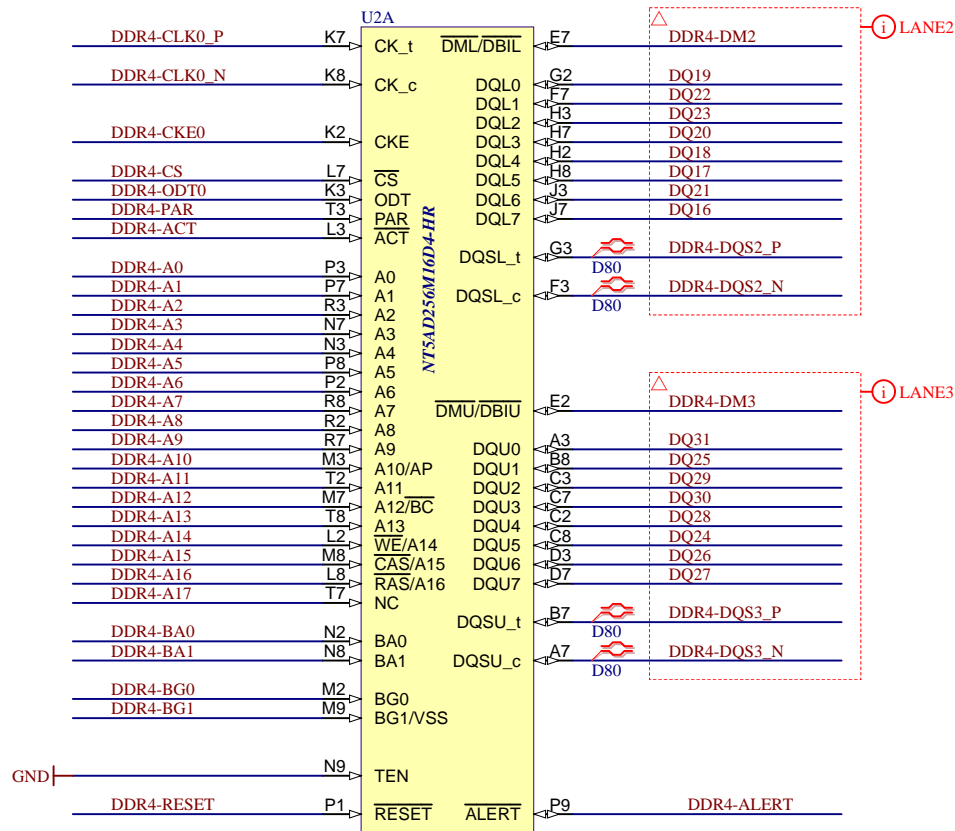
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 14 of 26
Filename: B_GT.SchDoc		



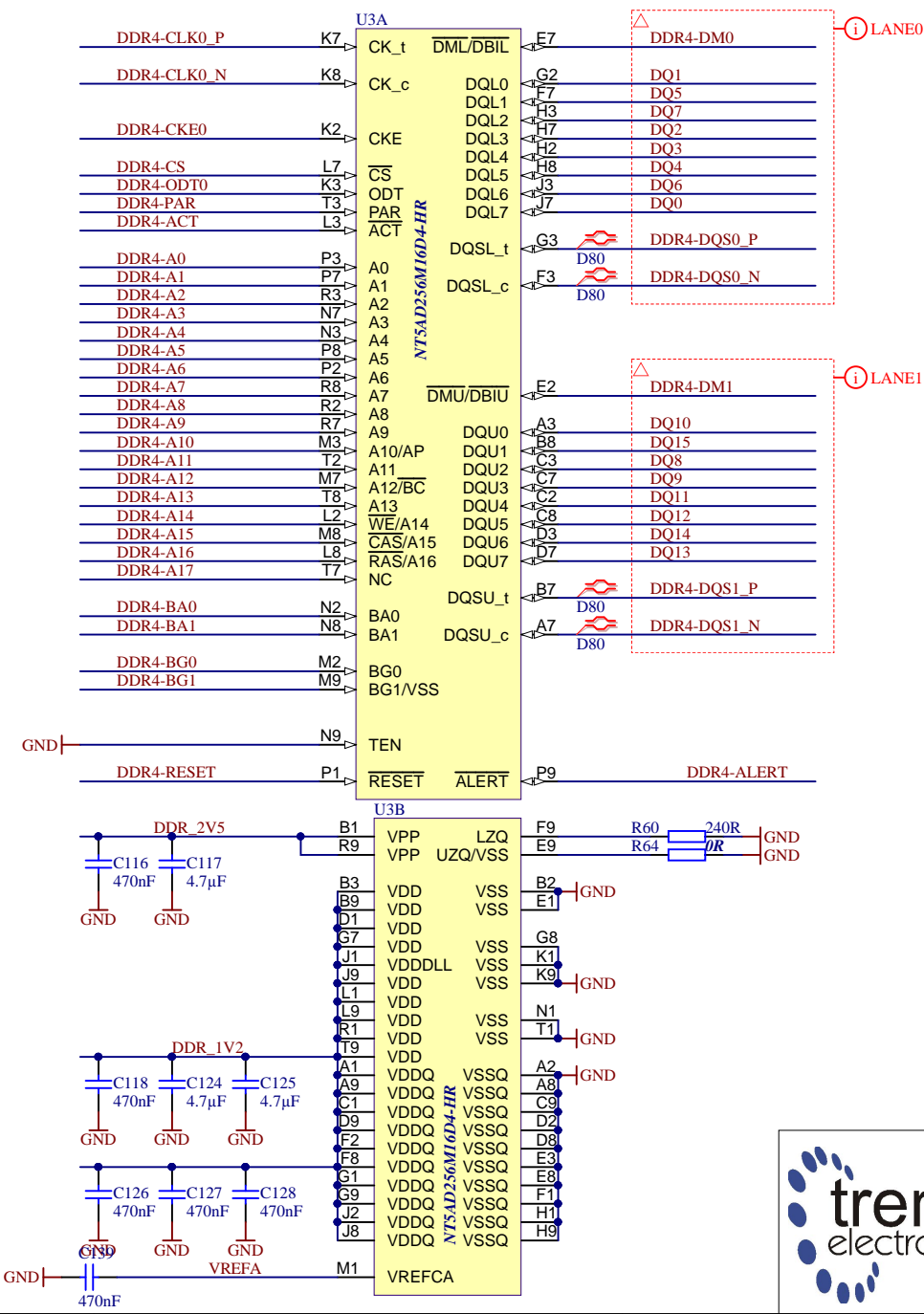
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Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_PS_POWER.SchDoc		Page 15 of 26	



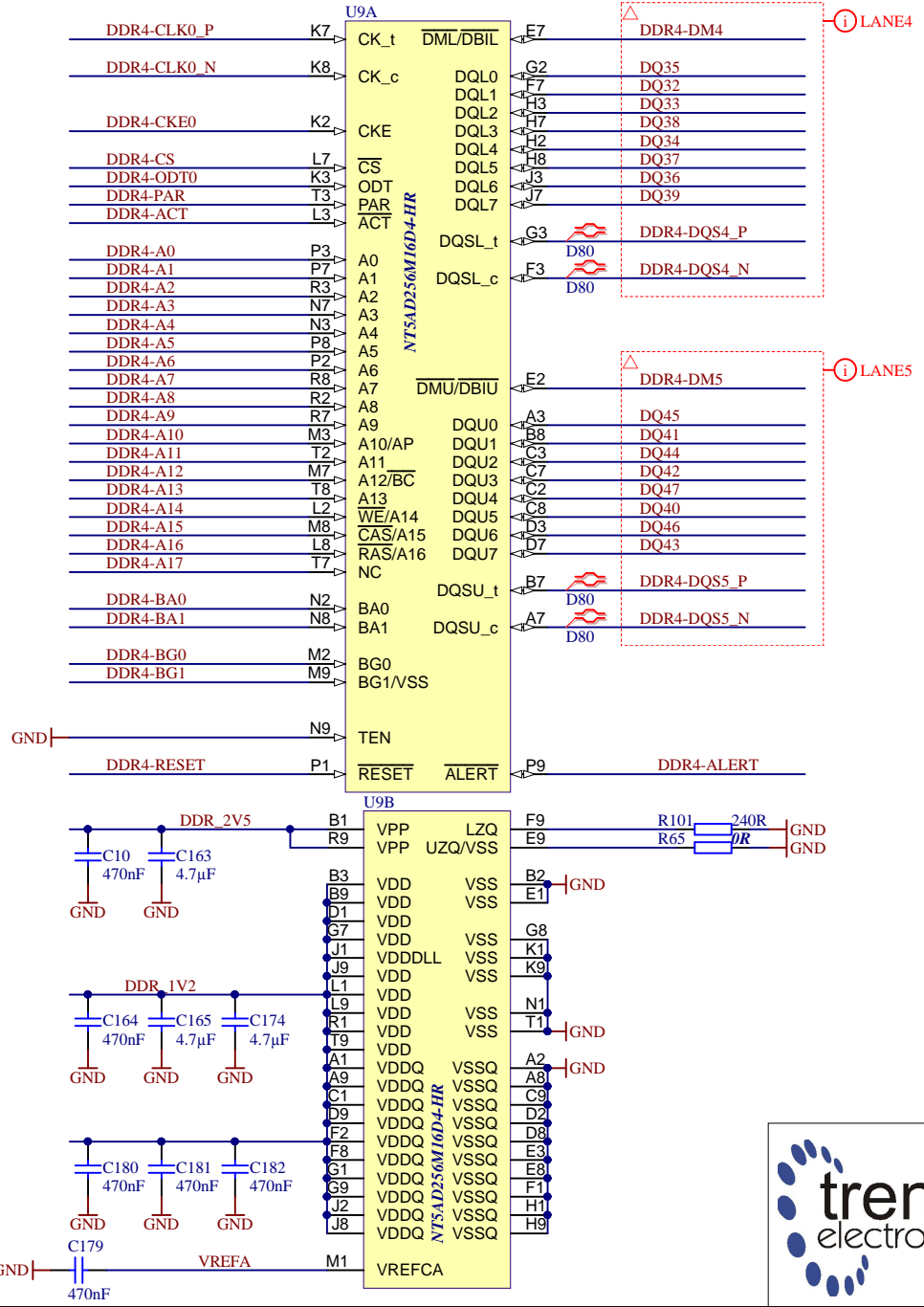
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Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Filename: ZU_POWER.SchDoc		Page 16 of 26	



Title: TE0803 - DDR4_1_RAM		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 17 of 26
Filename: DDR4-RAM.SchDoc		



Title: TE0803 - DDR4_2_RAM		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page18 of 26
Filename: DDR4-RAM_2.SchDoc		



Title: TE0803 - DDR4_3_RAM		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 19 of 26
Filename: DDR4-RAM_3.SchDoc		

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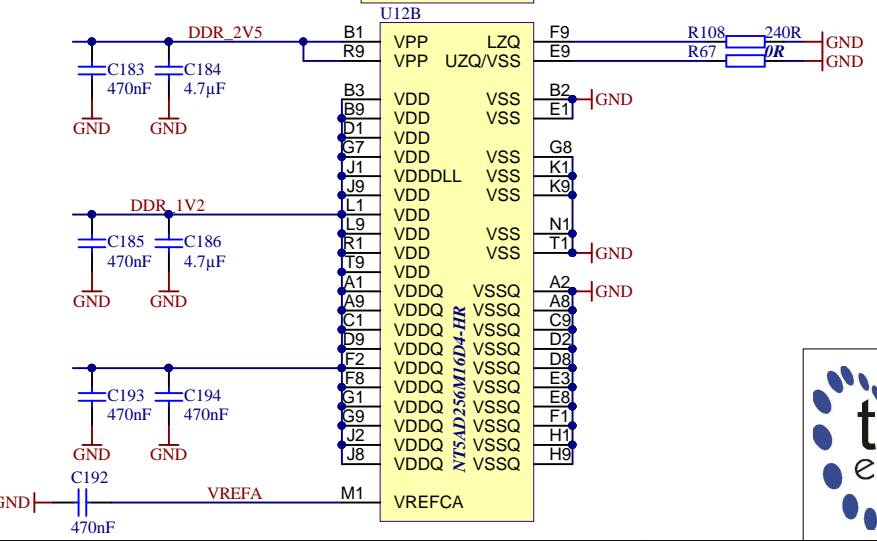
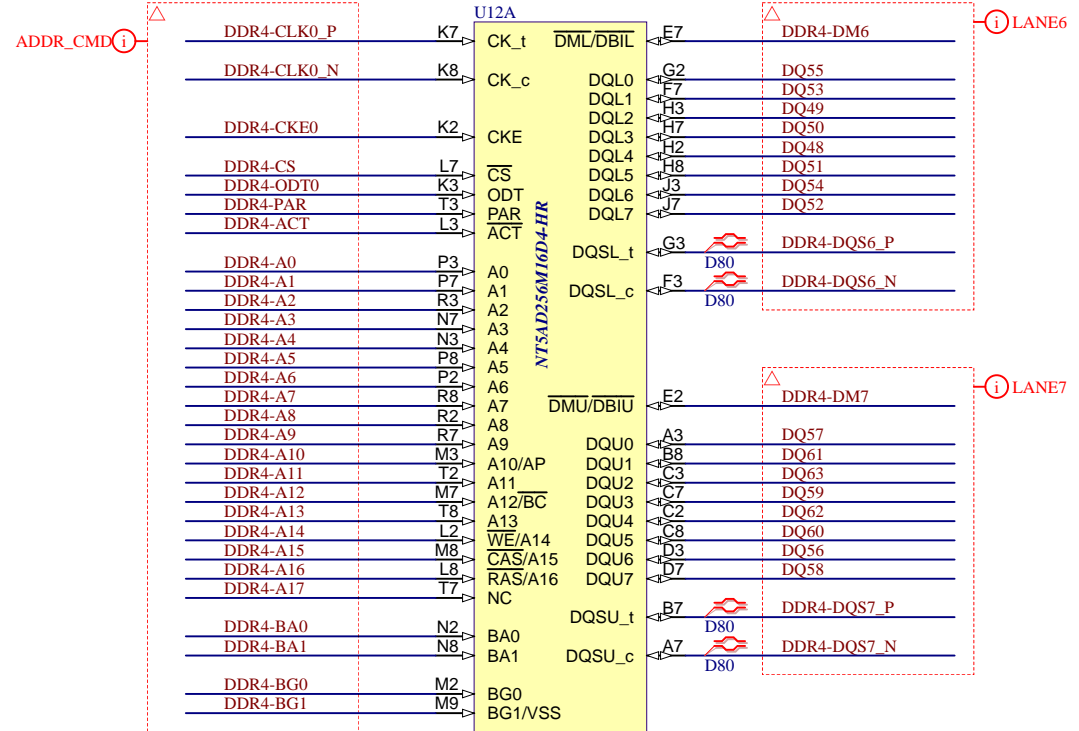

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Title: TE0803 - DDR4_4_RAM		
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 20 of 26
Filename: DDR4-RAM_4.SchDoc		

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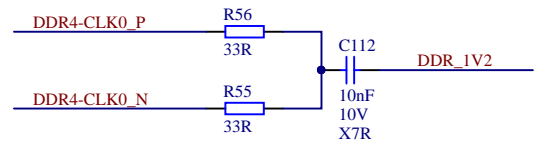
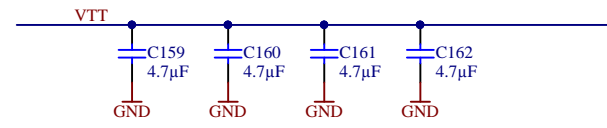
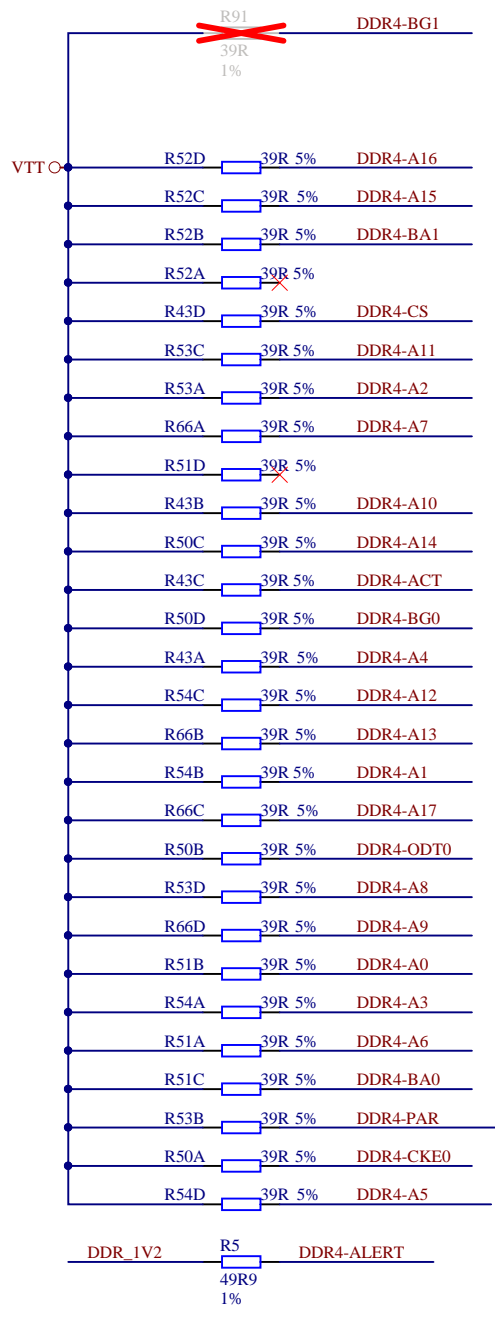
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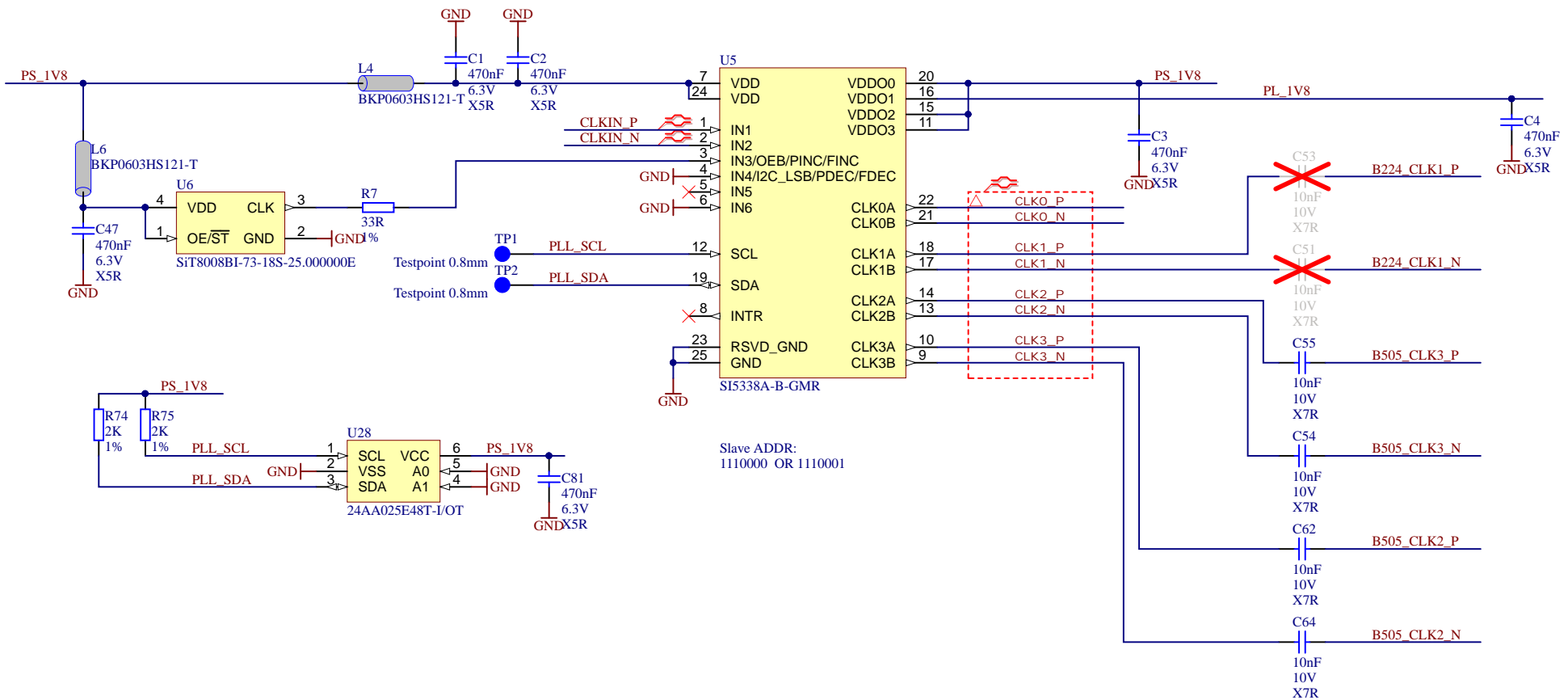
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Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page21 of 26
Filename: DDR4-TERM.SchDoc		


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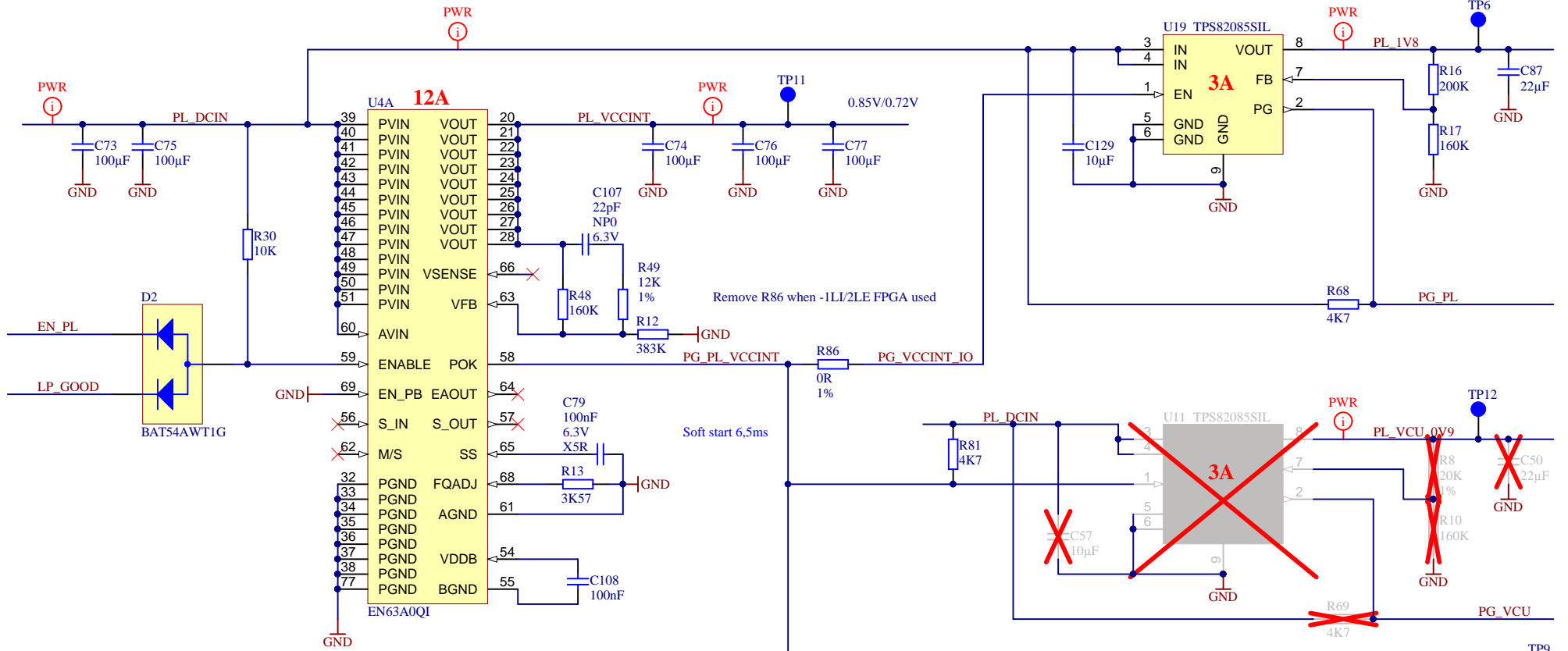
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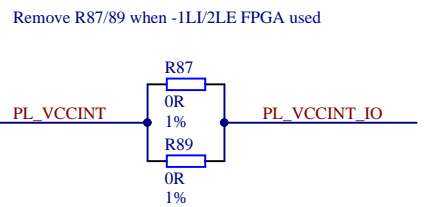

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Date: 2019-02-21		Copyright: Trenz Electronic GmbH / TT	
Page 22 of 26		Filename: Clock.SchDoc	



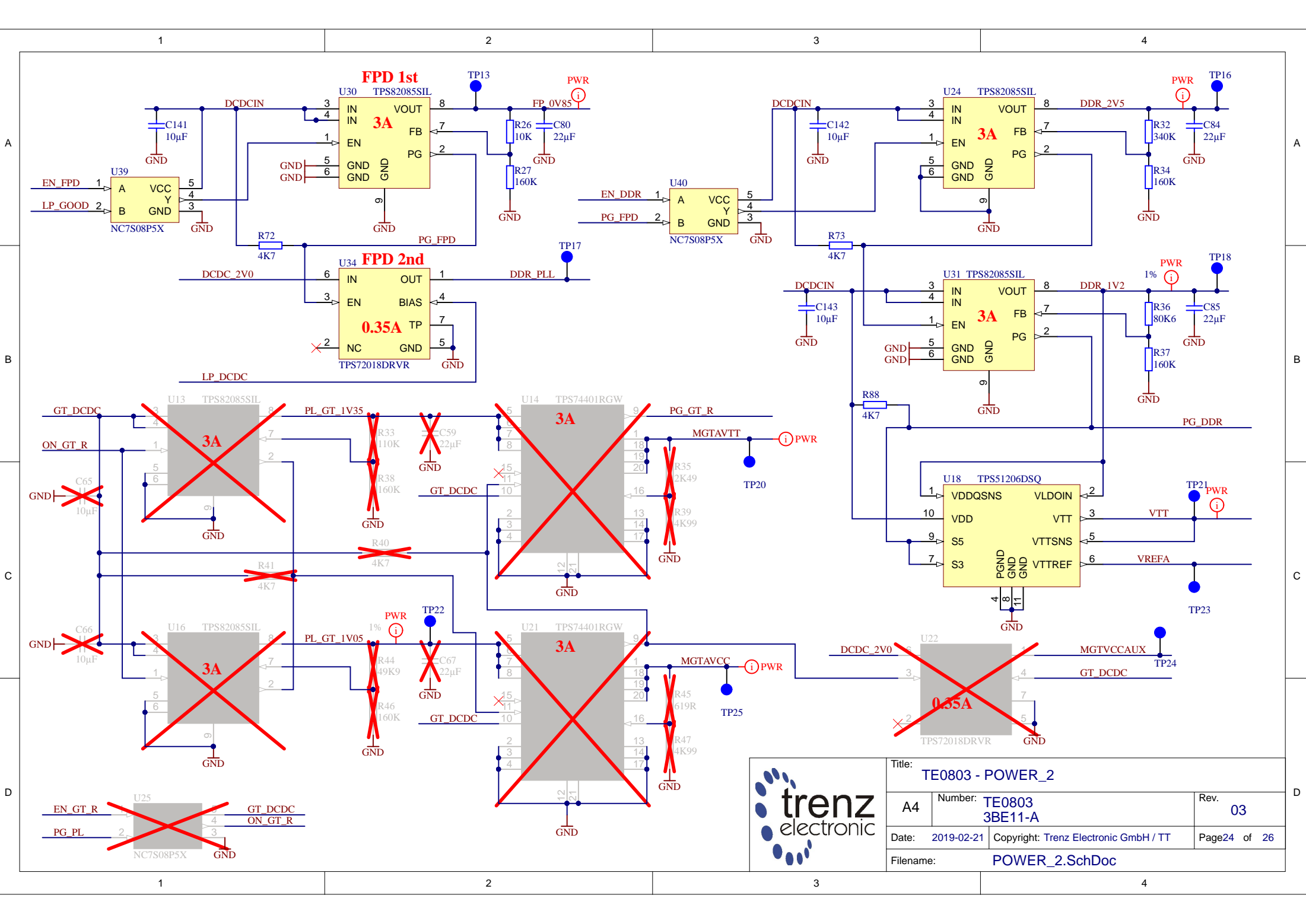
U4B

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2	NC	NC	18
3	NC	NC	19
4	NC	NC	29
5	NC	NC	30
6	NC	NC(SW)	31
7	NC	NC(SW)	52
8	NC	NC	53
9	NC	NC	67
10	NC	NC	70
11	NC	NC(SW)	71
12	NC	NC(SW)	72
13	NC	NC	73
14	NC	NC	74
15	NC	NC	75
16	NC	NC	76

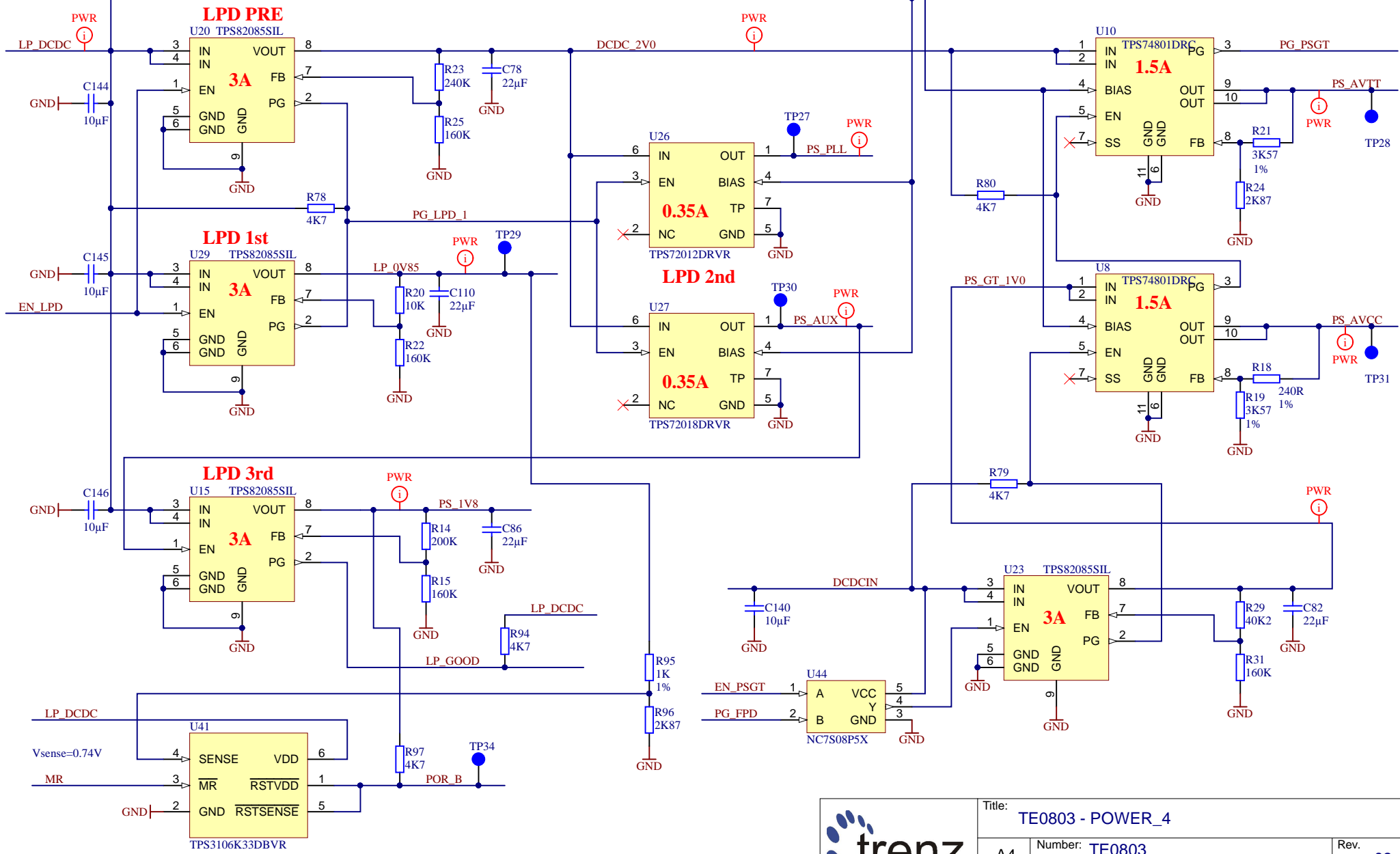
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A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 23 of 26
Filename:	POWER.SchDoc	



Title: TE0803 - POWER_2		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	Page 24 of 26
Filename: POWER_2.SchDoc		



Title: TE0803 - POWER_4		
A4	Number: TE0803 3BE11-A	Rev. 03
Date: 2019-02-21	Copyright: Trenz Electronic GmbH / TT	
Page 25 of 26		Page 25 of 26
Filename: POWER_4.SchDoc		

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CHANGES REV01a (20.11.2017):

- 1) VCU voltage set to 0.9V, R20 changed to 40K , PL_VCU_1V0 renamed to PL_VCU_0V9.

CHANGES REV02 (20.06.2018):

- 1) Added LDO to DDR_PLL
- 2) All differential pairs wath length matched with tollerance 0.1mm (excluding package delays)
- 3) Added MAC EEPROM U28
- 4) VPS_MGTRAVCC set to 0.85V
- 5) Added pull-up resistors R68,R69

CHANGES REV03 (21.02.2019):

- 1) Added support of DDP DDR4
- 2) Added support of Low power FPGA (-L1/L2).
- 3) Revised testpoints
- 4) Revised J1-J4 connectors net label style

A

A

B


B

C

C

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D

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