







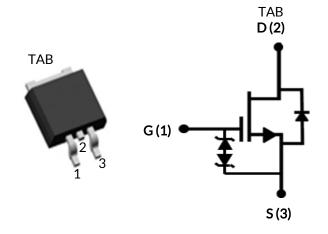








JJ3C065080B3



Part Number	Package	Marking
UJ3C065080B3	D ² PAK-3L	UJ3C065080B3







650V-80mΩ SiC FET

Rev. C, May 2023

Description

This SiC FET device is based on a unique 'cascode' circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device's standard gate-drive characteristics allows for a true "drop-in replacement" to Si IGBTs, Si FETs, SiC MOSFETs or Si superjunction devices. Available in the D²PAK-3L package, this device exhibits ultralow gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.

Features

- Typical on-resistance R_{DS(on),typ} of 80mΩ
- Maximum operating temperature of 175°C
- Excellent reverse recovery
- Low gate charge
- Low intrinsic capacitance
- ESD protected: HBM class 2 and CDM class C3

Typical applications

- EV charging
- PV inverters
- Switch mode power supplies
- Power factor correction modules
- Motor drives
- Induction heating













Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		650	V
Gate-source voltage	V_{GS}	DC	-25 to +25	V
Continuous drain current ¹	I _D	T _C = 25°C	25	Α
Continuous drain current		T _C = 100°C	18.2	Α
Pulsed drain current ²	I _{DM}	T _C = 25°C	65	Α
Single pulsed avalanche energy ³	E _{AS}	L=15mH, I _{AS} =2.1A	33	mJ
Power dissipation	P _{tot}	T _C = 25°C	115	W
Maximum junction temperature	$T_{J,max}$		175	°C
Operating and storage temperature	T_J, T_{STG}		-55 to 175	°C
Reflow soldering temperature	T_{solder}	reflow MSL 1	245	°C

- 1. Limited by $T_{J,max}$
- 2. Pulse width t_p limited by $T_{J,max}$
- 3. Starting $T_J = 25^{\circ}C$

Thermal Characteristics

Parameter	Symbol	Test Conditions		Units		
			Min	Тур	Max	Units
Thermal resistance, junction-to-case	$R_{ heta$ JC			1	1.3	°C/W













Electrical Characteristics (T_J = +25°C unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions		Units		
	Syllibol		Min	Тур	Max	Units
Drain-source breakdown voltage	BV _{DS}	$V_{GS}=0V, I_D=1mA$	650			V
Total drain leakage current		V _{DS} =650V, V _{GS} =0V, T _J =25°C		6	100	- μΑ
	I _{DSS}	V _{DS} =650V, V _{GS} =0V, T _J =175°C		40		
Total gate leakage current	I _{GSS}	V _{DS} =0V, T _J =25°C, V _{GS} =-20V / +20V		6	±20	μА
Drain-source on-resistance	R _{DS(on)}	V_{GS} =12V, I_{D} =20A, T_{J} =25°C		80	100	
		V _{GS} =12V, I _D =20A, T _J =125°C		111		mΩ
		V_{GS} =12V, I_{D} =20A, T_{J} =175°C		141		
Gate threshold voltage	$V_{G(th)}$	V_{DS} =5V, I_{D} =10mA	4	5	6	V
Gate resistance	R_{G}	f=1MHz, open drain		4.5		Ω

Typical Performance - Reverse Diode

Parameter	Symbol	Test Conditions		Units		
Parameter			Min	Тур	Max	Units
Diode continuous forward current ¹	I _S	T _C =25°C			25	Α
Diode pulse current ²	I _{S,pulse}	T _C =25°C			65	Α
Forward voltage	V _{FSD}	V _{GS} =0V, I _S =10A, T _J =25°C		1.5	2	. V
		V _{GS} =0V, I _S =10A, T _J =175°C		1.75		
Reverse recovery charge	Q _{rr}	V_R =400V, I_S =20A, V_{GS} =0V, R_{G_EXT} =20 Ω		111		nC
Reverse recovery time	t _{rr}	di/dt=1600A/μs, Τ _J =150°C		16		ns













Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Тур	Max	Offics
Input capacitance	C _{iss}	V _{DS} =100V, V _{GS} =0V		1500		
Output capacitance	C _{oss}	f=100kHz		104		pF
Reverse transfer capacitance	C_{rss}	1-100KH2		2.6		
Effective output capacitance, energy related	C _{oss(er)}	V_{DS} =0V to 400V, V_{GS} =0V		77		pF
Effective output capacitance, time related	C _{oss(tr)}	V_{DS} =0V to 400V, V_{GS} =0V		176		pF
C _{OSS} stored energy	E _{oss}	V_{DS} =400V, V_{GS} =0V		6.2		μЈ
Total gate charge	Q_{G}	V _{DS} =400V, I _D =20A, V _{GS} = -5V to 15V		51		
Gate-drain charge	Q_{GD}			11		nC
Gate-source charge	Q_{GS}			19		
Turn-on delay time	$t_{d(on)}$	$V_{DS}\text{=}400\text{V}, I_{D}\text{=}20\text{A}, \text{Gate}$ $-\text{Driver} = \text{-}5\text{V to} + \text{15V}, \\ -\text{Turn-on } R_{G,\text{EXT}}\text{=}1\Omega, \\ -\text{Turn-off } R_{G,\text{EXT}}\text{=}20\Omega$ $-\text{Inductive Load}, \\ \text{FWD: UJ3D06510TS}, \\ -\text{T}_{J}\text{=}150^{\circ}\text{C}$		18		ns
Rise time	t _r			13		
Turn-off delay time	$t_{d(off)}$			59		
Fall time	t_f			11		
Turn-on energy	E _{ON}			85		
Turn-off energy	E _{OFF}			62		μJ
Total switching energy	E _{TOTAL}			147		





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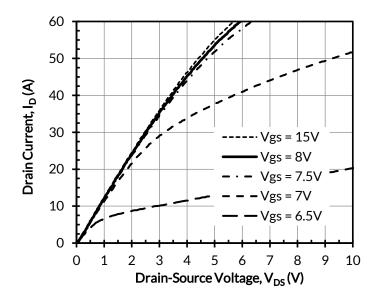








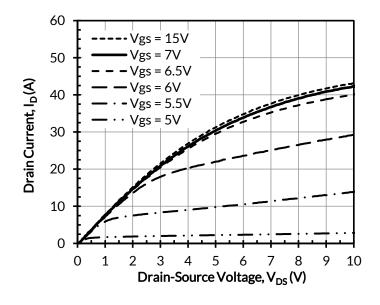
Typical Performance Diagrams



50 Drain Current, I_D (A) 40 30 Vgs = 15V Vgs = 8V 20 Vgs = 7V Vgs = 6.5V10 Vgs = 6V 10 0 1 2 Drain-Source Voltage, V_{DS} (V)

Figure 1. Typical output characteristics at $T_J = -55$ °C, tp < 250 μ s

Figure 2. Typical output characteristics at $T_J = 25$ °C, tp < 250 μ s



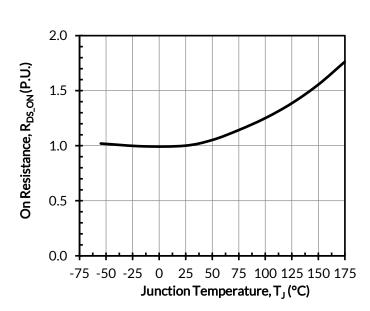


Figure 3. Typical output characteristics at T_J = 175°C, tp < 250 μ s

Figure 4. Normalized on-resistance vs. temperature at V_{GS} = 12V and I_D = 20A



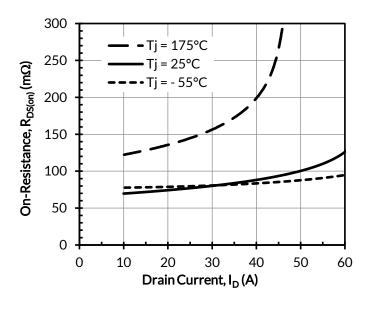








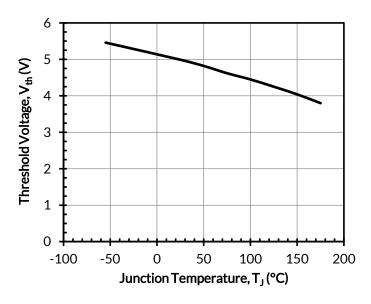




Tj = -55°C Tj = 25°C **-** Tj = 175°C Drain Current, I_D (A) Gate-Source Voltage, $V_{GS}(V)$

Figure 5. Typical drain-source on-resistances at V_{GS} = 12V

Figure 6. Typical transfer characteristics at V_{DS} = 5V



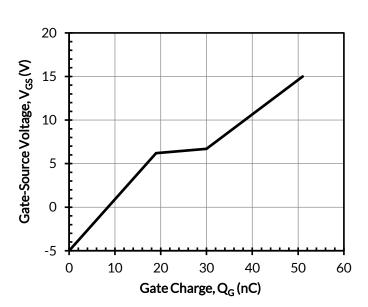


Figure 7. Threshold voltage vs. junction temperature at V_{DS} = 5V and I_{D} = 10mA

Figure 8. Typical gate charge at V_{DS} = 400V and I_{D} = 20A















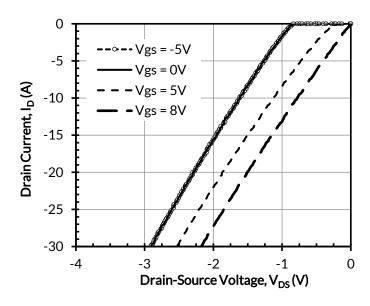


Figure 9. 3rd quadrant characteristics at $T_J = -55$ °C

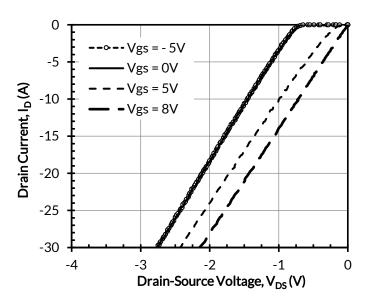


Figure 10. 3rd quadrant characteristics at $T_J = 25$ °C

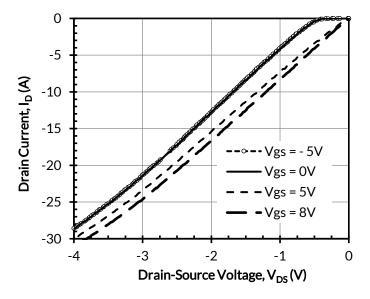


Figure 11. 3rd quadrant characteristics at $T_J = 175$ °C

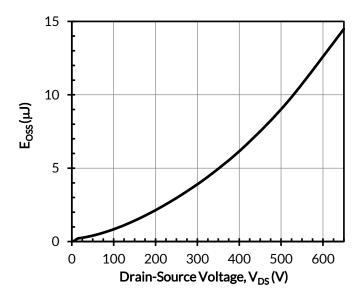


Figure 12. Typical stored energy in C_{OSS} at $V_{GS} = 0V$



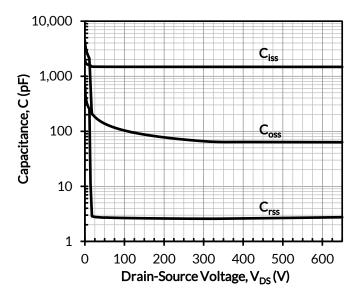








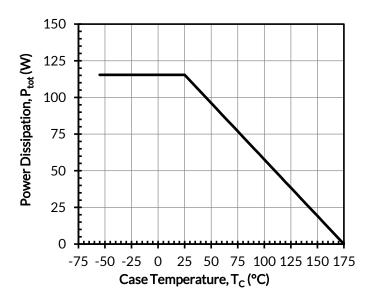




30 25 20 15 10 -75 -50 -25 0 25 50 75 100 125 150 175 Case Temperature, T_c (°C)

Figure 13. Typical capacitances at f = 100kHz and V_{GS} = 0V

Figure 14. DC drain current derating



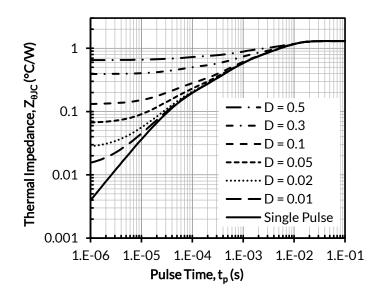


Figure 15. Total power dissipation

Figure 16. Maximum transient thermal impedance













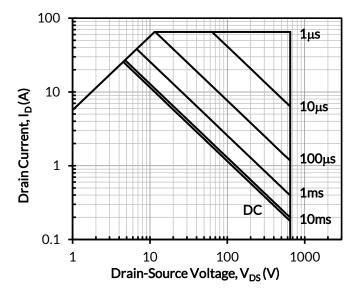


Figure 17. Safe operation area at T_C = 25°C, D = 0, Parameter t_p

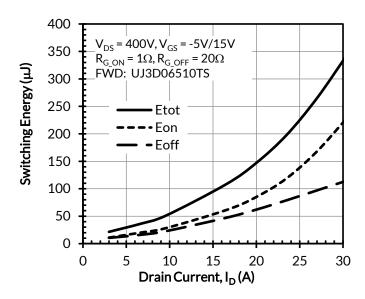


Figure 18. Clamped inductive switching energy vs. drain current at $T_J = 150$ °C

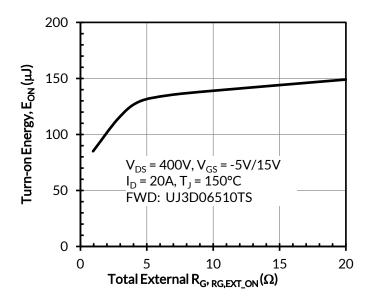


Figure 19. Clamped inductive switching turn-on energy vs. $R_{G,EXT\ ON}$

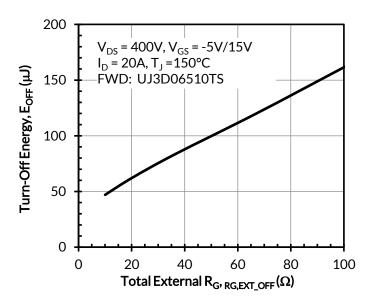


Figure 20. Clamped inductive switching turn-off energy vs. $R_{G,EXT\ OFF}$















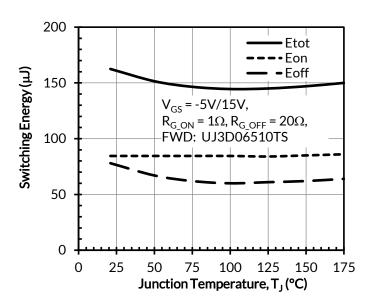


Figure 21. Clamped inductive switching energy vs. junction temperature at V_{DS} = 400V and I_D = 20A

Applications Information

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum reverse recovery performance. For more information on SiC FET operation, see www.unitedsic.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the UnitedSiC website at www.unitedsic.com













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