

EVB-USB7x02

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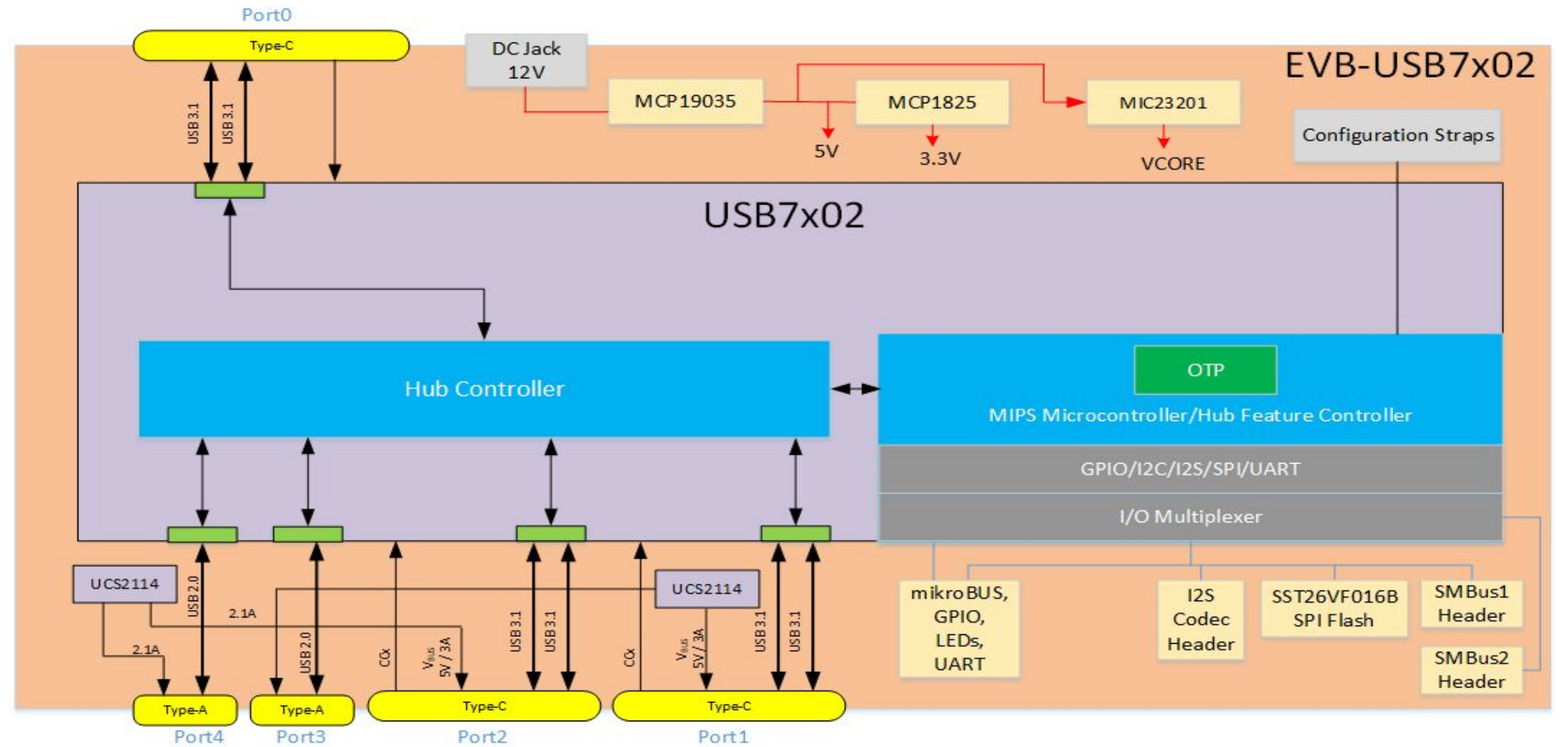
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Notes

1	All resistors are 1% unless specified otherwise
2	Shunt jumper default selections are marked with an asterisk [*].

Revision History

Revision	Date	Revision Summary	Author
A	12/11/2017	Initial release of design	J. Hunt
B	2/20/2018	Corrected various minor errors. List of changes in the Specification.	J. Hunt
C	6/26/2018	Corrected various minor errors. List of changes in the Specification.	J. Hunt

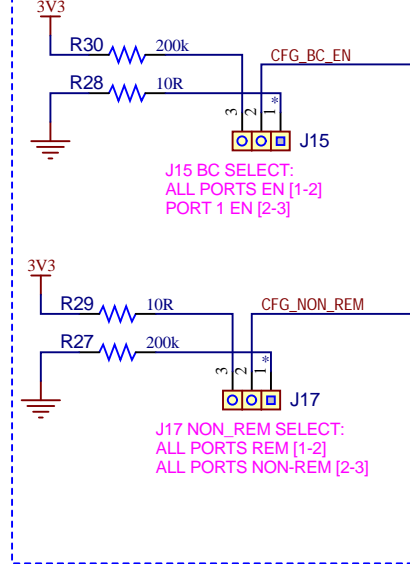


USB7x02 Part A

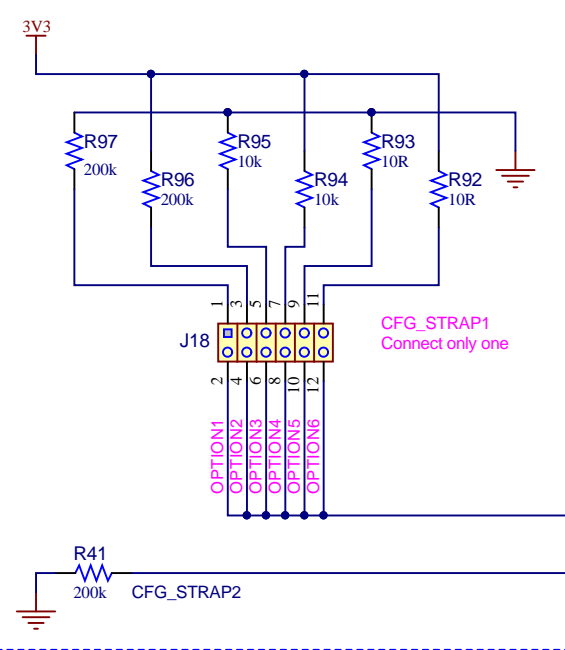
SPI_DI/CFG_BC_EN/
SPI_CE_N/CFG_NON_REM
*Default Open

For SPI (1-2, 4-5)
For BC (2-3)
For NON_REM (5-6)

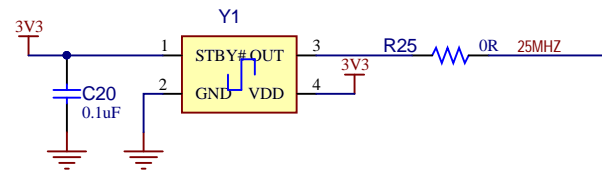
BC/Non-Rem Select



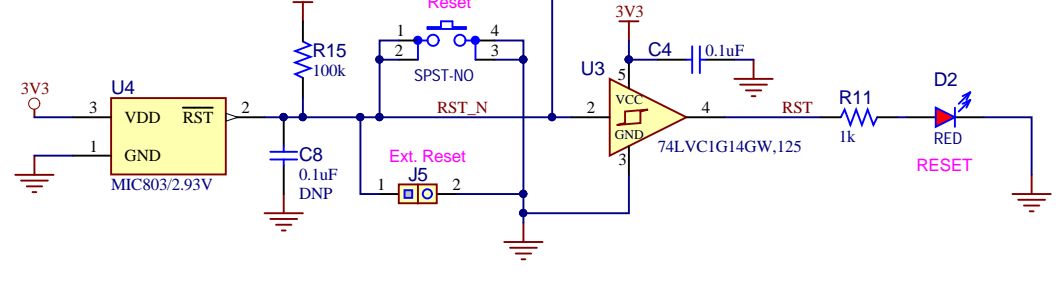
Configuration Option



25 MHz Oscillator

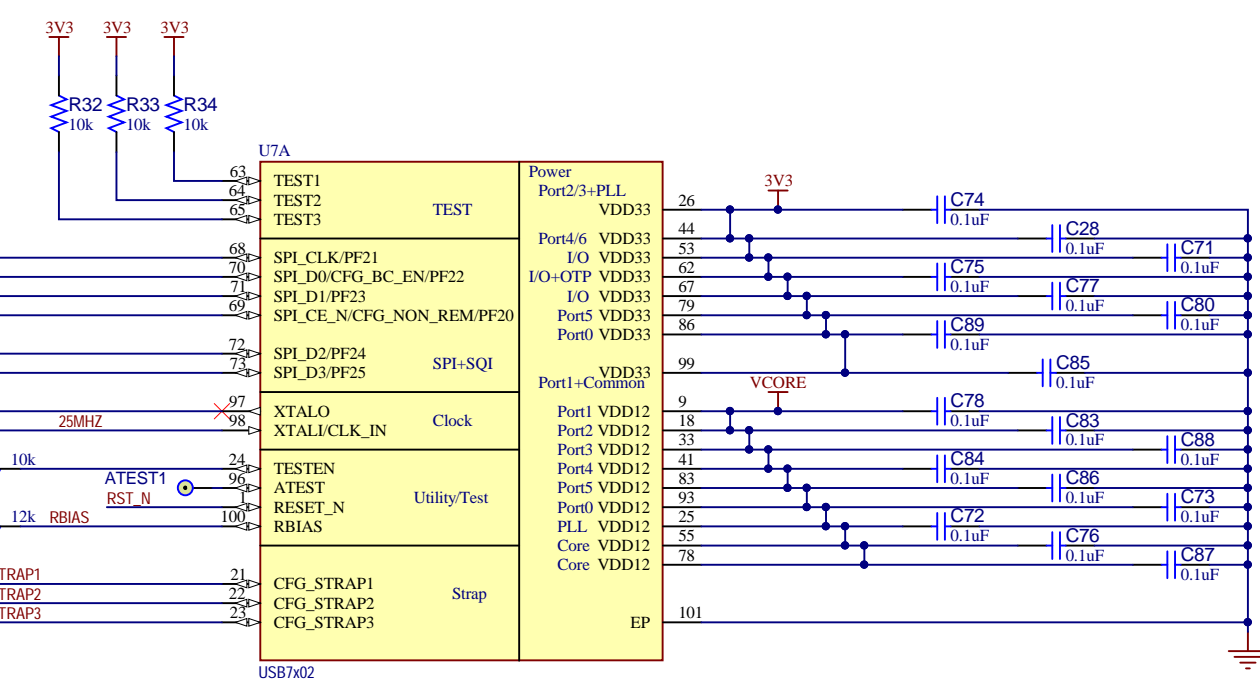
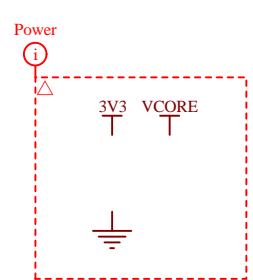
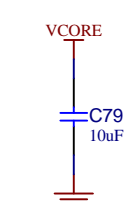


Reset



Default PF Functions by Configuration Option

	OPTION1	OPTION2	OPTION3	OPTION4	OPTION5	OPTION6
PF4	DP2_DISCHARGE	DP2_DISCHARGE	DP2_DISCHARGE	DP2_DISCHARGE	RESERVED	RESERVED
PF5	DP1_DISCHARGE	DP1_DISCHARGE	DP1_DISCHARGE	DP1_DISCHARGE		
PF6	GPIO	GPIO	UART-RX	FLEX_STATE0		
PF7	GPIO	GPIO(MIC_DET)	UART_TX	FLEX_STATE1		
PF8	DP1_VCONN1	DP1_VCONN1	DP1_VCONN1	DP1_VCONN1		
PF9	DP1_VCONN2	DP1_VCONN2	DP1_VCONN2	DP1_VCONN2		
PF10	DP2_VCONN1	DP2_VCONN1	DP2_VCONN1	DP2_VCONN1		
PF11	DP2_VCONN2	DP2_VCONN2	DP2_VCONN2	DP2_VCONN2		
PF12	GPIO	GPIO	GPIO	GPIO		
PF13	PRT_CTL4/OCS	PRT_CTL4/OCS	PRT_CTL4/OCS	PRT_CTL4/OCS		
PF14	GPIO	I2S_SDI	UART_nCTS	FLEX_STATE2		
PF15	PRT_CTL2/OCS	PRT_CTL2/OCS	PRT_CTL2/OCS	PRT_CTL2/OCS		
PF16	PRT_CTL3/OCS	PRT_CTL3/OCS	PRT_CTL3/OCS	PRT_CTL3/OCS		
PF17	PRT_CTL1/OCS	PRT_CTL1/OCS	PRT_CTL1/OCS	PRT_CTL1/OCS		
PF18	MSTR_I2C_CLK	I2S_LRCK	UART_nDCD	FLEX4_CMD		
PF19	MSTR_I2C_DATA	I2S_SDO	UART_nRTS	FLEX1_CMD		
PF20	SPI_CE_N	SPI_CE_N	SPI_CE_N	SPI_CE_N		
PF21	SPI_CLK	SPI_CLK	SPI_CLK	SPI_CLK		
PF22	SPI_D0	SPI_D0	SPI_D0	SPI_D0		
PF23	SPI_D1	SPI_D1	SPI_D1	SPI_D1		
PF24	SPI_D2	SPI_D2	SPI_D2	SPI_D2		
PF25	SPI_D3	SPI_D3	SPI_D3	SPI_D3		
PF26	SLV_I2C_CLK	I2S_SCK	UART_nDSR	FLEX2_CMD		
PF27	SLV_I2C_DATA	I2S_MCLK	UART_nDTR	FLEX3_CMD		
PF28	GPIO	GPIO	GPIO	GPIO		
PF29	GPIO	GPIO	GPIO	GPIO		
PF30	GPIO	MSTR_I2C_CLK	GPIO	GPIO		
PF31	GPIO	MSTR_I2C_DATA	GPIO	GPIO		



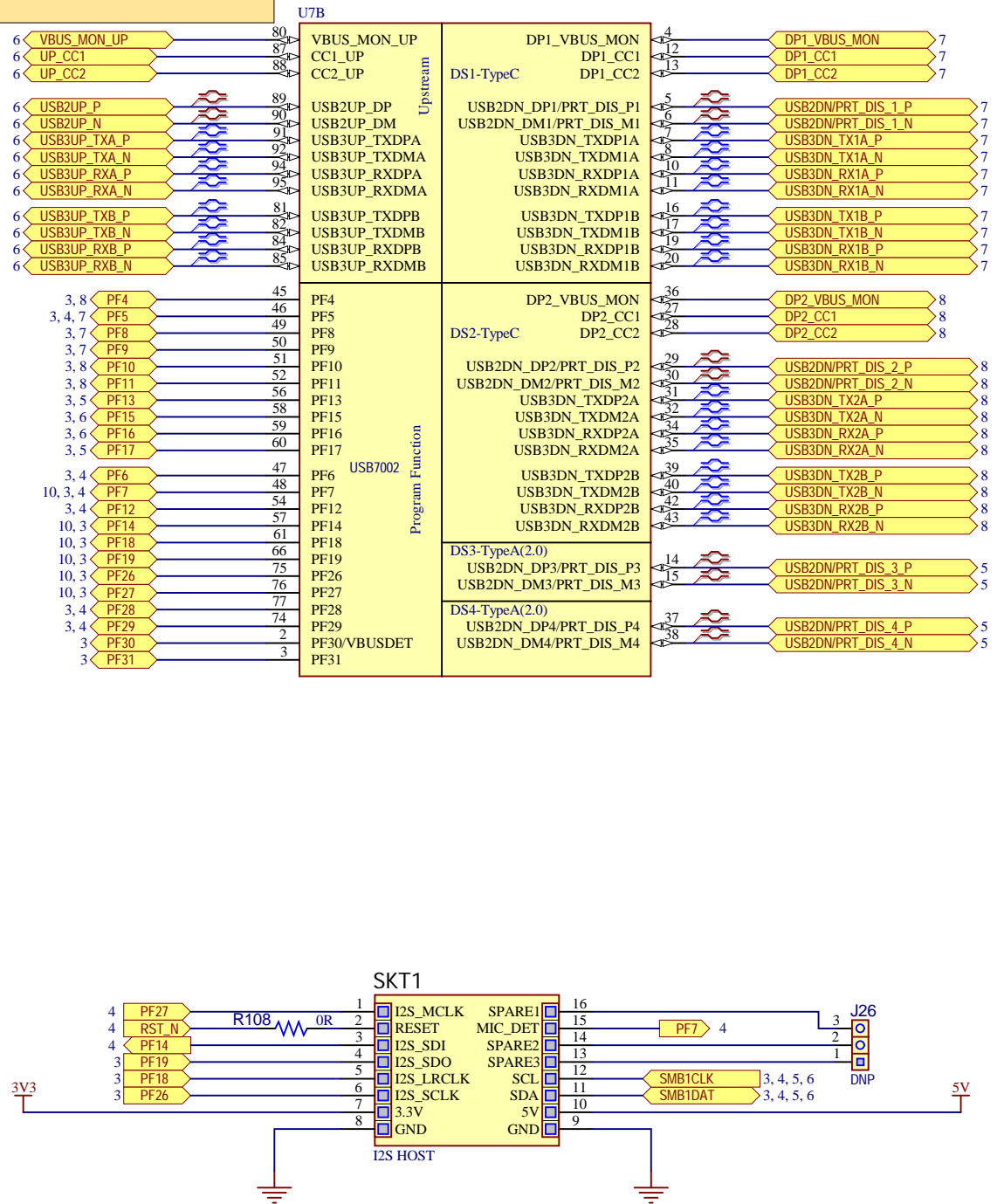
MICROCHIP Microchip Technology, Inc. USB/Network Group - UNG www.Microchip.com

Altium Altium.com

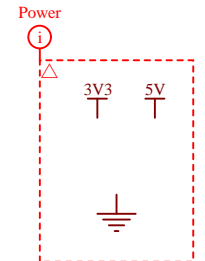
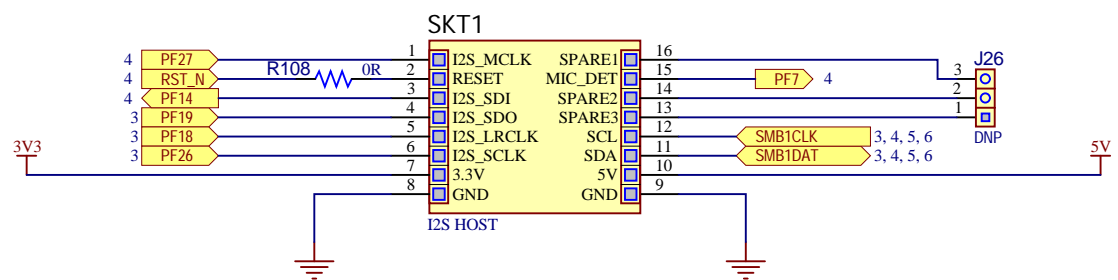
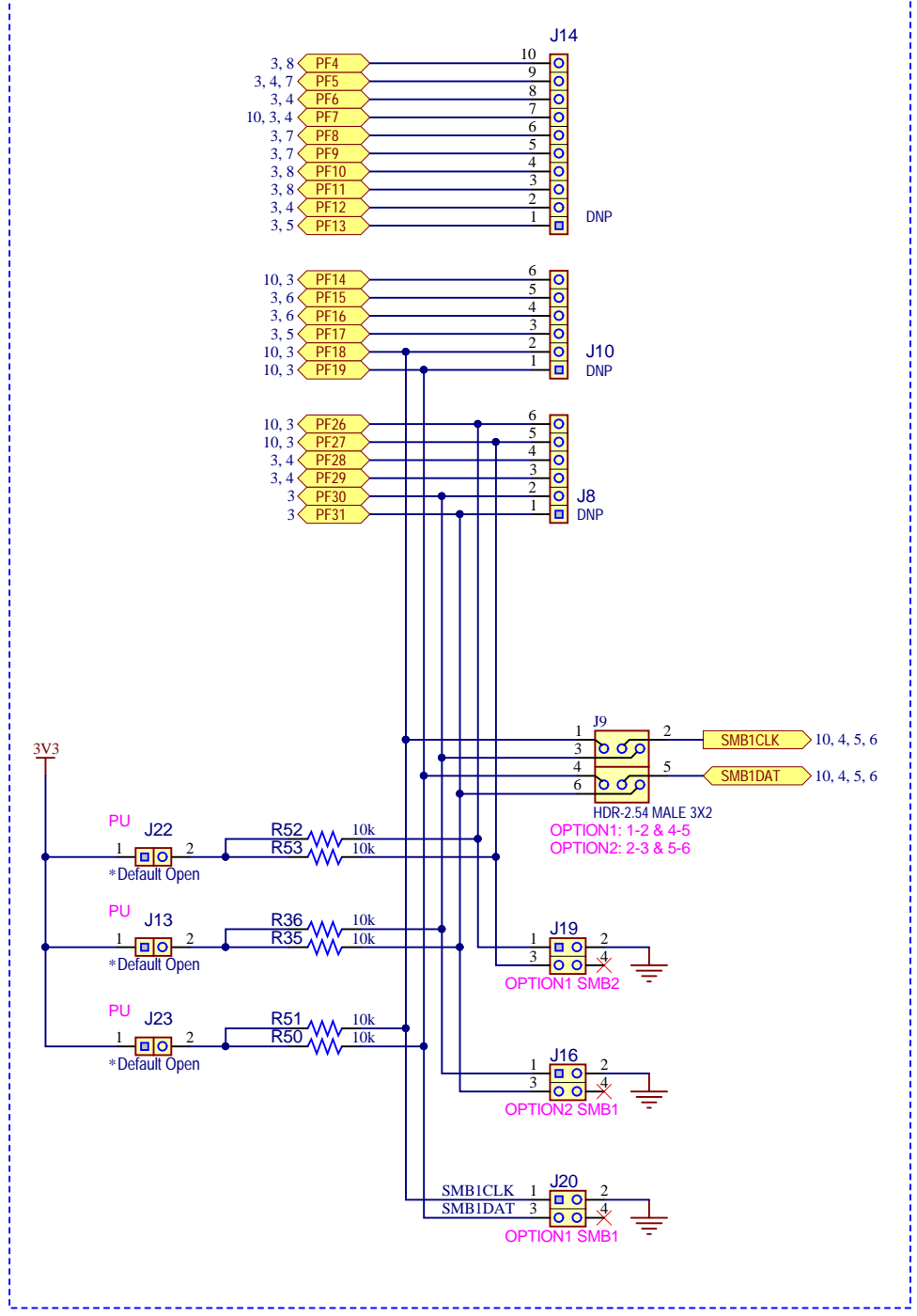
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 Page Title: **USB7x02 Part A**
 Project Name: **Tootsie EVB-USB7x02** PN: **UNG_8137**
 Size: B Date: **7/5/2018** Designer: **J. Hunt** Sheet 2 of 9 Rev A

USB7x02 Part B and Audio Codec Interface

On this upstream port implementation, USB3 signals for the A and B PHYs have been swapped for layout purposes. An additional configuration setting is required to allow for USB3 communication to function with this swap: 0xBF803C02 = 0x40. Normally, CC1 corresponds to the A PHY and CC2 corresponds to the B PHY.

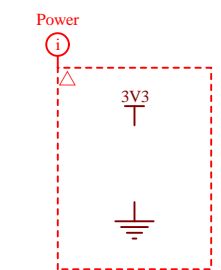
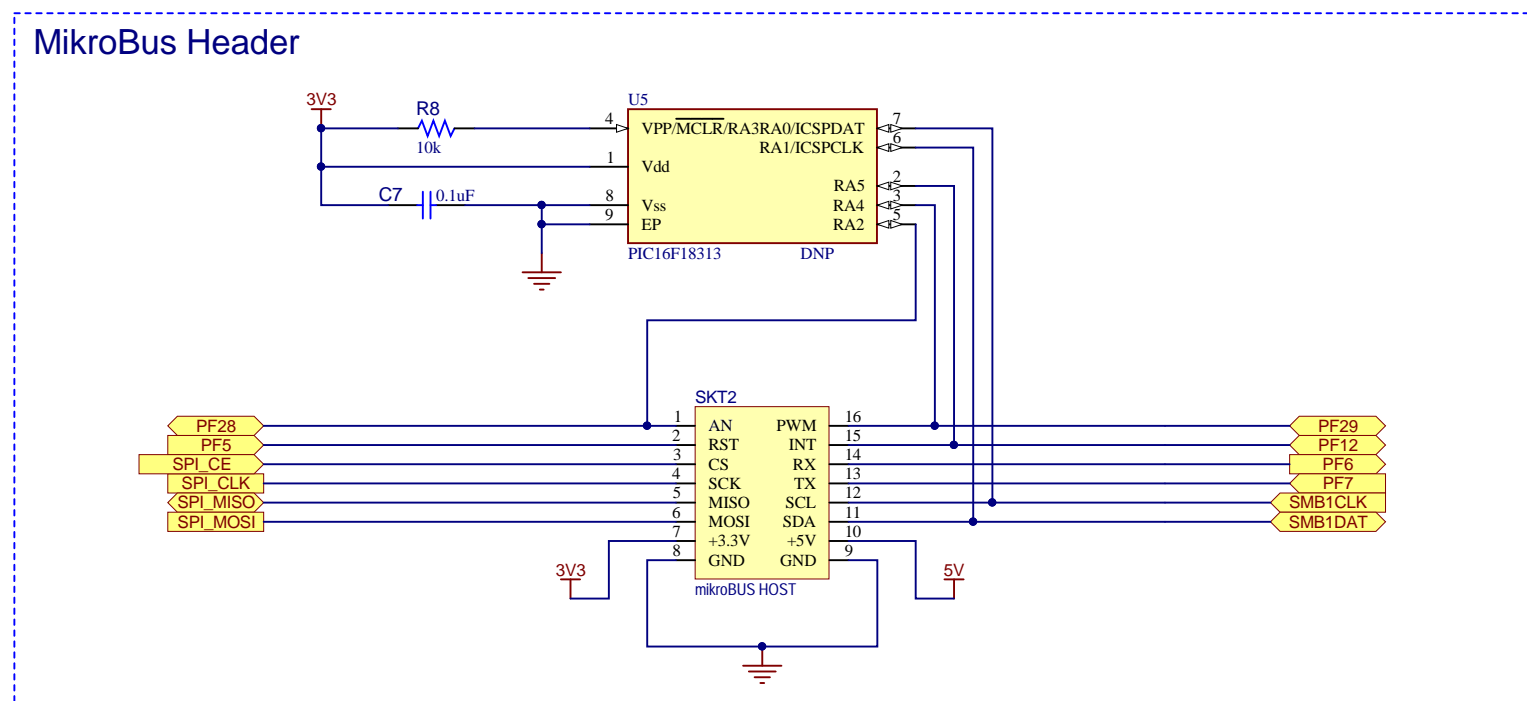
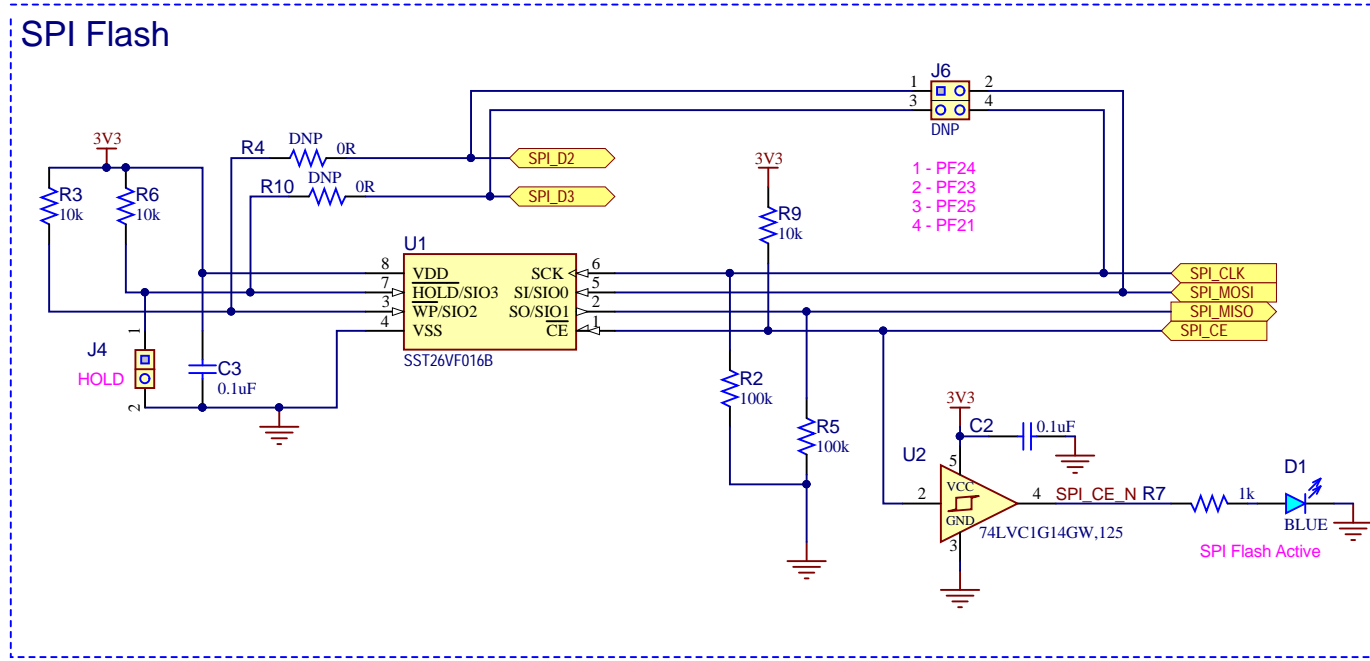


GPIO and SMBUS options



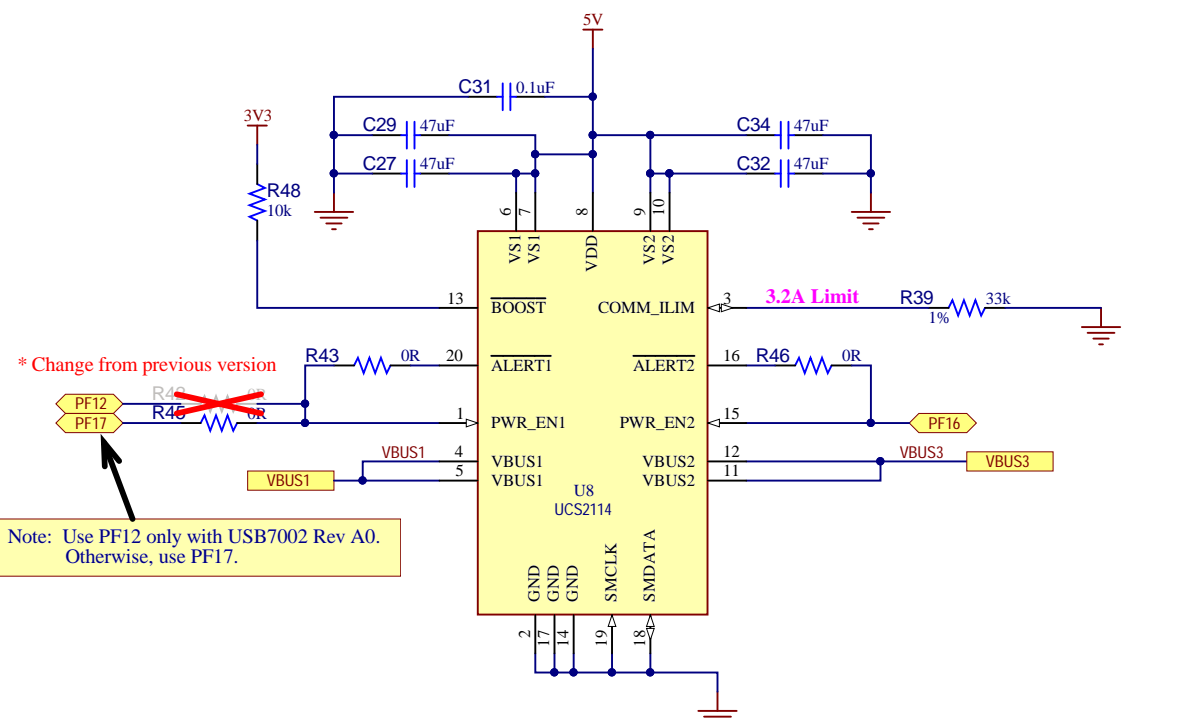
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Memory and MikroBUS

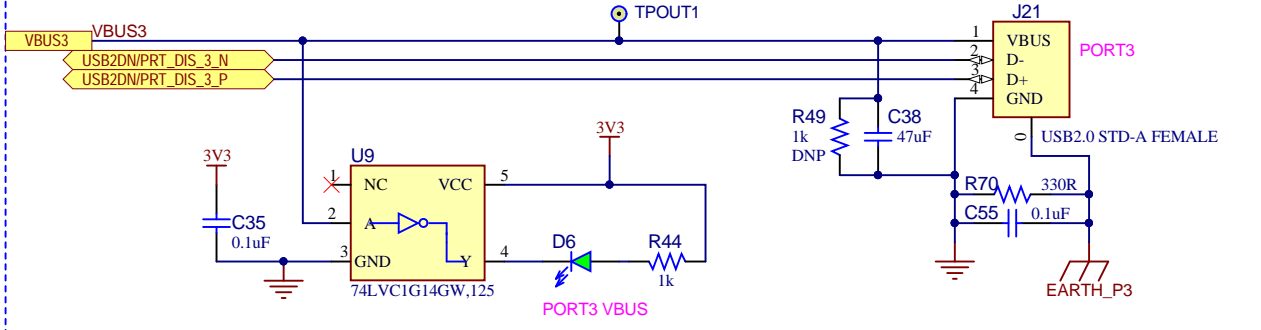


USB A Ports and Power Switch

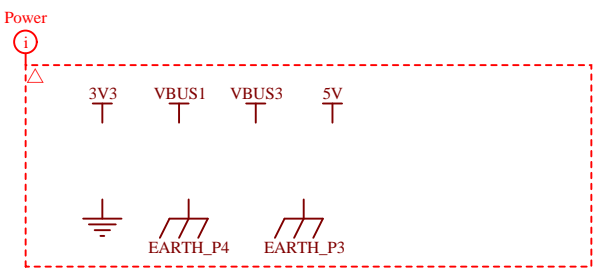
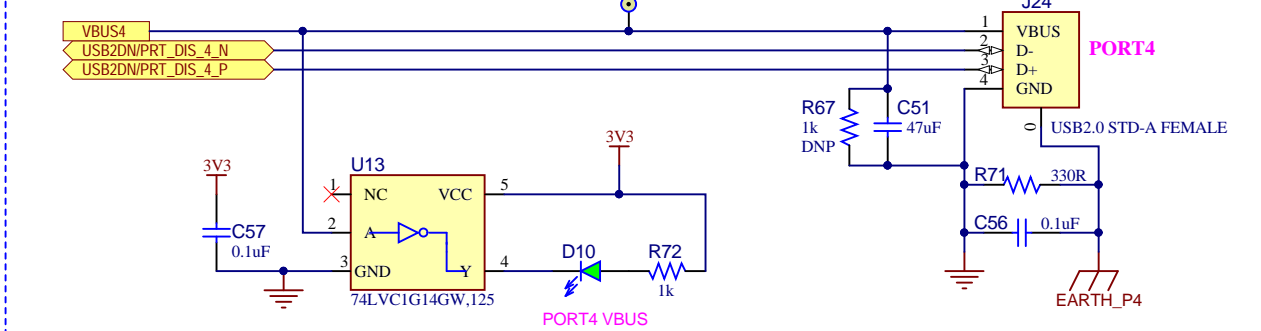
UCS2114 Power Switch For Port1 and Port3



USB-A Downstream Port 3

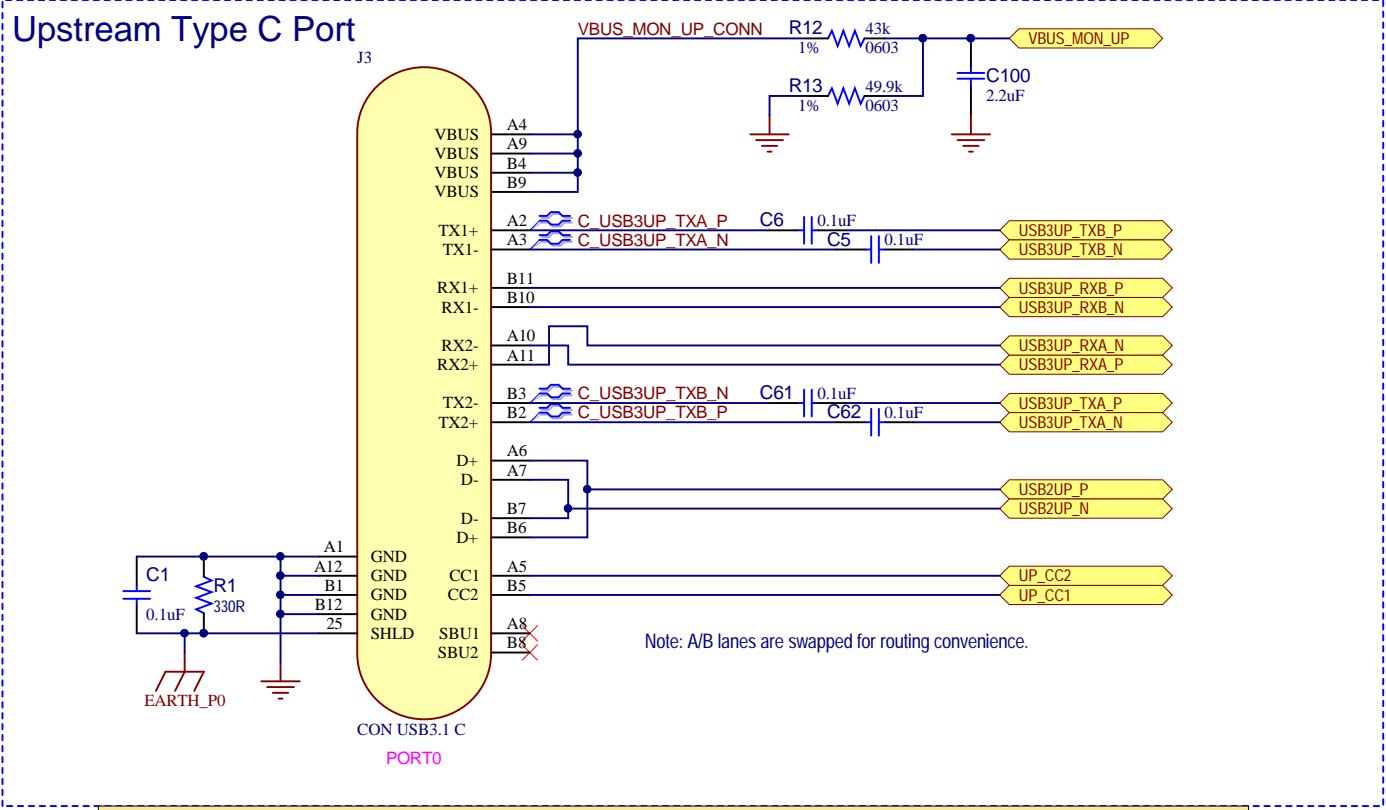


USB-A Downstream Port 4

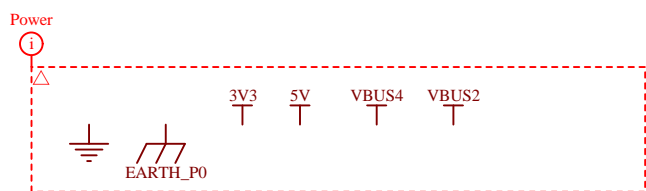
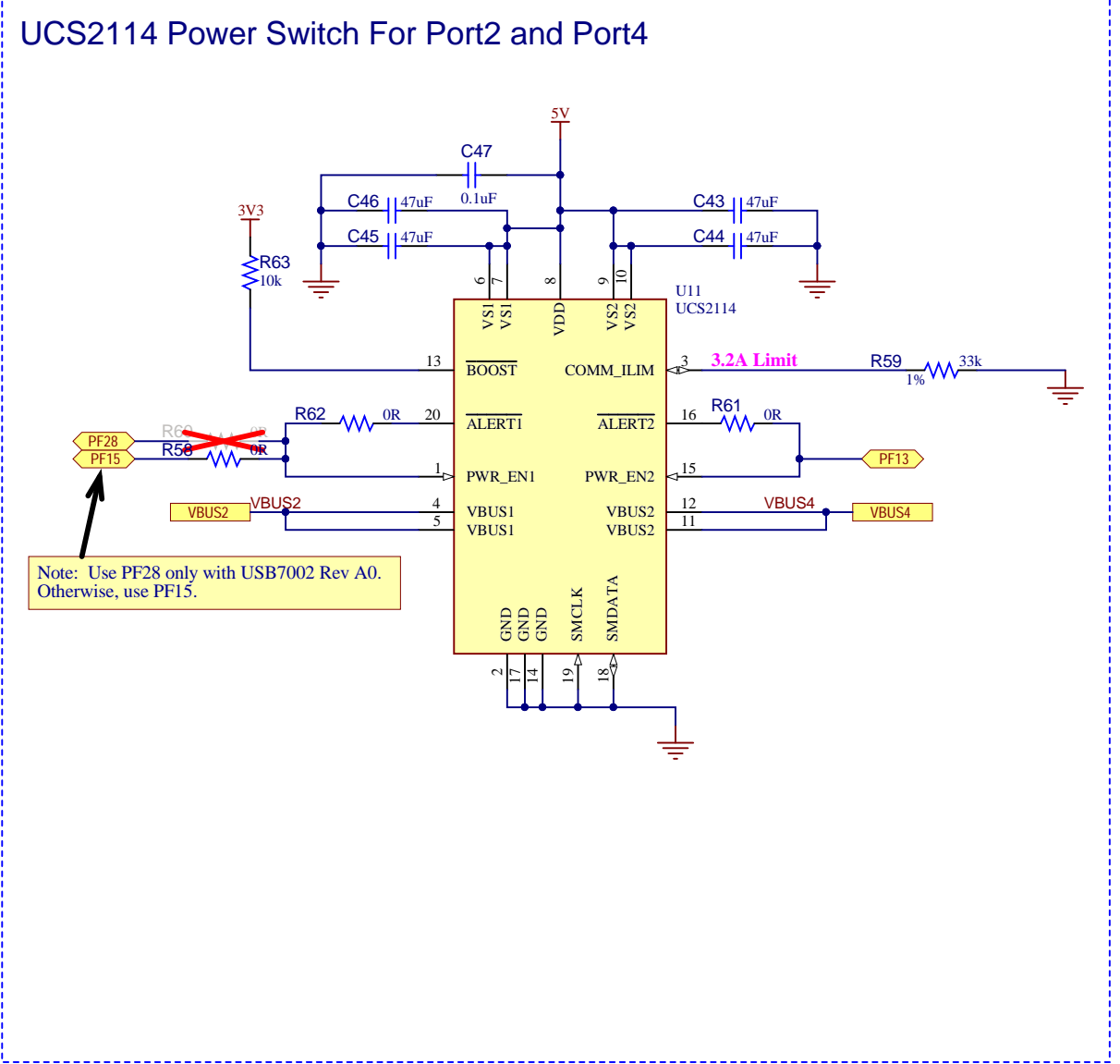


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Page Title: USB A Ports and Power Switch		
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Size: B	Date: 7/5/2018	Designer: J. Hunt
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USB C Upstream and Power Switch

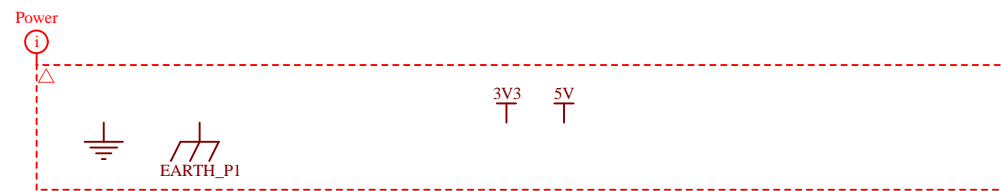
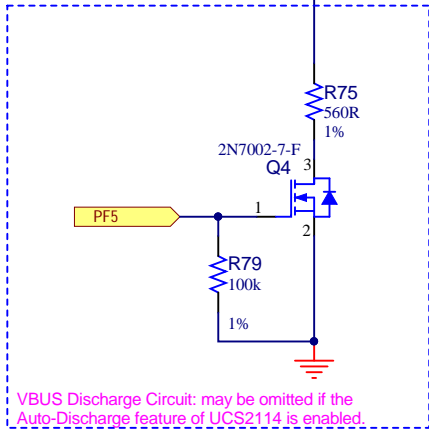
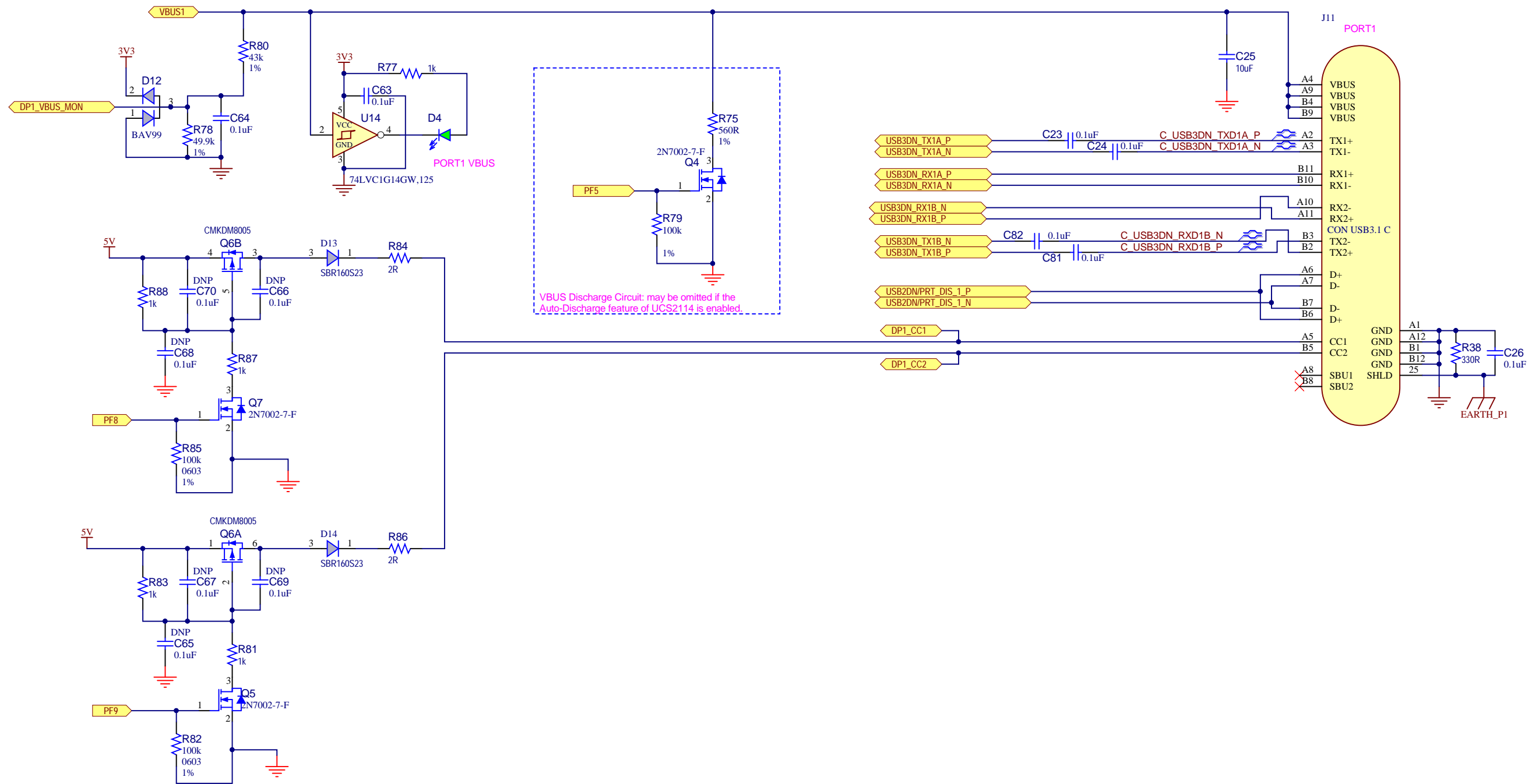


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USB C Downstream 1

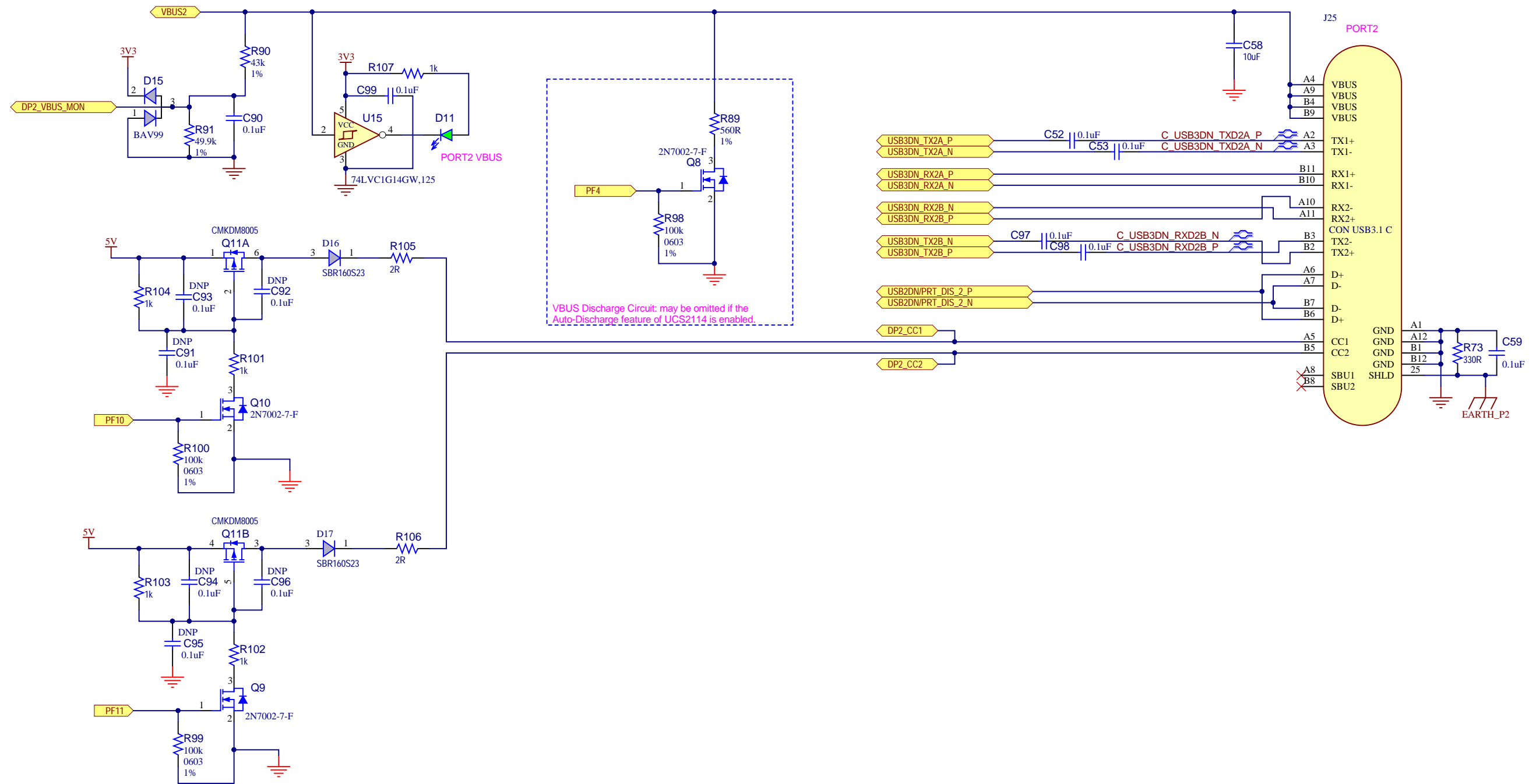
USB-C Downstream Port 1



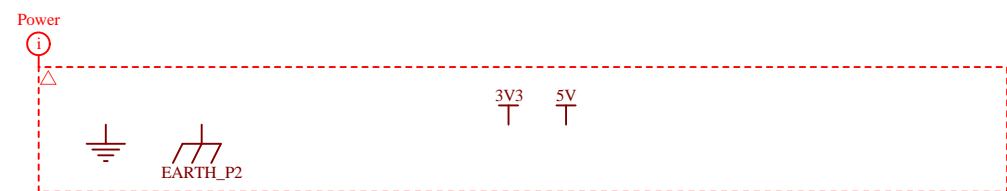
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Page Title: USB C Downstream 1		
Project Name: Tootsie EVB-USB7x02		PN: UNG_8137
Size: B	Date: 7/5/2018	Designer: J. Hunt
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USB C Downstream 2

USB-C Downstream Port 2

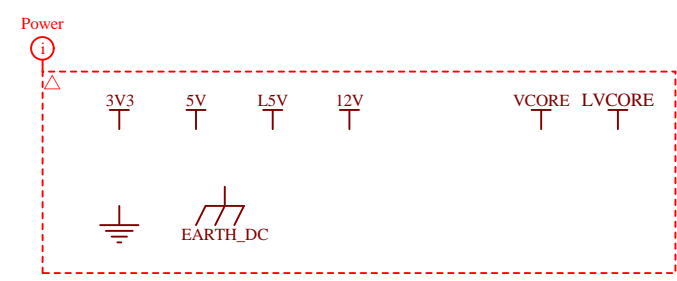
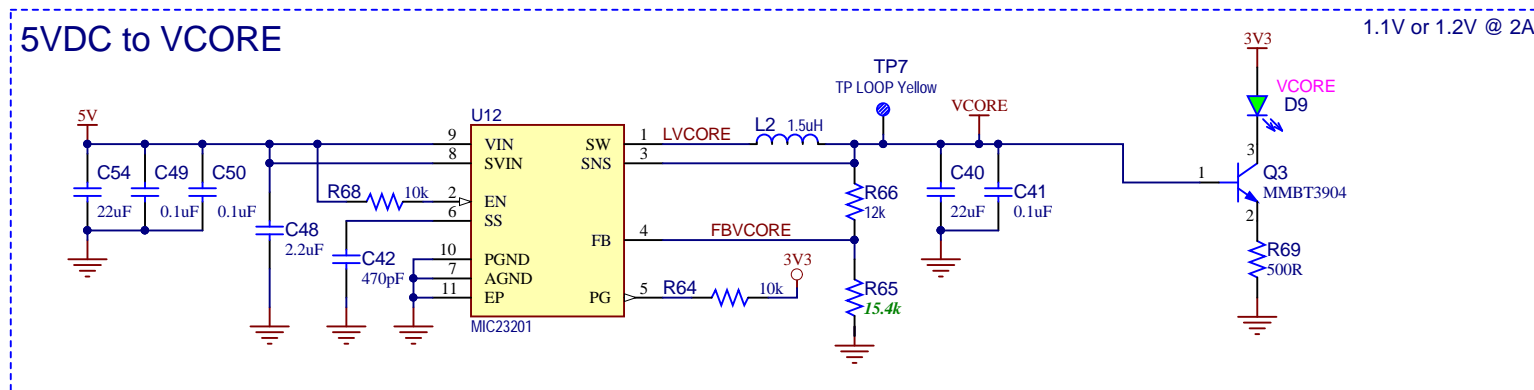
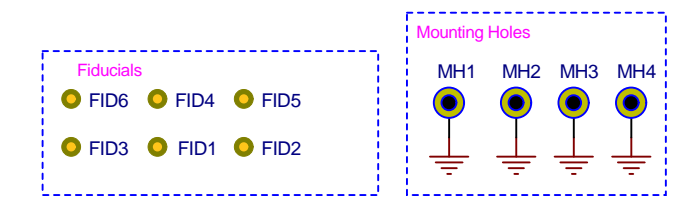
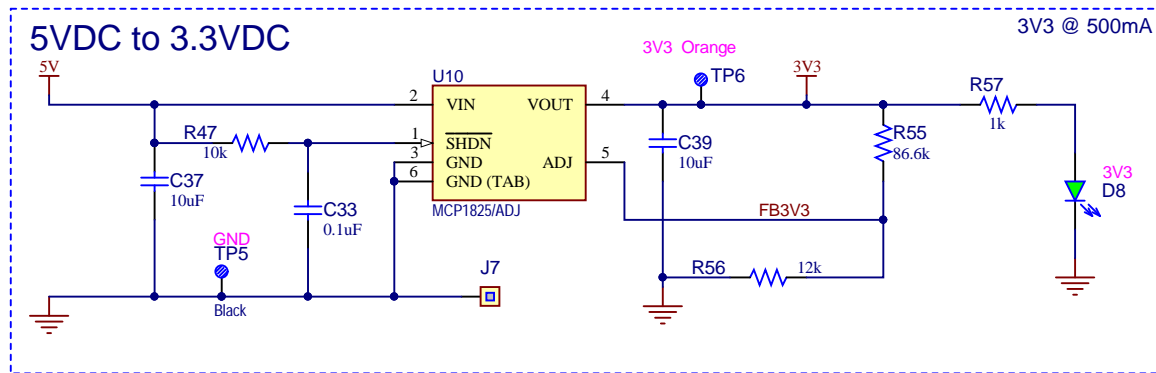
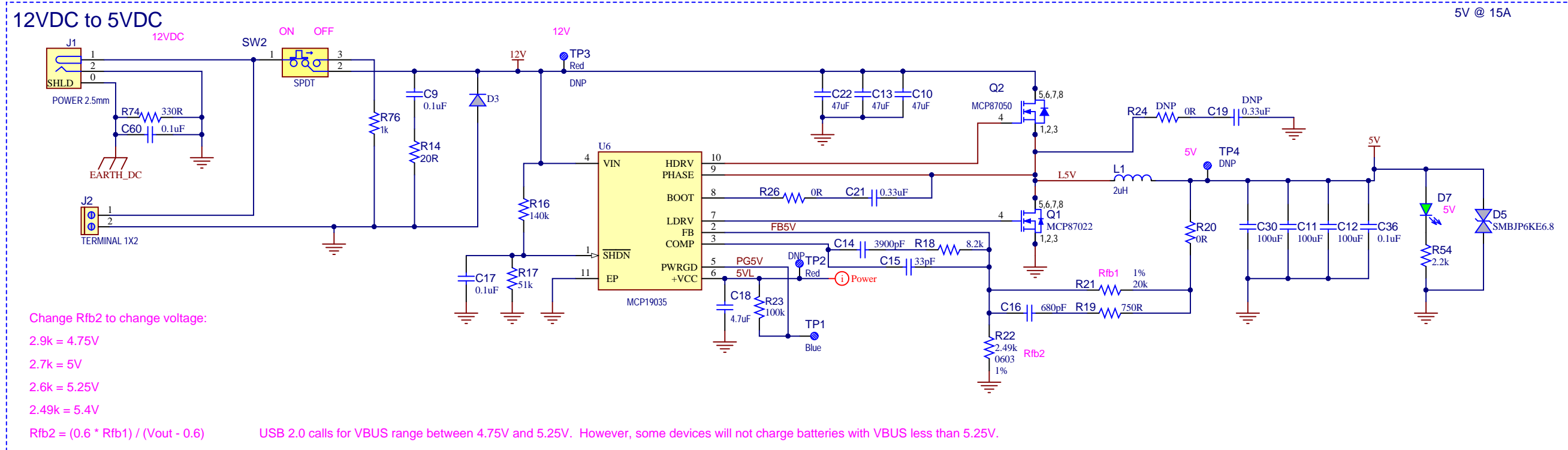


VBUS Discharge Circuit: may be omitted if the Auto-Discharge feature of UCS2114 is enabled.



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Size: B	Date: 7/5/2018	Designer: J. Hunt
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Voltage Regulators



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Page Title: Voltage Regulators		
Project Name: Tootsie EVB-USB7x02		PN: UNG_8137
Size: B	Date: 7/5/2018	Designer: J. Hunt
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