

36V System Power Supply with Watchdog Timer for Industrial Applications

No. EA-372-190115

OUTLINE

R5111x is the system power supply and supervisor IC based on the high-voltage CMOS process technology, and has high accuracy and ultra low supply current voltage.

R5111x consists of a voltage regulator (VR), a voltage detector (VD), and a normal / window type of watchdog timer (WDT) in a chip, and can provide three functions of the system power supply, the supply voltage supervisor, and the supervision of system's misoperation.

Voltage Regulator allows the output current of 300 mA. And, VR has the inrush current protection circuit for rising pulse (Typ.250 mA or less).

Voltage Detector outputs a reset signal when a reduction of supply voltage (SENSE / V_{OUT}) is detected, and the reset signal is used as system reset. The detection voltage is internally fixed in an IC. And, the delay time is adjustable with an external capacitor because VD has the built-in release delay circuit (the power-on reset circuit). When the supply voltage is higher than the release output voltage, VD maintains the reset state during the delay time. The output type of RESETB and D_{OUT} are Nch open-drain. In addition, R5111xxx2C and R5111xxx2D (Detector with SENSE pin) have a manual reset (MR) pin.

Watchdog Timer detects the microprocessor output pulse. In addition to the normal type of WDT (R5111Sxx1A / R5111xxx2C) that outputs a reset signal when the detected pulse period is longer than normal, R5111S supports the window type of WDT (R5111Sxx1B / R5111xxx2D) that outputs a reset signal when the detected pulse period is shorter or longer. RESETB outputs the reset signal when using R5111Sxx1A / R5111Sxx1B, and the WDO pin outputs "L" as the reset signal when using R5111xxx2C / R5111xxx2D. The output type of WDO is Nch open-drain. In addition, R5111xxx2C and R5111xxx2D have an inhibiting (INH) pin to stop the watchdog timer's monitoring function. The time out period of Watchdog Timer is also adjustable with an external capacitor.

R5111x supports the packages of HSOP-8E, HSOP-18 and HQFN0808-28.

This is a high-reliability semiconductor device for industrial applications (-Y) that has passed both the screening at high temperature and the reliability test with extended hours.

FEATURES

- Operating Voltage Range (Maximum Rating) 3.5 V to 36.0 V (50.0 V)
- Operating Temperature Range -40°C to 105°C
- Supply Current Typ. 25 μ A
- Supply Current (On standby) Typ. 0.2 μ A

<Voltage Regulator (VR)>

- Output Voltage Range 1.8 V to 5.0 V
- Dropout Voltage Typ. 0.3 V ($V_{OUT} = 5.0$ V, 300 mA)

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- Output Voltage Accuracy $\pm 1.5\%$ ($-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$)
- Output Voltage Temperature Coefficient Typ. ± 100 ppm/ $^{\circ}\text{C}$
- Built-in Short Current Limit Circuit Typ. 110 mA
- Built-in Overcurrent Protection Circuit Min. 300 mA
- Built-in Thermal Shutdown Circuit Typ. 165°C
- Recommended Ceramic Capacitor 0.1 μF or more

<Voltage Detector (VD)>

- Detector Threshold Range 1.6 V to 5.5 V
- Detector Threshold Accuracy $\pm 1.8\%$ ($-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$)
- Release Delay Accuracy $\pm 20\%$ ($-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$)
- Release Delay Time Typ. 242 ms ($C_D = 0.22 \mu\text{F}$)
Delay Time is adjustable with an external capacitor.

<Watchdog Timer (WDT)>

- Open Window Accuracy $\pm 20\%$ ($-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$)
- Open Window Time Typ. 18 ms ($C_{TW} = 10$ nF)
- Closed Window Time Typ. 18 ms ($C_{TW} = 10$ nF)
- Long Open Window Time Typ. 72 ms ($C_{TW} = 10$ nF)
- Ignoring Time Typ. 18 ms ($C_{TW} = 10$ nF)
- Monitoring Time Typ. 18 ms ($C_{TW} = 10$ nF)
- Reset Time Typ. 9.5 ms ($C_{TW} = 10$ nF)
Each time is adjustable with an external capacitor.

APPLICATIONS

- Industrial equipments such as FAs and smart meters
- Equipments used under high-temperature conditions such as surveillance camera and vending machine
- Equipments accompanied by self-heating such as motor and lighting

SELECTION GUIDE

R5111x user selectable options (Watchdog Timer type, Detector type, and additional functions with using MR / INH / WDO pins) are as follows:

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R5111Sxx1*-E2-YE	HSOP-8E	1,000 pcs	Yes	Yes
R5111Sxx2*-E2-YE	HSOP-18	1,000 pcs	Yes	Yes
R5111Lxx2*-TR-YE	HQFN0808-28	2,000 pcs	Yes	Yes

xx: Specify the set output voltage (V_{SET}) and the set detector threshold ($-V_{SET}$) by using serial numbers starting from 01.

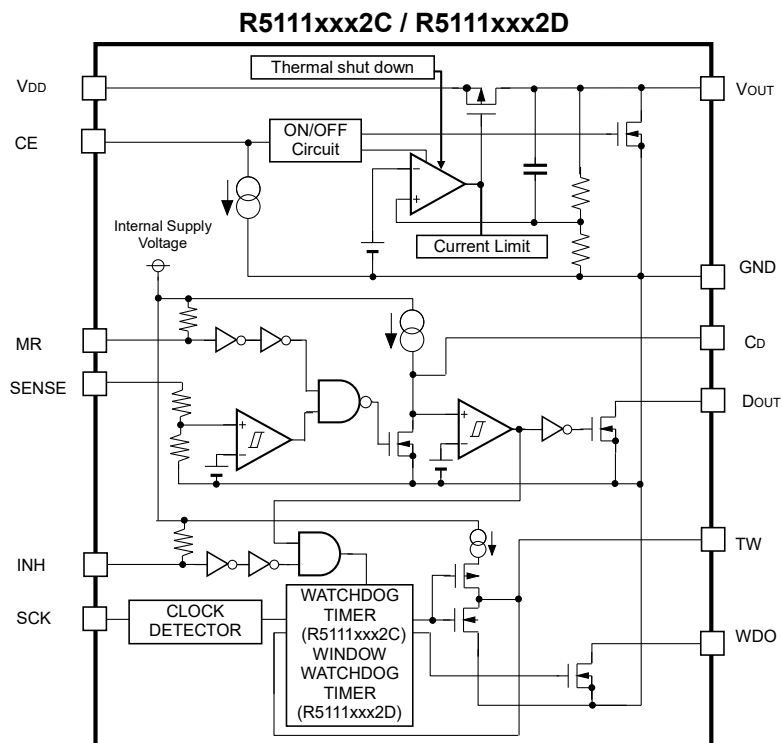
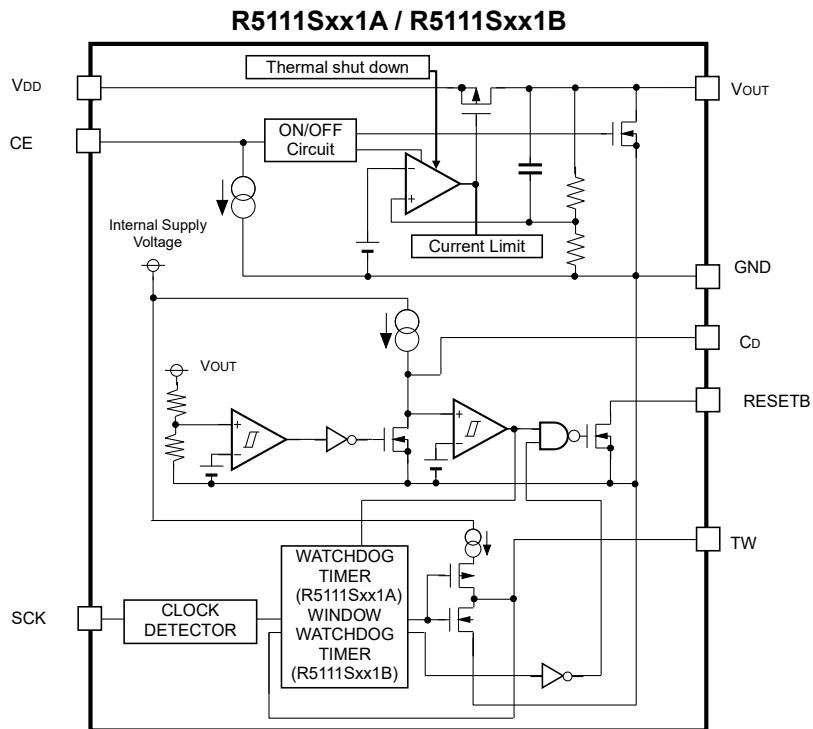
Refer to "Mark Specification Table" for details.

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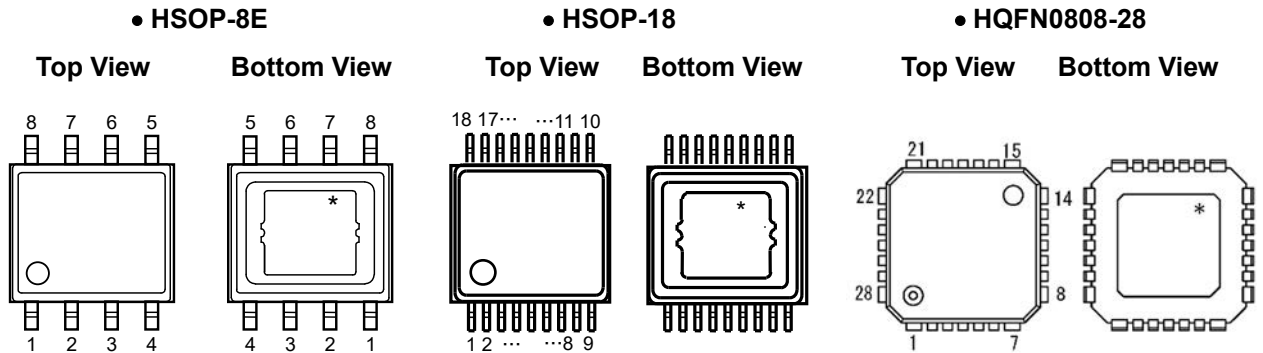
	Detector Monitoring Voltage	Package	Watchdog Timer Type	MR / INH / WDO pins	RESETB/ D _{OUT} pins
A	V_{OUT}	HSOP-8E	Normal	-	RESETB
B	V_{OUT}	HSOP-8E	Window	-	RESETB
C	SENSE	HSOP-18 HQFN0808-28	Normal	Yes	D _{OUT}
D	SENSE	HSOP-18 HQFN0808-28	Window	Yes	D _{OUT}

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BLOCK DIAGRAMS

PIN DESCRIPTION



HSOP-8E (R5111Sxx1A / R5111Sxx1B)

Pin No.	Symbol	Description
1	V _{DD}	Supply Voltage pin
2	CE	Chip Enable pin (Active "H")
3	GND	GND pin
4	C _D	VD Release Delay Time Set pin
5	TW	WDT Monitoring Time Set pin
6	SCK	WDT Pulse Input pin
7	RESETB ⁽¹⁾	Reset Output pin (Active "L"), Nch Open Drain Output type
8	V _{OUT}	VR Output pin

* The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left open.

⁽¹⁾ RESETB pin is required to pull up to a suitable voltage with an external capacitor.

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HSOP-18 (R5111Sxx2C / R5111Sxx2D)

Pin No.	Symbol	Description
1	V _{DD}	Supply Voltage pin
2	CE	Chip Enable pin (Active "H")
3	NC	No Connection
4	NC	No Connection
5	GND	GND pin
6	NC	No Connection
7	NC	No Connection
8	C _D	VD Release Delay Time Set pin
9	MR	Manual Reset pin (Active "L")
10	TW	WDT Monitoring Time Set pin
11	INH	Inhibition pin (Active "L")
12	SCK	WDT Pulse Input pin
13	WDO ⁽¹⁾	WDT Output pin, Nch Open Drain Output type
14	D _{OUT} ⁽²⁾	Reset Output pin (Active "L"), Nch Open Drain Output type
15	SENSE	VD Voltage SENSE pin
16	NC	No Connection
17	NC	No Connection
18	V _{OUT}	VR Output pin

* The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left open.

⁽¹⁾ WDO pin is required to pull up to a suitable voltage with an external capacitor.

⁽²⁾ D_{OUT} pin is required to pull up to a suitable voltage with an external capacitor.

HQFN0808-28 (R5111Lxx2C / R5111Lxx2D)

Pin No.	Symbol	Description
1	GND	GND pin
2	NC	No Connection
3	V _{DD}	Supply Voltage pin
4	NC	No Connection
5	CE	Chip Enable pin (Active "H")
6	NC	No Connection
7	GND	GND pin
8	GND	GND pin
9	GND	GND pin
10	C _D	VD Release Delay Time Set pin
11	MR	Manual Reset pin (Active "L")
12	TW	WDT Monitoring Time Set pin
13	INH	Inhibition pin (Active "L")
14	GND	GND pin
15	GND	GND pin
16	SCK	WDT Pulse Input pin
17	NC	No Connection
18	WDO ⁽¹⁾	WDT Output pin, Nch Open Drain Output type
19	D _{OUT} ⁽²⁾	Reset Output pin (Active "L"), Nch Open Drain Output type
20	SENSE	VD Voltage SENSE pin
21	GND	GND pin
22	GND	GND pin
23	NC	No Connection
24	NC	No Connection
25	NC	No Connection
26	V _{OUT}	VR Output pin
27	NC	No Connection
28	GND	GND pin

* The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left open.

⁽¹⁾ WDO pin is required to pull up to a suitable voltage with an external capacitor.

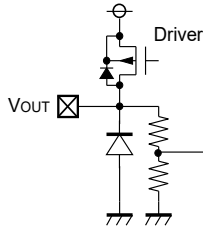
⁽²⁾ DOUT pin is required to pull up to a suitable voltage with an external capacitor.

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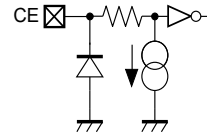
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PIN EQUIVALENT CIRCUIT DIAGRAMS

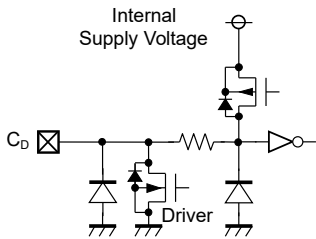
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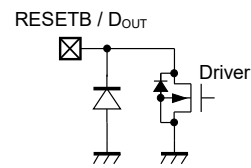
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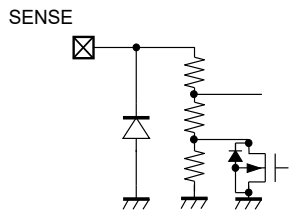
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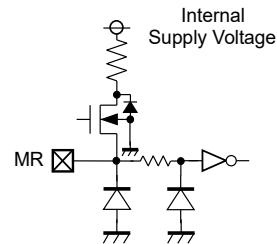
<RESETB Pin (R5111Sxx1x)/D_{OUT} Pin (R5111xxx2x)>



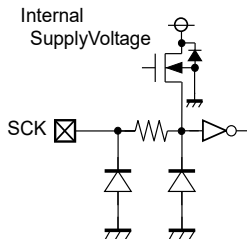
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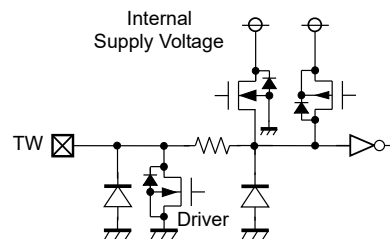
<MR Pin (R5111xxx2x) >



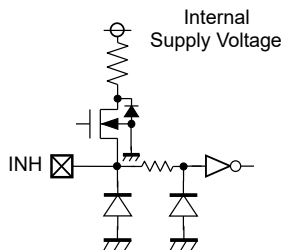
<SCK Pin >



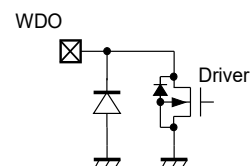
<TW Pin >



<INH Pin (R5111xxx2x) >



<WDO Pin (R5111xxx2x) >



ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V _{IN}	Input Voltage	-0.3 to 50	V
	Peak Voltage ⁽¹⁾	60	V
V _{CE}	CE Pin Input Voltage	-0.3 to 50	V
V _{OUT}	Output Voltage	-0.3 to V _{IN} + 0.3 ≤ 50	V
V _{CD}	C _D Pin Output Voltage	-0.3 to 7.0	V
V _{TW}	TW Pin Output Voltage	-0.3 to 7.0	V
V _{RESETB}	RESETB Pin Output Voltage	-0.3 to 7.0	V
V _{DOUT}	D _{OUT} Pin Output Voltage	-0.3 to 7.0	V
V _{WDO}	WDO Pin Output Voltage	-0.3 to 7.0	V
V _{SCK}	SCK Pin Input Voltage	-0.3 to 7.0	V
V _{INH}	INH Pin Input Voltage	-0.3 to 7.0	V
V _{MR}	MR Pin Input Voltage	-0.3 to 7.0	V
V _{SENSE}	SENSE Pin Input Voltage	-0.3 to 7.0	V
P _D	Power Dissipation ⁽²⁾	HSOP-8E (JEDEC STD.51)	2900
		HSOP-18 (JEDEC STD.51)	3100
		HQFN0808-28 (JEDEC STD. 51)	4600
T _j	Junction Temperature	-40 to 125	°C
T _{stg}	Storage Temperature	-55 to 125	°C

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings are not assured.

RECOMMENDED OPERATING CONDITIONS

Symbol	Item	Rating	Unit
V _{IN}	Input Voltage	3.5 to 36.0	V
V _{CE}	CE Pin Input Voltage	0 to 36.0	V
V _{SCK}	SCK Pin Input Voltage	0 to 5.5	V
V _{INH}	INH Pin Input Voltage	0 to 5.5	V
V _{MR}	MR Pin Input Voltage	0 to 5.5	V
V _{SENSE}	SENSE Pin Input Voltage	0 to 5.5	V
T _a	Operating Temperature Range	-40 to 105	°C

RECOMMENDED OPERATING CONDITONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such ratings by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Within application time of 200ms

⁽²⁾ Refer to *POWER DISSIPATION* for detailed information.

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ELECTRICAL CHARACTERISTICS $C_{IN} = C_{OUT} = 0.1\mu\text{F}$, $V_{IN} = 14\text{ V}$, unless otherwise noted.The specification in is checked and guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$.**R5111xxxxx**

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
I _{SS}	Supply Current	I _{OUT} = 0 mA		25	38	μA
I _{standby}	Power Consumption (on standby)	V _{IN} = 36 V, V _{CE} = 0 V		0.2	4.0	μA
I _{PD}	CE Pull-down Constant Current	V _{CE} = 5 V		0.2	0.6	μA
		V _{CE} = 36 V		0.5	1.3	μA
V _{CEH}	CE Input Voltage "H"		2.2		36	V
V _{CEL}	CE Input Voltage "L"				1.0	V

VR Part

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
V _{OUT}	Output Voltage	I _{OUT} = 1 mA	×0.985		×1.015	V	
ΔV _{OUT} /ΔI _{OUT}	Load Regulation	V _{IN} = V _{SET} + 2.0 V 1mA ≤ I _{OUT} ≤ 300 mA	-15	0	24	mV	
V _{DIF}	Dropout Voltage	I _{OUT} = 300 mA	V _{SET} = 1.8		-	1.70	V
			V _{SET} = 2.5		-	1.00	V
			V _{SET} = 3.3		0.36	0.71	V
			V _{SET} = 5.0		0.30	0.57	V
ΔV _{OUT} /ΔV _{IN}	Line Regulation	3.5 V ≤ V _{SET} + 0.5 V ≤ V _{IN} ≤ 36V I _{OUT} = 1 mA		0.01	0.02	%/V	
I _{LIM}	Output Current Limit	V _{IN} = V _{SET} + 3.0 V	300	470	650	mA	
I _{SC}	Short current Limit	V _{IN} = 5 V, V _{OUT} = 0 V	60	110	170	mA	
T _{TSD}	Thermal Shutdown Temperature	Junction Temperature	150	165		°C	
T _{TSR}	Thermal Shutdown Release Temperature	Junction Temperature	125	140		°C	
R _{LOW}	V _{OUT} Low Output Nch Tr.ON Resistance	V _{CE} = 0 V, V _{OUT} = 0.1 V		3.2	7.0	kΩ	

$C_{IN} = C_{OUT} = 0.1\mu\text{F}$, $V_{IN} = 14\text{ V}$, unless otherwise noted.

The specification in is checked and guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$.

VD Part

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
$-V_{DET}$	Detector Threshold	V_{OUT} Set Detector Threshold	<input type="checkbox"/> 0.982		<input type="checkbox"/> 1.018	V
V_{HYS}	Detector Threshold Hysteresis		$\frac{(-V_{DET})}{\text{input}}$ <input type="checkbox"/> 0.01	$(-V_{DET})$ x0.02	$\frac{(-V_{DET})}{\text{input}}$ <input type="checkbox"/> 0.03	V
t _{delay}	Release Output Delay Time (Power-On Reset)	$C_D = 0.22\ \mu\text{F}$	<input type="checkbox"/> 194	242	<input type="checkbox"/> 290	ms
V_{RESETB}	RESETB Pull-up Voltage	R5111Sxx1A / R5111Sxx1B			<input type="checkbox"/> 5.5	V
V_{DOUT}	D _{OUT} Pull-up Voltage	R5111xxx2C / R5111xxx2D			<input type="checkbox"/> 5.5	V
$I_{OUTNRSTB}$	Nch. Output Current (RESETB Output Pin)	R5111Sxx1A / R5111Sxx1B $V_{IN} = 3.5\text{ V}$, $V_{RESETB} = 0.1\text{ V}$	<input type="checkbox"/> 0.7	1.5		mA
$I_{LEAKRSTB}$	Nch. Leakage Current (RESETB Output Pin)	R5111Sxx1A / R5111Sxx1B $V_{RESETB} = 5.5\text{ V}$			<input type="checkbox"/> 0.3	μA
$I_{OUTDOUT}$	Nch. Output Current (D _{OUT} Output Pin)	R5111xxx2C / R5111xxx2D $V_{IN} = 3.5\text{ V}$, $V_{DOUT} = 0.1\text{ V}$	<input type="checkbox"/> 0.7	1.5		mA
$I_{LEAKDOUT}$	Nch. Leakage Current (D _{OUT} Output Pin)	R5111xxx2C / R5111xxx2D $V_{DOUT} = 5.5\text{ V}$			<input type="checkbox"/> 0.3	μA
V_{MRH}	MR Input "H"		<input type="checkbox"/> 1.5		<input type="checkbox"/> 5.5	V
V_{MRL}	MR Input "L"		<input type="checkbox"/> 0		<input type="checkbox"/> 0.6	V
MRW	MR Input Pulse Width		<input type="checkbox"/> 2			μs
RMR	MR Pull-up Resistance		<input type="checkbox"/> 50	110	<input type="checkbox"/> 160	k Ω
R_{LCD}	C_D Pin Discharge Nch Tr.ON Resistance	$V_{CE} = 0\text{ V}$, $V_{CD} = 0.1\text{ V}$		7.5	<input type="checkbox"/> 20	k Ω

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$C_{IN} = C_{OUT} = 0.1\mu F$, $V_{IN} = 14V$, unless otherwise noted.

The specification in is checked and guaranteed by design engineering at $-40^{\circ}C \leq T_a \leq 105^{\circ}C$.

WDT Part

($T_a = 25^{\circ}C$)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
t_{OW}	Open Window Time	R5111Sxx1B/ R5111xxx2D	$C_{TW} = 10\text{ nF}$	14.4	18.0	21.6	ms
t_{CW}	Closed Window Time			14.4	18.0	21.6	ms
t_{OWL}	Long Open Window Time			36.0	72.0	108.0	ms
t_{IGN}	Ignoring Time	$C_{TW} = 10\text{ nF}$	14.4	18.0	21.6	ms	
t_{WD}	Monitoring Time	R5111Sxx1A/ R5111xxx2C	$C_{TW} = 10\text{ nF}$	14.4	18.0	21.6	ms
t_{WR}	Reset Time	$C_{TW} = 10\text{ nF}$	7.6	9.5	11.4	ms	
V_{SCKH}	SCK Input "H"		1.5		5.5	V	
V_{SCKL}	SCK Input "L"		0		0.65	V	
$V_{INH H}$	INH Input "H"		1.5		5.5	V	
$V_{INH L}$	INH Input "L"		0		0.6	V	
R_{INH}	INH Pull-up Resistance		50	110	160	k Ω	
t_{SCKWH}	SCK Minimum Input Pulse Width "H"	$V_{SCKL} = 0.5$, $V_{SCKH} = 1.6$	500			ns	
t_{SCKWL}	SCK Minimum Input Pulse Width "L"	$V_{SCKL} = 0.5$, $V_{SCKH} = 1.6$	1500			ns	
V_{WDO}	WDO Pull-up Voltage				5.5	V	
$I_{OUTNWDO}$	Nch. Output Current (WDO Output Pin)	R5111xxx2C / R5111xxx2D $V_{IN} = 3.5V$, $V_{DS} = 0.1V$	0.7	1.5		mA	
$I_{LEAKWDO}$	Nch. Leakage Current (WDO Output Pin)	R5111xxx2C / R5111xxx2D $V_{WDO} = 5.5\text{ V}$			0.3	μA	
R_{LTW}	C_{TW} Discharge Nch Tr.ON Resistance	$V_{CE} = 0\text{ V}$, $V_{CTW} = 0.1\text{ V}$		7.5	20	k Ω	

All test items listed under Electrical Characteristics are done under the pulse load condition ($T_j \approx T_a = 25^{\circ}C$).

The specification in is checked and guaranteed by design engineering at $-40^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$.

R5111xxxx-VE Product-specific Electrical Characteristics

VR Part

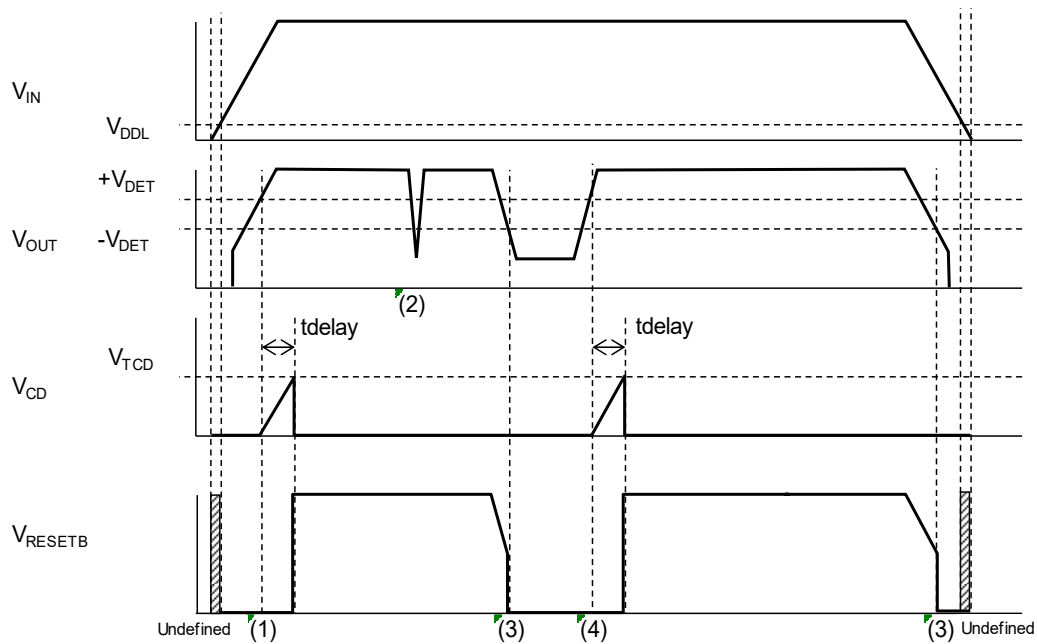
($T_a = 25^{\circ}\text{C}$)

Product Name	V _{OUT} [V]			V _{DIF} [V]	
	Min.	Typ.	Max.	Typ.	Max.
R5111x01xx	4.925	5.000	5.075	0.30	0.57
R5111x02xx	1.773	1.800	1.827	-	1.70
R5111x03xx	4.925	5.000	5.075	0.30	0.57
R5111x04xx	4.925	5.000	5.075	0.30	0.57
R5111x05xx	4.925	5.000	5.075	0.30	0.57
R5111x06xx	4.925	5.000	5.075	0.30	0.57
R5111x07xx	4.925	5.000	5.075	0.30	0.57
R5111x08xx	3.251	3.300	3.349	0.36	0.71
R5111x09xx	3.251	3.300	3.349	0.36	0.71
R5111x10xx	3.251	3.300	3.349	0.36	0.71
R5111x11xx	3.251	3.300	3.349	0.36	0.71
R5111x12xx	4.925	5.000	5.075	0.30	0.57
R5111x13xx	3.349	3.400	3.451	0.36	0.71
R5111x142x	3.251	3.300	3.349	0.36	0.71

VD Part

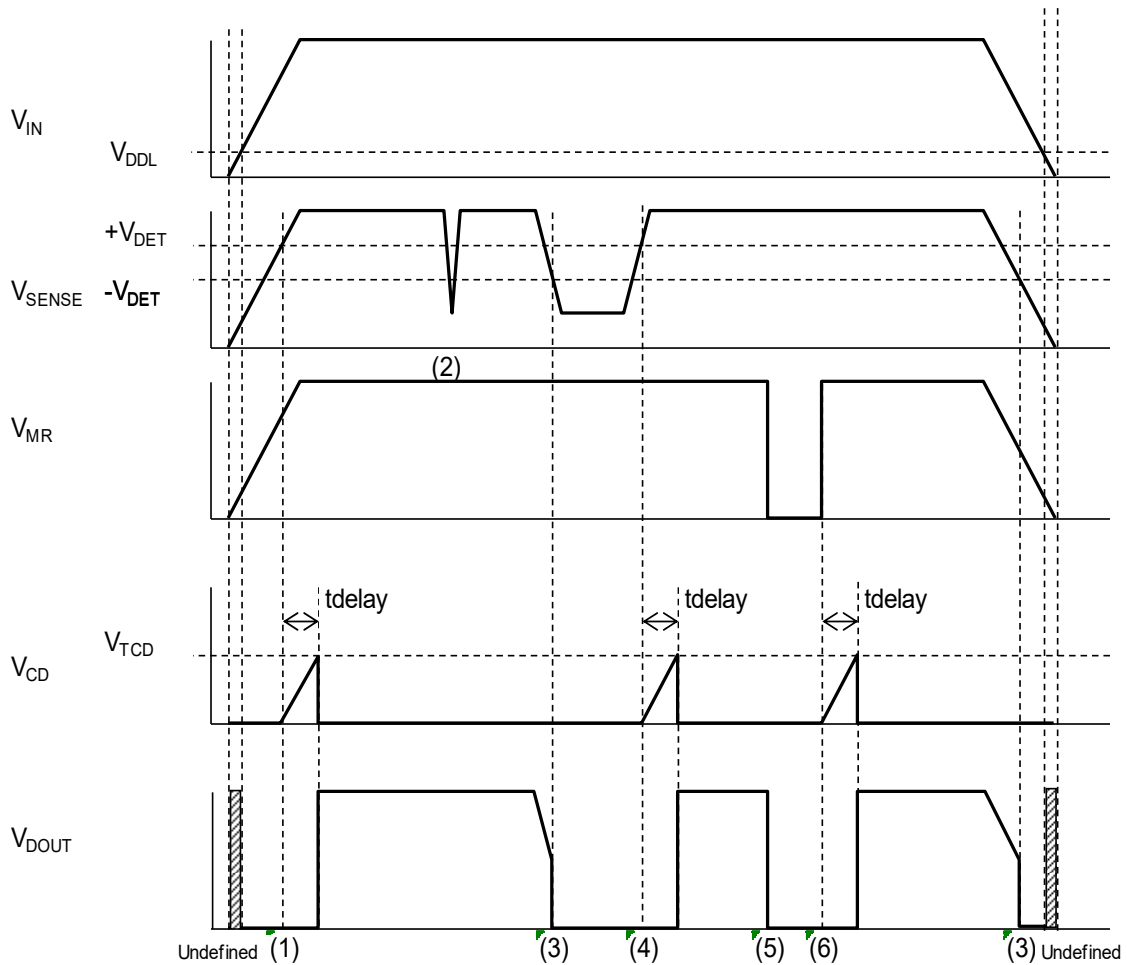
($T_a = 25^{\circ}\text{C}$)

Product Name	-V _{DET} [V]			V _{HYS} [V]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
R5111x01xx	4.518	4.600	4.682	0.046	0.092	0.138
R5111x02xx	1.572	1.600	1.628	0.016	0.032	0.048
R5111x03xx	4.419	4.500	4.581	0.045	0.090	0.135
R5111x04xx	4.321	4.400	4.479	0.044	0.088	0.132
R5111x05xx	4.223	4.300	4.377	0.043	0.086	0.129
R5111x06xx	4.125	4.200	4.275	0.042	0.084	0.126
R5111x07xx	3.634	3.700	3.766	0.037	0.074	0.111
R5111x08xx	2.946	3.000	3.054	0.030	0.060	0.090
R5111x09xx	2.848	2.900	2.952	0.029	0.058	0.087
R5111x10xx	2.750	2.800	2.850	0.028	0.056	0.084
R5111x11xx	2.652	2.700	2.748	0.027	0.054	0.081
R5111x12xx	4.027	4.100	4.173	0.041	0.082	0.123
R5111x13xx	3.045	3.100	3.155	0.031	0.062	0.093
R5111x142x	4.518	4.600	4.682	0.046	0.092	0.138

OPERATION DESCRIPTION**Timing Chart****R5111Sxx1A / R5111Sxx1B Voltage Detector****R5111Sxx1A / R5111Sxx1B VD Timing Chart**

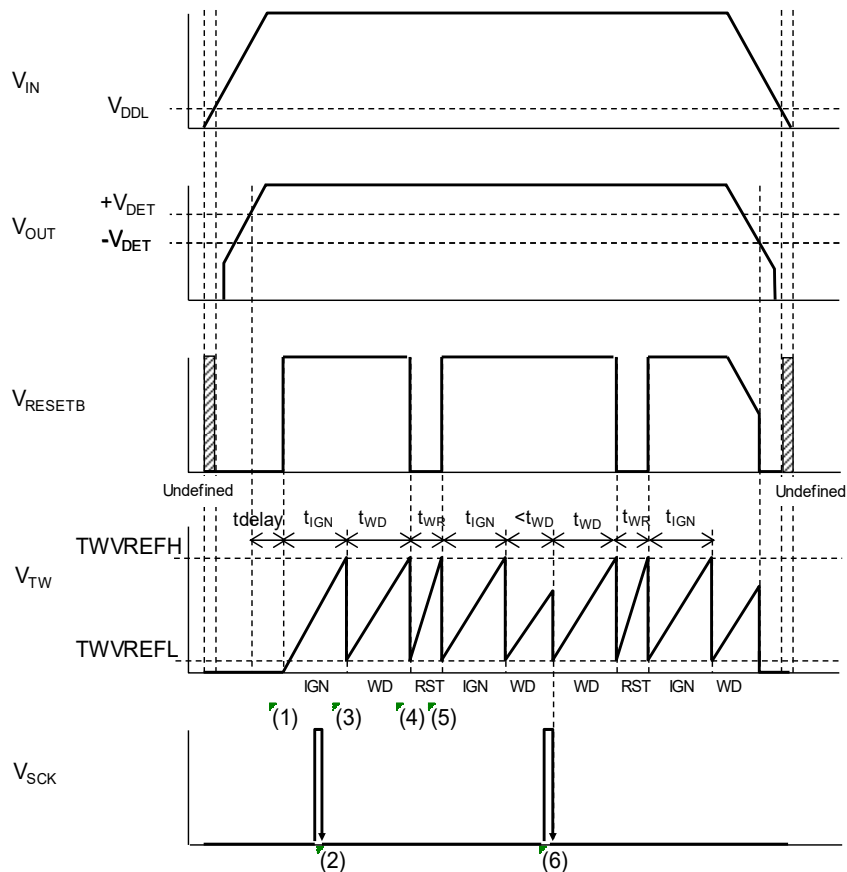
- (1) When the V_{OUT} pin voltage (V_{OUT}) becomes more than the release voltage ($+V_{DET}$), the $RESETB$ pin voltage (V_{RESETB}) becomes "H" after the release output delay time (t_{delay}).
- (2) When the detect output delay time is less than 30 μs (Typ.) even if V_{OUT} becomes lower than the detector threshold ($-V_{DET}$), the voltage detector (VD) does not go into the detecting state.
- (3) When V_{OUT} becomes lower than $-V_{DET}$, V_{RESETB} becomes "L" after the detect output delay time (Typ. 30 μs) and the VD goes into the detecting state.
- (4) When V_{OUT} becomes more than $+V_{DET}$, V_{RESETB} becomes "H" after the release output delay time. ($V_{TCD} = \text{Typ. } 1 \text{ V}$)

R5111xxx2C / R5111xxx2D Voltage Detector



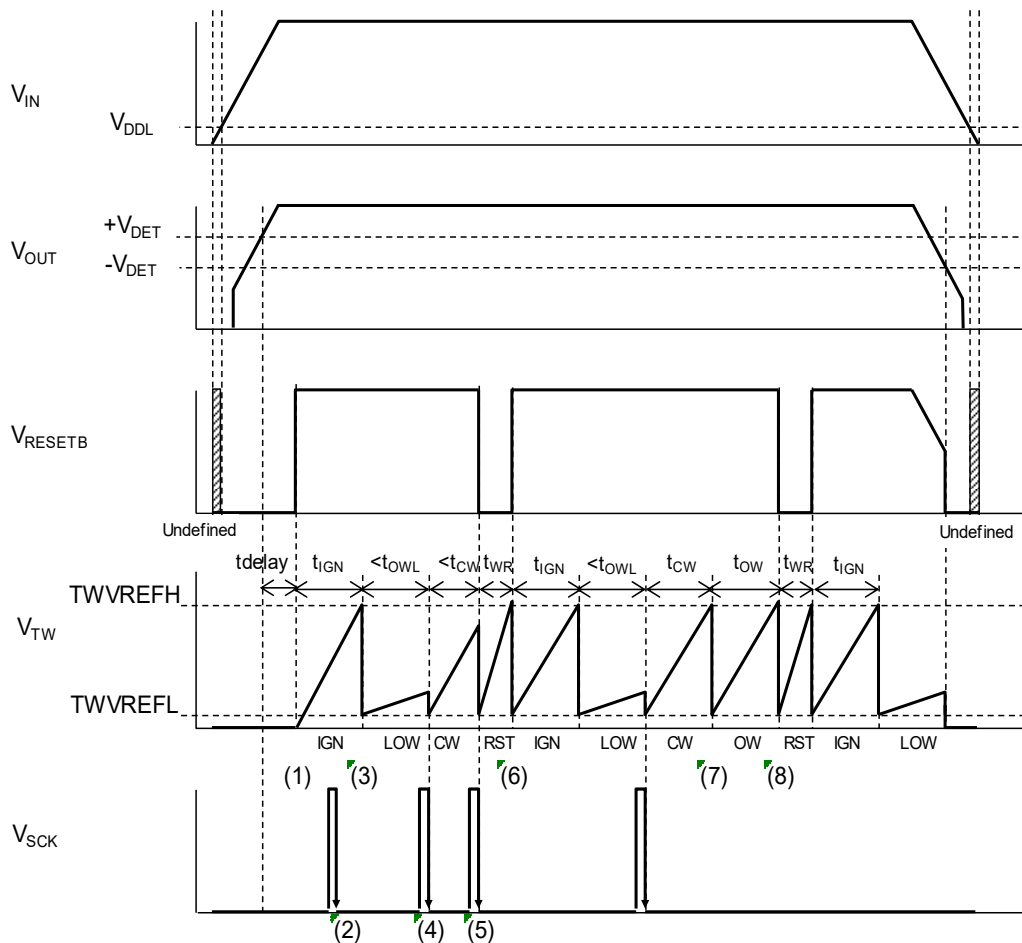
R5111xxx2C / R5111xxx2D VD Timing Chart

- (1) When the SENSE pin voltage (V_{SENSE}) becomes more than the release voltage ($+V_{\text{DET}}$), the DOUT pin voltage (V_{DOUT}) becomes "H" after the release output delay time (t_{delay}).
- (2) When the detect output delay time is 30 μs (Typ.) or less even if V_{SENSE} becomes lower than the detector threshold ($-V_{\text{DET}}$), the voltage detector (VD) does not go into the detecting state.
- (3) When V_{SENSE} becomes lower than $-V_{\text{DET}}$, V_{DOUT} becomes "L" after the detect output delay time (Typ. 30 μs) and the VD goes into the detecting state.
- (4) When V_{SENSE} becomes more than $+V_{\text{DET}}$, V_{DOUT} becomes "H" after the release output delay time. ($V_{\text{TCD}} = \text{Typ. } 1 \text{ V}$)
- (5) When the MR pin voltage (V_{MR}) becomes "L", V_{DOUT} is fixed to "L".
- (6) When V_{MR} becomes "L" to "H", V_{DOUT} becomes "H" after the release output delay time.

R5111Sxx1A Watchdog Timer (Normal Type)**R5111Sxx1A WDT Timing Chart**

- (1) When the V_{OUT} pin voltage (V_{OUT}) becomes more than the release voltage ($+V_{DET}$), the RESETB pin voltage (V_{RESETB}) becomes "H" after the release output delay time (t_{delay}) and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has three states: Ignoring, Reset, and Monitoring. In each state, the TW pin is charged from 0 V or $TWVREFL$ (Typ.0.08 V).
- (2) After the WDT starts, the WDT is in an ignoring state until V_{TW} is charged up to $TWVREFH$ (Typ.2 V). So, a pulse to the SCK pin is ignored during the ignoring state.
- (3) When charging V_{TW} up to $TWVREFH$ has completed, the TW pin starts discharging and the WDT goes into a monitoring state.
- (4) When a pulse is not sent to the SCK pin before V_{TW} reaches $TWVREFH$ during the monitoring state, the TW pin starts discharging and the WDT goes into a reset state. During the reset state, V_{RESETB} becomes "L".
- (5) When V_{TW} is charged up to $TWVREFH$ during the reset state, the TW pin starts discharging and the WDT goes into the ignoring state.
- (6) When a pulse is sent to the SCK pin before V_{TW} reaches $TWVREFH$ during the monitoring state, the TW pin start discharging and the WDT goes into the next open window state.

R5111Sxx1B Watchdog Timer (Window Type)



R5111Sxx1B WDT Timing Chart

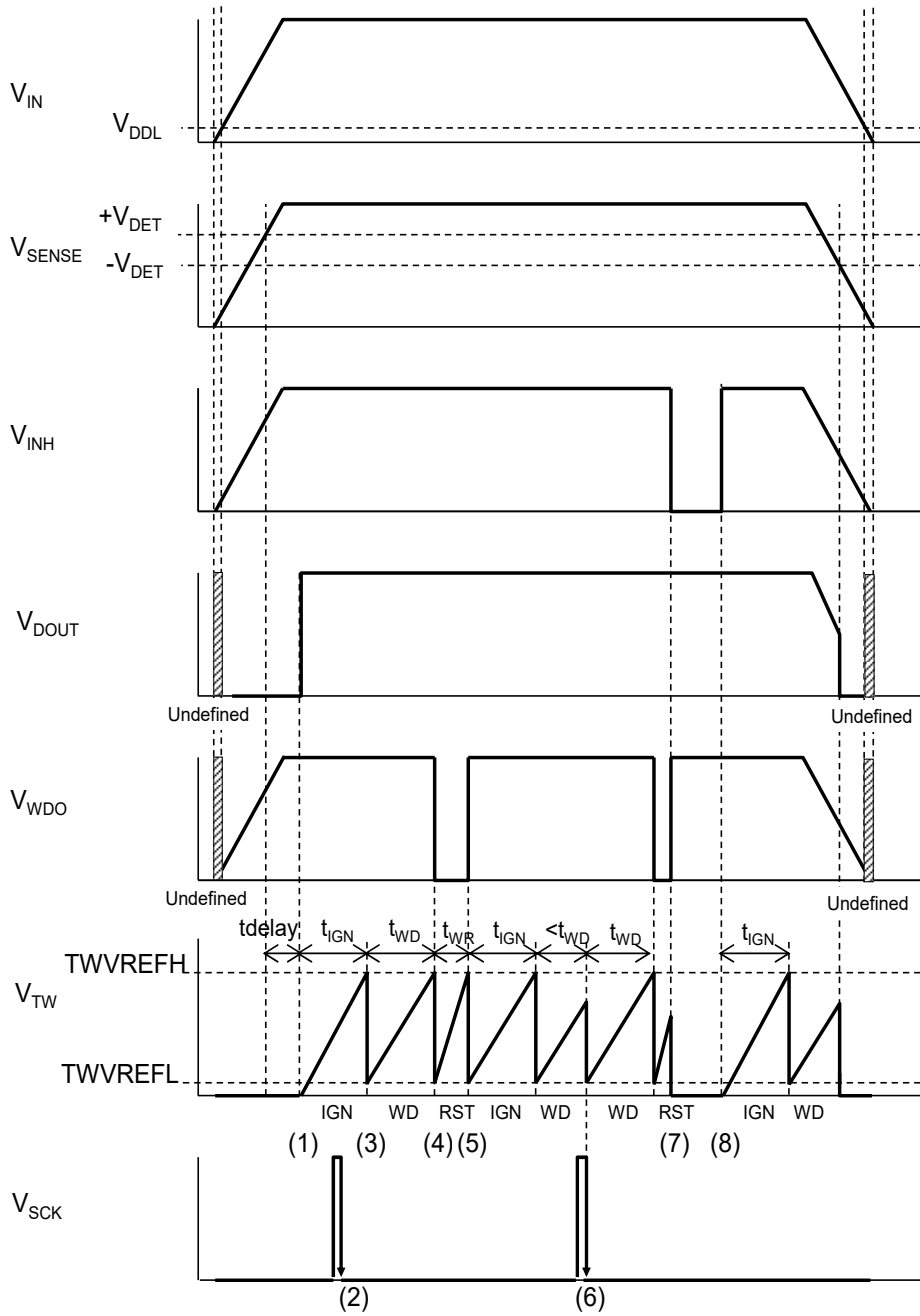
- (1) When the V_{OUT} pin voltage (V_{OUT}) becomes more than the release voltage ($+V_{DET}$), the RESETB pin voltage (V_{RESETB}) becomes “H” after the release output delay time (t_{delay}) and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has four states: Ignoring, Reset, Open Window, and Closed Window. In each state, the TW pin is charged from 0 V or TWVREFL (Typ.0.08 V).
- (2) After WDT starts, the WDT is in an ignoring state until V_{TW} is charged up to TWVREFH (Typ.2 V). So, a pulse to the SCK pin is ignored during the ignoring state.
- (3) When V_{TW} is charged up to TWVREFH during the ignoring state, the TW pin starts discharging and the WDT goes into an open window state. This open window state is four times longer than the normal open window state.
- (4) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREFH during the open window state, the TW pin starts discharging and the WDT goes into a closed window state.
- (5) When a pulse is sent to the SCK pin before V_{TW} reaches TWVREF during the closed window state, the TW pin starts discharging and the WDT goes into a reset state. During the reset state, V_{RESETB} becomes “L”.
- (6) When V_{TW} reaches TWVREFH during the reset state, the TW pin starts discharging and the WDT goes into the ignoring state.

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- (7) When a pulse is not sent to the SCK pin before V_{TW} reaches $TWVREFH$ during the closed window state, the TW pin starts discharging and the WDT goes into the open window state.
- (8) When a pulse is not sent to the SCK pin before V_{TW} reaches $TWVREFH$ during the open window state, the TW pin starts discharging and the WDT goes into the reset state.

R5111xxx2C Watchdog Timer (Normal Type)



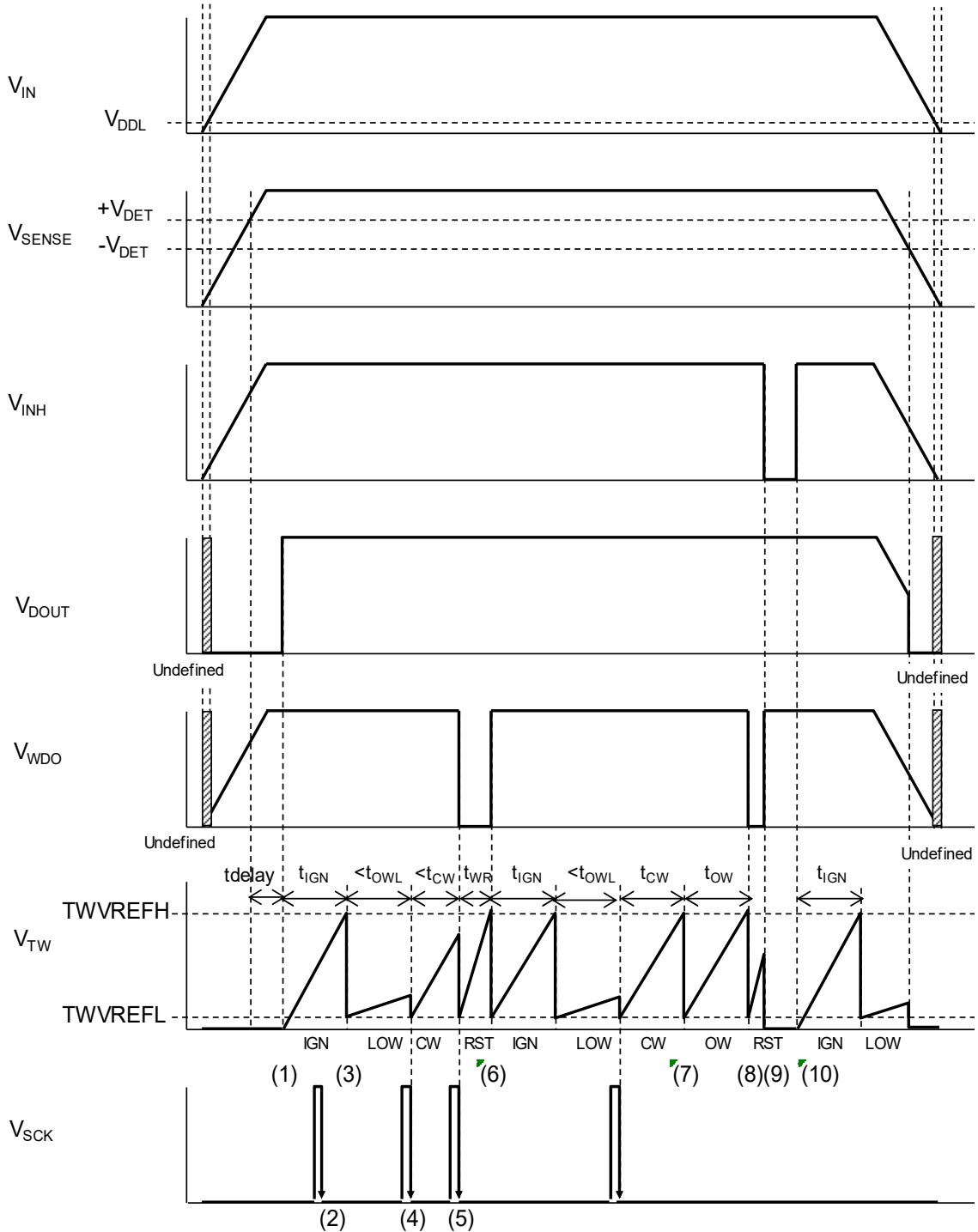
R5111xxx2C WDT Timing Chart

- (1) When the SENSE pin voltage (V_{SENSE}) becomes more than the release voltage ($+V_{\text{DET}}$), the DOUT pin voltage (V_{DOUT}) becomes “H” after the release output delay time (t_{delay}) and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has three states: Ignoring, Reset, and Monitoring. In each state, the TW pin is charged from 0 V or TWV_{REFL} (Typ.0.08V).
- (2) After the WDT starts, the WDT is in an ignoring state until V_{TW} is charged up to TWV_{REFH} . So, a pulse to the SCK pin is ignored during the ignoring state.
- (3) When V_{TW} is charged up to TWV_{REFH} during the ignoring state, the TW pin starts discharging and the WDT goes into a monitoring state.
- (4) When a pulse is not sent to the SCK pin before V_{TW} reaches TWV_{REFH} during the monitoring state, the TW pin starts discharging and the WDT goes into a reset state. During the reset state, the WDO pin voltage (V_{WDO}) becomes “L”.
- (5) When V_{TW} reaches TWV_{REFH} during the reset state, the TW pin starts discharging and the WDT goes into an ignoring state.
- (6) When a pulse is sent to the SCK pin before V_{TW} reaches TWV_{REFH} during the monitoring, the TW pin starts discharging and the WDT goes into the next monitoring state.
- (7) The WDT stops monitoring by setting the INH pin voltage (V_{INH}) to “L”. Then, V_{WDO} is fixed to “H” and V_{TW} is fixed to “L”.
- (8) When changed V_{INH} from “L” to “H”, the WDT goes into the ignoring state and restarts monitoring.

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R5111xxx2D Watchdog Timer (Window Type)

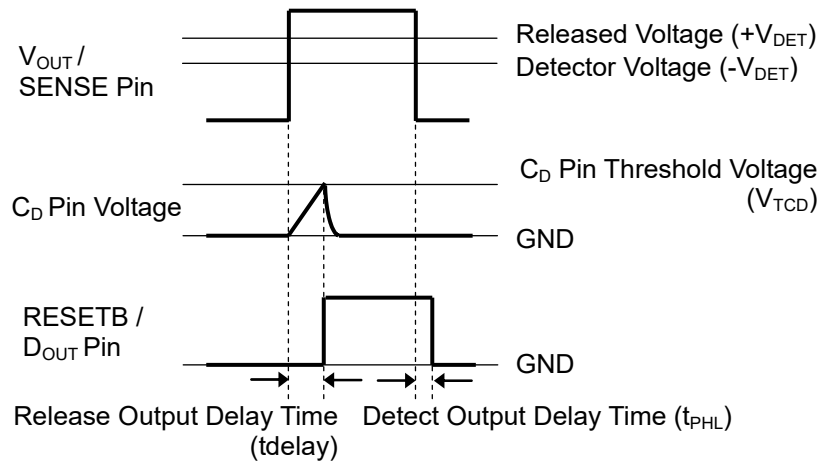


R5111xxx2D WDT Timing Chart

- (1) When the SENSE pin voltage (V_{SENSE}) becomes more than the release voltage ($+V_{\text{DET}}$), the DOUT pin voltage (V_{DOUT}) becomes “H” after the release output delay time (t_{delay}) and the watchdog timer (WDT) starts monitoring a pulse. After that, the TW pin voltage (V_{TW}) repeats charge and discharge. As a result, a sawtooth wave is generated. The WDT has four states: Ignoring, Reset, Open Window, and Closed Window. In each state, the TW pin is charged from 0 V or TWV_{REFL} (Typ.0.08 V).
- (2) After WDT starts, the WDT is in an ignoring state until V_{TW} is charged up to TWV_{REFH} . So, a pulse to the SCK pin is ignored during the ignoring state.
- (3) When V_{TW} is charged up to TWV_{REFH} during the ignoring state, the TW pin starts discharging and the WDT goes into an open window state. This open window state is four times longer than the normal open window state.
- (4) When a pulse is sent to the SCK pin before V_{TW} reaches TWV_{REFH} during the open window state, the TW pin starts discharging and the WDT goes into a closed window state.
- (5) When a pulse is sent to the SCK pin before V_{TW} reaches TWV_{REFH} during the close window state, the TW pin starts discharging and the WDT goes into a reset state. During the reset state, V_{DOUT} becomes “L”.
- (6) When V_{TW} reaches TWV_{REFH} during the reset state, the TW pin starts discharging and the WDT goes into an ignoring state.
- (7) When a pulse is not sent to the SCK pin before V_{TW} reaches TWV_{REFH} during a closed window state, the TW pin starts discharging and the WDT goes into an open window state.
- (8) When a pulse is not sent to the SCK pin before V_{TW} reaches TWV_{REFH} during the open window state, the TW pin starts discharging and the WDT goes into a reset state.
- (9) The WDT stops monitoring by setting the INH pin voltage (V_{INH}) to “L”. Then, V_{WDO} is fixed to “H” and V_{TW} is fixed to “L”.
- (10) When changed V_{INH} from “L” to “H”. the WDT goes into the ignoring state and restarts monitoring.

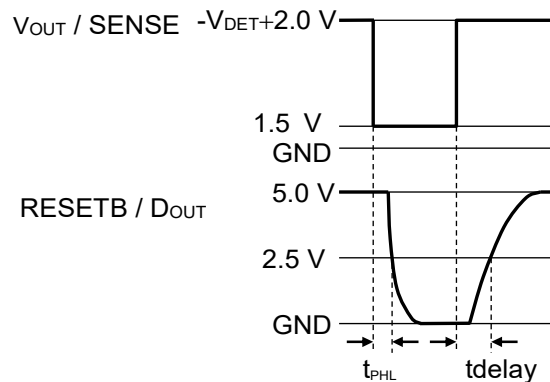
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Delay Operation and Released Output Delay Time (t_{delay})**Released Output Delay Timing Diagram**

When the operating voltage higher than the released voltage is applied to V_{OUT} pin (R5111Sxx1A/R5111Sxx1B) or SENSE pin (R5111xxx2C/R5111xxx2D), charge to an external capacitor starts, then C_{D} pin voltage (V_{CD}) increases. RESETB pin (R5111Sxx1A/R5111Sxx1B) or D_{OUT} pin (R5111xxx2C/R5111xxx2D) maintains the released output until V_{CD} reaches the threshold voltage of the release output delay pin (V_{TCD}). And when V_{CD} is over V_{TCD} , RESETB pin or D_{OUT} pin is inverted from “L” to “H”. That is, the charged external capacitor starts discharging.

When the operating voltage lower than the detector threshold is applied to V_{DD} pin, the detect output delay time, which is the time until the output voltage is inverted from “H” to “L”, remains constant independent of the external capacitor.

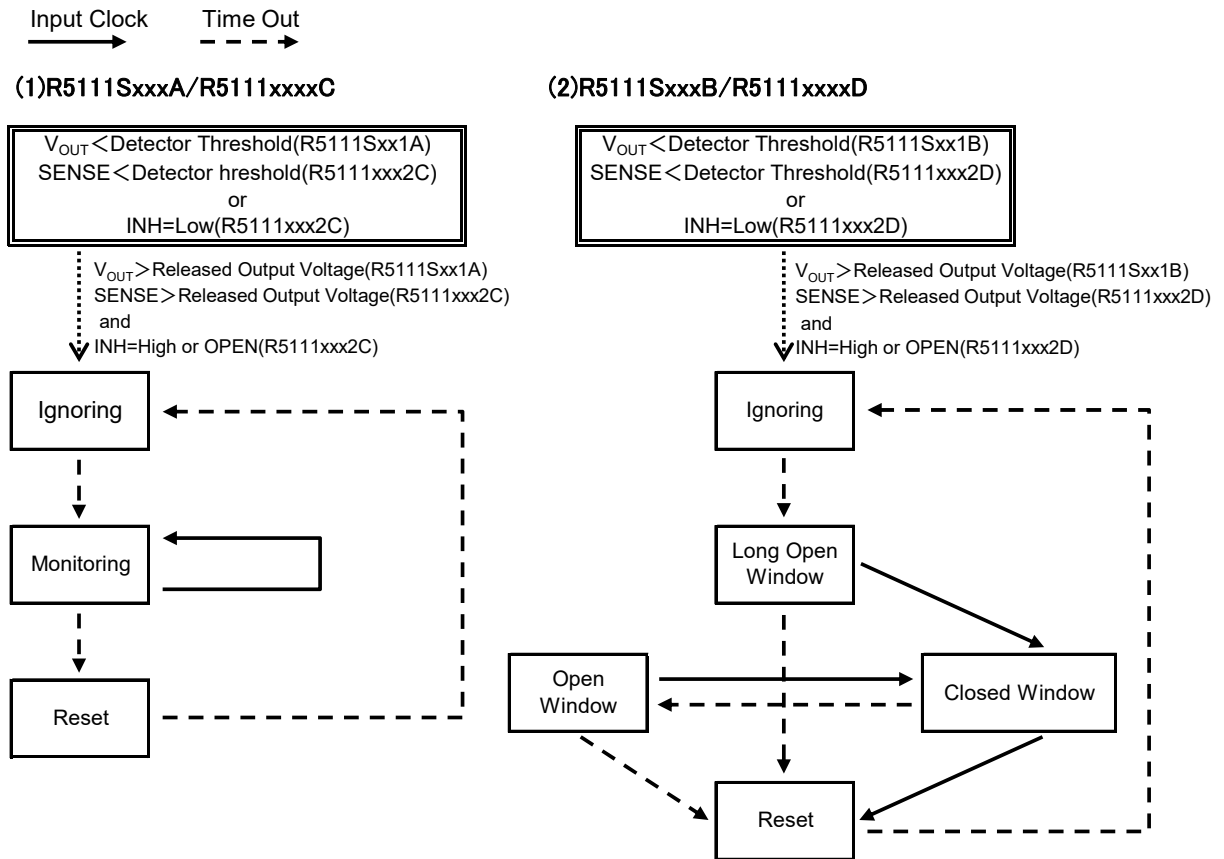
**Released Output Delay Time**

Released Output Delay Time (t_{delay}) indicates the time between the instance when V_{OUT} pin (R5111Sxx1A / R5111Sxx1B) or SENSE pin (R5111xxx2C / R5111xxx2D) shifts from “1.5 V” to “ $-V_{\text{DET}} + 2.0 \text{ V}$ ” by the application of a pulse voltage and the instance when the output voltage reaches 2.5 V after pulled up RESETB pin (R5111Sxx1A / R5111Sxx1B) or D_{OUT} pin (R5111xxx2C/ R5111xxx2D) to 5.0 V with a resistor of 100 k Ω .

This is given by the expression $t_{delay} (s) = 1.1 \times C_D (F) / (1.0 \times 10^{-6})$, where $C_D (F)$ represents capacitance of the external capacitor.

If $V_{OUT} / SENSE$ pin goes up at a mild pace of 0.1V/s or less, connect a capacitor of 100 pF or more to C_D pin.

WDT State Transition Diagram



Time Setting for Watchdog Timer

The following time of WDT is dependent on a capacitor connecting to the TW pin. Relationship between the value of capacitor and time can be expressed by the following equations.

$$t_{ow} (s) = 1.8 \times C(F) / (1.0 \times 10^{-6})$$

$$t_{cw} (s) = 1.8 \times C(F) / (1.0 \times 10^{-6})$$

$$t_{owl} (s) = 1.8 \times C(F) / (0.25 \times 10^{-6})$$

$$t_{ign} (s) = 1.8 \times C(F) / (1.0 \times 10^{-6})$$

$$t_{wd} (s) = 1.8 \times C(F) / (1.0 \times 10^{-6})$$

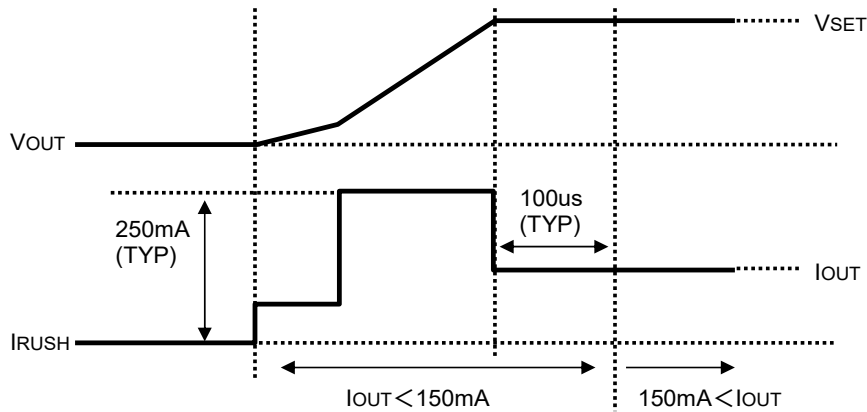
$$t_{wr} (s) = 1.9 \times C(F) / (2.0 \times 10^{-6})$$

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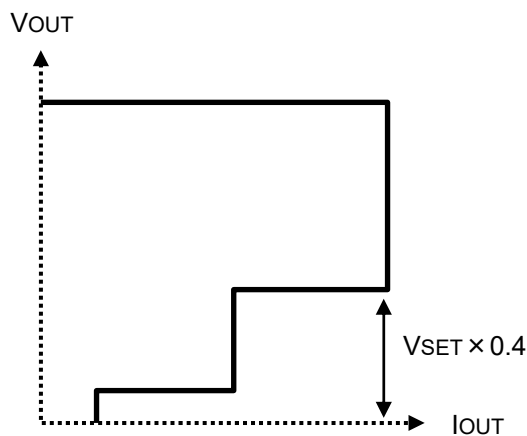
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Inrush Current Prevention at Rising Characteristics

R5111x has the inrush current preventing circuit to control the inrush current within about 250 mA limited. This circuit works during the rising periods. Therefore, the load current must be increased after rising up the output voltage (at typ.100 μ s after being out of the inrush current limited condition) by the sequence control. When the load current is increased during the rising periods, the inrush current must be controlled within 150 mA.



Likewise, on the thermal shutdown and the foldback characteristic, the inrush current preventing circuit works when the output voltage re-rises after the output voltage fall down to a guideline ($V_{SET} \times 0.4$) or less.



Standby Function

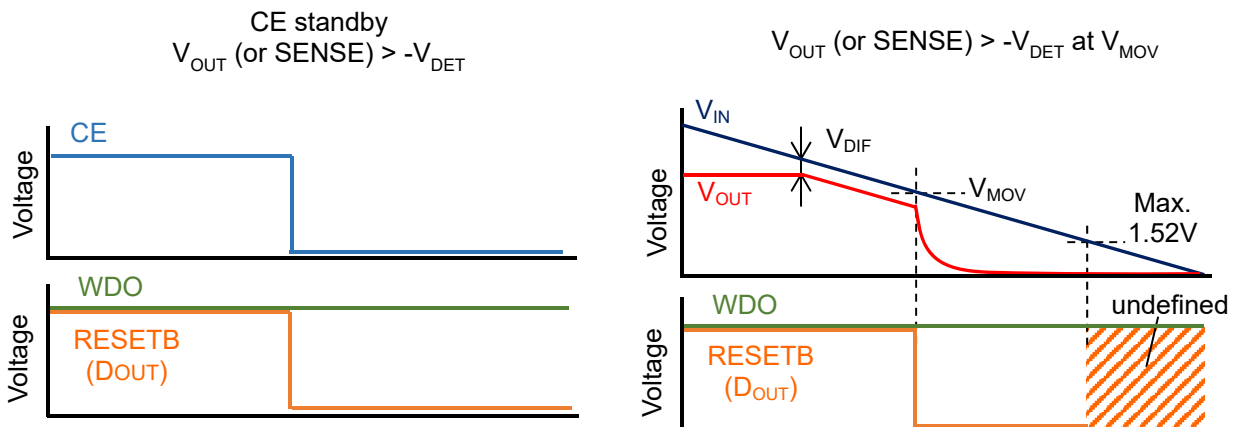
When CE turns to low, the R5111x goes into the standby mode. During this mode, the voltage regulator (VR) stops the output, the watchdog timer (WDT) stops the pulse monitoring, and the voltage detector (VD) stops the voltage monitoring.

Even if $V_{IN} < 3.5$ V (Minimum Operating Voltage V_{MOV}), VR stops the output, WDT stops the pulse monitoring, and VD stops the voltage monitoring. When CE = low or $V_{IN} < 3.5$ V (Minimum Operating Voltage), the output of WDT and VD become as follows regardless of SENSE voltage.

R5111Sxx1A/ R5111Sxx1B: The RESETB output is fixed to "L".

R5111xxx2C/ R5111xxx2D: The D_{OUT} is fixed to "L", and WDO output is fixed to the pull-up voltage.

When V_{IN} is under 1.52 V, values of RESETB output (R5111Sxx1A/ R5111Sxx1B) and D_{OUT} output (R5111xxx2C/ R5111xxx2D) become indefinite, 0.1 V or more (pull-up voltage 5 V, pull-up resistance 100 k Ω).



Voltage Setting (R5111Sxx1A / R5111Sxx1B)

VD detects the drop of the VR output voltage (V_{OUT}). When the VD release voltage ($+V_{DET}$) is set to a voltage above the VR output voltage, the reset signal of VD is not released even if VD monitors the VR output voltage returns to the normal value after detecting the drop of VR. To prevent this issue, the following condition is required between V_{OUT} and $+V_{DET}$.

$$(VR \text{ Set Output Voltage}) \times 0.985 - 30 \text{ mV} > (VD \text{ Set Detector Threshold}) \times 1.018 \times 1.030$$

When using a device with the above conditions of V_{OUT} and $+V_{DET}$, careful consideration must be given to the system operation before use.

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Manual Reset (MR) Function (R5111xxx2C, R5111xxx2D)

Setting the MR pin to “L” forcefully sets D_{OUT} to “L”. The maximum value of the delay time (t_{MR}), which is until D_{OUT} outputs “L”, is 1 μ s as an index of the performance. The MR pin is pulled-up by an internal resistor (Typ.110 k Ω). Current is passed to the MR pin when the voltage of MR > V_{DD}. But, this current has no effect to the operation because the current is limited with a pull-up resistor.

When setting the MR pin from “L” to “H”, D_{OUT} is changed from “L” to “H” after the released output delay time and the WDT starts from the ignoring state.

When the MR pin is “L”, the WDO pin outputs “H”.

SENSE Function (R5111xxx2C, R5111xxx2D)

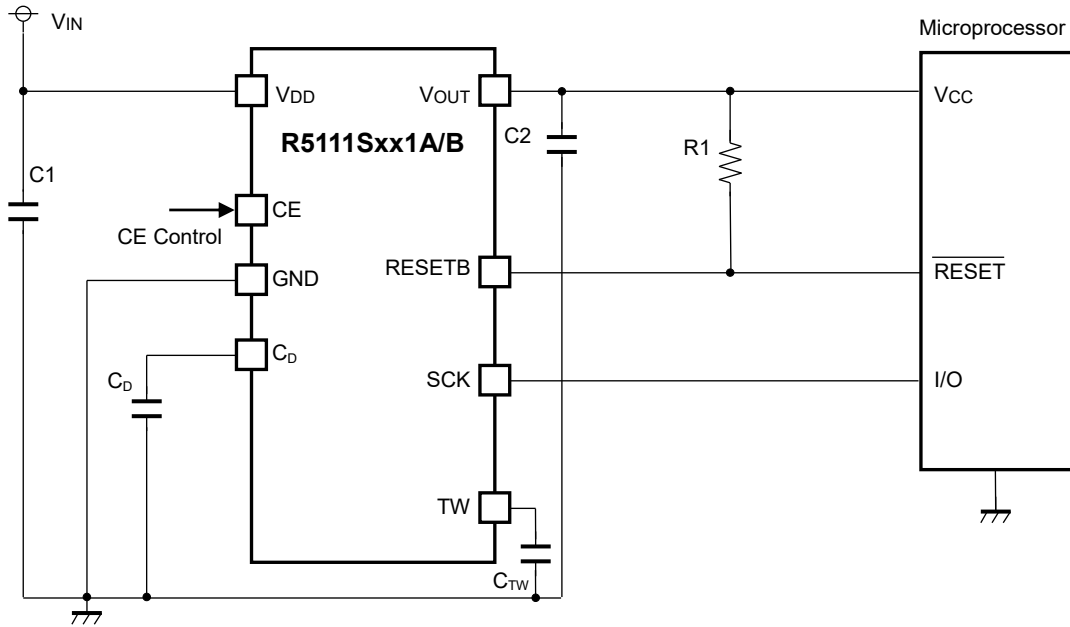
The internal voltage detector monitors the input voltage to the SENSE pin. To measure the proper detector threshold, setting of V_{IN} \geq 3.5 V is required.

Inhibition (INH) Function (R5111xxx2C, R5111xxx2D)

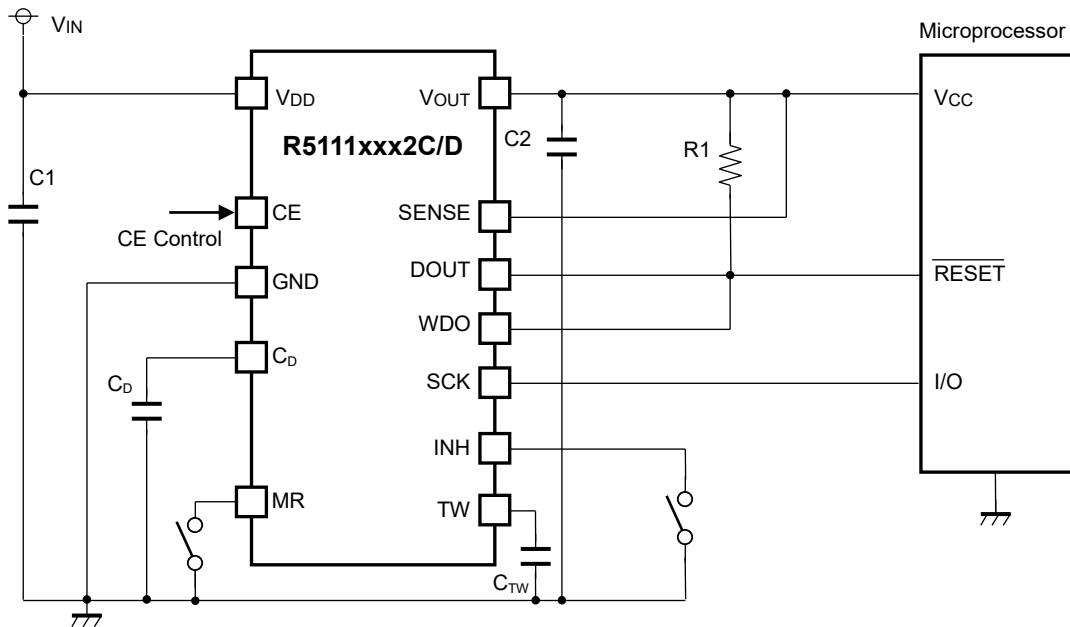
Setting the INH pin to “L” stops the WDT pulse monitoring function and the WDO pin is fixed to “H”. The INH pin is pulled up with an internal resistor (Typ.110 k Ω).

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUITS



R5111Sxx1A/B Typical Application



R5111xxx2C/D Typical Application

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External Components

Symbol	Description
C1 (C _{IN})	0.1 μ F, Ceramic Capacitor
C2 (C _{OUT})	0.1 μ F, Ceramic Capacitor
C _{TW}	A capacitor corresponding to time setting for Watchdog Timer is required. Refer to " <i>Time Setting for WDT</i> " in Operation Description for details.
C _D	A capacitor corresponding to setting for Release Output Delay Time is required. Refer to " <i>Delay Operation and Release Output Delay Time (t_{delay})</i> " in Operation Description for details.
R1	A resistor is required to set with consideration of the output current and the leakage current. Refer to " <i>Electrical Characteristic</i> " for details.

TECHNICAL NOTES

Phase Compensation

In the ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a capacitor C2 with 0.1 μ F or more.

If a tantalum capacitor is used, and its ESR (Equivalent Series Resistance) of C2 is large, the loop oscillation may result. Because of this, select C2 carefully considering its frequency characteristics.

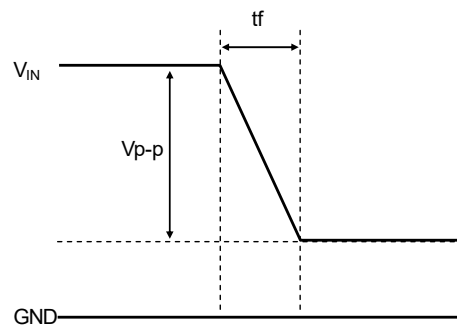
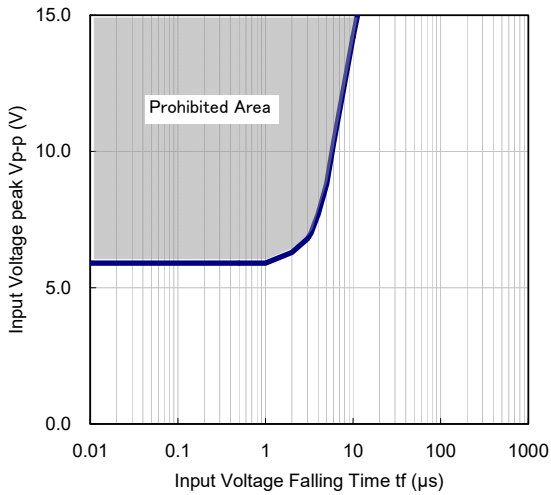
PCB Layout

Make V_{DD} and GND lines sufficient. If their impedance is too high, noise pickup or unstable operation may result. Connect 0.1 μ F or more of the capacitor C1 between the V_{DD} and GND, and as close as possible to the pins.

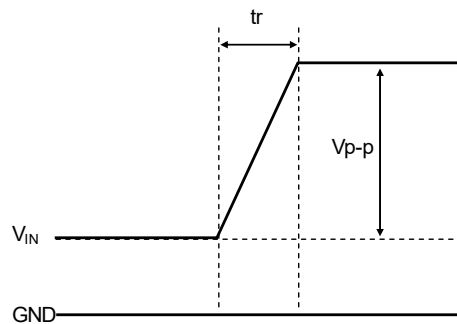
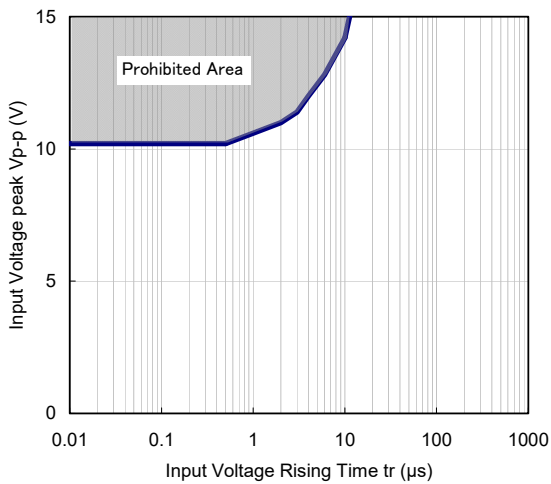
In addition, connect the capacitor C2 between V_{OUT} and GND, and as close as possible to the pins.

Prohibited Area for Fluctuations in Input Voltage

Please take note that miss-detection or miss-release might be invited when changing an input voltage abruptly in the following prohibited area.



Prohibited Area of Fluctuation at Falling of V_{IN}

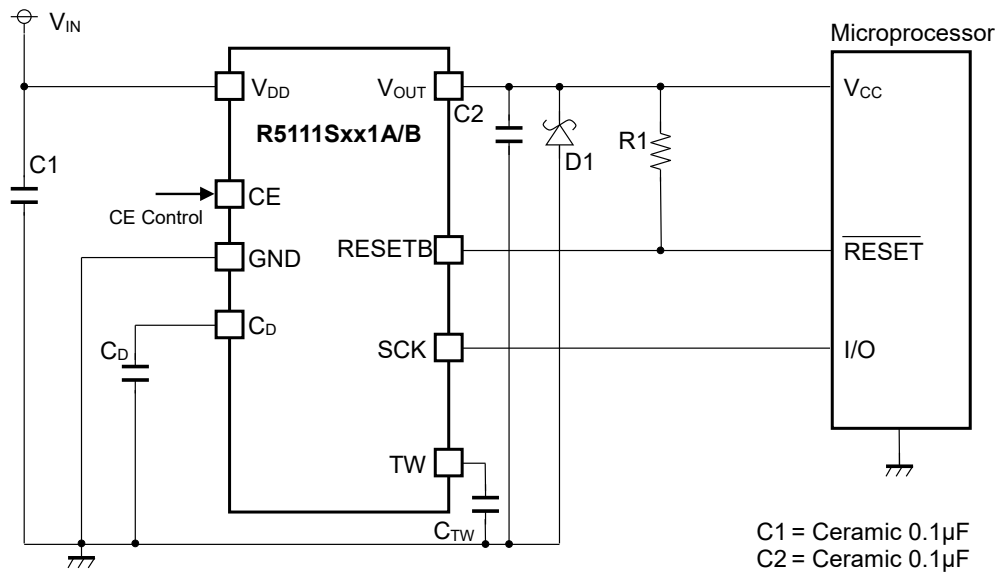


Prohibited Area of Fluctuation at Rising of V_{IN}

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Typical Application for IC Chip Breakdown Prevention



R5111Sxxxx Typical Application

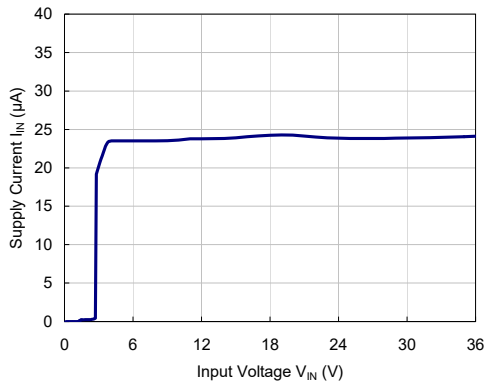
When a sudden surge of electrical current travels along the VOUT pin and GND due to a short-circuit, electrical resonance of a circuit involving an output capacitor (C2) and a short circuit inductor generates a negative voltage and may damage the device or the load devices. Connecting a schottky diode (D1) between the VOUT pin and GND has the effect of preventing damage to them.

TYPICAL CHARACTERISTICS

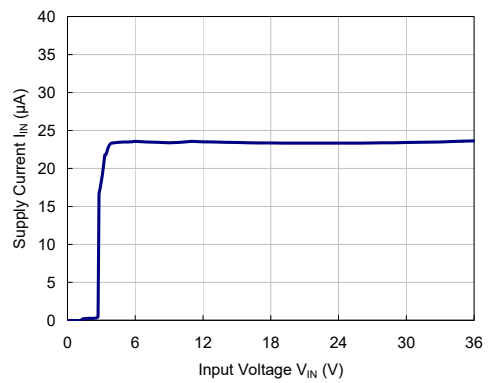
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Power Consumption vs. Input Voltage ($T_a = 25^\circ\text{C}$)

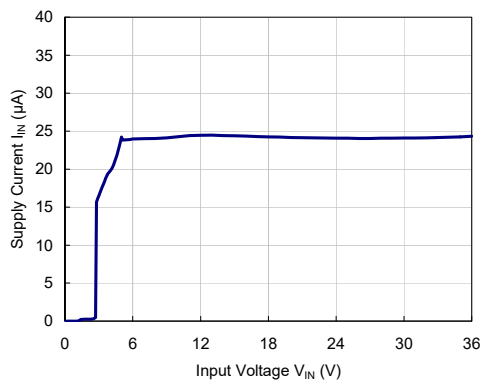
VR=1.8V



VR=3.3V

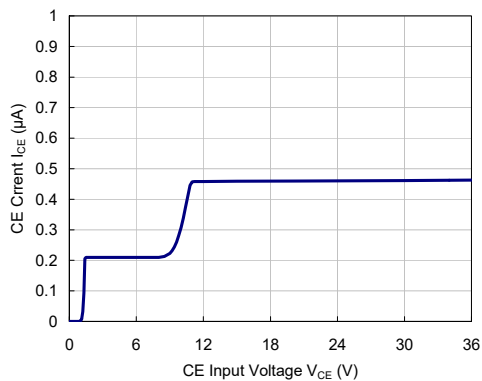


VR=5.0V



2) CE Pin Current vs. CE Pin Voltage ($T_a = 25^\circ\text{C}$, $V_{IN}=14\text{V}$)

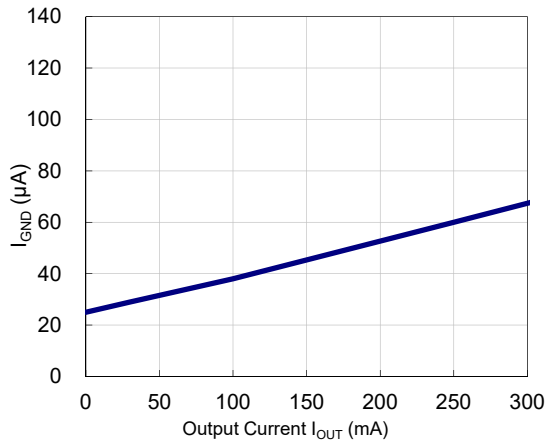
VR=5.0V



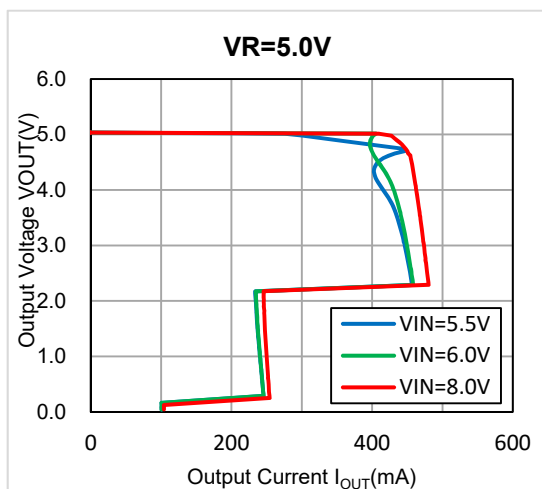
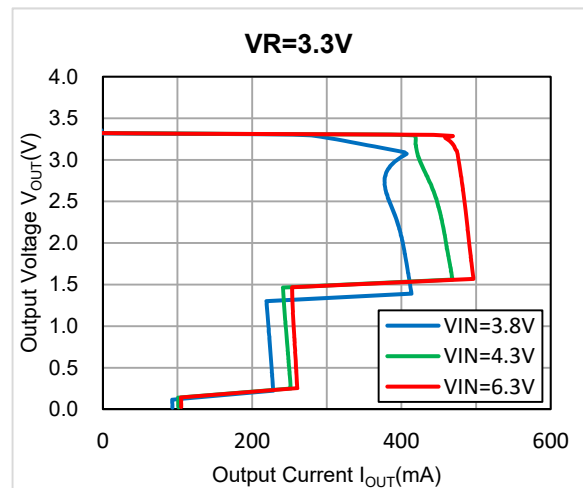
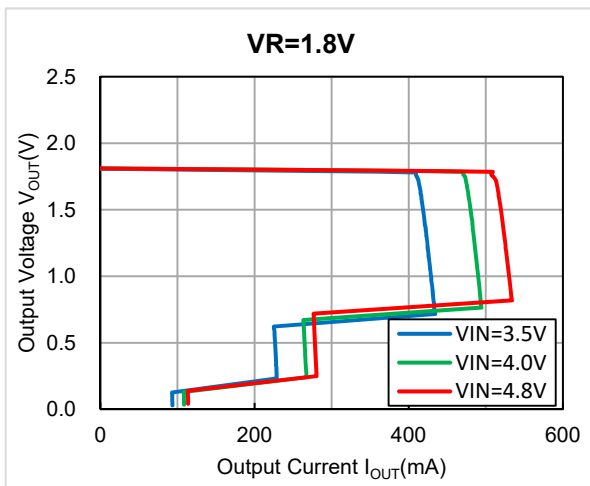
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3) GND Pin Current vs. Output Current (Ta = 25°C)

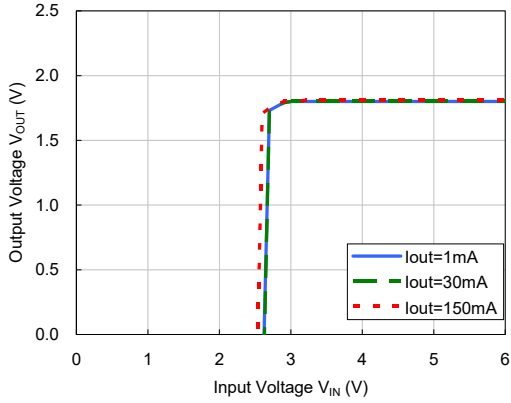


4) Output Voltage vs. Output Current (Ta = 25°C)

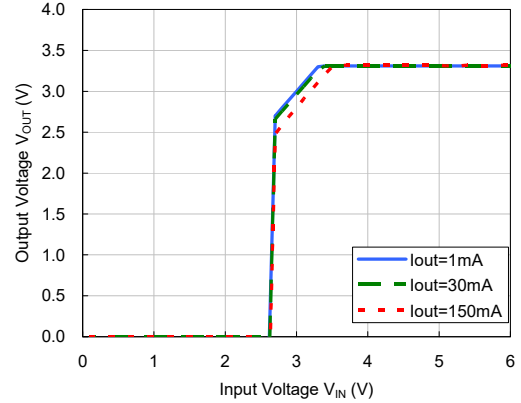


5) Output Voltage vs. Input Voltage ($T_a = 25^\circ\text{C}$)

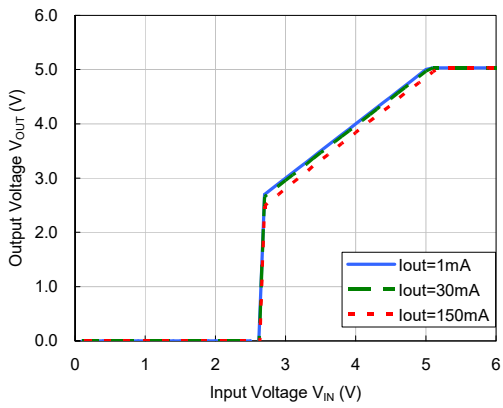
VR=1.8V



VR=3.3V

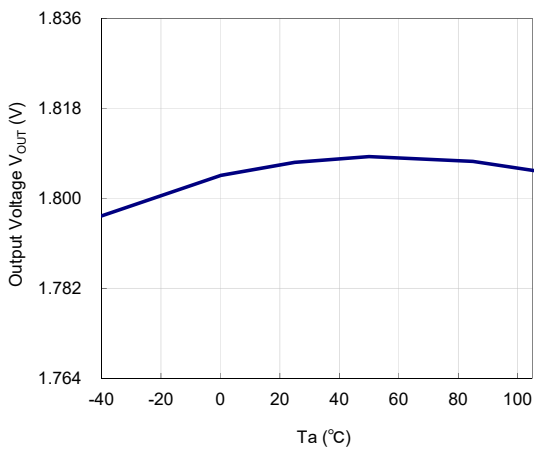


VR=5.0V

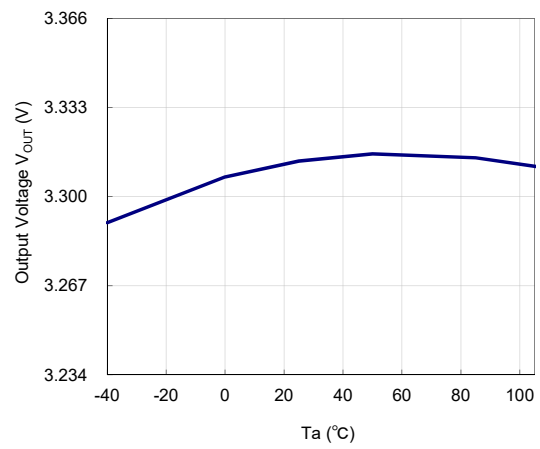


6) Output Voltage vs. Temperature ($V_{IN}=14\text{V}$, $I_{OUT}=1\text{mA}$)

VR=1.8V



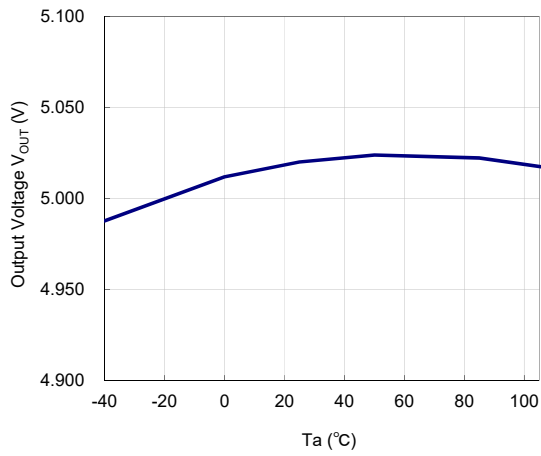
VR=3.3V



R5111x-Y

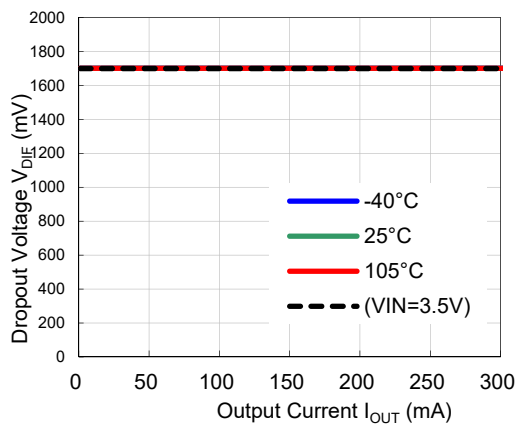
No. EA-372-190115

VR=5.0V

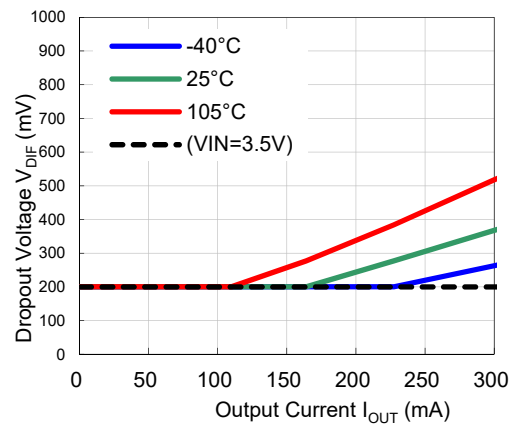


7) Dropout Voltage vs. Output Current

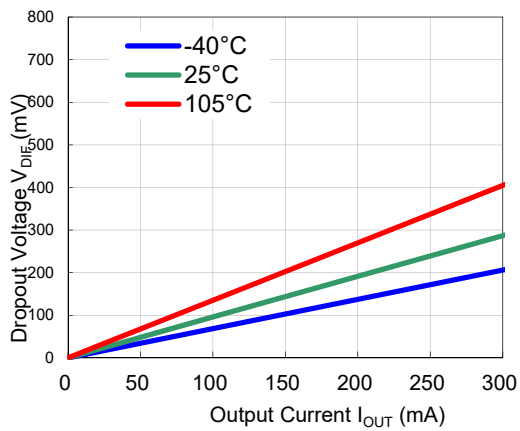
VR=1.8V



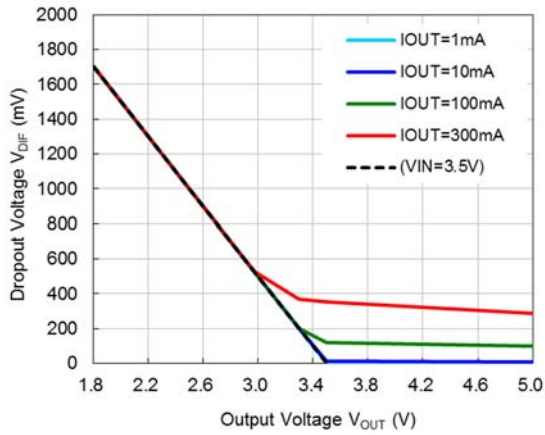
VR=3.3V



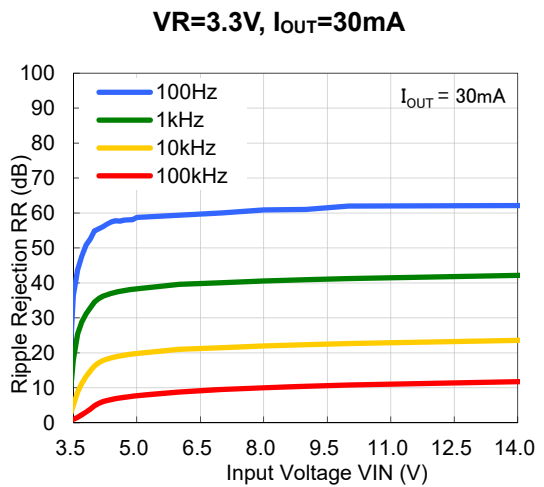
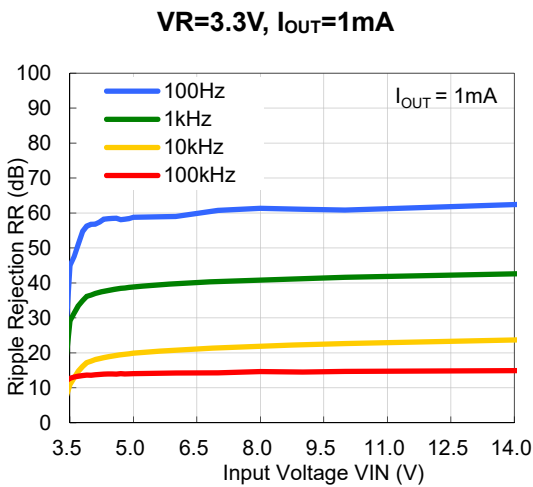
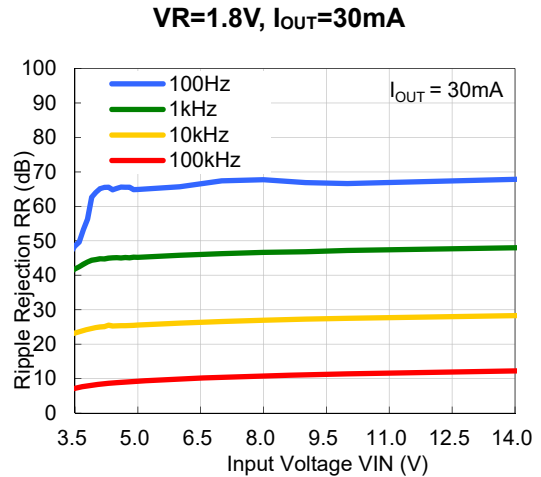
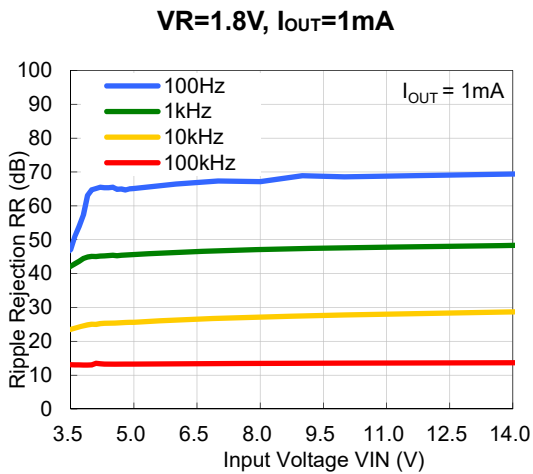
VR=5.0V

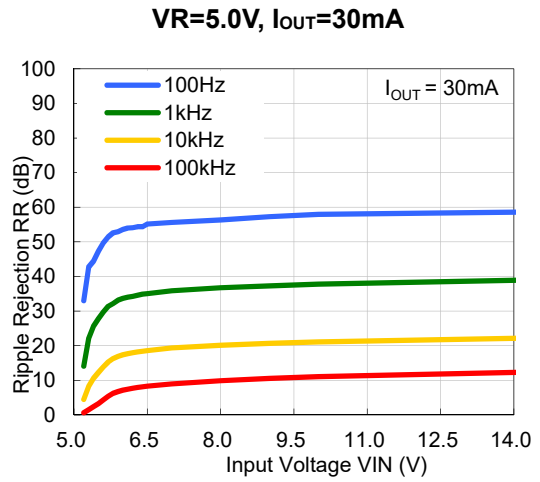
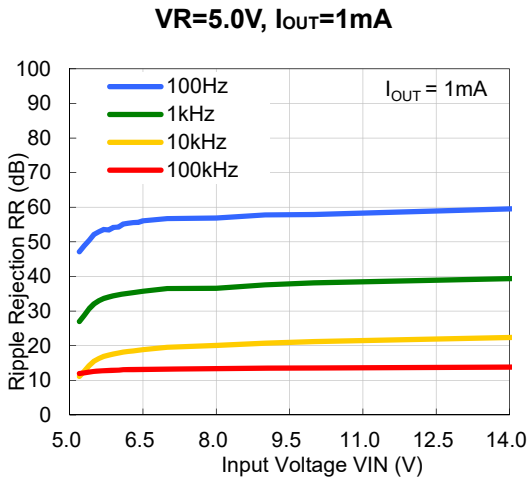


8) Dropout Voltage vs. Output Voltage (Ta=25°C)

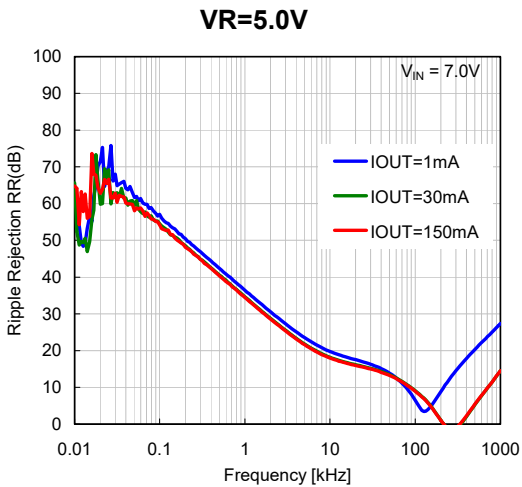
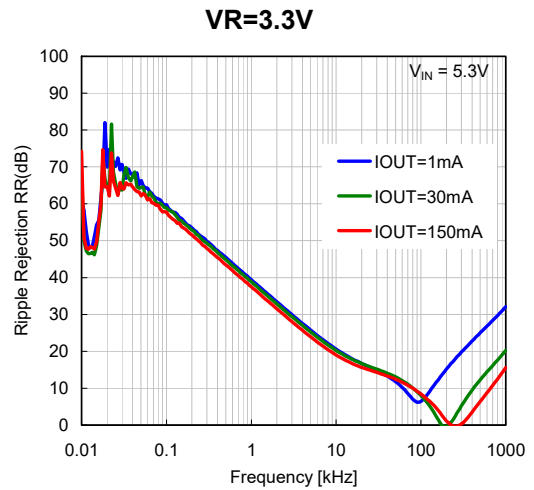
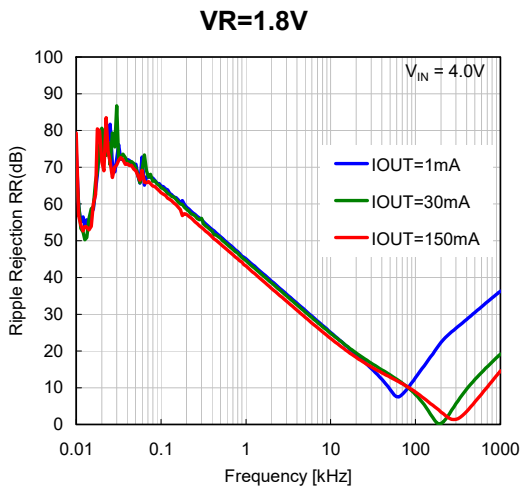


9) Ripple Rejection vs. Input Voltage (Ta=25°C, Ripple = 0.2 Vpp)



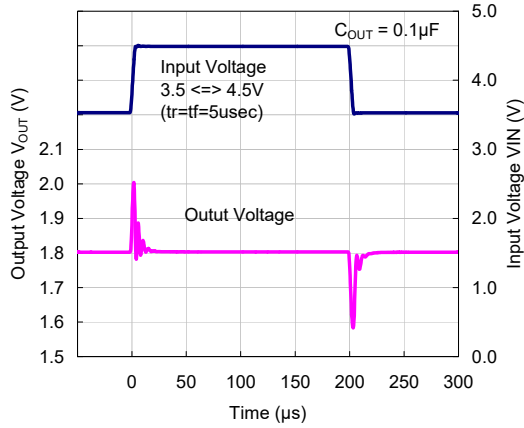


10) Ripple Rejection vs. Frequency (Ta=25°C, Ripple=0.2 Vpp)

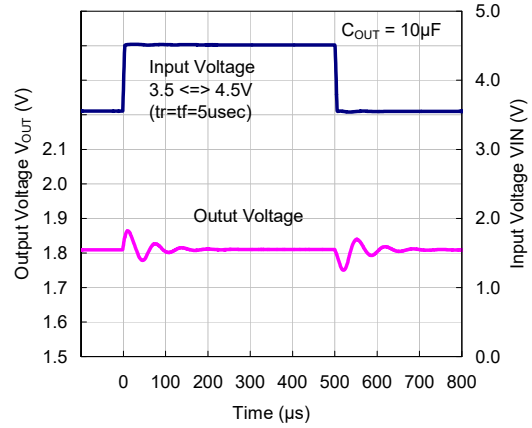


11) Input Transient Respon (Ta=25°C)

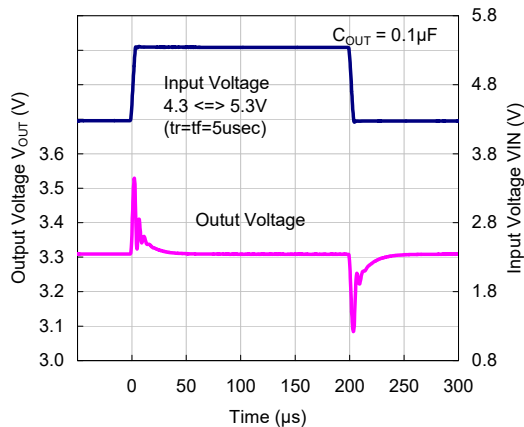
VR=1.8V, I_{OUT}=30mA, C_{OUT}=0.1μF



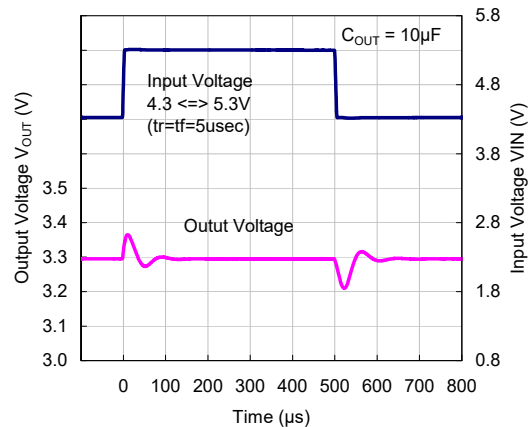
VR=1.8V, I_{OUT}=30mA, C_{OUT}=10μF



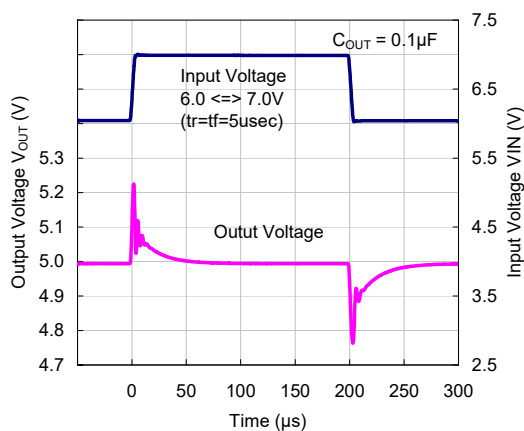
VR=3.3V, I_{OUT}=30mA, C_{OUT}=0.1μF



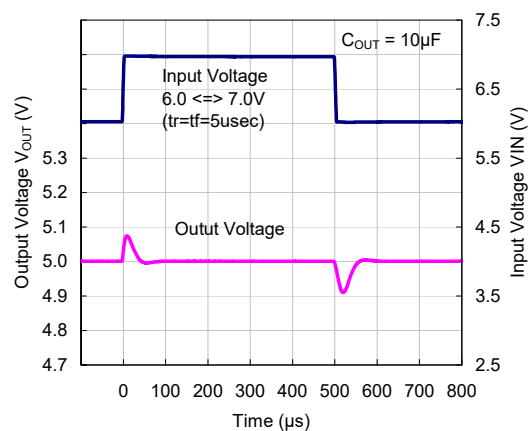
VR=3.3V, I_{OUT}=30mA, C_{OUT}=10μF



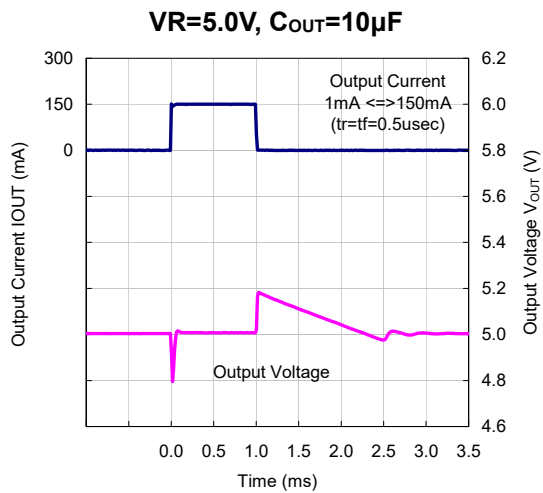
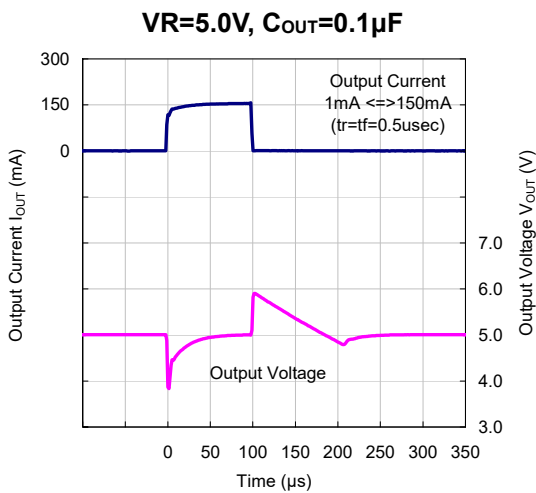
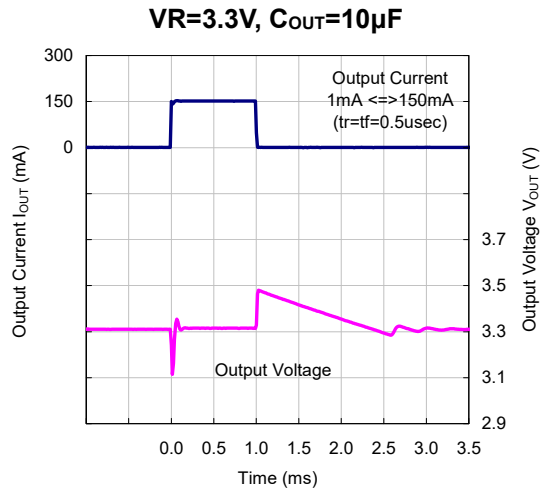
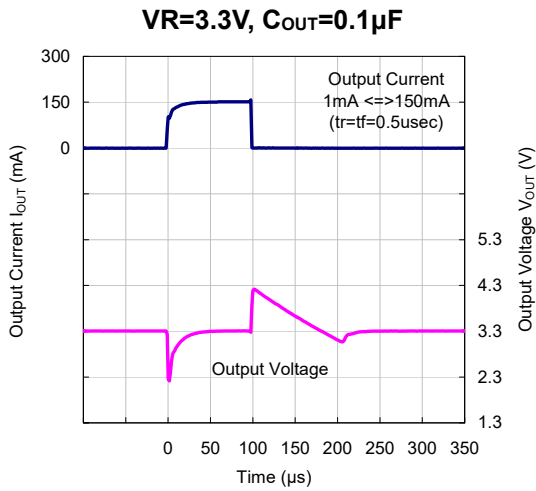
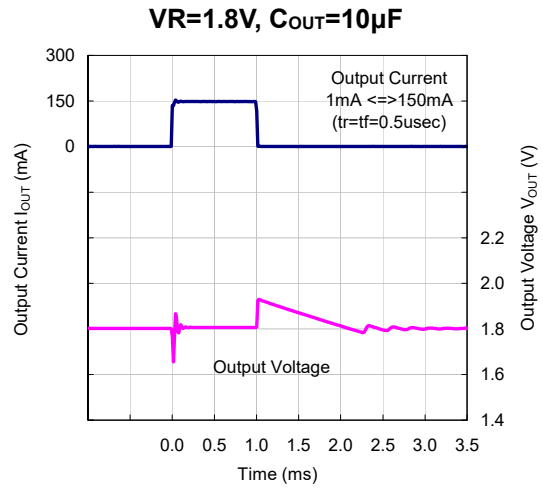
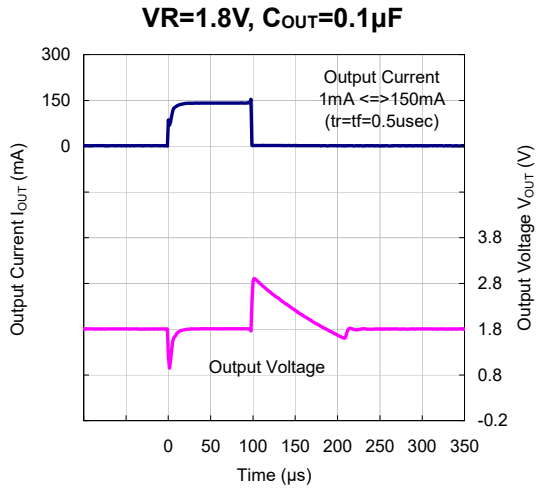
VR=5.0V, I_{OUT}=30mA, C_{OUT}=0.1μF



VR=5.0V, I_{OUT}=30mA, C_{OUT}=10μF

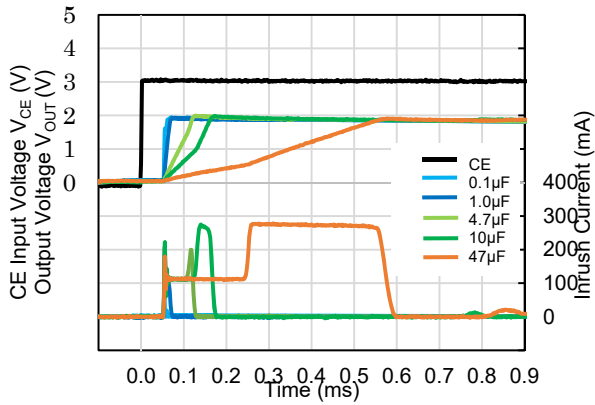


12) Load Transient Response (Ta=25°C)

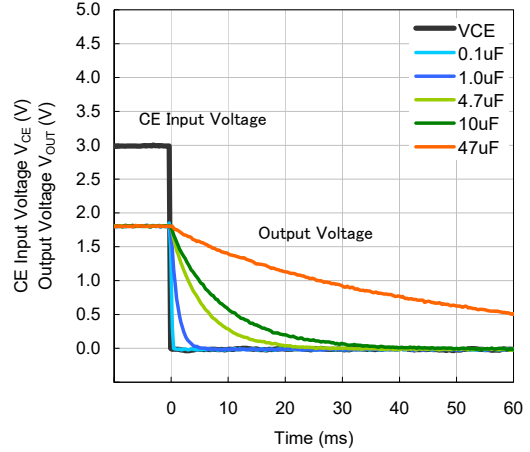


13) CE Transient Response ($T_a=25^\circ\text{C}$, $V_{IN}=14\text{V}$, $I_{OUT}=1\text{mA}$, $C_{OUT}=0.1\mu\text{F}$ to $47\mu\text{F}$)

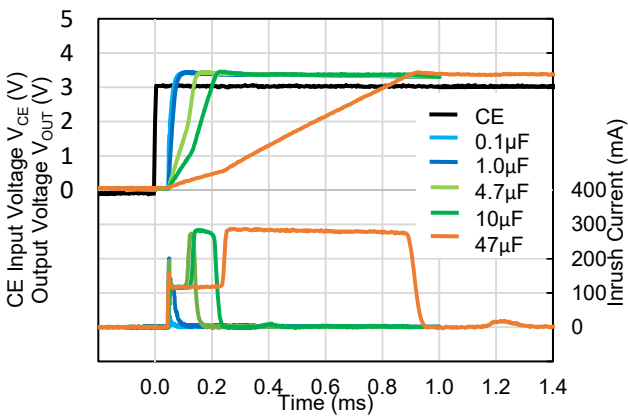
VR=1.8V, CE at rising



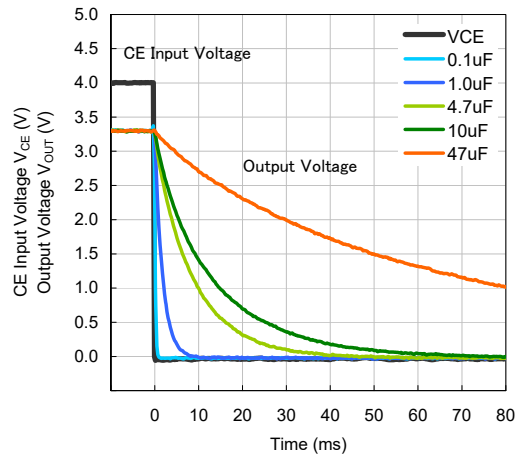
VR=1.8V, CE at falling



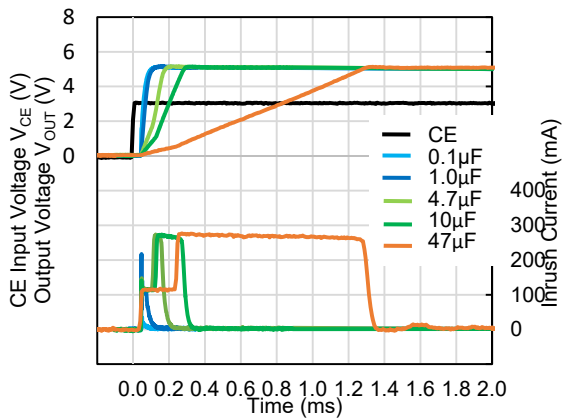
VR=3.3V, CE at rising



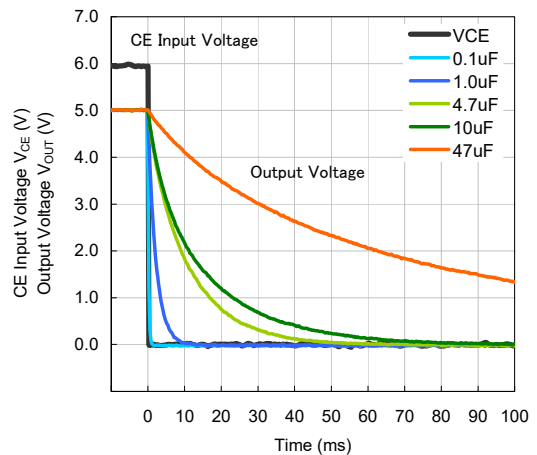
VR=3.3V, CE at falling

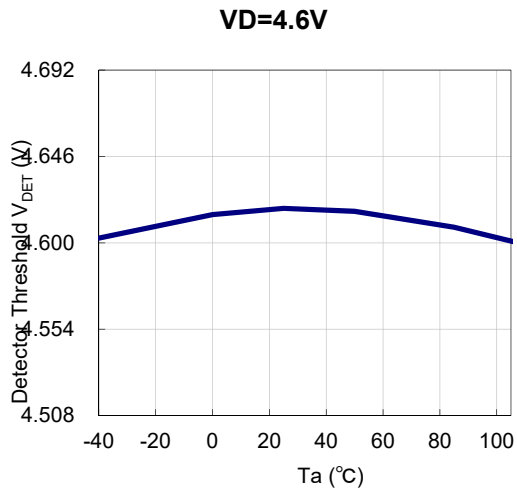
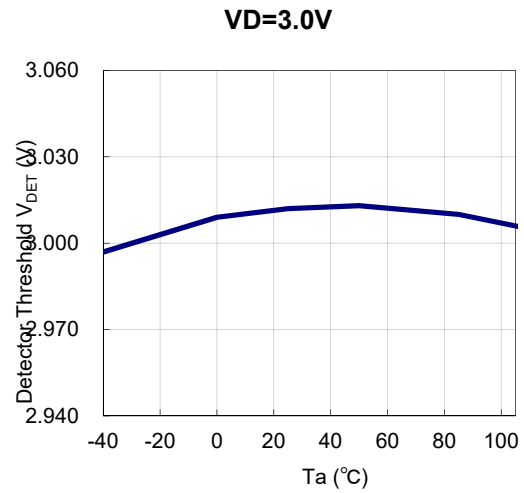
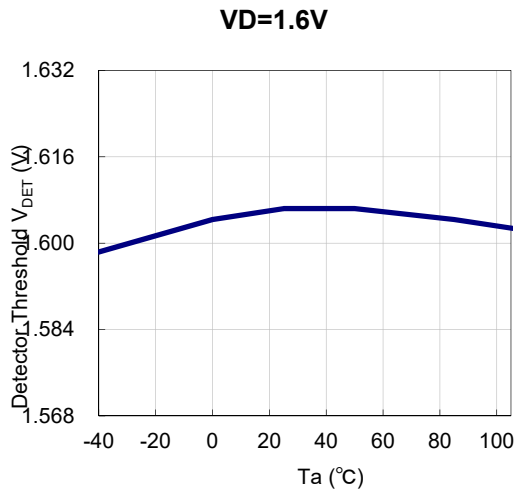
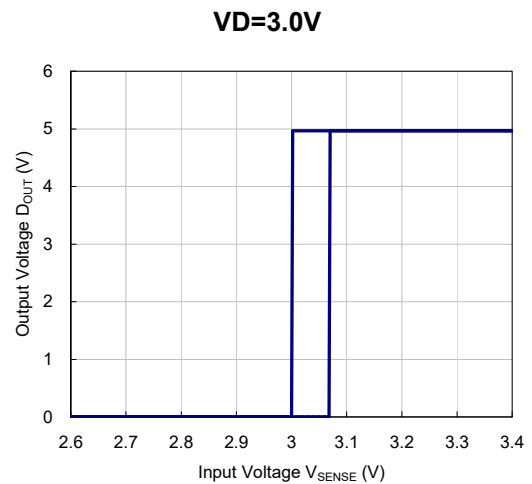
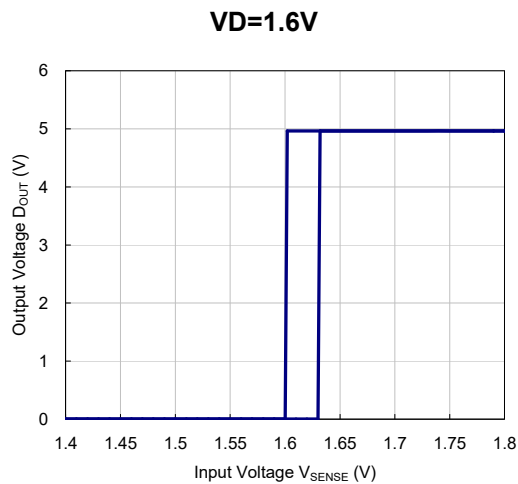


VR=5.0V, CE at rising

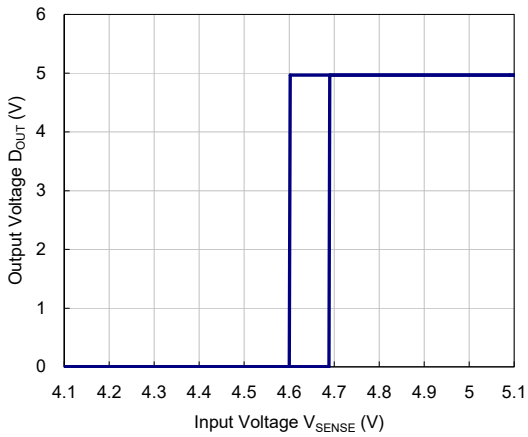


VR=5.0V, CE at falling

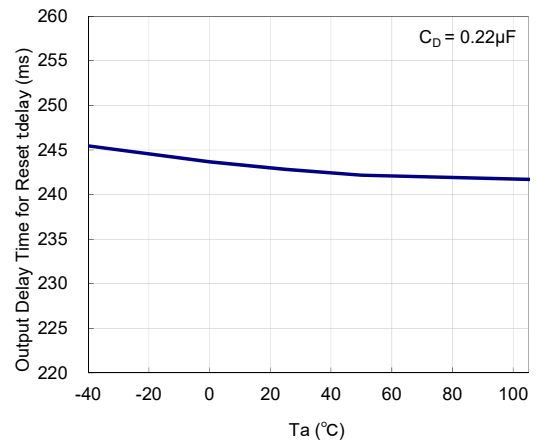
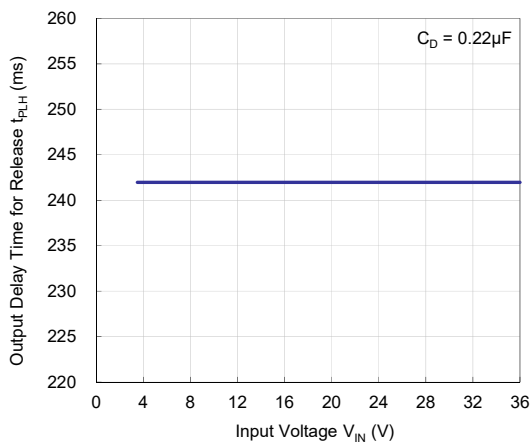


14) Detector Threshold vs. Temperature**15) D_{OUT} Pin Voltage vs. SENSE Pin Input Voltage (D_{OUT} pulled-up to 5V with 100kΩ)**

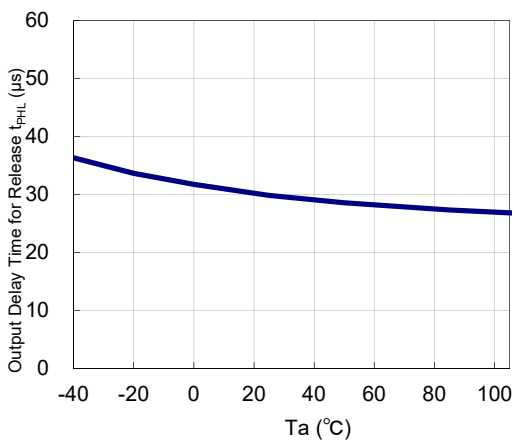
VD=4.6V



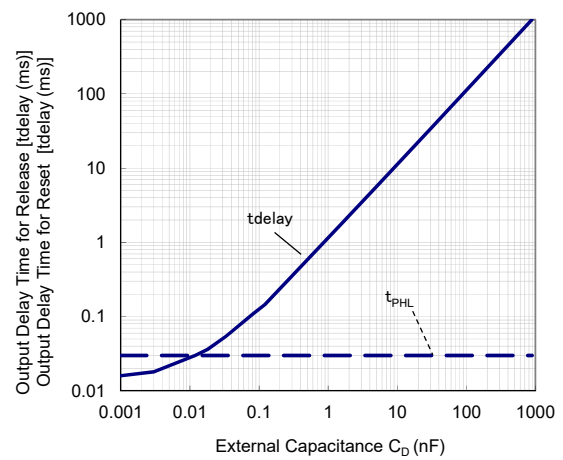
16) Release Output Delay Time vs. Input Voltage 17) Release Output Delay Time vs. Temperature



18) Detect Output Delay Time vs. Temperature



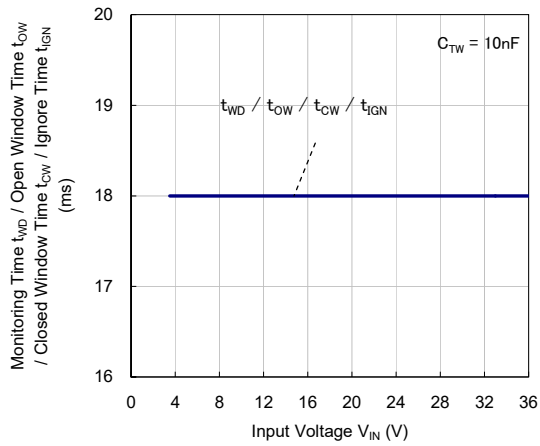
19) Release/ Detect Delay Time vs. External Capacitor for C_D Pin



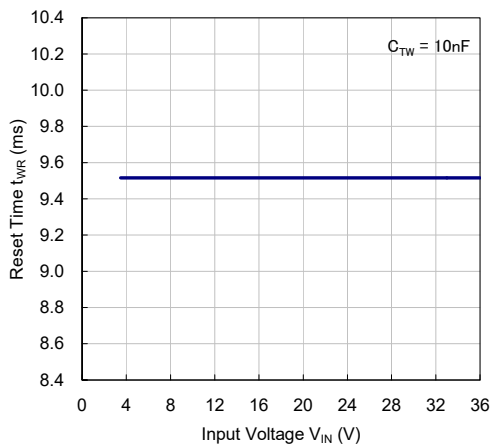
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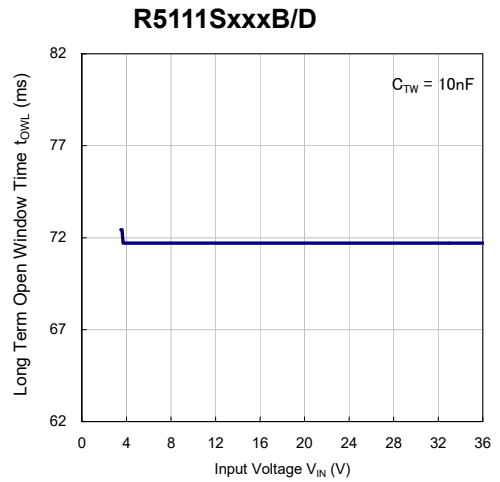
20) WDT t_{WD} / t_{OW} / t_{CW} / t_{IGN} vs. Input Voltage



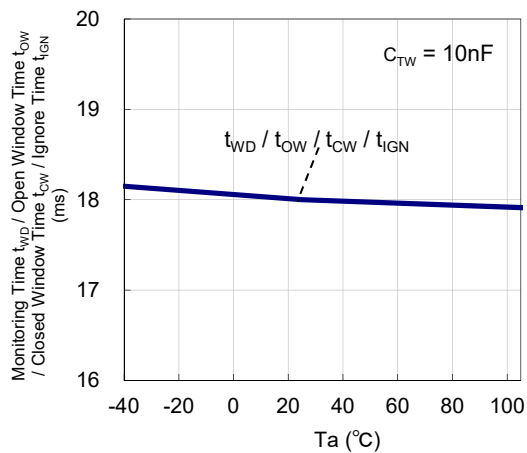
21) Reset Time vs. Input Voltage



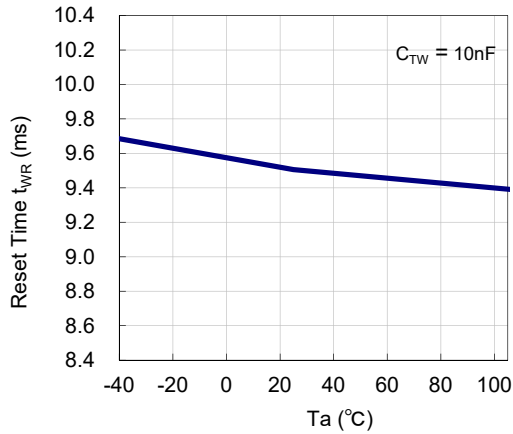
22) Long Open Window Time vs. Input Voltage



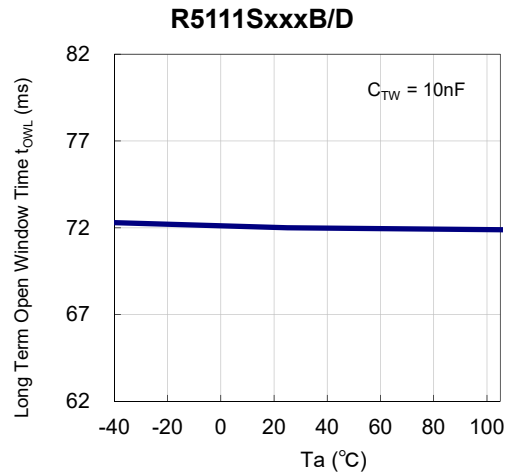
23) WDT t_{WD} / t_{OW} / t_{CW} / t_{IGN} vs. Temperature



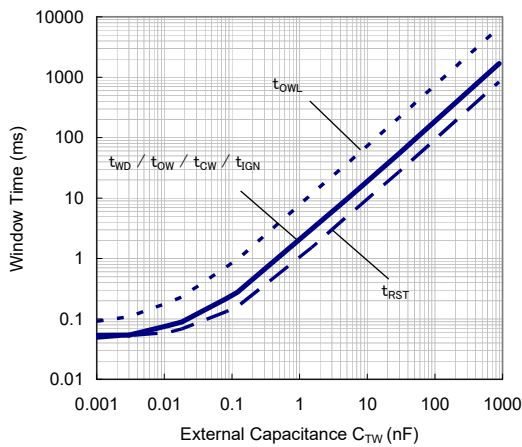
24) Reset Time vs. Temperature



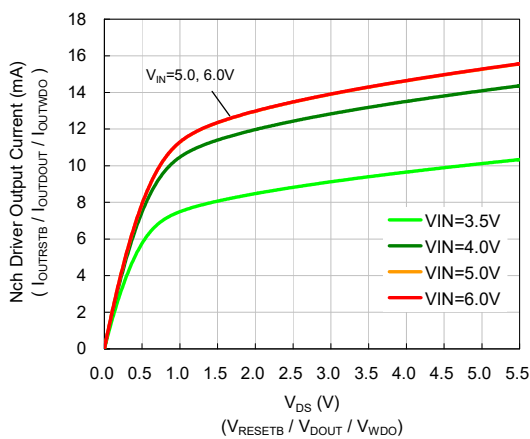
25) Long Open Window Time vs. Temperature



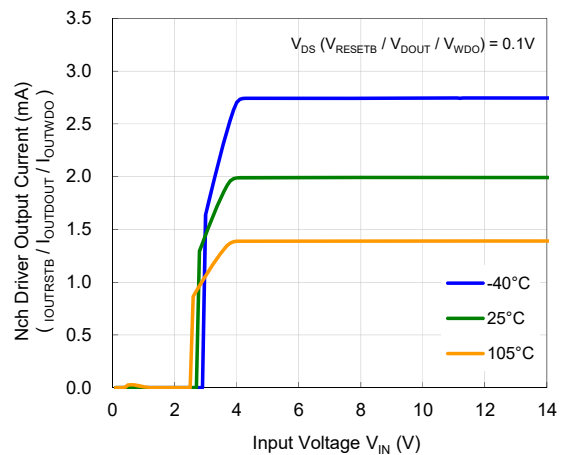
26) WDT t_WD / t_OW / t_CW / t_IGN / t_OWL / t_RST Vs. External Capacitor for C_TW Pin



27) Nch. Driver Output Current vs. V_DS



28) Nch. Driver Output Current vs. Input Voltage

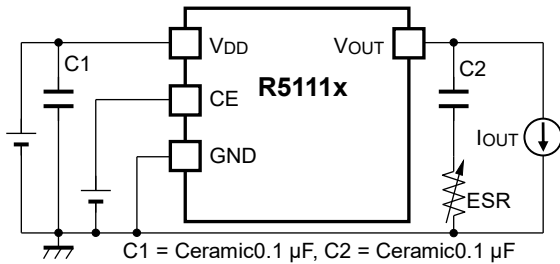


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ESR vs. Output Current

The IC is recommended to use a ceramic type capacitor, but the IC can be used other capacitors of the lower ESR type. The relation between the output current (I_{OUT}) and the ESR of output capacitor is shown below.



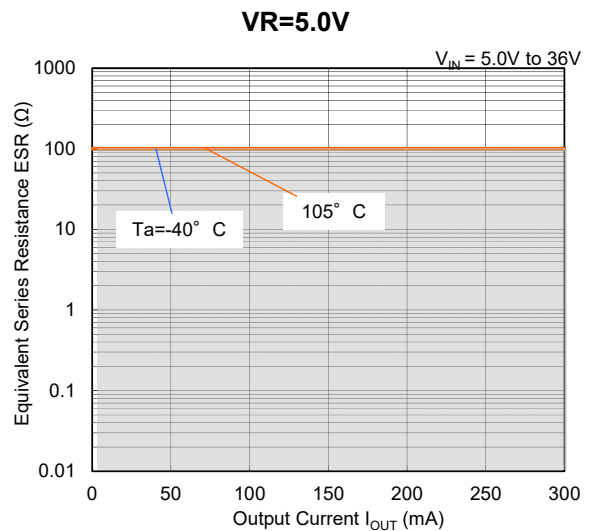
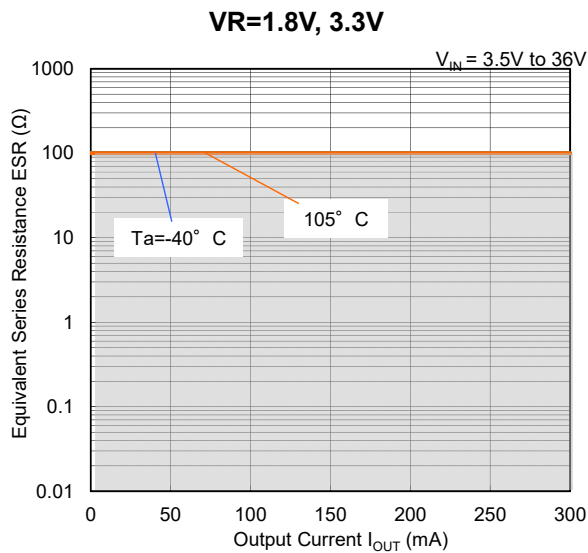
Measurement Conditions:

Frequency Band: 10 Hz to 2 MHz

Measurement Temperature: -40°C to 105°C

Hatched area: Noise level is 40 μ V (average) or below

Ceramic Capacitor: C1 = C2 = Ceramic 0.1 μ F



The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 21 pcs

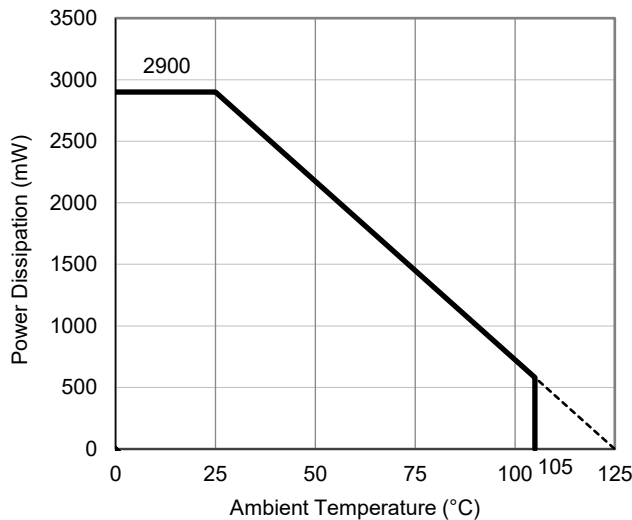
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

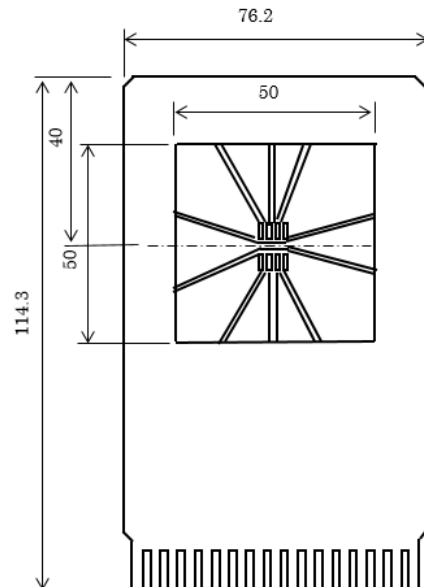
Item	Measurement Result
Power Dissipation	2900 mW
Thermal Resistance (θja)	θja = 34.5°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 10°C/W

θja: Junction-to-ambient thermal resistance.

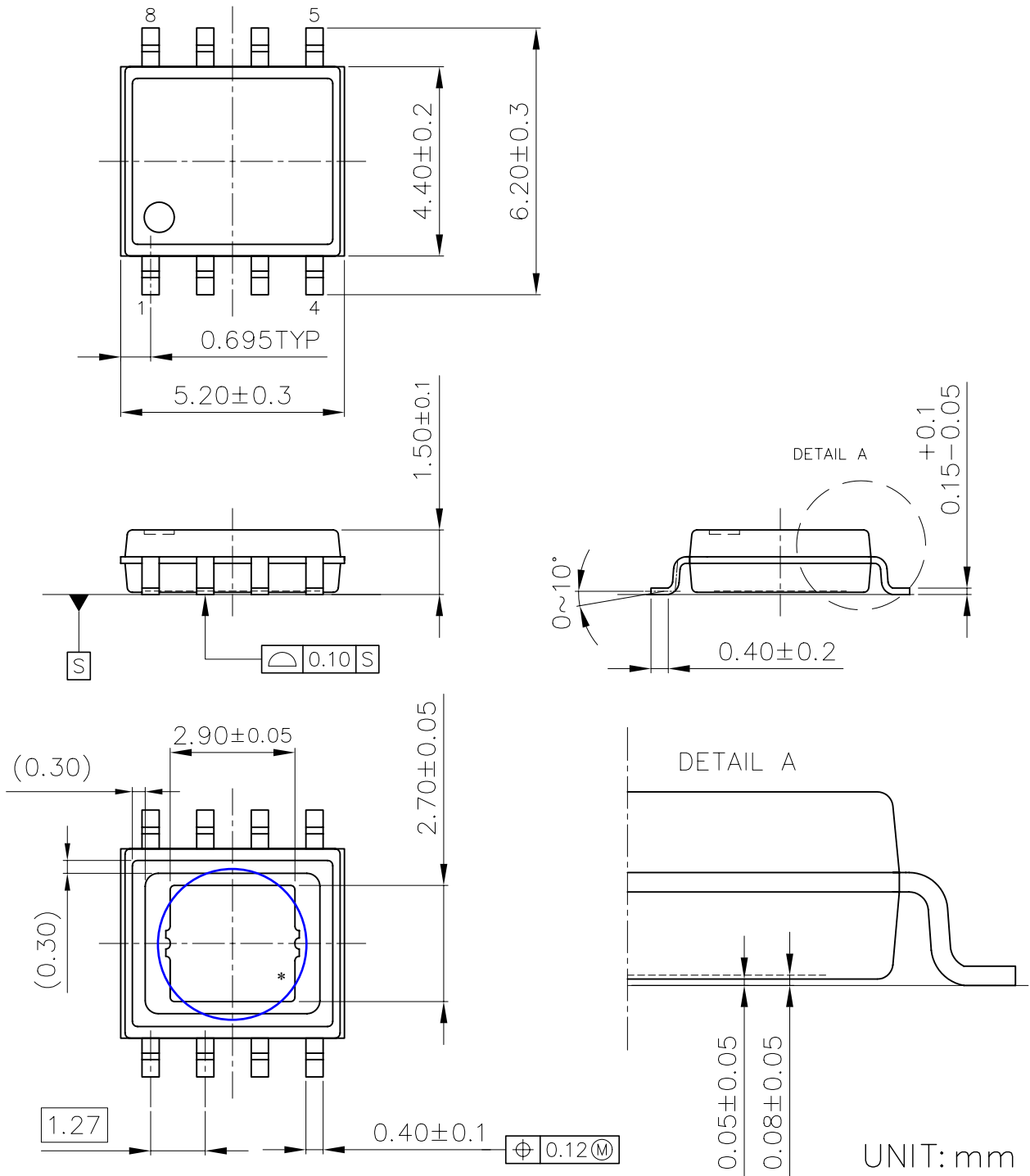
ψjt: Junction-to-top of package thermal characterization parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



HSOP-8E Package Dimensions

* The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board but it is possible to leave the tab floating.

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 21 pcs

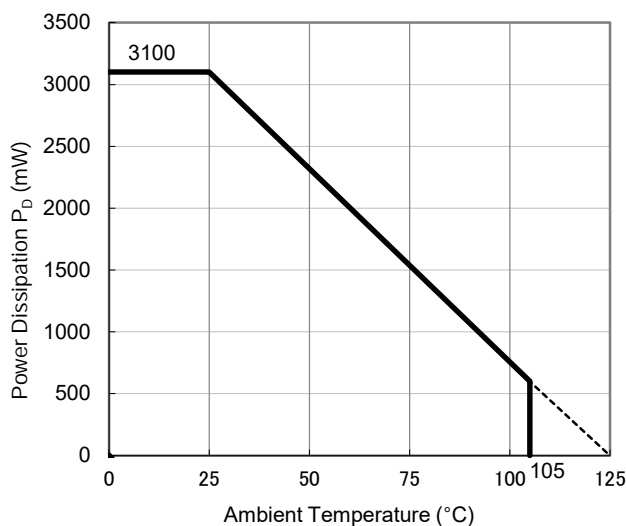
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

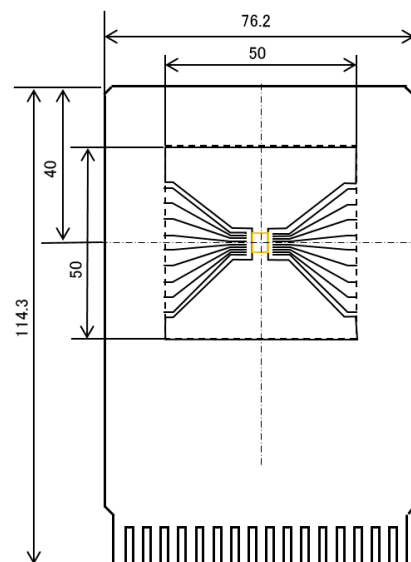
Item	Measurement Result
Power Dissipation	3100 mW
Thermal Resistance (θja)	θja = 32°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 8°C/W

θja: Junction-to-Ambient Thermal Resistance

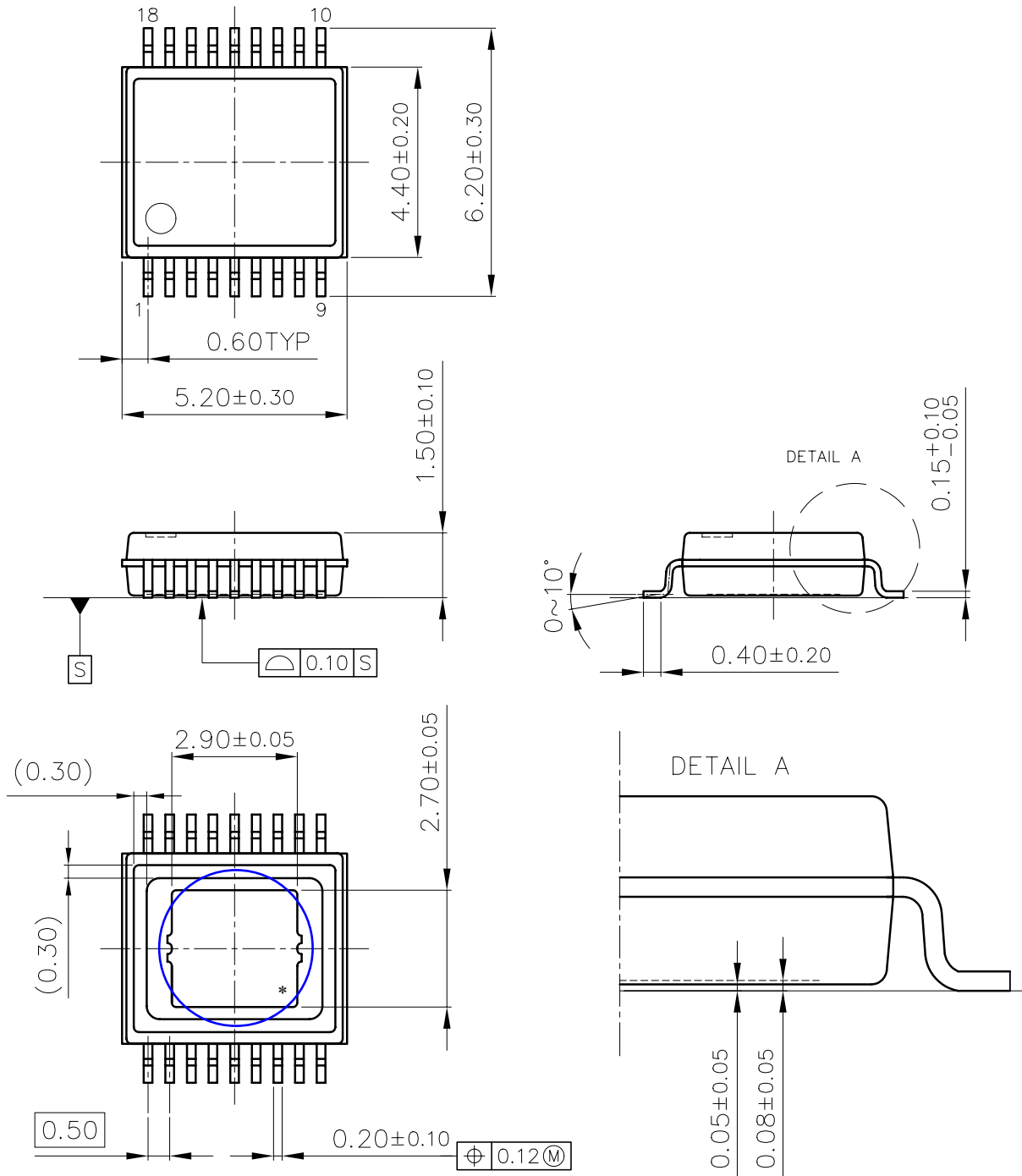
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



UNIT: mm

HSOP-18 Package Dimensions

* The tab on the bottom of the package shown by blue circle is substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board but it is possible to leave the tab floating.

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 72 pcs

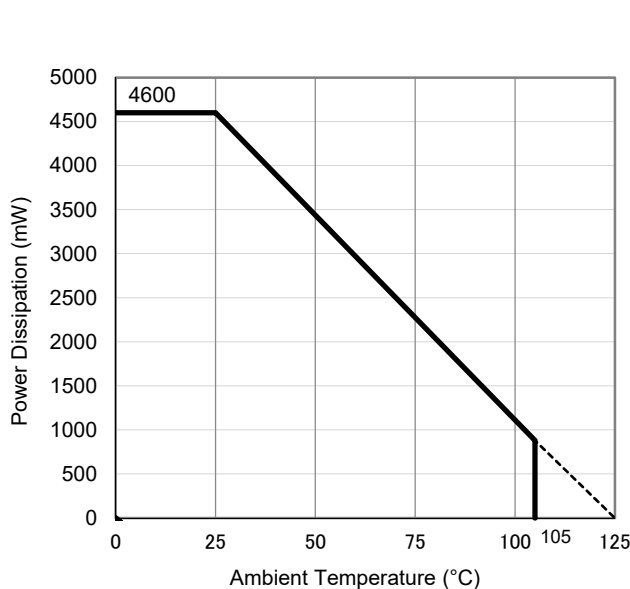
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

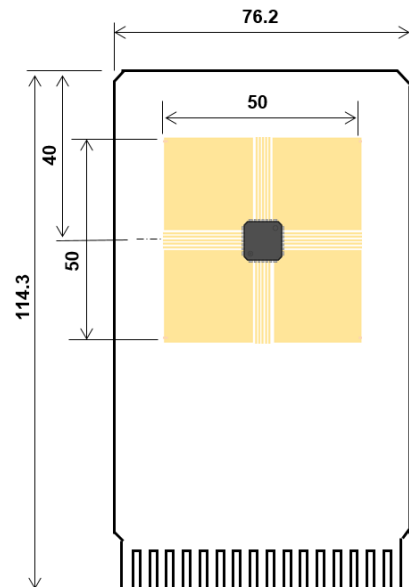
Item	Measurement Result
Power Dissipation	4600 mW
Thermal Resistance (θ_{ja})	$\theta_{ja} = 21.5^\circ\text{C/W}$
Thermal Characterization Parameter (ψ_{jt})	$\psi_{jt} = 5^\circ\text{C/W}$

θ_{ja} : Junction-to-ambient thermal resistance.

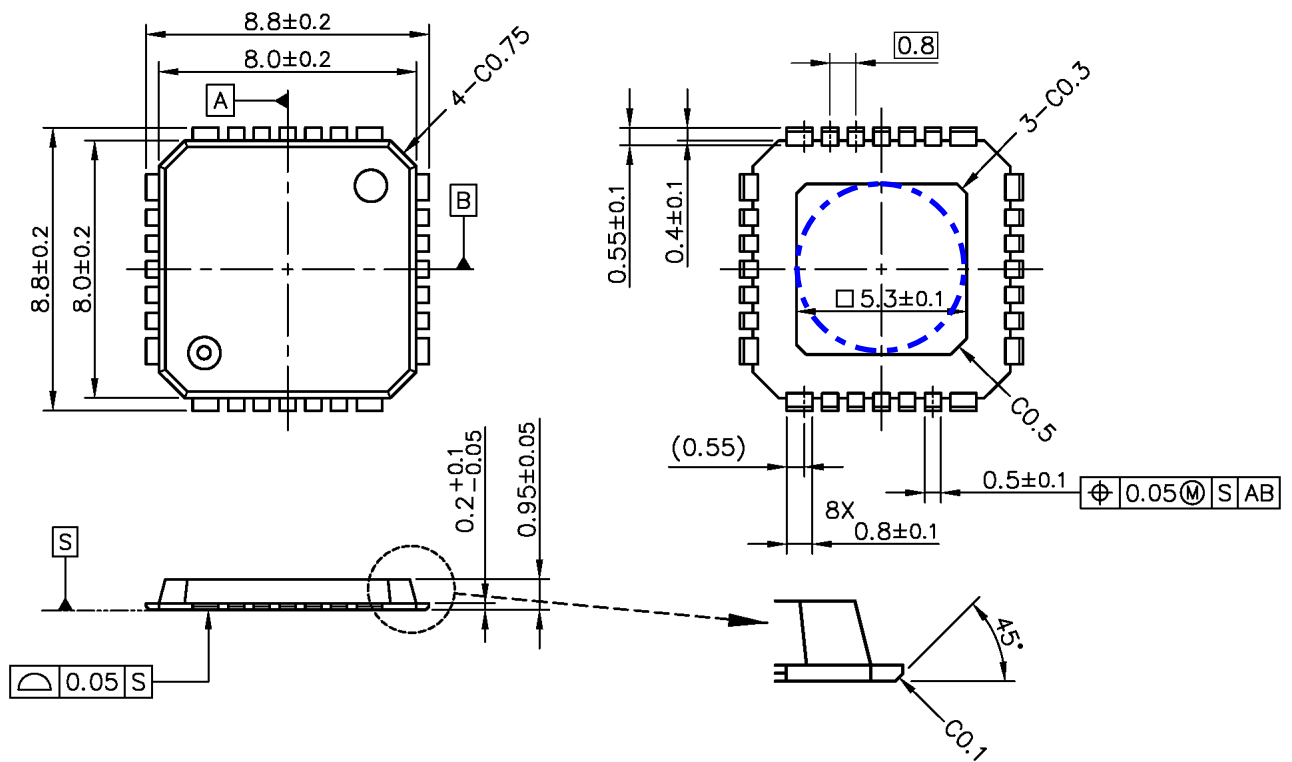
ψ_{jt} : Junction-to-top of package thermal characterization parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



UNIT: mm

HQFN0808-28 Package Dimensions

*The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane pin on the board but it is possible to leave the tab floating.



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Official website

<https://www.nisshinbo-microdevices.co.jp/en/>

Purchase information

<https://www.nisshinbo-microdevices.co.jp/en/buy/>

