GaAs, pHEMT, MMIC, Low Noise Amplifier, 0.025 GHz to 12 GHz

FEATURES

- Low noise figure: 2.5 dB typical at 0.025 GHz to 10 GHz
- Single positive supply (self biased)
- High gain: 16.5 dB typical at 0.025 GHz to 10 GHz
- High OIP3: 36 dBm typical at 0.025 GHz to 10 GHz
- RoHS-compliant, 2 mm × 2 mm, 6-lead LFCSP

APPLICATIONS

- Test instrumentation
- Military communications
- Military radar
- Telecommunications

GENERAL DESCRIPTION

The ADL8121 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise wideband amplifier that operates from 0.025 GHz to 12 GHz.

The ADL8121 provides a typical gain of 16.5 dB, a 2.5 dB typical noise figure, and a typical output third-order intercept (OIP3) of 36 dBm across the 0.025 GHz to 10 GHz frequency range, requiring only 95 mA from a 5 V supply voltage. The saturated output power (P_{SAT}) of 21.5 dBm typical across the 0.025 GHz to 10 GHz frequency range enables the low noise amplifier (LNA) to function as a local oscillator (LO) driver for many of Analog Devices, Inc., balanced, in-phase and quadrature (I/Q) or image rejection mixers.

The ADL8121 also features inputs and outputs that are internally matched to 50 Ω, making the device ideal for surface-mounted technology (SMT)-based and is housed in a RoHS-compliant, 2 mm × 2 mm, 6-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

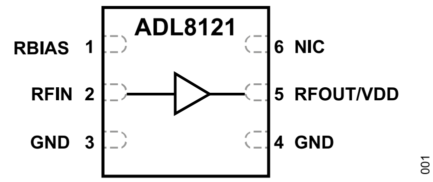

Figure 1.

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REVISION HISTORY

4/2022—Revision 0: Initial Version

SPECIFICATIONS

0.025 GHz TO 10 GHz FREQUENCY RANGE

Supply voltage (V_{DD}) = 5 V, supply current (I_{DQ}) = 95 mA, bias resistance (R_{BIAS}) = 324 Ω, and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.025		10	GHz	
GAIN	14.5	16.5		dB	
Gain Variation over Temperature		0.006		dB/°C	
NOISE FIGURE		2.5		dB	
RETURN LOSS					
Input (S11)		12		dB	
Output (S22)		14		dB	
OUTPUT					
Power for 1 dB Compression (OP1dB)	18.5	21		dBm	
P_{SAT}		21.5		dBm	
OIP3		36		dBm	Measurement taken at output power (P_{OUT}) per tone = 5 dBm
Second-Order Intercept (OIP2)		40		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
POWER ADDED EFFICIENCY (PAE)		27		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		95		mA	
Drain Current (I_{DQ_AMP})		90		mA	
R_{BIAS} Current (I_{RBIAS})		5		mA	
V_{DD}	2	5	6	V	

10 GHz TO 12 GHz FREQUENCY RANGE

V_{DD} = 5 V, I_{DQ} = 95 mA, R_{BIAS}= 324 Ω, and T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	10		12	GHz	
GAIN	15	17		dB	
Gain Variation over Temperature		0.006		dB/°C	
NOISE FIGURE		3.5		dB	
RETURN LOSS					
S11		11		dB	
S22		15		dB	
OUTPUT					
OP1dB	14.5	17		dBm	
P_{SAT}		19.5		dBm	
OIP3		34		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
OIP2		45		dBm	Measurement taken at P_{OUT} per tone = 5 dBm
PAE		17		%	Measured at P_{SAT}
SUPPLY					
I_{DQ}		95		mA	
I_{DQ_AMP}		90		mA	
I_{RBIAS}		5		mA	
V_{DD}	2	5	6	V	

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{DD}	7 V
RFIN Power	32 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 13.9 mW/°C Above 85°C)	1.25 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Nominal Junction (T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 95 mA)	119.2°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JC} is the channel-to-case thermal resistance (channel to exposed metal ground pad on the underside of the device).

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-6-12	72	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

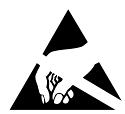
Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8121

Table 5. ADL8121, 6-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±500	1B

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

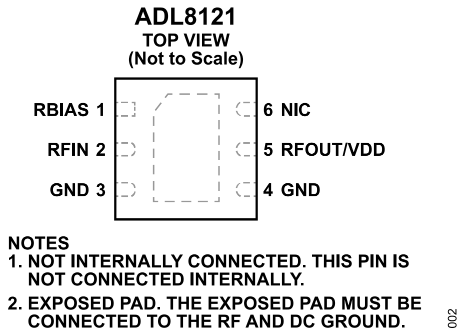


Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor Between RBIAS and VDD to set quiescent drain current. See Figure 3 for the interface schematic.
2	RFIN	RF Input. The RFIN pin is dc-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
3, 4	GND	Ground. This pin must be connected to the RF and dc ground. See Figure 6 for the interface schematic.
5	RFOUT/VDD	RF Output/Drain Bias for the Amplifier. RFOUT/VDD is dc-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
6	NIC	Not Internally Connected. This pin is not connected internally.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and dc ground.

INTERFACE SCHEMATICS

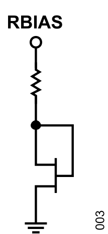


Figure 3. RBIAS Interface Schematic

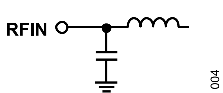


Figure 4. RFIN Interface Schematic

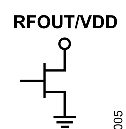


Figure 5. RFOUT/VDD Interface Schematic

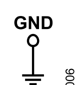


Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

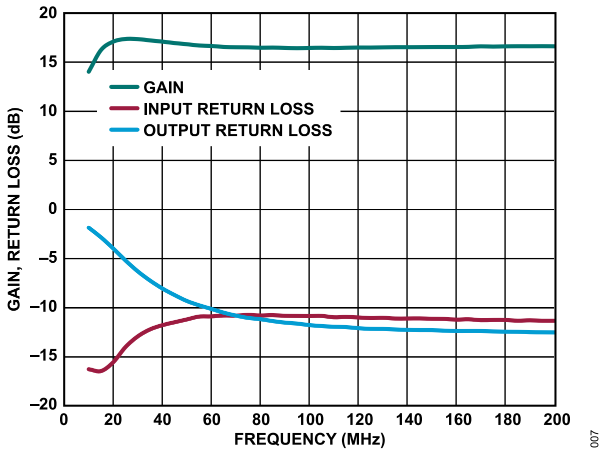


Figure 7. Gain and Return Loss vs. Frequency, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

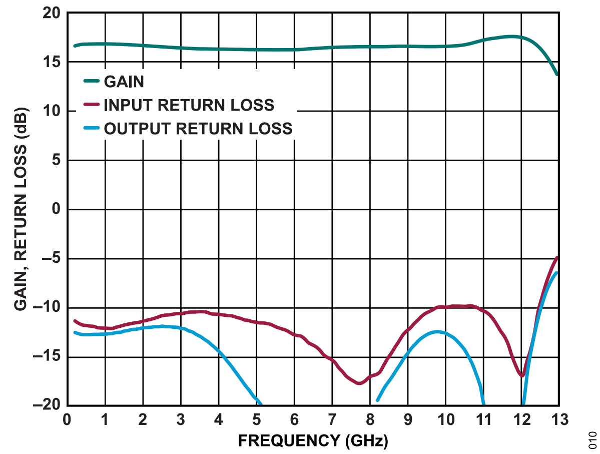


Figure 10. Gain and Return Loss vs. Frequency, 200 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

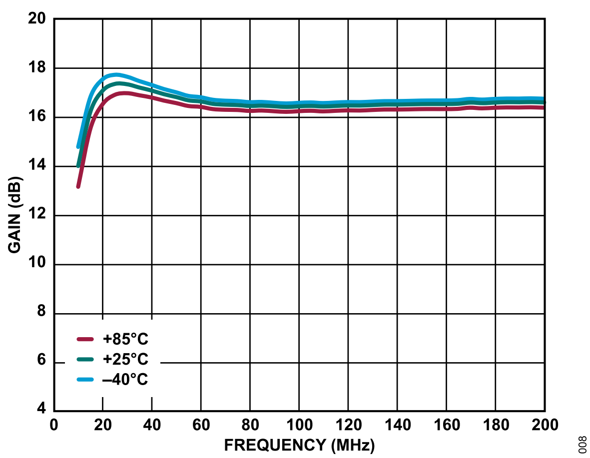


Figure 8. Gain vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

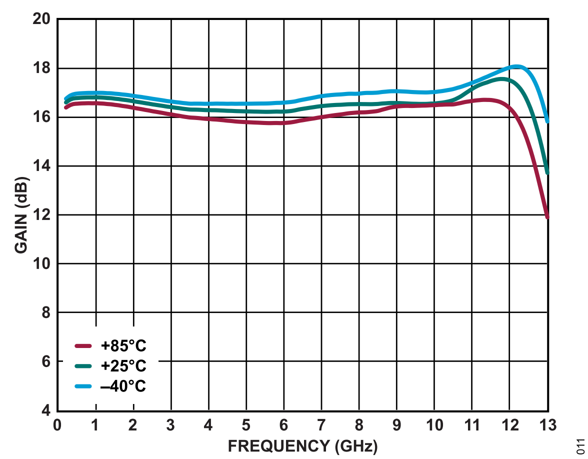


Figure 11. Gain vs. Frequency for Various Temperatures, 200 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

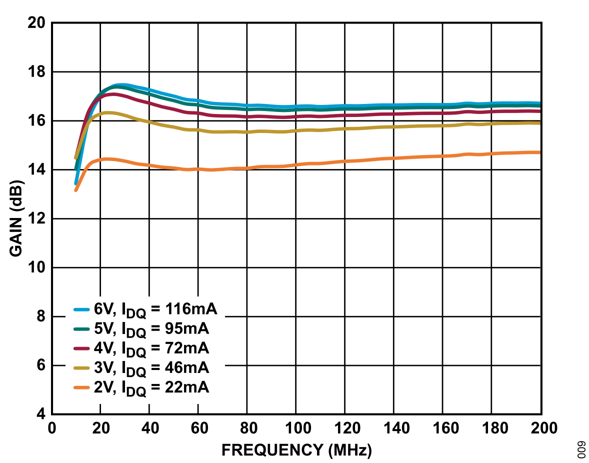


Figure 9. Gain vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 200 MHz, R_{BIAS} = 324 Ω

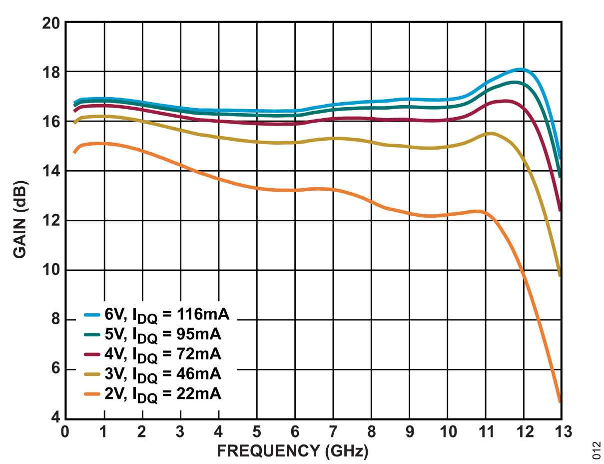


Figure 12. Gain vs. Frequency for Various Supply Voltages and I_{DQ} Values, 200 MHz to 13 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

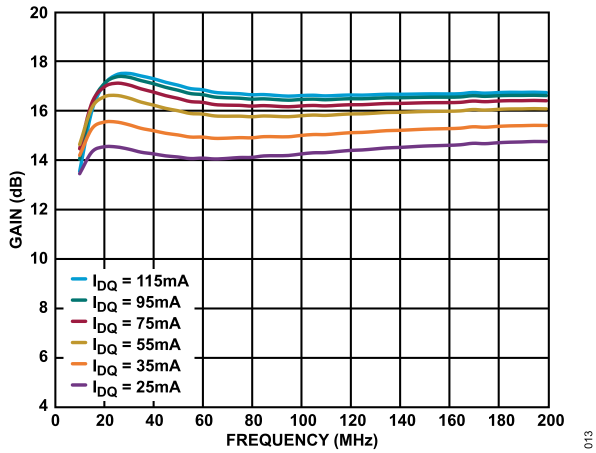


Figure 13. Gain vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

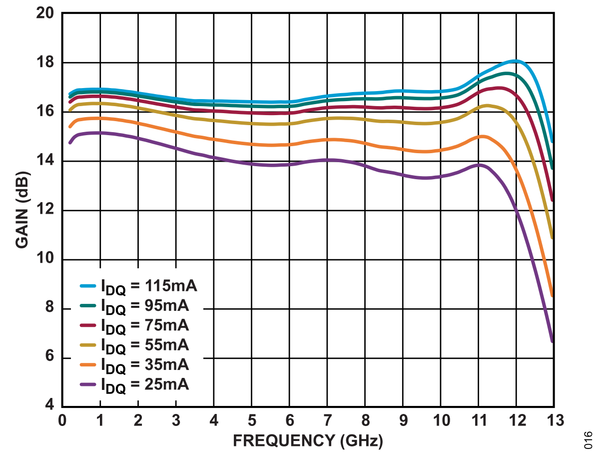


Figure 16. Gain vs. Frequency for Various I_{DQ} Values, 200 MHz to 13 GHz, V_{DD} = 5 V

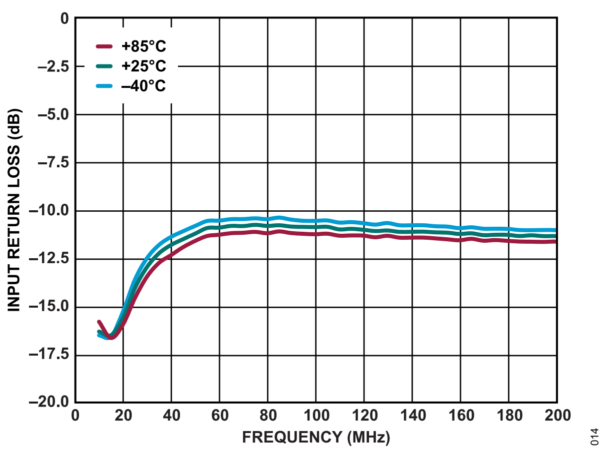


Figure 14. Input Return Loss vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

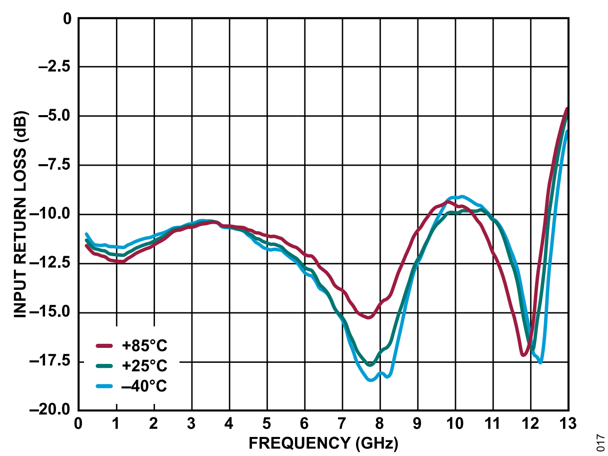


Figure 17. Input Return Loss vs. Frequency for Various Temperatures, 200 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

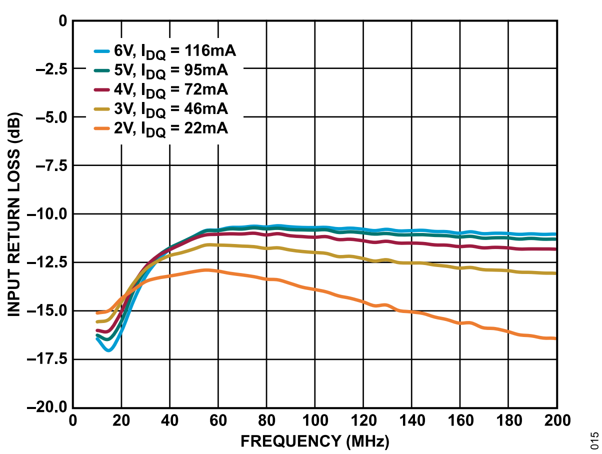


Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 200 MHz, R_{BIAS} = 324 Ω

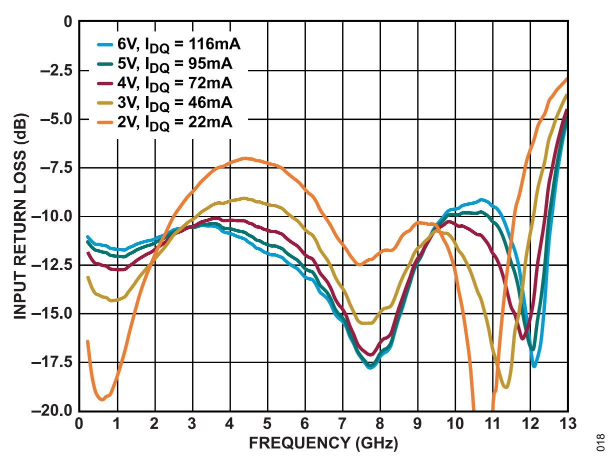


Figure 18. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, 200 MHz to 13 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

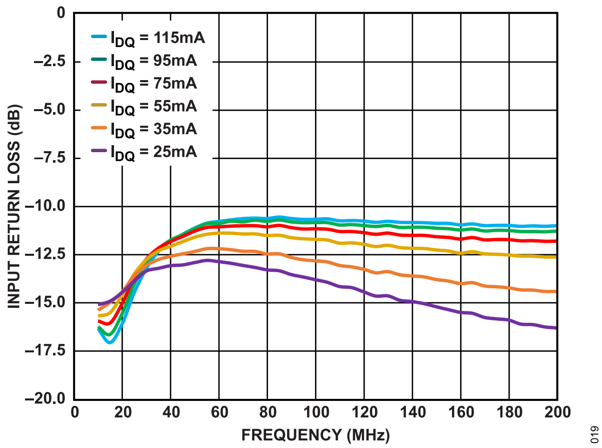


Figure 19. Input Return Loss vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

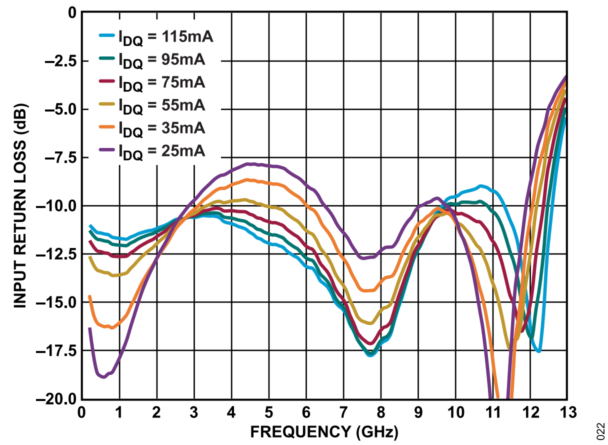


Figure 22. Input Return Loss vs. Frequency for Various I_{DQ} Values, 200 MHz to 13 GHz, V_{DD} = 5 V

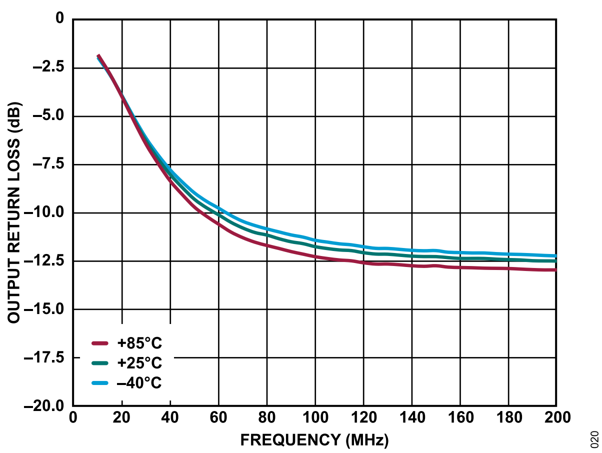


Figure 20. Output Return Loss vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

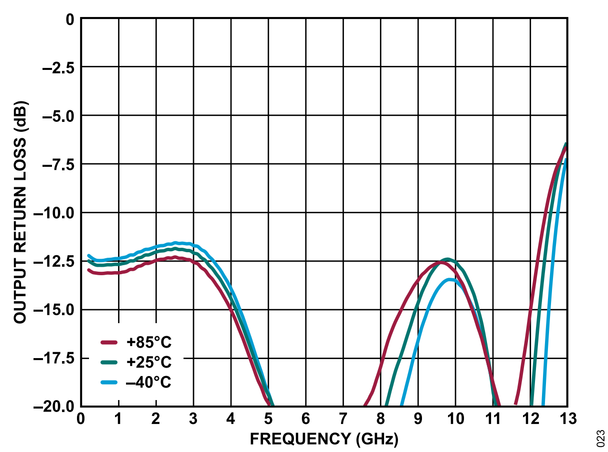


Figure 23. Output Return Loss vs. Frequency for Various Temperatures, 200 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

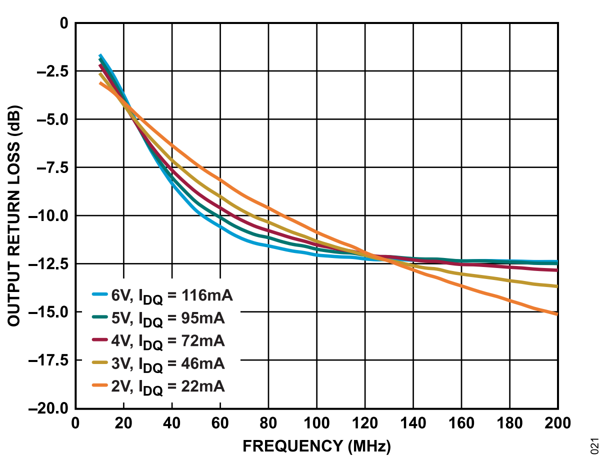


Figure 21. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 200 MHz, R_{BIAS} = 324 Ω

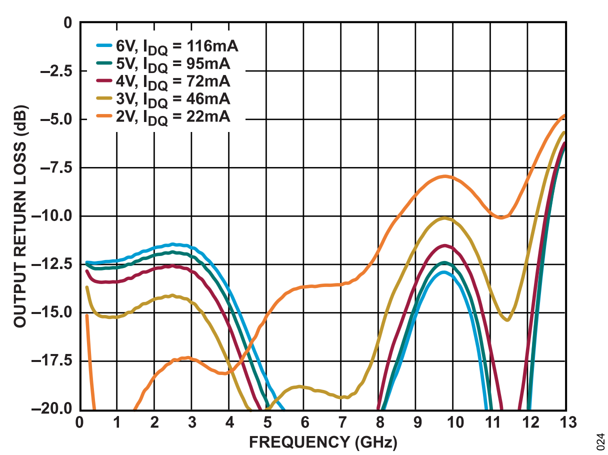


Figure 24. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ} Values, 200 MHz to 13 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

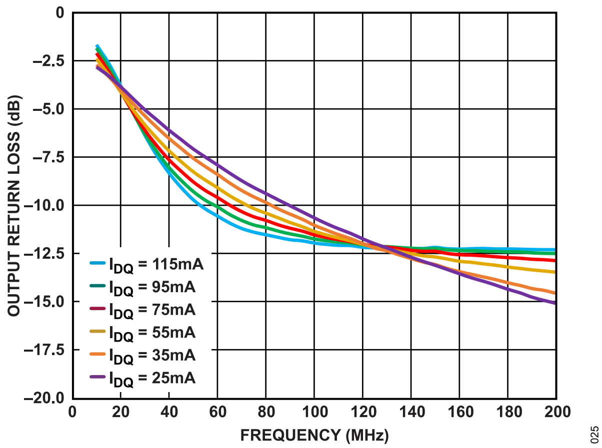


Figure 25. Output Return Loss vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

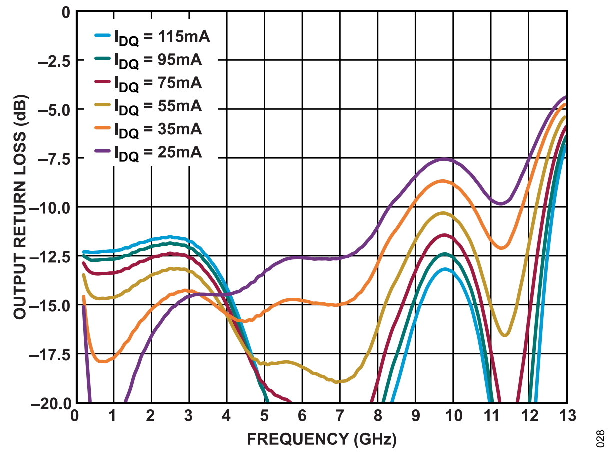


Figure 28. Output Return Loss vs. Frequency for Various I_{DQ} Values, 200 MHz to 13 GHz, V_{DD} = 5 V

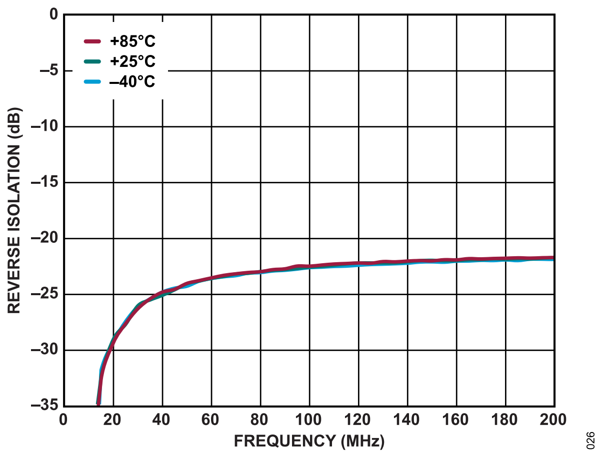


Figure 26. Reverse Isolation vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

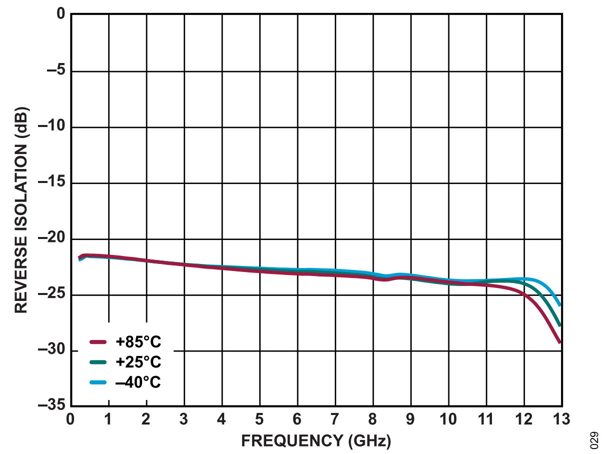


Figure 29. Reverse Isolation vs. Frequency for Various Temperatures, 200 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

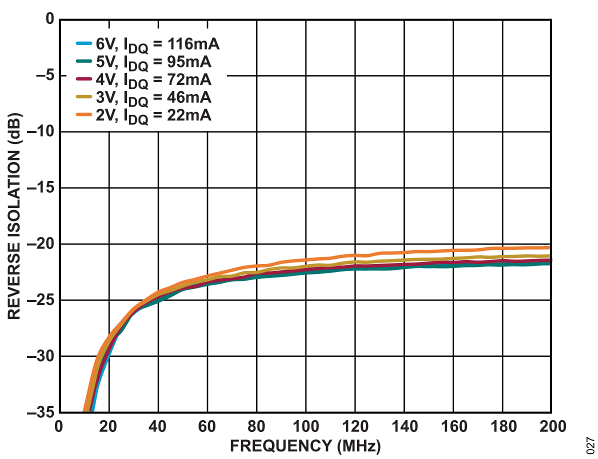


Figure 27. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 200 MHz, R_{BIAS}= 324 Ω

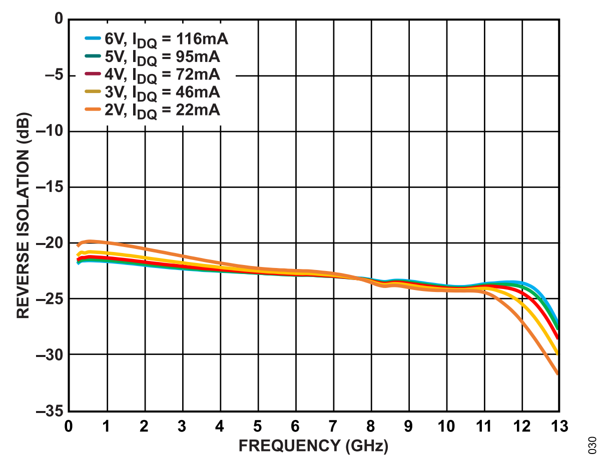


Figure 30. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ} Values, 200 MHz to 13 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

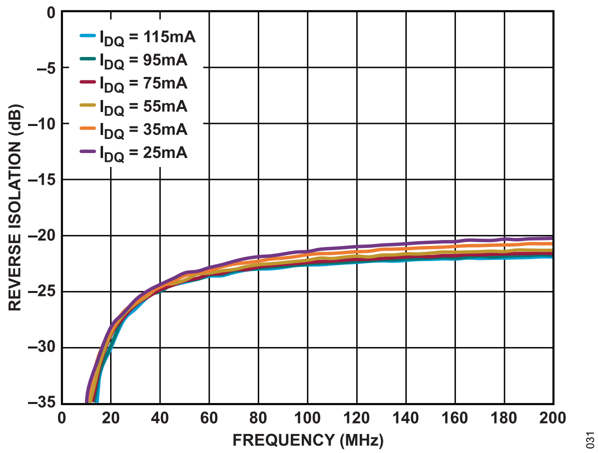


Figure 31. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

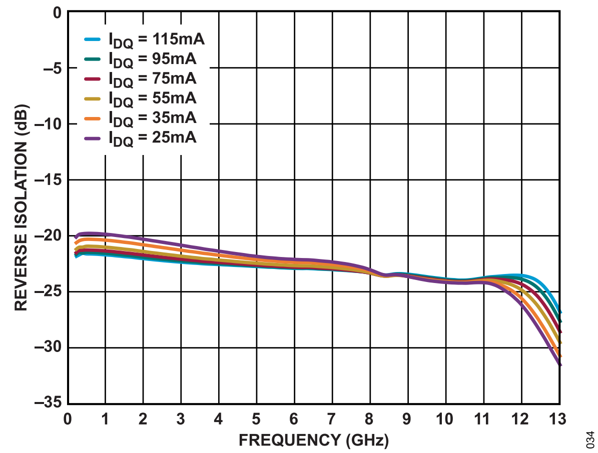


Figure 34. Reverse Isolation vs. Frequency for Various I_{DQ} Values, 200 MHz to 13 GHz, V_{DD} = 5 V

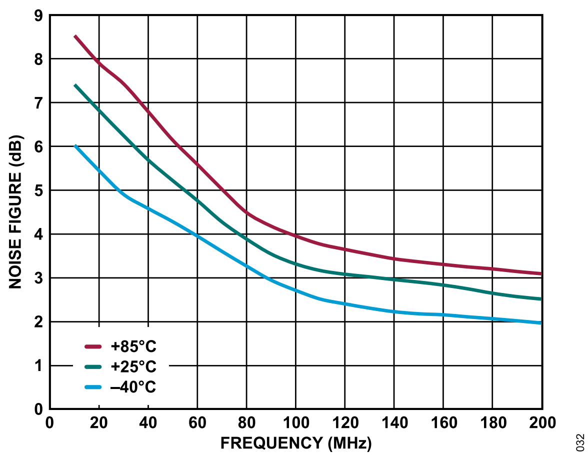


Figure 32. Noise Figure vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

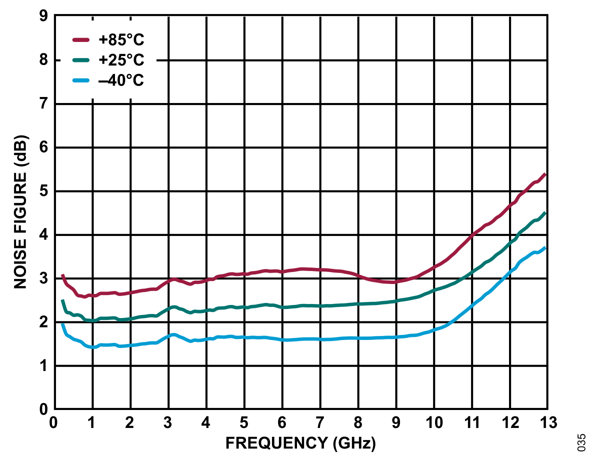


Figure 35. Noise Figure vs. Frequency for Various Temperatures, 200 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

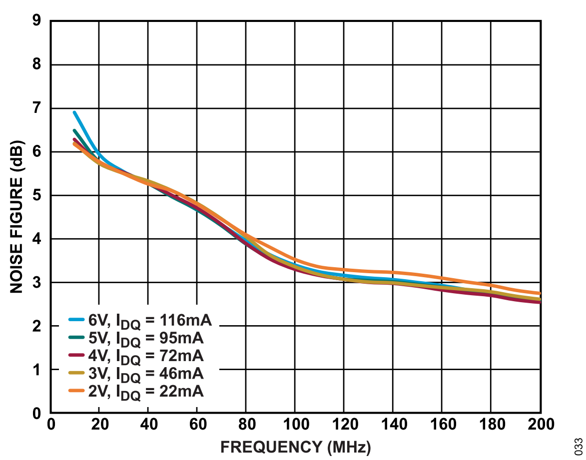


Figure 33. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 200 MHz, R_{BIAS} = 324 Ω

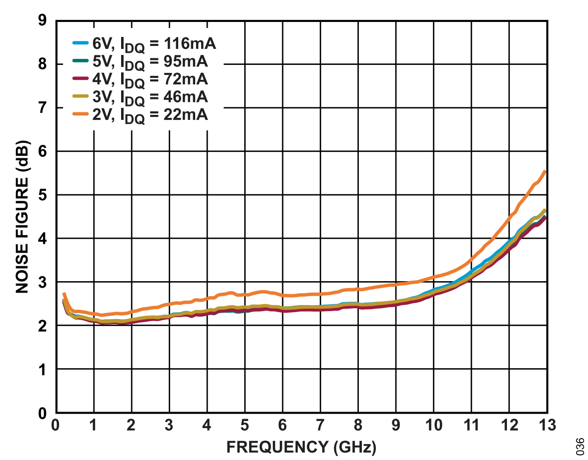


Figure 36. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ} Values, 200 MHz to 13 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

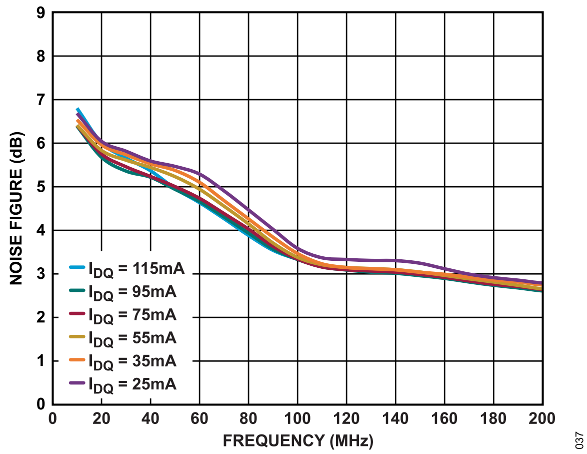


Figure 37. Noise Figure vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

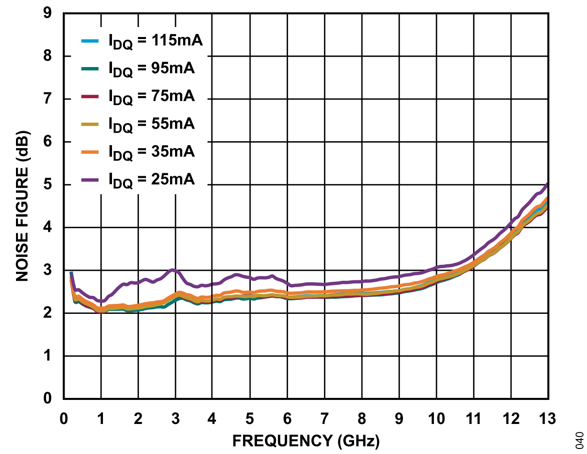


Figure 40. Noise Figure vs. Frequency for Various I_{DQ} Values, 200 MHz to 13 GHz, V_{DD} = 5 V

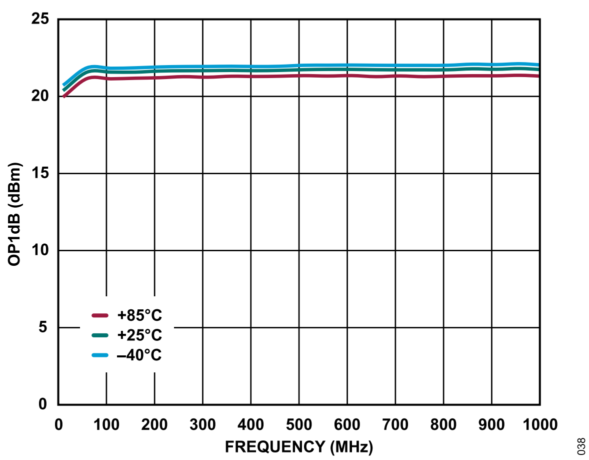


Figure 38. OP1dB vs. Frequency for Various Temperatures, 10 MHz to 1000 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

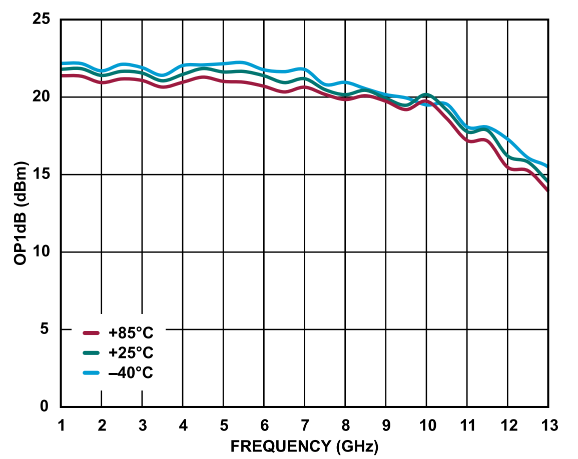


Figure 41. OP1dB vs. Frequency for Various Temperatures, 1 GHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

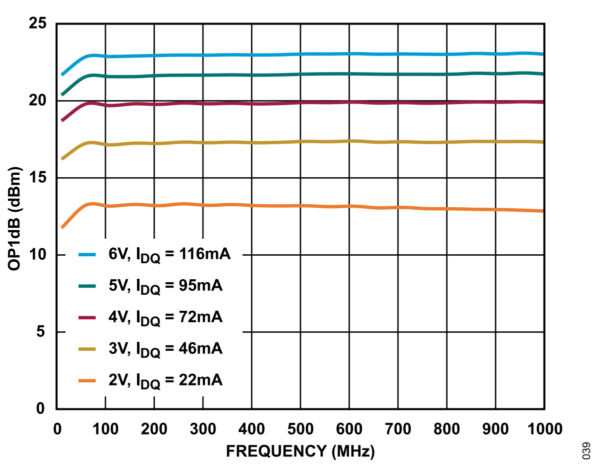


Figure 39. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1000 MHz, R_{BIAS} = 324 Ω

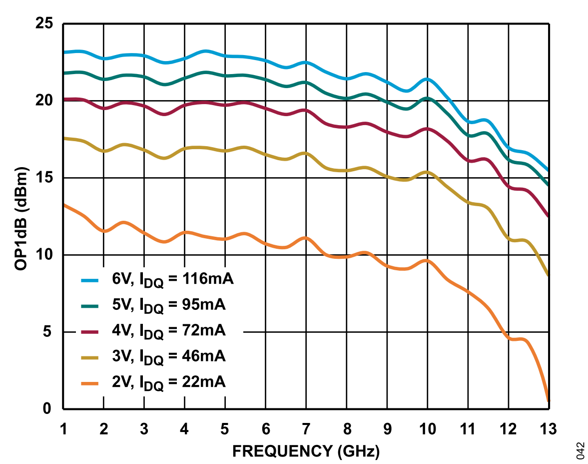


Figure 42. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 13 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

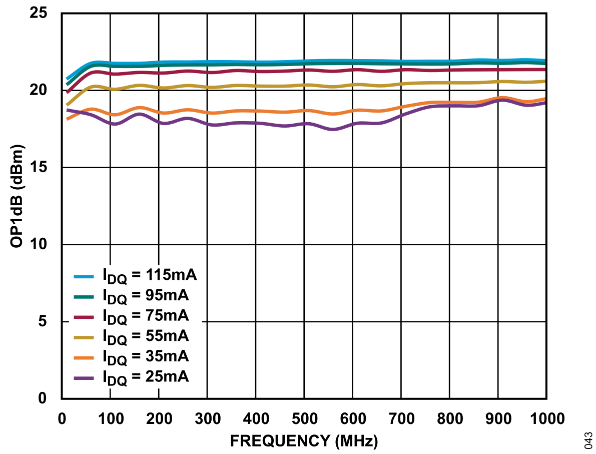


Figure 43. OP1dB vs. Frequency for Various I_{DQ} Values, 10 MHz to 1000 MHz, V_{DD} = 5 V

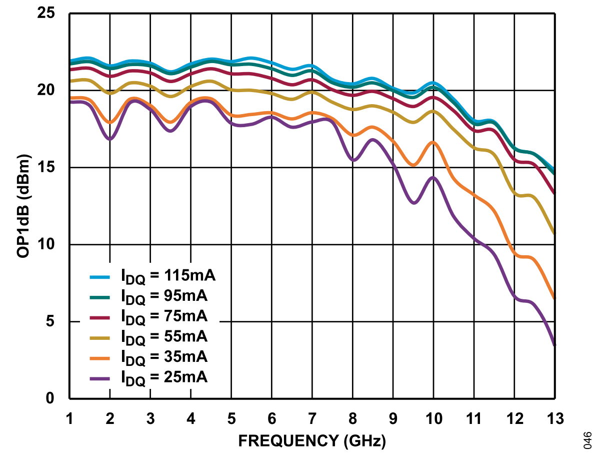


Figure 46. OP1dB vs. Frequency for Various I_{DQ} Values, 1 GHz to 13 GHz, V_{DD} = 5 V

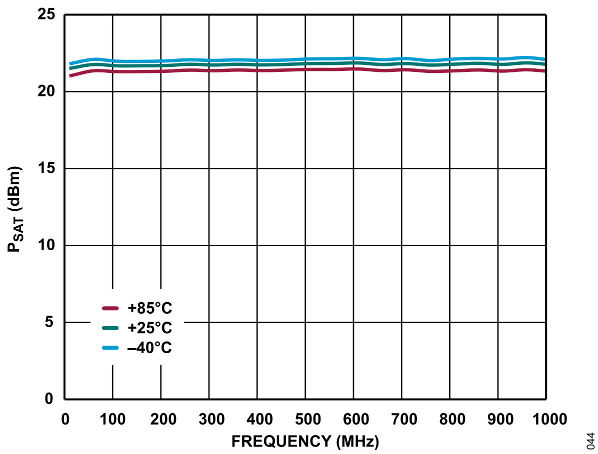


Figure 44. P_{SAT} vs. Frequency for Various Temperatures, 10 MHz to 1000 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

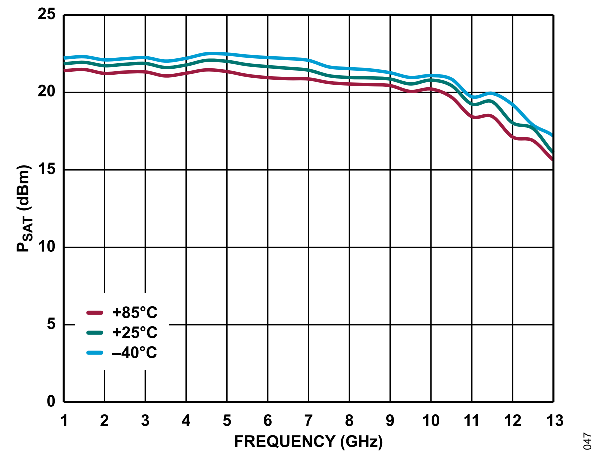


Figure 47. P_{SAT} vs. Frequency for Various Temperatures, 1 GHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

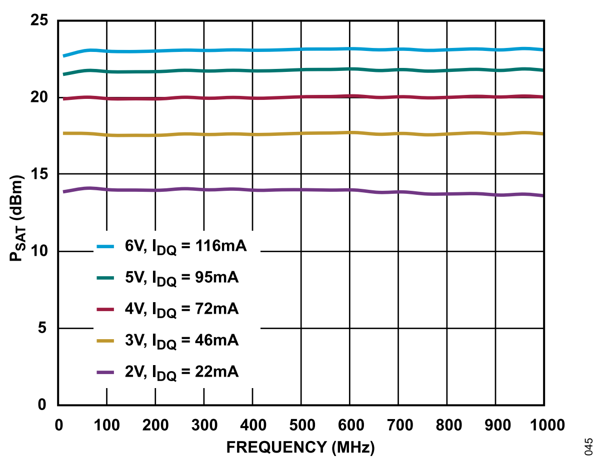


Figure 45. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 1000 MHz, R_{BIAS}= 324 Ω

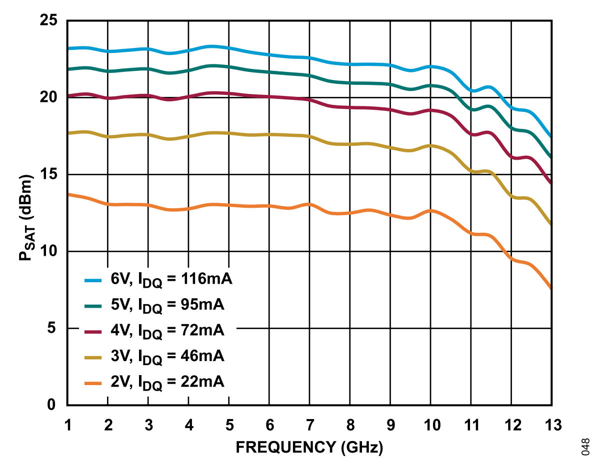


Figure 48. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ} Values, 1 GHz to 13 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

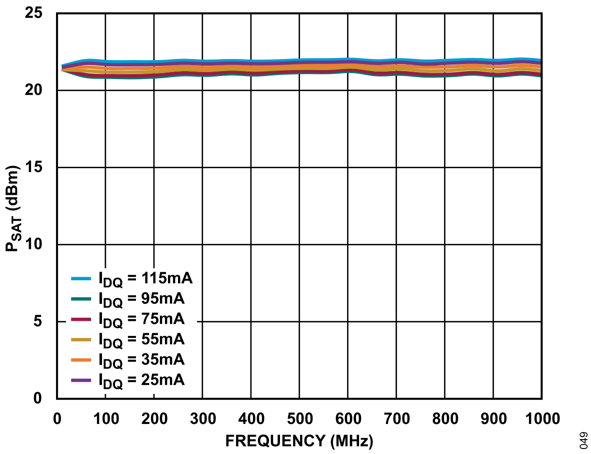


Figure 49. P_{SAT} vs. Frequency for Various I_{DQ} Values, 10 MHz to 1000 MHz, V_{DD} = 5 V

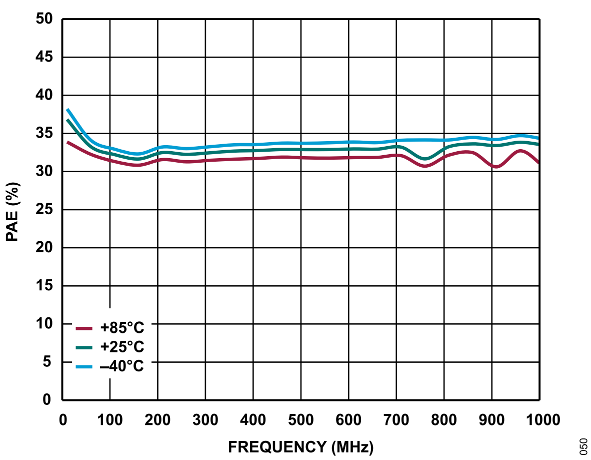


Figure 50. PAE vs. Frequency for Various Temperatures, 10 MHz to 1000 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

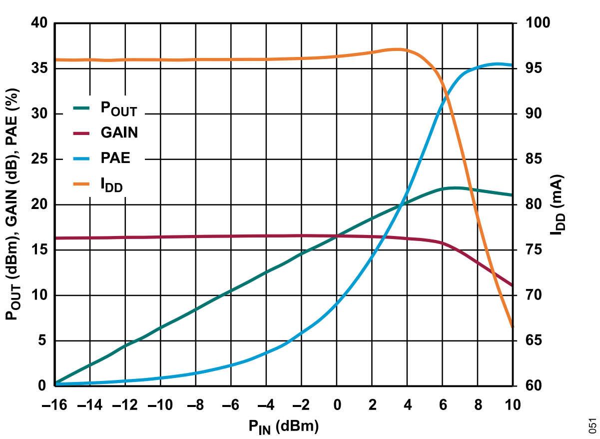


Figure 51. P_{OUT}, Gain, PAE, and Drain Current (I_{DD}) vs. Input Power (P_{IN}) at 1 GHz, R_{BIAS} = 324 Ω

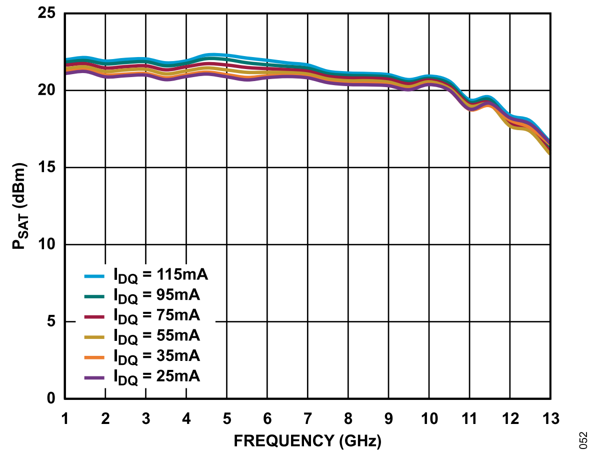


Figure 52. P_{SAT} vs. Frequency for Various I_{DQ} Values, 1 GHz to 13 GHz, V_{DD} = 5 V

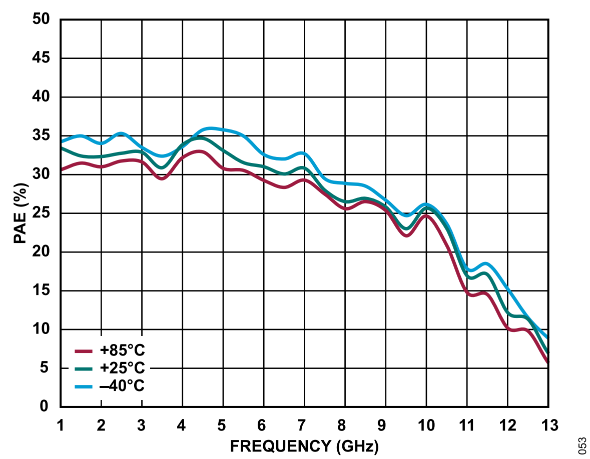


Figure 53. PAE vs. Frequency for Various Temperatures, 1 GHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

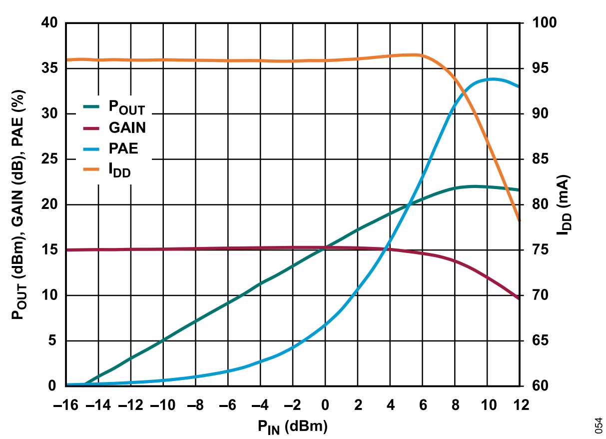


Figure 54. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 5 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

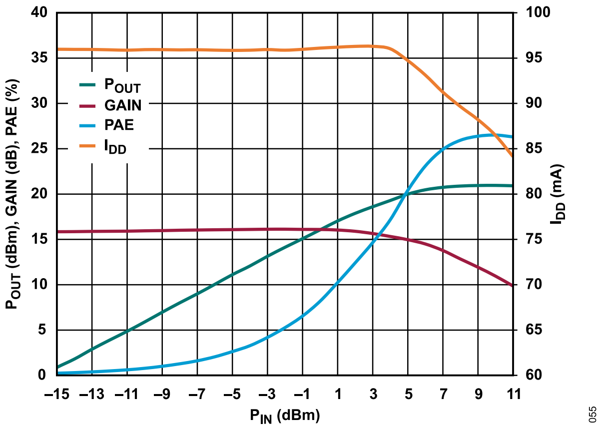


Figure 55. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 8 GHz, R_{BIAS} = 324 Ω

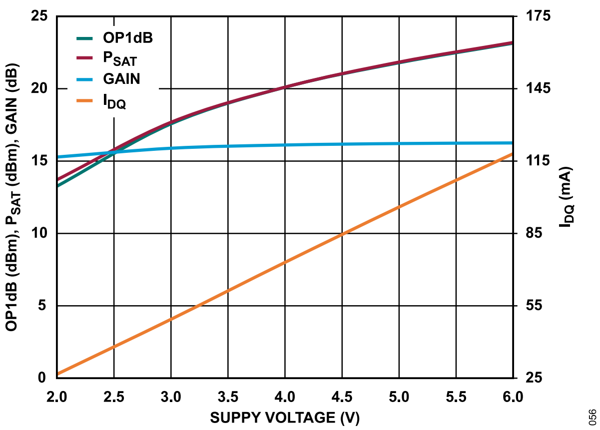


Figure 56. OP1dB, P_{SAT}, Gain, and I_{DQ} vs. Supply Voltage, at 1 GHz, R_{BIAS} = 324 Ω

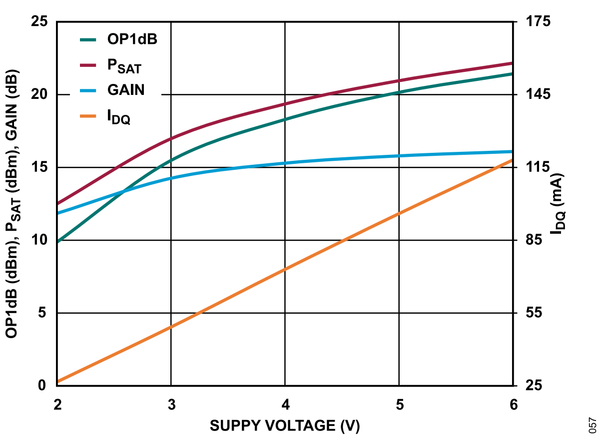


Figure 57. OP1dB, P_{SAT}, Gain, and I_{DQ} vs. Supply Voltage, at 8 GHz, R_{BIAS} = 324 Ω

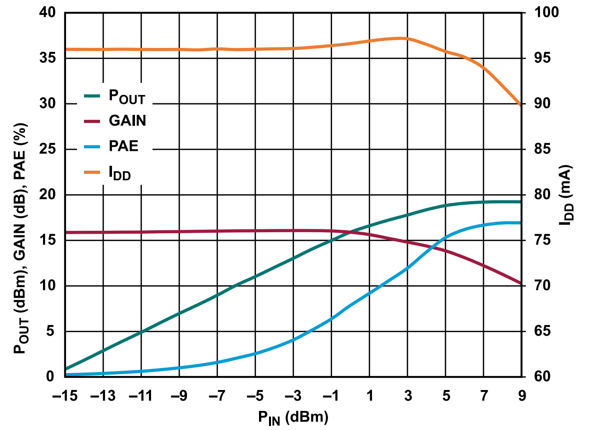


Figure 58. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN} at 11 GHz, R_{BIAS} = 324 Ω

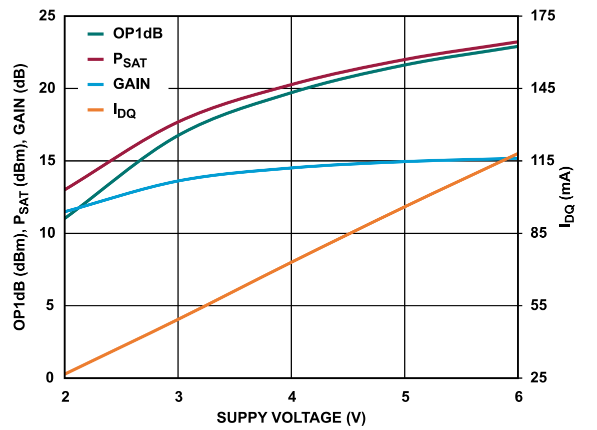


Figure 59. OP1dB, P_{SAT}, Gain, and I_{DQ} vs. Supply Voltage, at 5 GHz, R_{BIAS} = 324 Ω

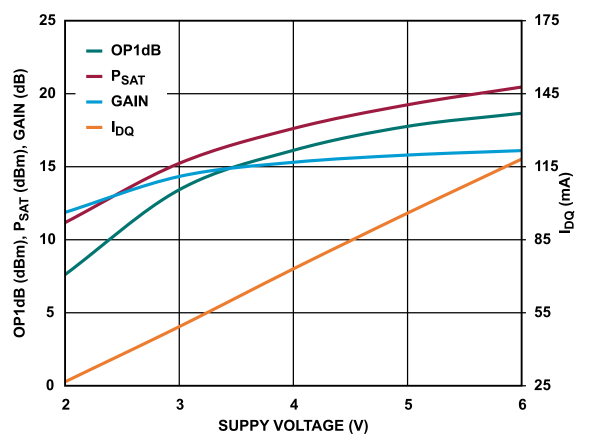


Figure 60. OP1dB, P_{SAT}, Gain, and I_{DQ} vs. Supply Voltage at 11 GHz, R_{BIAS} = 324 Ω

TYPICAL PERFORMANCE CHARACTERISTICS

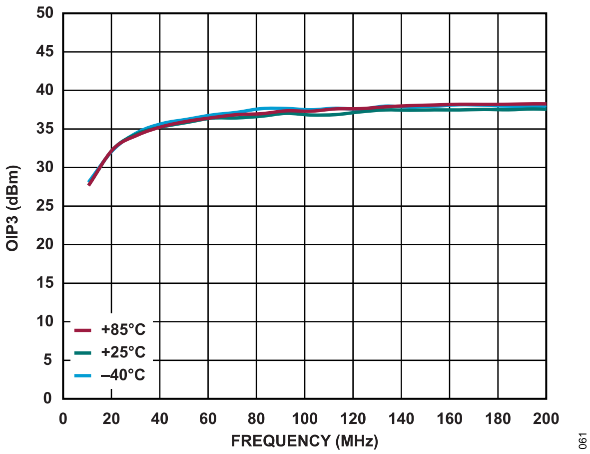


Figure 61. OIP3 vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

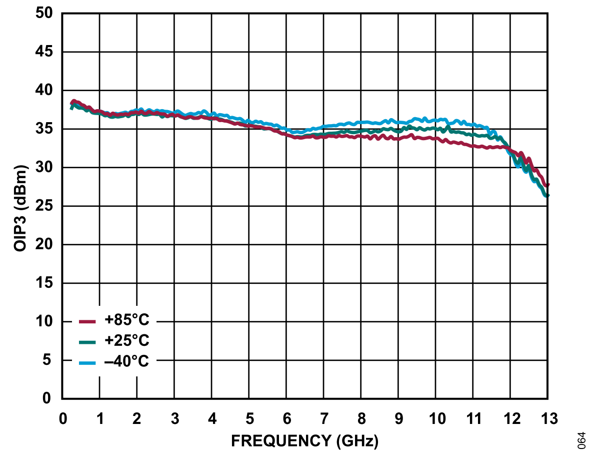


Figure 64. OIP3 vs. Frequency for Various Temperatures, 200 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

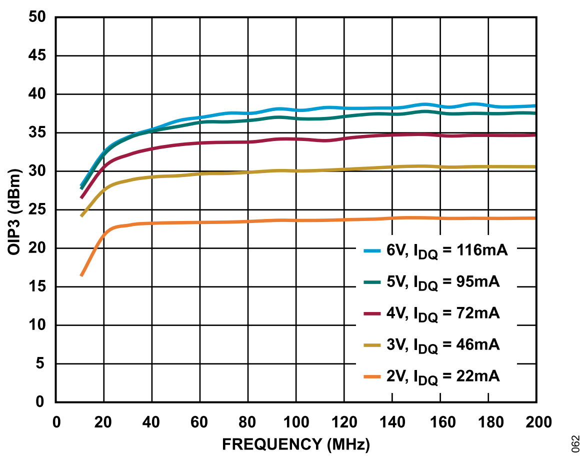


Figure 62. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 200 MHz, R_{BIAS} = 324 Ω

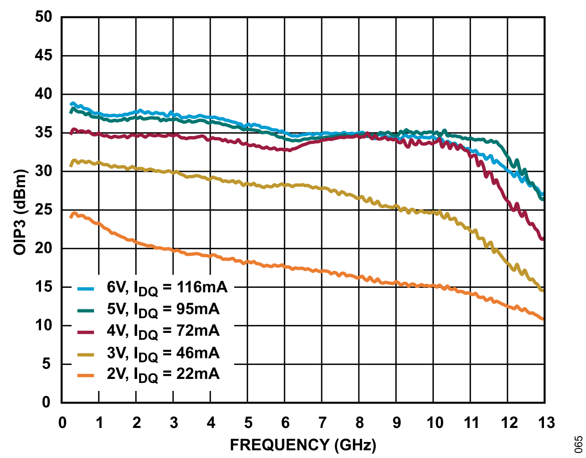


Figure 65. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 200 MHz to 13 GHz, R_{BIAS} = 324 Ω

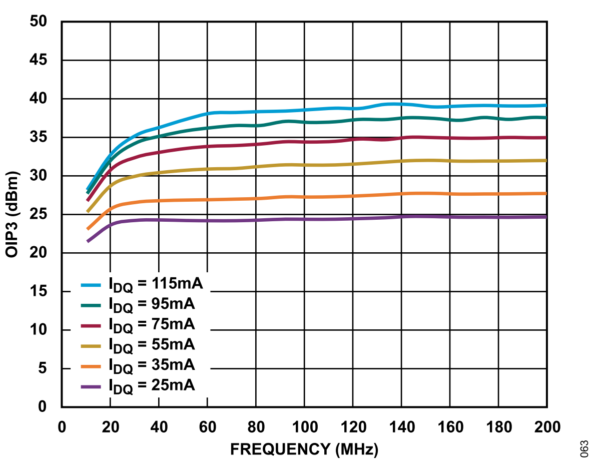


Figure 63. OIP3 vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

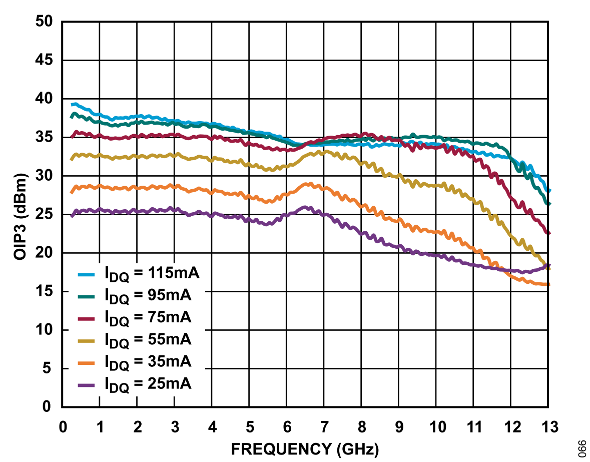


Figure 66. OIP3 vs. Frequency for Various I_{DQ} Values, 200 MHz to 13 GHz, V_{DD} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

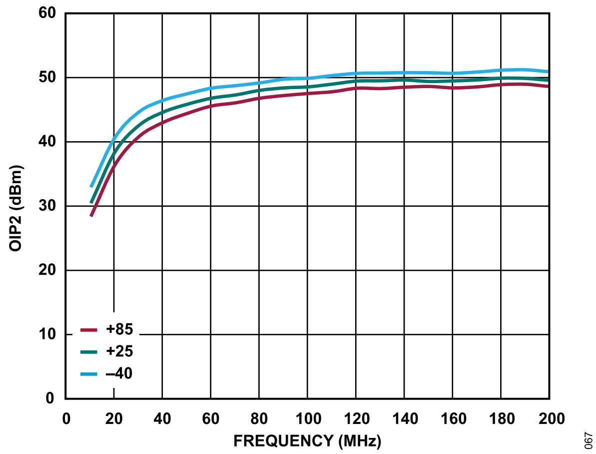


Figure 67. OIP2 vs. Frequency for Various Temperatures, 10 MHz to 200 MHz, V_{DD} = 5 V, I_{DQ} = 95 mA

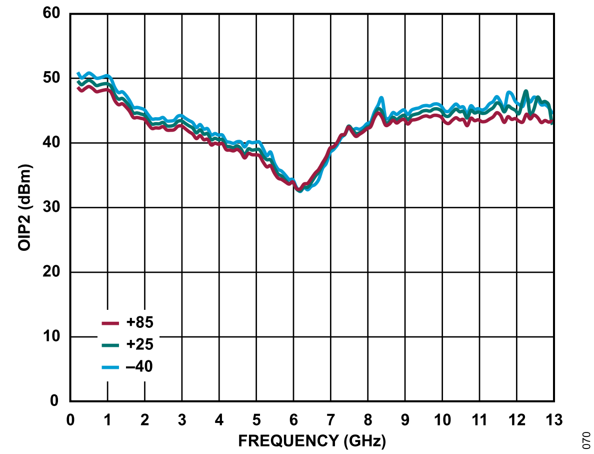


Figure 70. OIP2 vs. Frequency for Various Temperatures, 200 MHz to 13 GHz, V_{DD} = 5 V, I_{DQ} = 95 mA

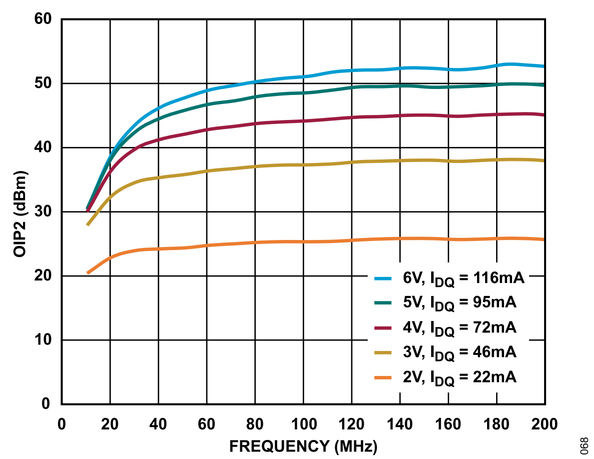


Figure 68. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 10 MHz to 200 MHz, R_{BIAS} = 324 Ω

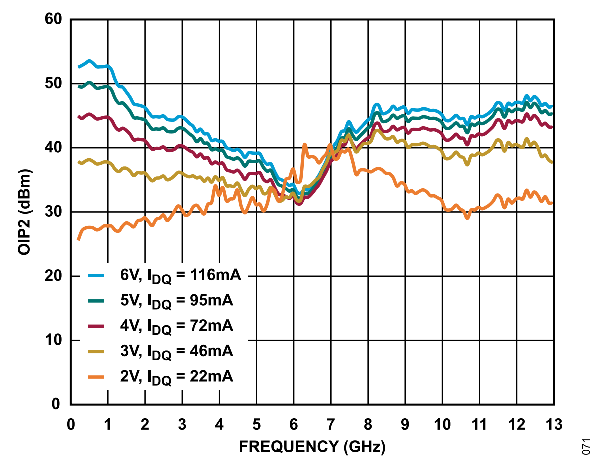


Figure 71. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ} Values, 200 MHz to 13 GHz, R_{BIAS} = 324 Ω

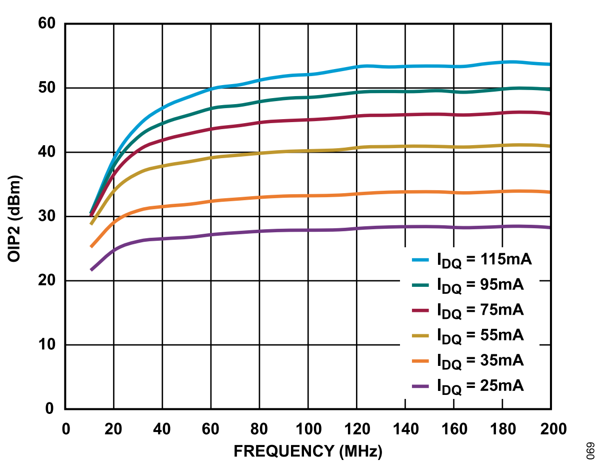


Figure 69. OIP2 vs. Frequency for Various I_{DQ} Values, 10 MHz to 200 MHz, V_{DD} = 5 V

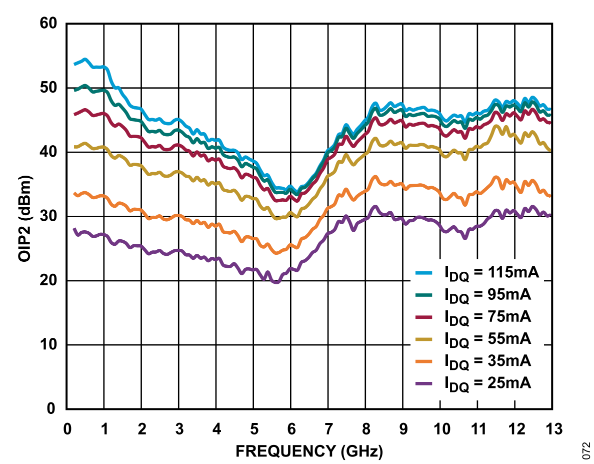


Figure 72. OIP2 vs. Frequency for Various I_{DQ} Values, 200 MHz to 13 GHz, V_{DD} = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

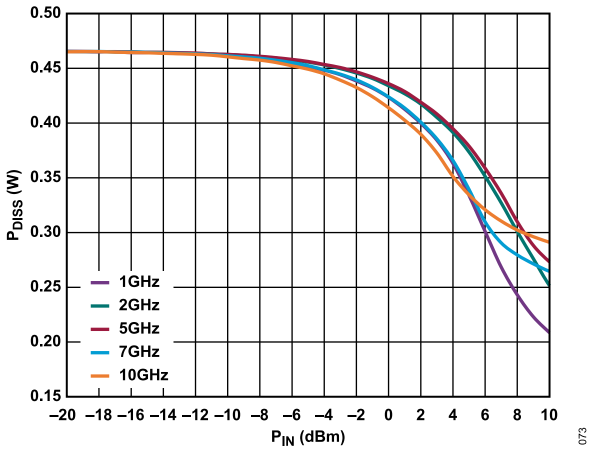


Figure 73. P_{DISS} vs. P_{IN} for Various Frequencies at 85°C, V_{DD} = 5 V, I_{DQ} = 95 mA

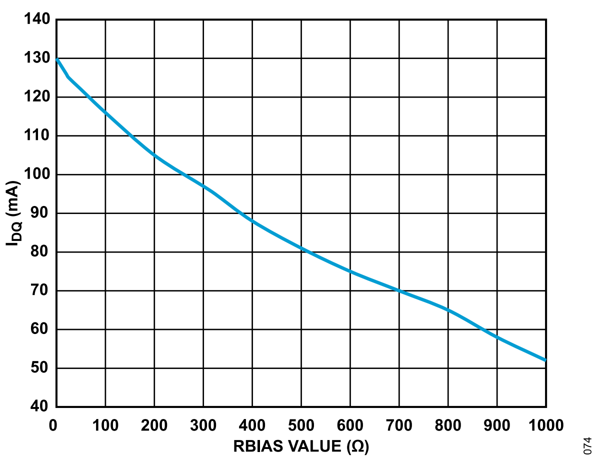


Figure 74. I_{DQ} vs. RBIAS Value, 0 Ω to 1 kΩ, V_{DD} = 5 V

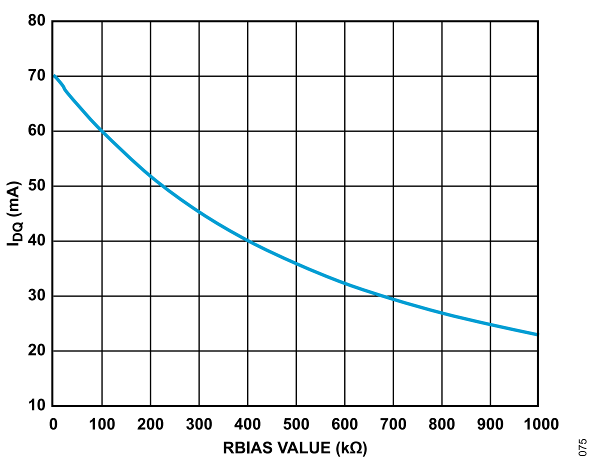


Figure 75. I_{DQ} vs. RBIAS Value, 0 Ω to 1 kΩ, V_{DD} = 3 V

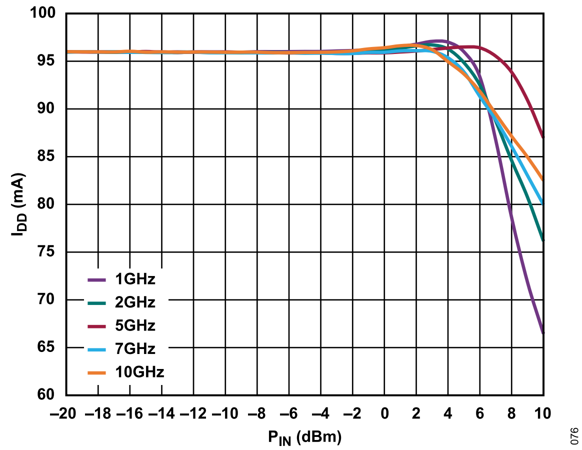


Figure 76. I_{DD} vs. P_{IN} for Various Frequencies, V_{DD} = 5 V

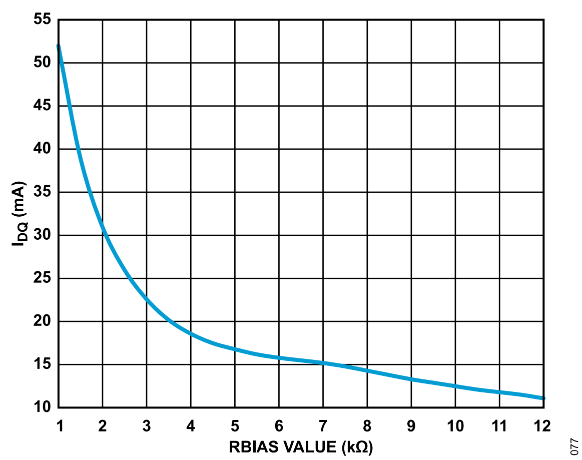


Figure 77. I_{DQ} vs. RBIAS Value, 1 kΩ to 12 kΩ, V_{DD} = 5 V

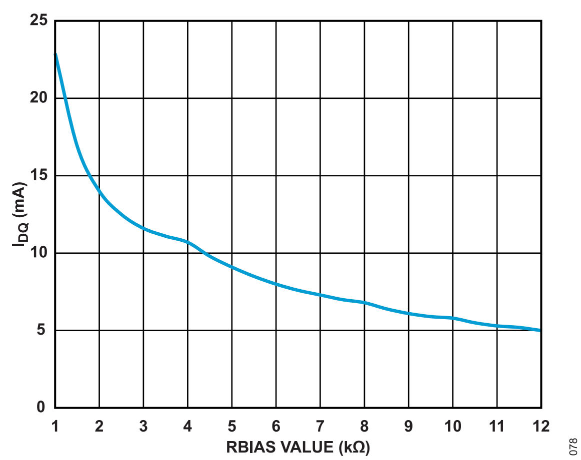


Figure 78. I_{DQ} vs. RBIAS Value, 1 kΩ to 12 kΩ, V_{DD} = 3 V

THEORY OF OPERATION

The ADL8121 is a GaAs, MMIC, pHEMT, low noise wideband amplifier. Figure 79 shows the simplified architecture of the ADL8121.

The ADL8121 has single-ended input and output ports with impedances that nominally equal 50 Ω over the 0.025 GHz to 12 GHz frequency range.

It is critical to supply low inductance ground connections to the GND pins as well as to the backside exposed pad to ensure stable operation.

To achieve optimal performance from the ADL8121 and prevent damage to the device, do not exceed the absolute maximum ratings (see Table 3).

The RBIAS pin is used to set the I_{DQ} with an external resistor, which allows single positive supply operation.

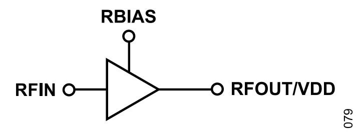


Figure 79. Simplified Architecture

APPLICATIONS INFORMATION

The basic connections for operating the ADL8121 over the specified frequency range are shown in Figure 80. AC-couple the input and output of the ADL8121 with appropriately sized capacitors (such as American Technical Ceramics Part Number 531Z104KTR16T).

A 5 V dc bias is supplied to the amplifier through the choke inductor connected to the RFOUT/VDD pin. The recommended bias inductor is the Murata® ferrite bead BL15GG471SZ1D, 470 Ω.

The bias conditions, V_{DD} = 5 V and I_{DQ} = 95 mA, are the recommended operating point to achieve optimum performance. To set other bias conditions, adjust the value of R_{BIAS}. Table 7 shows the recommended R_{BIAS} values and their associated I_{DQ} values.

Table 7. Recommended Bias Resistor Values for V_{DD} = 5 V

R_{BIAS} (Ω)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
2800	25	24	1.0
1800	35	33.6	1.4
970	55	51.8	3.2
560	75	70.9	4.1
324	95	90.1	4.9
130	115	109.7	5.3

The shunt resistor, inductor, capacitor (RLC) network on the input of the ADL8121 adds resistive loss to help stabilize the amplifier by reducing the gain at low frequencies. The shunt inductor makes the resistor frequency dependent. At low frequencies, the resistor becomes more active. The resistor has less influence at higher frequencies where the impedance of the choke is high. The capacitor blocks dc voltages and currents from flowing through the resistor and the inductor.

To achieve optimal performance from the ADL8121, it is critical to supply low inductance ground connections to the GND pins as well as to the backside exposed pad to ensure stable operation. To prevent damage to the device, do not exceed the absolute maximum ratings (see Table 3).

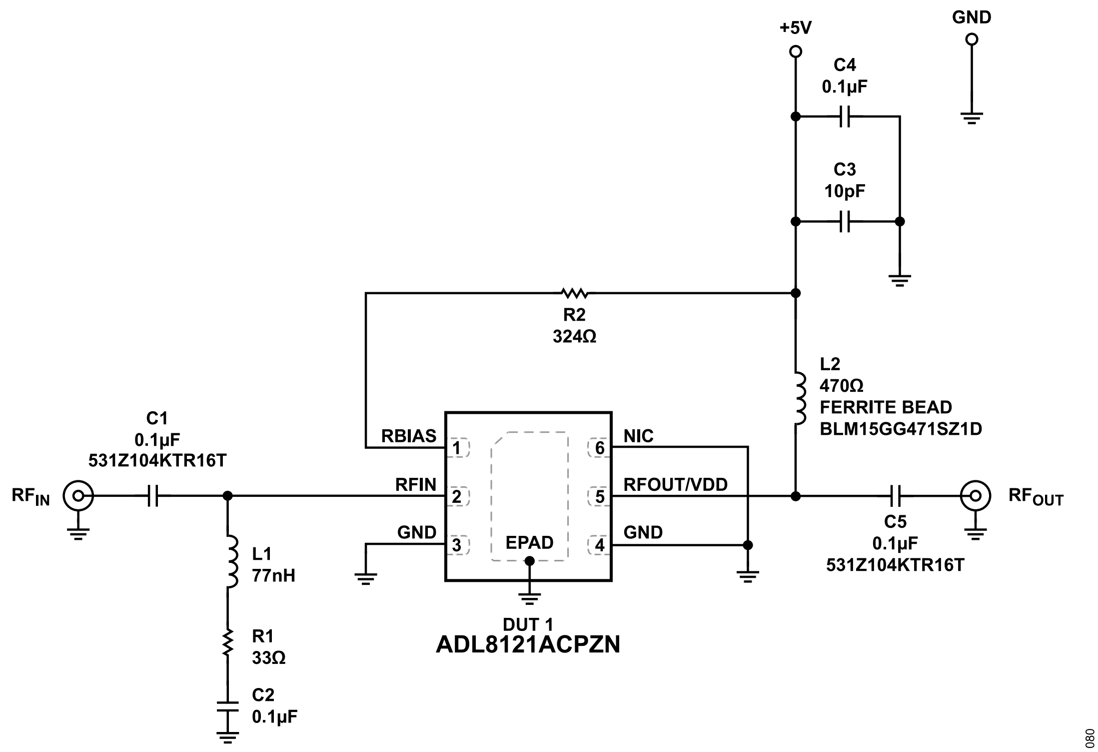


Figure 80. Typical Application Circuit

APPLICATIONS INFORMATION

RECOMMENDED BIAS SEQUENCING

Correct sequencing of the dc and RF power is required to safely operate the ADL8121. During power-up, apply VDD before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before VDD is powered off.

See the ADL8121-EVALZ user guide for the recommended bias sequencing information.

During Power-Up

The recommended bias sequence during power-up is as follows:

1. Set VDD to 5 V.
2. Apply the RF signal.

During Power-Down

The recommended bias sequence during power-down is as follows:

1. Turn off the RF signal.
2. Set VDD to 0 V.

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 81 shows a recommended power management circuit for the ADL8121. The LT8607 step-down regulator is used to step down a 12 V rail to 6.62 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 5 V output. While the circuit shown in Figure 81 has an input voltage (V_{IN}) of 12 V, the input range to the LT8607 can be as high as 42 V.

The 6.62 V regulator output of the LT8607 is set by the R2 and R3 resistors according to the following equation:

$R2 = R3((V_{OUT}/0.778\ V) − 1)$, where V_{OUT} is the output voltage.

The switching frequency is set to 2 MHz by the 18.2 kΩ resistor on the RT pin. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.2 MHz.

The output voltage of the LT3042 is set by the R4 resistor connected to the SET pin according to the following equation:

$V_{OUT} = 100\ \mu A \times R4$

The PGFB resistors are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 5 V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature and adding resistors results in a bit more (5%), therefore, putting 5% between the output and the PGFB resistors works well. In addition, the PG open-collector is pulled up to the 5 V output to give a convenient 0 V to 5 V voltage range. Table 8 provides the recommended resistor values for operation at 5 V to 2 V.

Table 8. Recommended Resistor Values for Operating from 5 V to 2 V

LDO V_{OUT} (V)	R4 (kΩ)	R7 (kΩ)	R8 (kΩ)
5	51.1	464	28.7
4	42.2	383	28.7
3	31.6	261	28.7
2	21.5	178	28.7

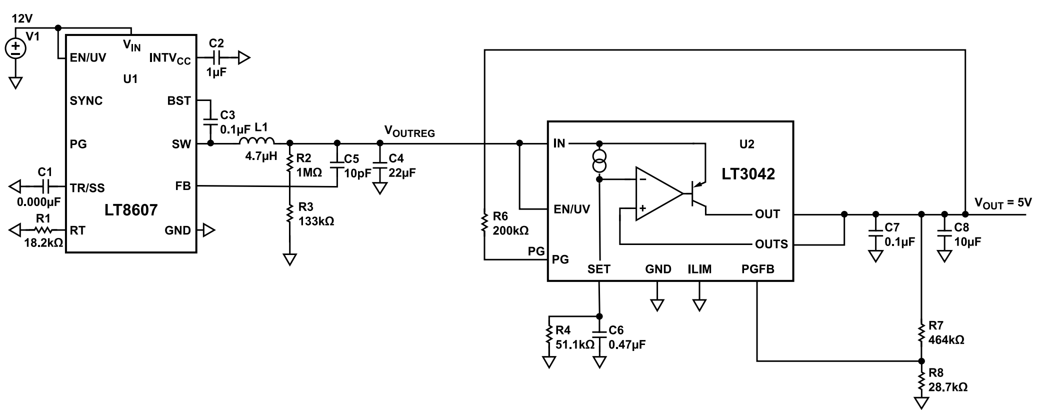


Figure 81. Recommended Power Management Circuit

USING RBIAS TO ENABLE AND DISABLE ADL8121

By attaching a single-pole, double throw (SPDT) switch to the RBIAS pin, an enable and disable circuit can be implemented as shown in Figure 82. The ADG719 CMOS switch is used to connect the RBIAS resistor either to supply or ground. When the RBIAS resistor is connected to ground, the overall current consumption reduces to 1.0 mA with no RF signal present and 4.0 mA when the RF input level is –10 dBm.

Figure 83 and Figure 84 show plots of the turn on and the turn off response time of the RF output envelope when the IN pin of the ADG719 is pulsed.

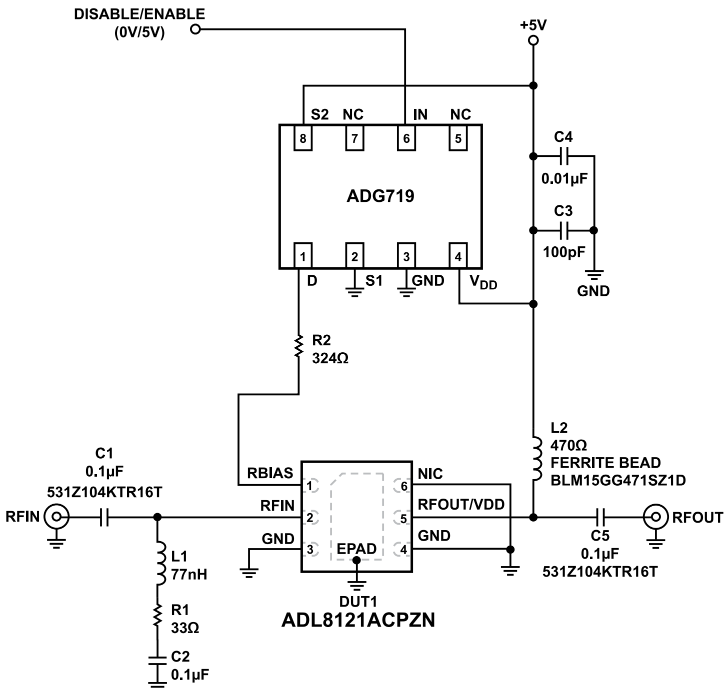


Figure 82. Fast Enable and Disable Using a 0 V to 5 V Pulse on the RBIAS Resistor

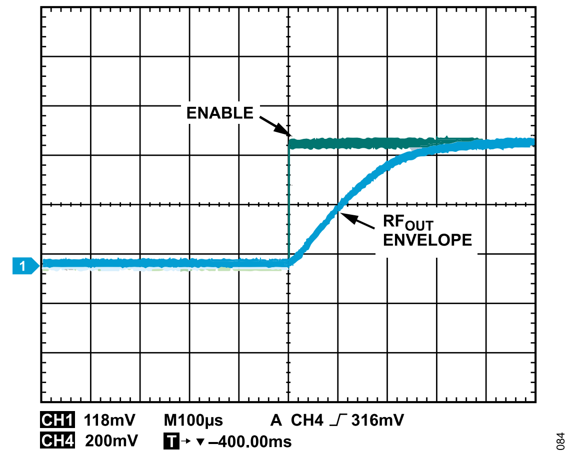


Figure 83. Turn-On Response Time of the RF Output (RF_{OUT}) Envelope When IN Pin of the ADG719 Is Pulsed

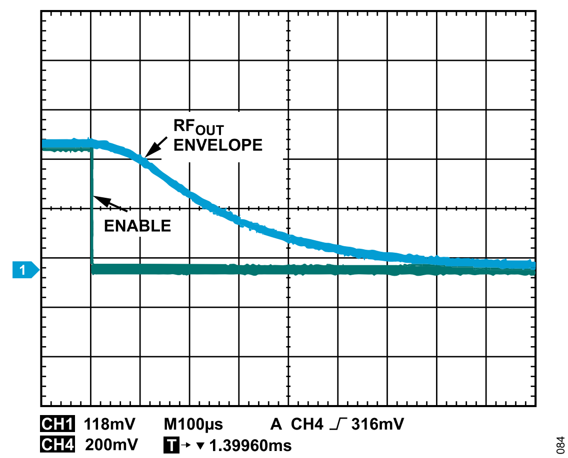


Figure 84. Turn-Off Response Time of the RF_{OUT} Envelope When IN Pin of the ADG719 Is Pulsed

OUTLINE DIMENSIONS

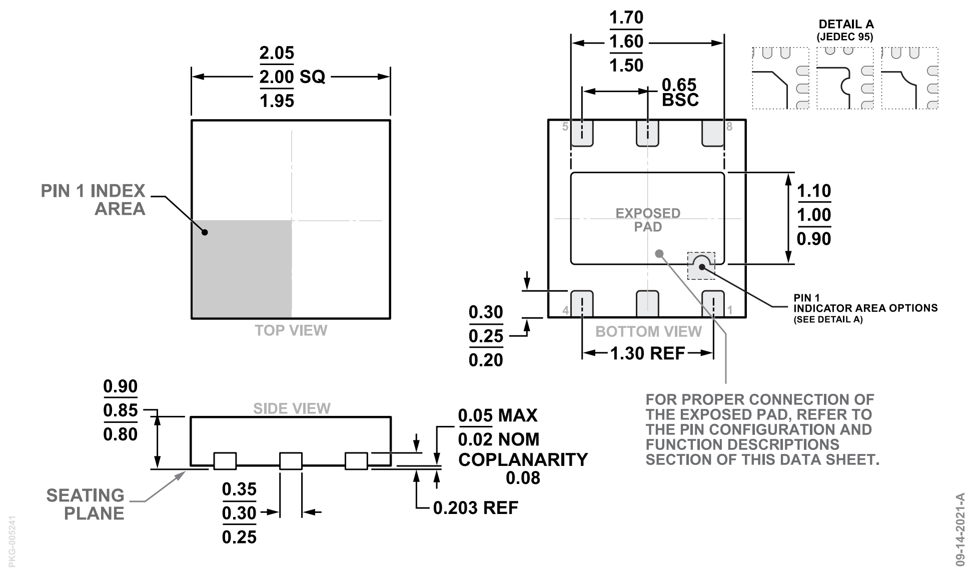


Figure 85. 6-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-6-12)
Dimensions shown in millimeters

Updated: April 26, 2022

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8121ACPZN	−40°C to +85°C	6-Lead LFCSP (2 mm × 2 mm)	Reel, 3000	CP-6-12
ADL8121ACPZN-R7	−40°C to +85°C	6-Lead LFCSP (2 mm × 2 mm)	Reel, 3000	CP-6-12

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADL8121-EVALZ	Evaluation Board

[1] Z = RoHS-Compliant Part.