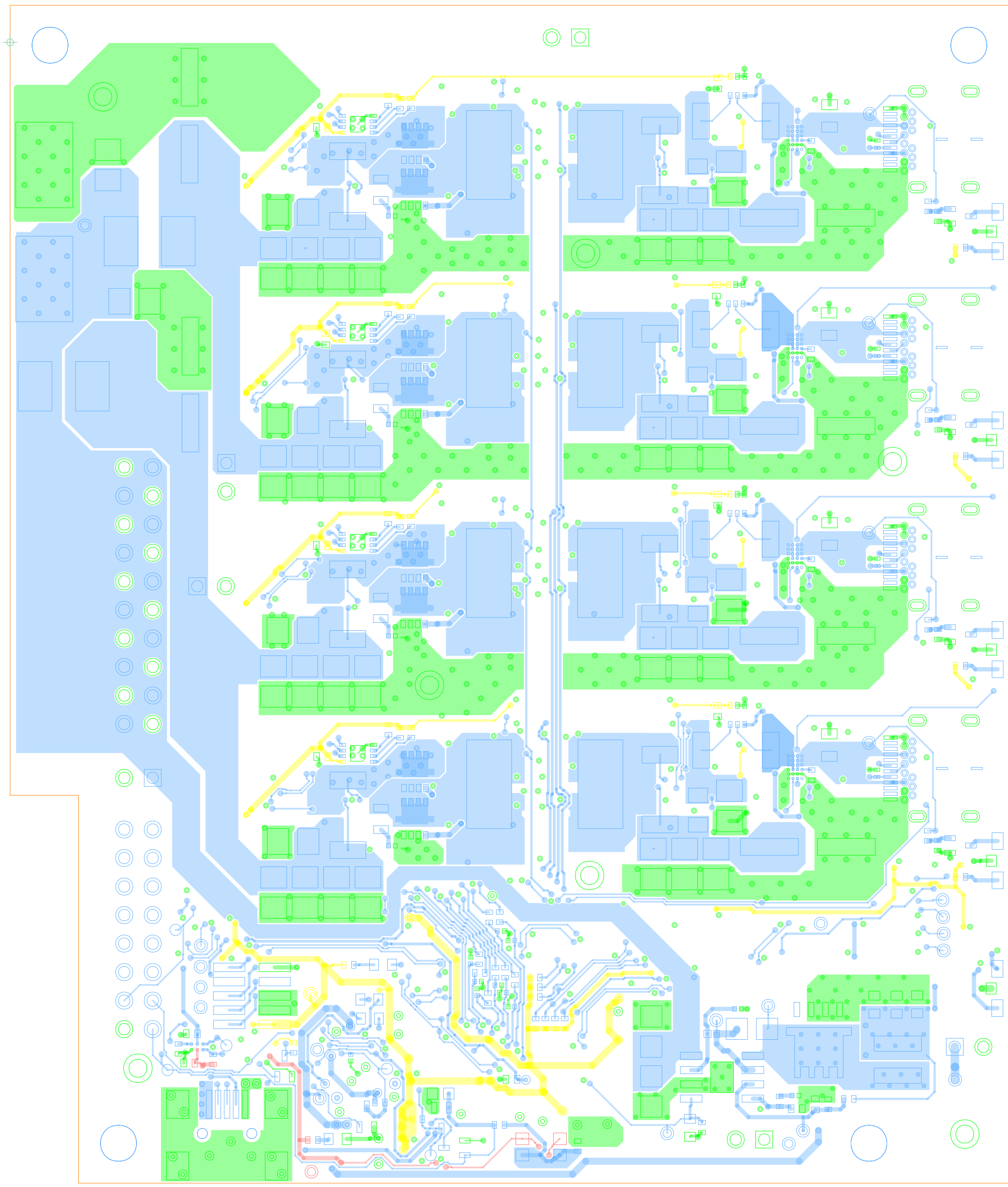
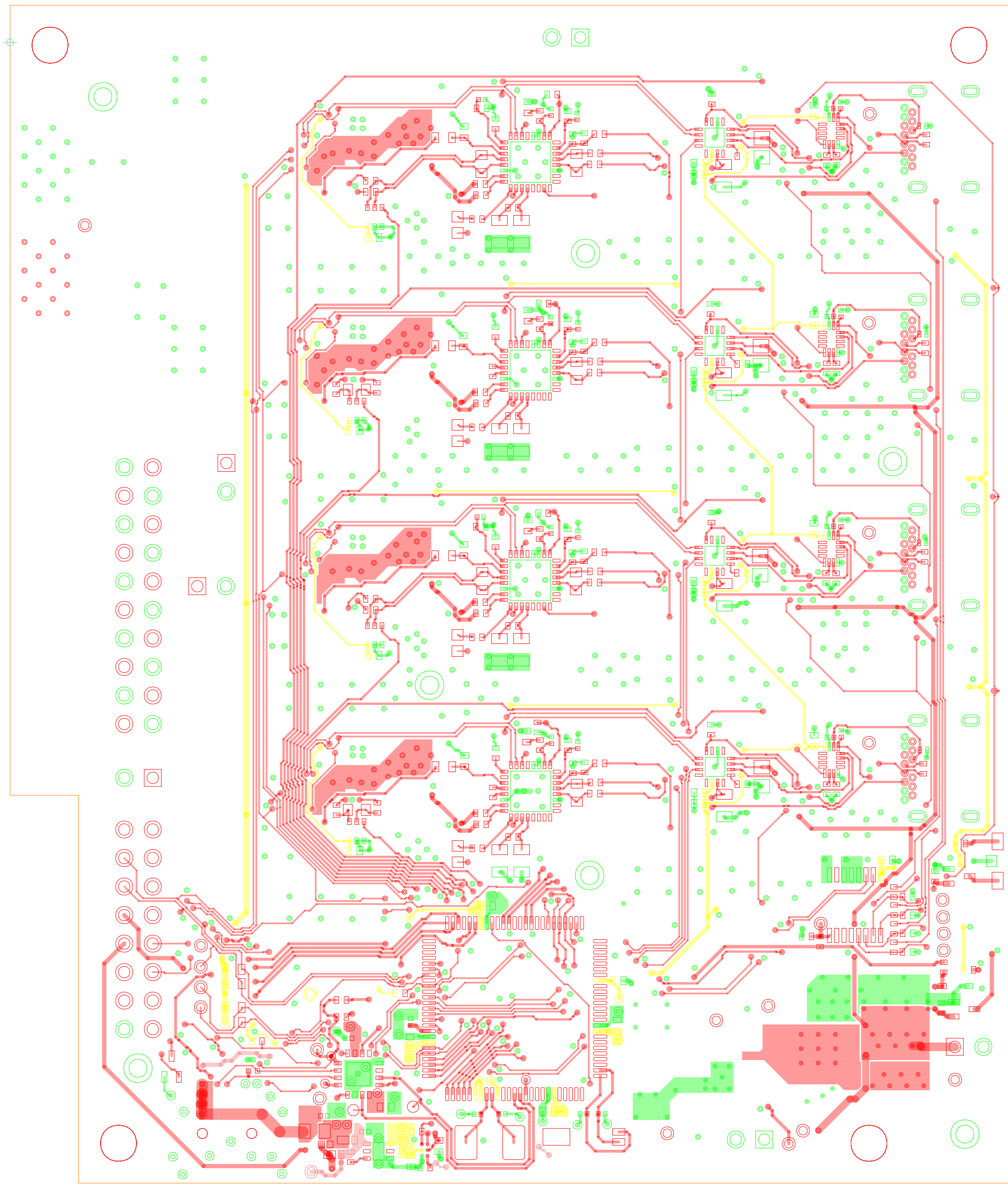
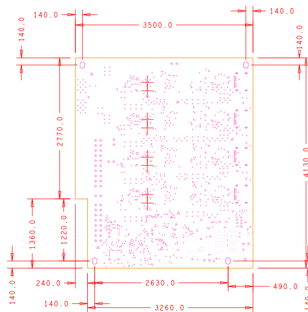


ART FILM - TOP



NOTES (UNLESS OTHERWISE SPECIFIED):

1. BUILD IN ACCORDANCE WITH IPC 6011, IPC 6012, OR IPC 6013 DEPENDANT ON TYPE OF PRINTED CIRCUIT BOARD. CLASS 2.
2. LAMINATE MATERIAL SHALL MEET THE REQUIREMENTS OF IPC 4101 TYPE 370HR PER STACKUP DETAIL OR EQUIVALENT. (NOMINAL DIELECTRIC THICKNESS WITHIN +/- 10% OF STACKUP DETAIL).
3. FINISH: ENIG 2 MICRO-INCHES MINIMUM OF GOLD OVER 118-236 MICRO-INCHES OF NICKEL.
4. TOP SIDE SHOWN.
5. HOLE DIAMETERS ARE AFTER PLATING. 0.8 MIL AVERAGE.
6. SILKSCREEN BOTH SIDES USING EPOXY OR ACRYLIC BASED WHITE NON-CONDUCTIVE SILKSCREEN.
   NOTE: LEGEND SHOULD BE REMOVED FROM ANY CONDUCTIVE SURFACE UNLESS OTHERWISE SPECIFIED.
   NO SILKSCREEN ON PADS.
7. SILK VENDOR ID, UL DESIGNATION, AND DATECODE ON THE BACKSIDE.
8. SOLDER MASK BOTH SIDES GREEN USING LIQUID PHOTO IMAGEABLE METHOD.
   NO SOLDERMASK ON PADS.
9. IMPEDANCE REQUIREMENTS ARE AS FOLLOWS. +/- 10%.
   IF PRESENT, ALL OUTER 6.25 MIL WIDE TRACES 50 OHM SINGLE ENDED.
   IF PRESENT, ALL INNER 5.25 MIL WIDE TRACES 50 OHM SINGLE ENDED.
   TRACE WIDTHS SHALL NOT BE MODIFIED WITHOUT APPROVAL FROM ON SEMICONDUCTOR.
10. ALL ARTWORK AND DESIGN MEDIA SHALL BE SPECIFIED BY ON SEMICONDUCTOR.
    NO CHANGES WILL BE ALLOWED WITHOUT SPECIFIC APPROVAL FROM ON SEMICONDUCTOR.
11. TOOLING HOLES ARE TO BE DRILLED AWAY AT THE SAME TIME AS OTHER HOLES.
12. ALL MATERIALS ARE TO BE ROHS AND WEE COMPLIANT.
13. LAYER STACKUP INFORMATION INCLUDED IN THIS DRAWING SHOWS OUTER LAYER THICKNESS AFTER PLATING AND SUPERSEDES ANY OTHER DESIGN DOCUMENTATION.
14. ELECTRICALLY DISCONNECTED COPPER THIEVING IS ACCEPTABLE TO HELP MAINTAIN COPPER PLATING DISTRIBUTION IN LOW PRESSURE AREAS TO AVOID DELAMINATION.
15. REMOVAL OF NON-FUNCTIONAL PADS ON INNER LAYERS IS ACCEPTABLE.
16. DO NOT PROVIDE BOARDS IN ARRAY FORMAT.



DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
·	6.0	+2.0/-4.0	PLATED	64
•	10.0	+2.0/-6.0	PLATED	1013
•	14.0	+2.0/-6.0	PLATED	46
•	15.7	+2.0/-2.0	PLATED	56
○	29.5	+2.0/-2.0	PLATED	24
◇	40.0	+2.0/-2.0	PLATED	48
△	63.0	+4.0/-4.0	PLATED	7
○	35.4	+2.0/-2.0	NON-PLATED	2
○	126.0	+10.0/-10.0	NON-PLATED	8
⬭	47.2x23.6	+6.0/-6.0	PLATED	16

STACKUP TABLE				
Unit = Mils				
#	NAME	TYPE	MATERIAL	THICKNESS
		SURFACE	AIR	0
1	TOP	CONDUCTOR	COPPER	2
		DIELECTRIC	FR-4	3.3
2	L2	PLANE	COPPER	1.2
		DIELECTRIC	FR-4	3
		DIELECTRIC	FR-4	8.7
		DIELECTRIC	FR-4	21
		DIELECTRIC	FR-4	8.7
		DIELECTRIC	FR-4	3
3	L3	PLANE	COPPER	1.2
		DIELECTRIC	FR-4	3.3
4	BOTTOM	CONDUCTOR	COPPER	2
		SURFACE	AIR	0
		TOTAL THICKNESS		57.5

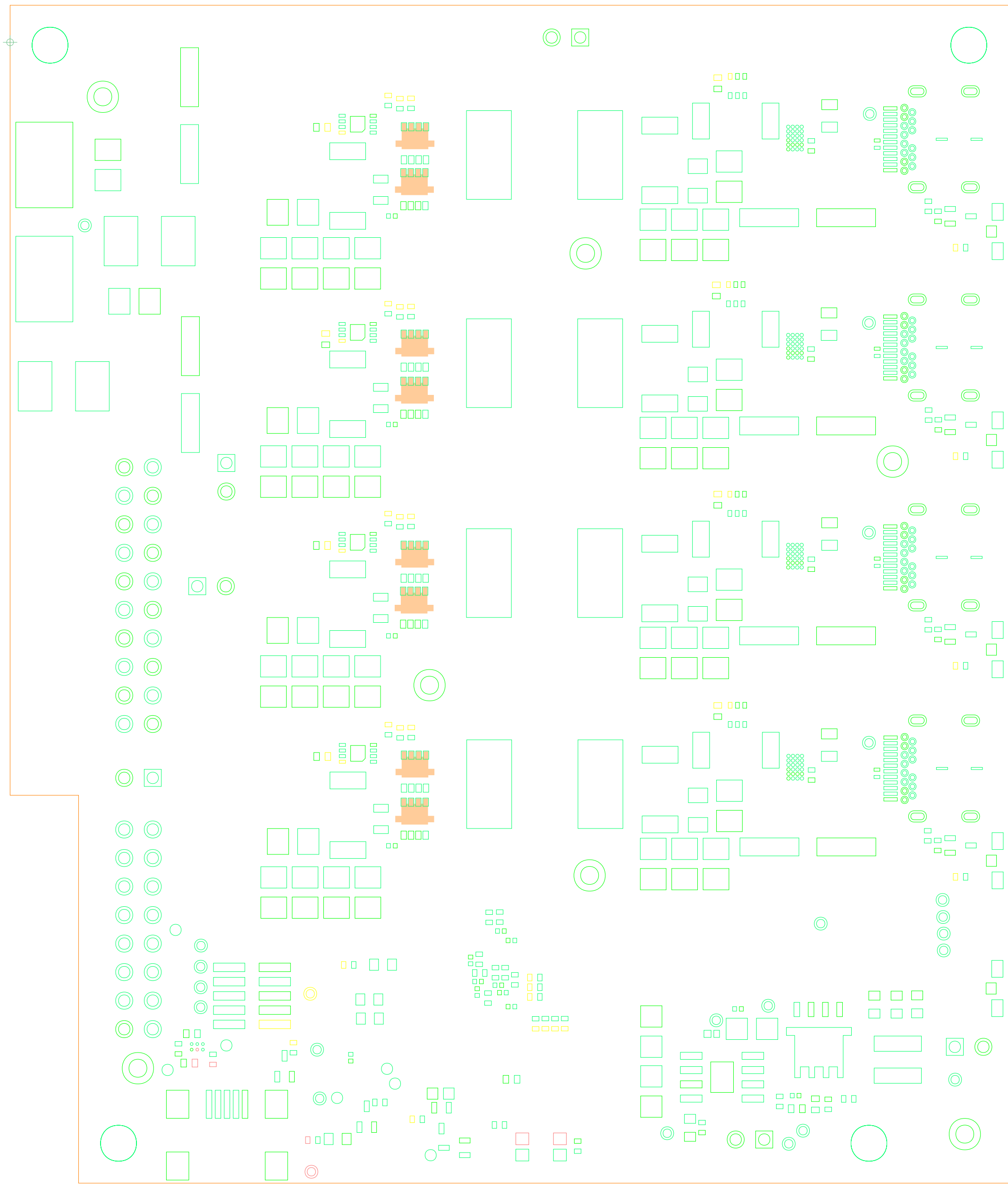
UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN MILS TOLERANCES ON:	DRAWN: THOMAS ASHE	02/07/19
	CHECKED: THOMAS ASHE	02/07/19
	ENGRG: THOMAS ASHE	02/07/19
	ISSUED: THOMAS ASHE	02/07/19

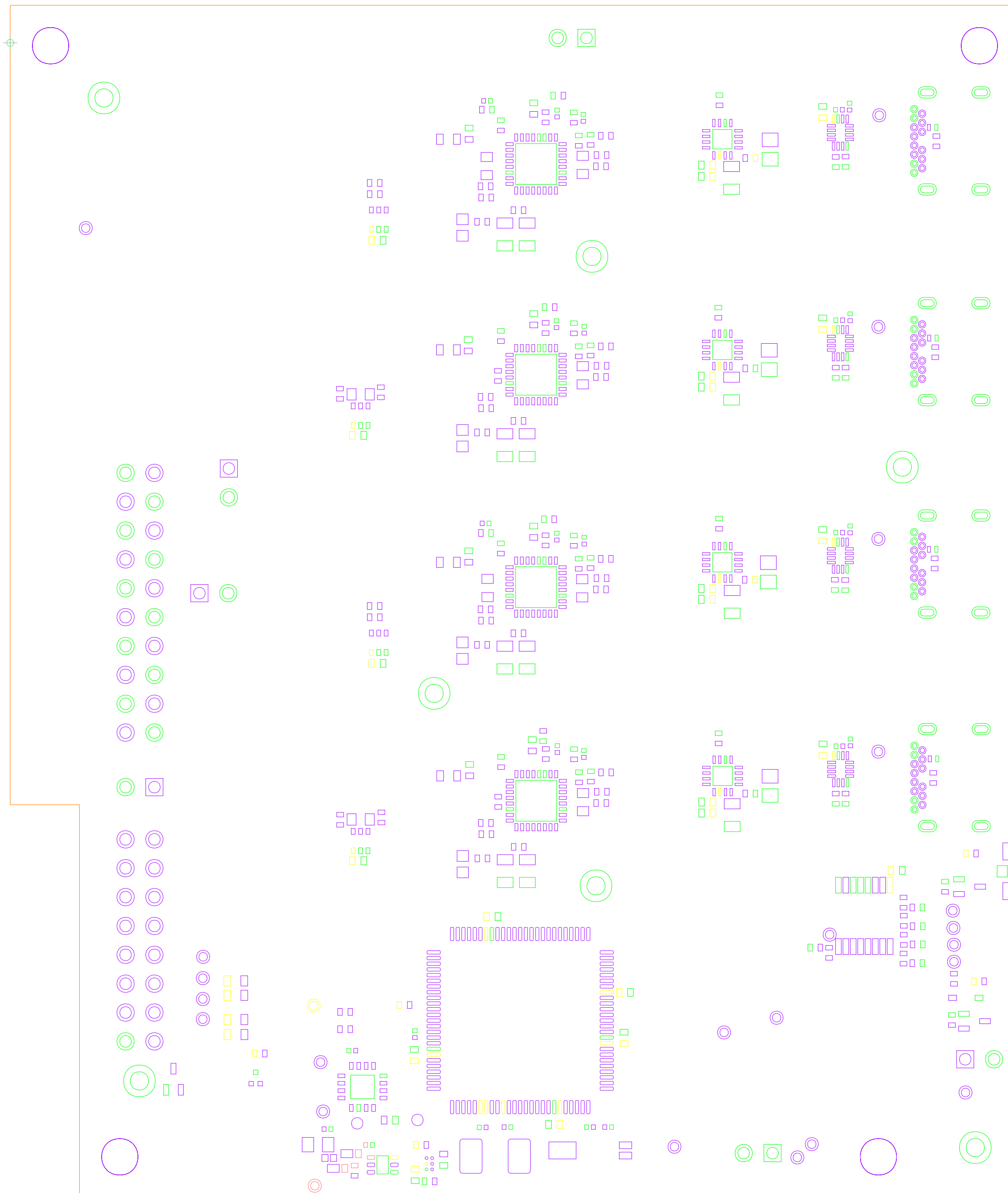
ON SEMICONDUCTOR

4-PORT USB TYPE-C PD SOURCE

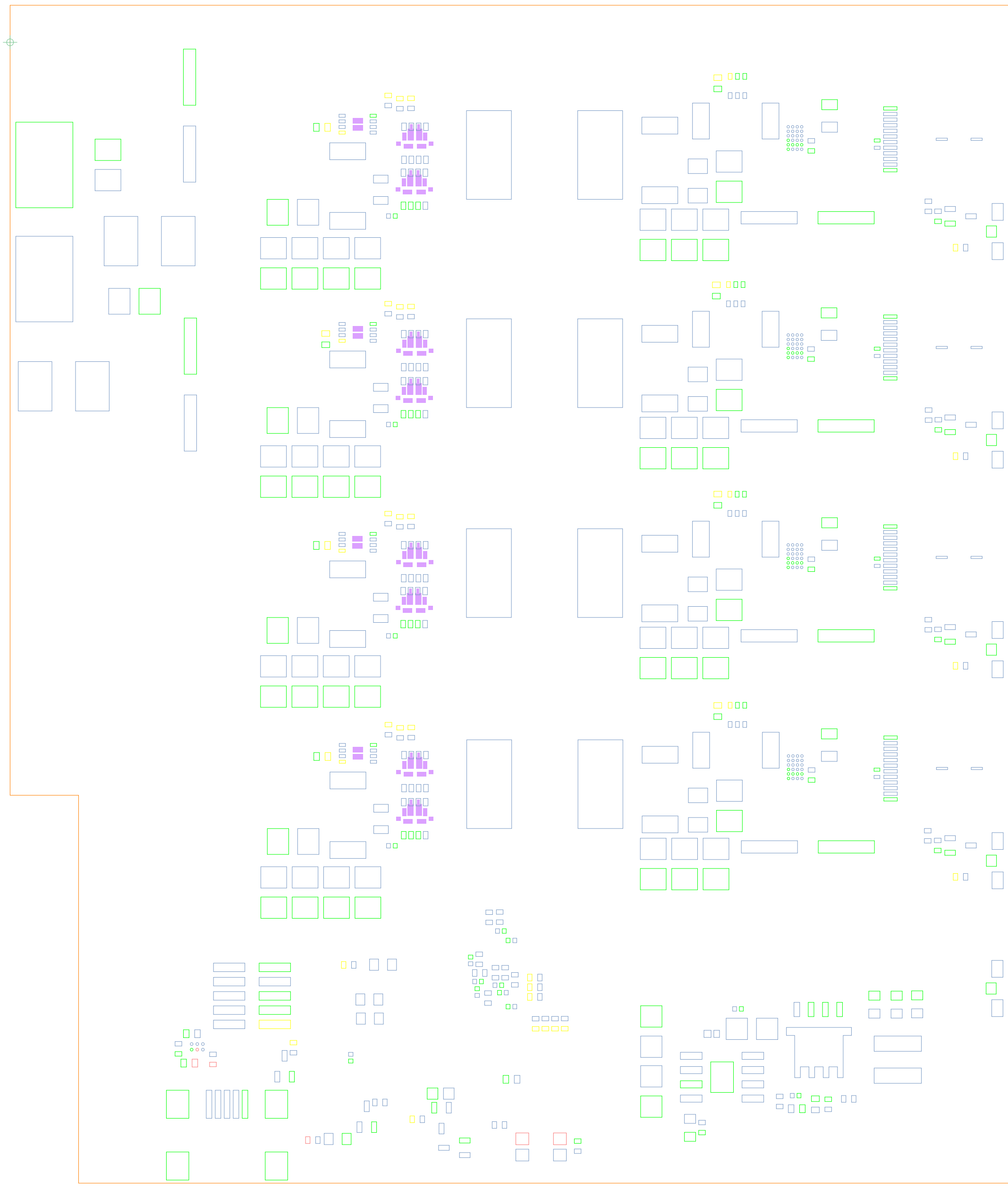
SIZE	REVISION	DWG NO
D	REV2	ONSEC-17-038

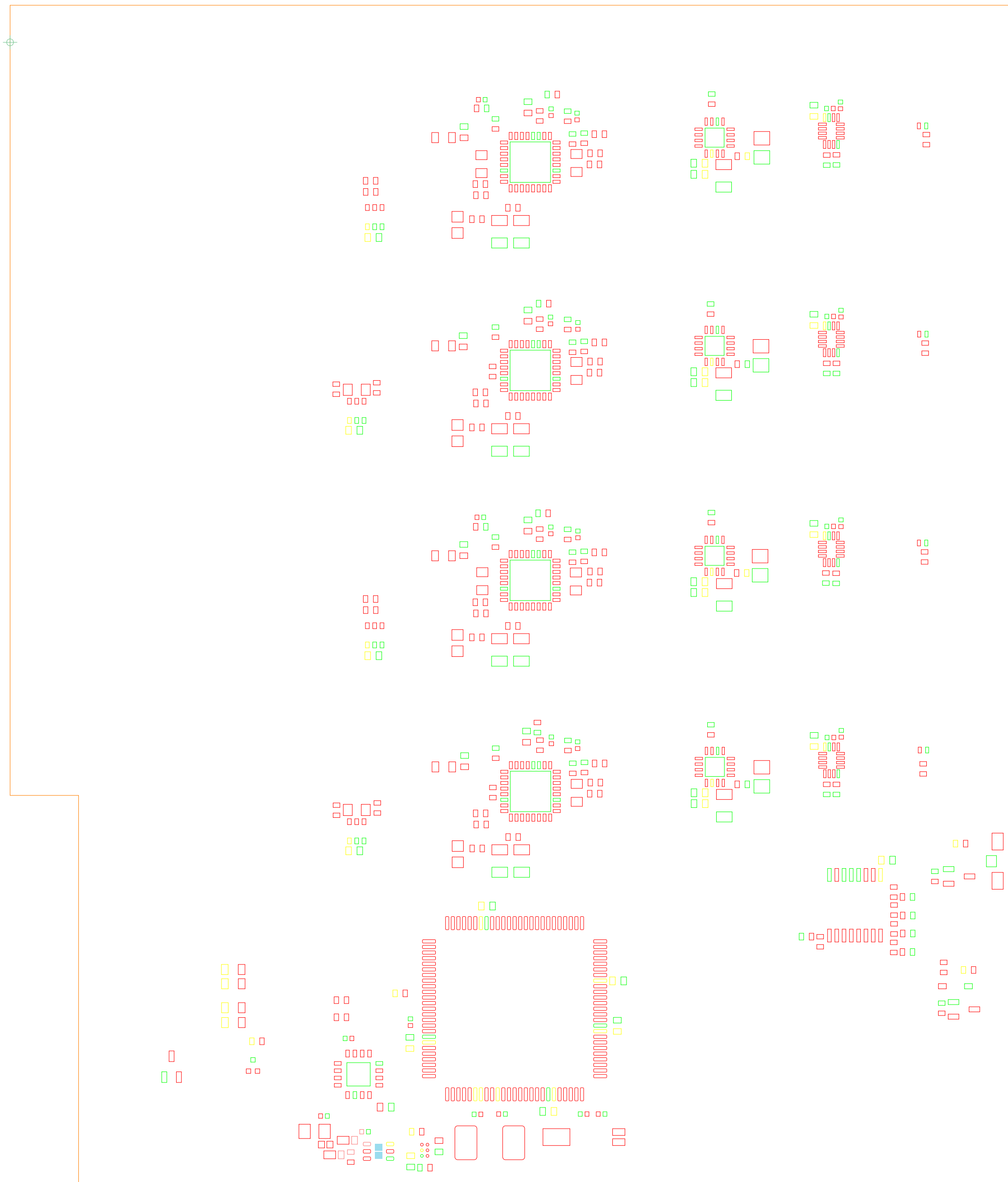
SCALE	DRAWING	SHEET
1/1	FABRICATION	1 OF 3





ART FILM - SMASKBOT





STR-USBC-4PORT-200W-EVK

COMPONENTS SUPPORTED BY

WÜRTH ELEKTRONIK

PORT4

PORT3

PORT2

PORT1

VBUS4_F

VBUS3_F

VBUS2_F

VBUS1_F

24V1/2

24V3/4

24V

VIN

GND

5V

VOUT

I2C_SCL_1

I2C_SDA_1

I2C_SCL_0

I2C_SDA_0

INT

24V_ADC

VBUS_2_ADC

VBUS_1_ADC

VBUS_3_ADC

VBUS_4_ADC

3V3

LINK

TX

RX

3V3_FT

5V_USB

USB_RST

RTS

CTS

FLT

RST

RST_MCU

BST

SWN

EN

FB

COMP

Strata

ON

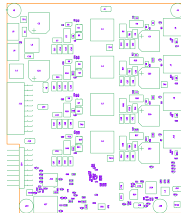
4-PORT USB-PD TYPE-C SOURCE

ONSEC-17-038 REV2

AWT

ASSEMBLY TOP NOTES (UNLESS OTHERWISE SPECIFIED):

1. ASSEMBLE AND INSPECT PER IPC-A-610 CLASS 3.
2. SOLDER, FLUX, AND ROHS TYPES SHOULD BE DEFINED IN QUOTATION FROM MANUFACTURER.
3. IF BARE BOARDS ARE SUPPLIED BY ON SEMICONDUCTOR THEY WILL BE AN <ARRAY OR INDIVIDUAL PEICES>.
4. ONLY PARTS CONTAINED IN BILL OF MATERIALS SHALL USED FOR TURN-KEY ASSEMBLY UNLESS EQUIVALENT PART APPROVED BY ON SEMICONDUCTOR.
5. REMOVE ANY KAPTON TAPE COVERING COMPONENTS EXCEPT FOR IMAGE SENSORS WHERE IT SHOULD ONLY BE REMOVED IF LENS OR LENS HOLDER INTERFERE WITH KAPTON TAPE REMOVAL.
6. "DNP" REFERENCE IN BILL OF MATERIALS MEANS DO NOT INSTALL AND THESE PARTS ARE NOT REQUIRED FOR BOARD BUILD.
7. RETURN ALL CONSIGNED AND TURN-KEY UNASSEMBLED OR EXTRA COMPONENTS WITH ASSEMBLED PCBS.
8. REFLOW HEAT PROFILE IS REQUIRED BY ASSEMBLER TO ENSURE PROPER SOLDER ATTACH.
9. HIDDEN PINS SUCH AS BGA PACKAGES ARE REQUIRED TO BE X-RAY'ED FOR PROPER SOLDER ATTACH.
10. NO ARRAY MOUSE BITES ARE ALLOWED ON EDGE OF FINISHED PCB. USE PLUNGE ROUTER TO REMOVE AFTER ASSEMBLY.
11. SOLDERMASK BARREL RELIEF TO AVOID ASSEMBLY ISSUES ON LARGE SURFACE MOUNT PADS IS ACCEPTABLE.
12. IF ASSEMBLY BOTTOM NOTES ARE NOT FOUND USE TOP NOTES.



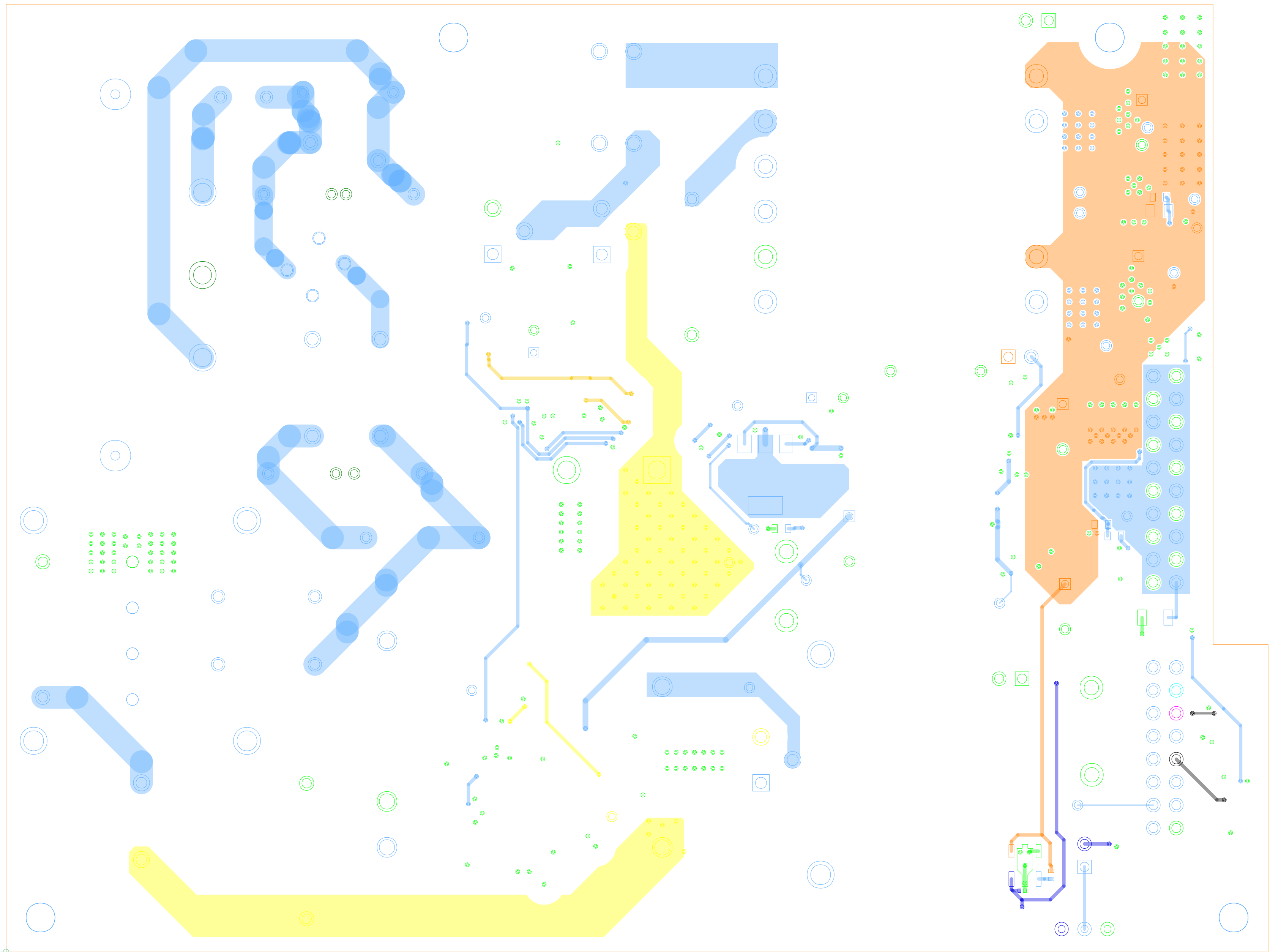
UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE	ON SEMICONDUCTOR		
DIMENSIONS ARE IN MILS TOLERANCES ON:	DRAWN: THOMAS ASHE	02/07/19	4-PORT USB TYPE-C PD SOURCE		
	CHECKED: THOMAS ASHE	02/07/19			
	ENGRG: THOMAS ASHE	02/07/19	SIZE: D	REVISION: REV2	DWG NO: ONSEC-17-038
	ISSUED: THOMAS ASHE	02/07/19			
			SCALE: 1/1	DRAWING: ASSEMBLY TOP	SHEET: 2 OF 3

ASSEMBLY BOTTOM NOTES (UNLESS OTHERWISE SPECIFIED):
1. USE ASSEMBLY TOP NOTES.

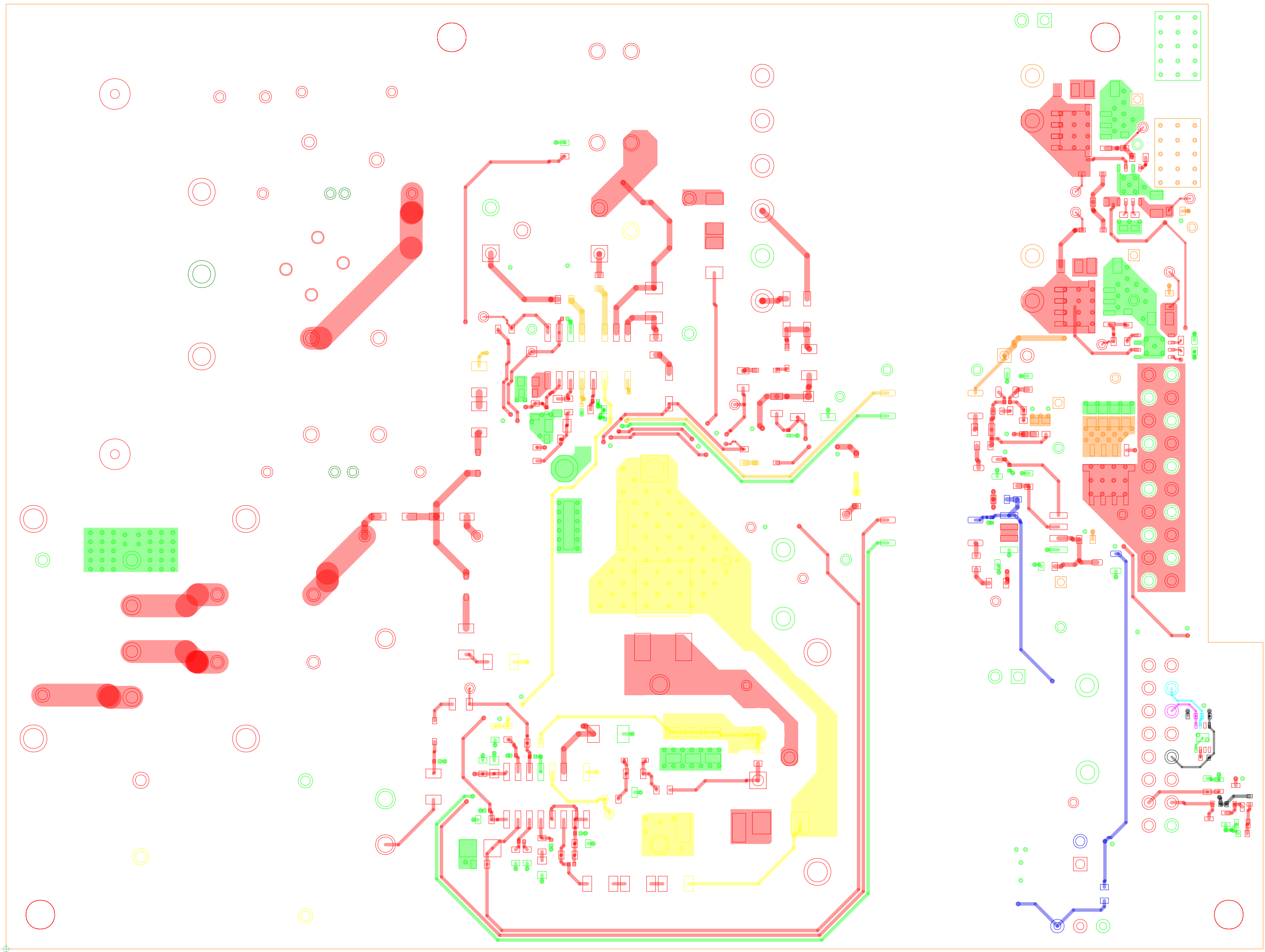
ON SEMICONDUCTOR			DATE	SIGNATURES	UNLESS OTHERWISE SPECIFIED
4-PORT USB TYPE-C PD SOURCE			02/07/19	DRAWN: THOMAS ASHE	DIMENSIONS ARE IN MILS TOLERANCES ON:
DWG NO ONSEC-17-038	REVISION REV2	SIZE D	02/07/19	CHECKED: THOMAS ASHE	
SHEET 3 OF 3	DRAWING ASSEMBLY BOTTOM	SCALE 1/1	02/07/19	ENGRG: THOMAS ASHE	
			02/07/19	ISSUED: THOMAS ASHE	

ART FILM - L2

ART FILM - L3



ART FILM - TOP



ART FILM - BOTTOM

5260.0
1950.0
2860.0
450.0
240.0
4130.0
3835.0
2790.0
1190.0
1340.0
5200.0
5500.0
150.0
150.0

NOTES (UNLESS OTHERWISE SPECIFIED):

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3. FINISH: ENIG 2 MICRO-INCHES MINIMUM OF GOLD OVER 118-236 MICRO-INCHES OF NICKEL.
4. TOP SIDE SHOWN.
5. HOLE DIAMETERS ARE AFTER PLATING. 0.8 MIL AVERAGE.
6. SILKSCREEN BOTH SIDES USING EPOXY OR ACRYLIC BASED WHITE NON-CONDUCTIVE SILKSCREEN.
   NOTE: LEGEND SHOULD BE REMOVED FROM ANY CONDUCTIVE SURFACE UNLESS OTHERWISE SPECIFIED.
   NO SILKSCREEN ON PADS.
7. SILK VENDOR ID, UL DESIGNATION, AND DATECODE ON THE BACKSIDE.
8. SOLDER MASK BOTH SIDES GREEN USING LIQUID PHOTO IMAGEABLE METHOD. NO SOLDERMASK ON PADS.
9. IMPEDANCE REQUIREMENTS ARE AS FOLLOWS. +/- 10%.
   IF PRESENT, ALL OUTER 6.25 MIL WIDE TRACES 50 OHM SINGLE ENDED.
   IF PRESENT, ALL INNER 5.25 MIL WIDE TRACES 50 OHM SINGLE ENDED.
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15. REMOVAL OF NON-FUNCTIONAL PADS ON INNER LAYERS IS ACCEPTABLE.
16. DO NOT PROVIDE BOARDS IN ARRAY FORMAT. 250 MILS ON ALL SIDES.

DRILL CHART: TOP to BOTTOM

ALL UNITS ARE IN MILS

FIGURE	FINISHED_SIZE	TOLERANCE_DRILL	PLATED	QTY
·	10.0	+2.0/-6.0	PLATED	365
□	28.3	+2.0/-2.0	PLATED	4
○	29.5	+2.0/-2.0	PLATED	19
○	31.5	+2.0/-2.0	PLATED	3
○	32.3	+2.0/-2.0	PLATED	10
◇	33.5	+2.0/-2.0	PLATED	14
△	35.4	+3.0/-3.0	PLATED	2
○	40.0	+3.0/-3.0	PLATED	44
○	41.3	+3.0/-3.0	PLATED	6
▭	43.3	+3.0/-3.0	PLATED	2
○	43.3	+3.9/-3.9	PLATED	4
B	47.2	+2.0/-2.0	PLATED	4
A	47.2	+4.0/-4.0	PLATED	2
C	48.4	+4.0/-4.0	PLATED	9
D	50.0	+4.0/-4.0	PLATED	4
E	55.1	+4.0/-4.0	PLATED	4
F	62.0	+4.0/-4.0	PLATED	10
G	63.0	+4.0/-4.0	PLATED	4
H	66.9	+3.9/-3.9	PLATED	5
I	78.7	+6.0/-6.0	PLATED	4
J	78.7	+6.0/-6.0	PLATED	1
K	87.0	+2.0/-2.0	PLATED	6
L	51.18	+4.0/-4.0	NON-PLATED	4
M	126.0	+8.0/-8.0	NON-PLATED	8
N	133.9	+8.0/-8.0	NON-PLATED	2

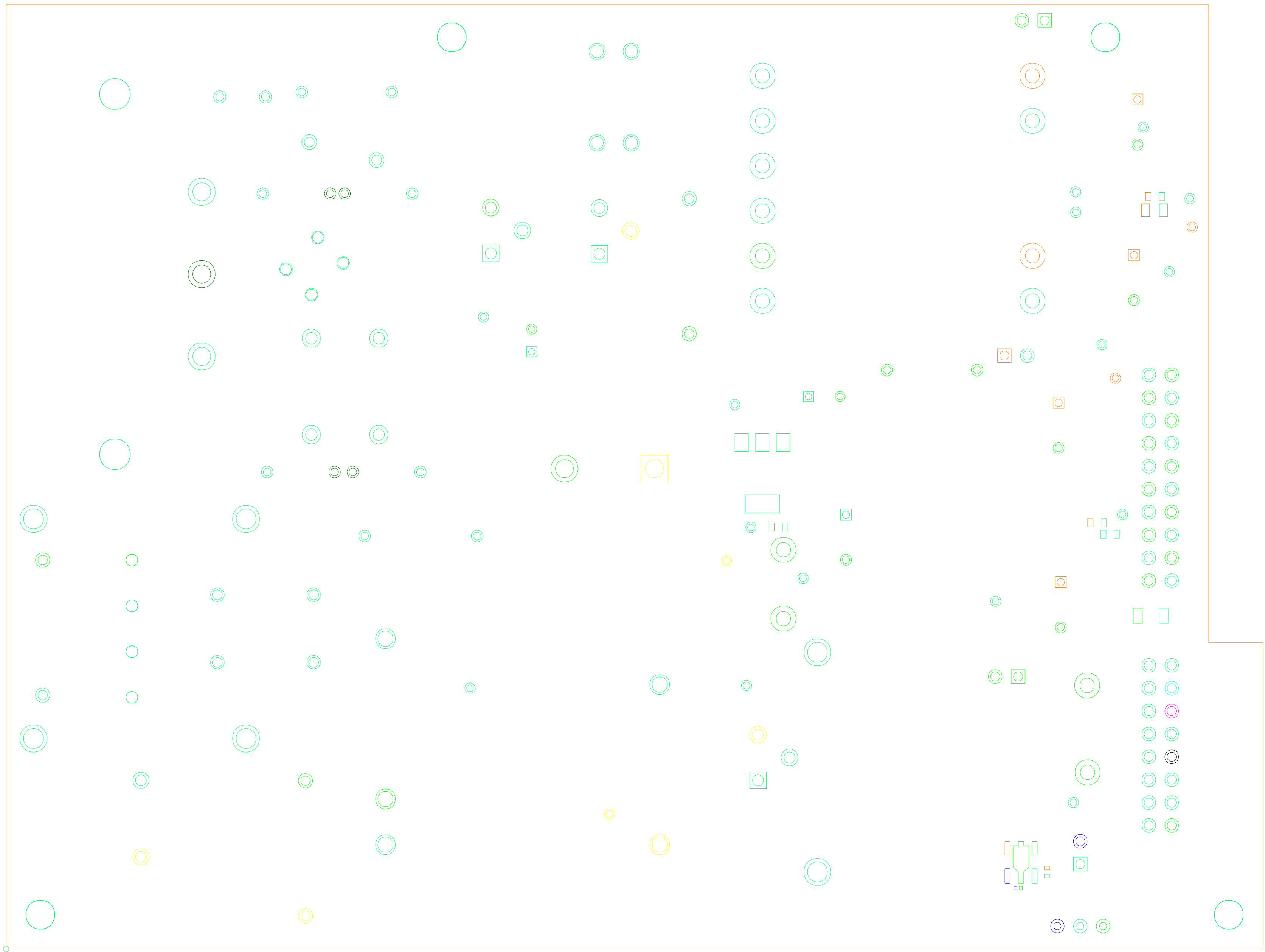
UNLESS OTHERWISE SPECIFIED	SIGNATURES	DATE
DIMENSIONS ARE IN MILS TOLERANCES ON:	DRAWN: THOMAS ASHE	02/07/19
	CHECKED: THOMAS ASHE	02/07/19
	ENGRG: THOMAS ASHE	02/07/19
	ISSUED: THOMAS ASHE	02/07/19

ON SEMICONDUCTOR

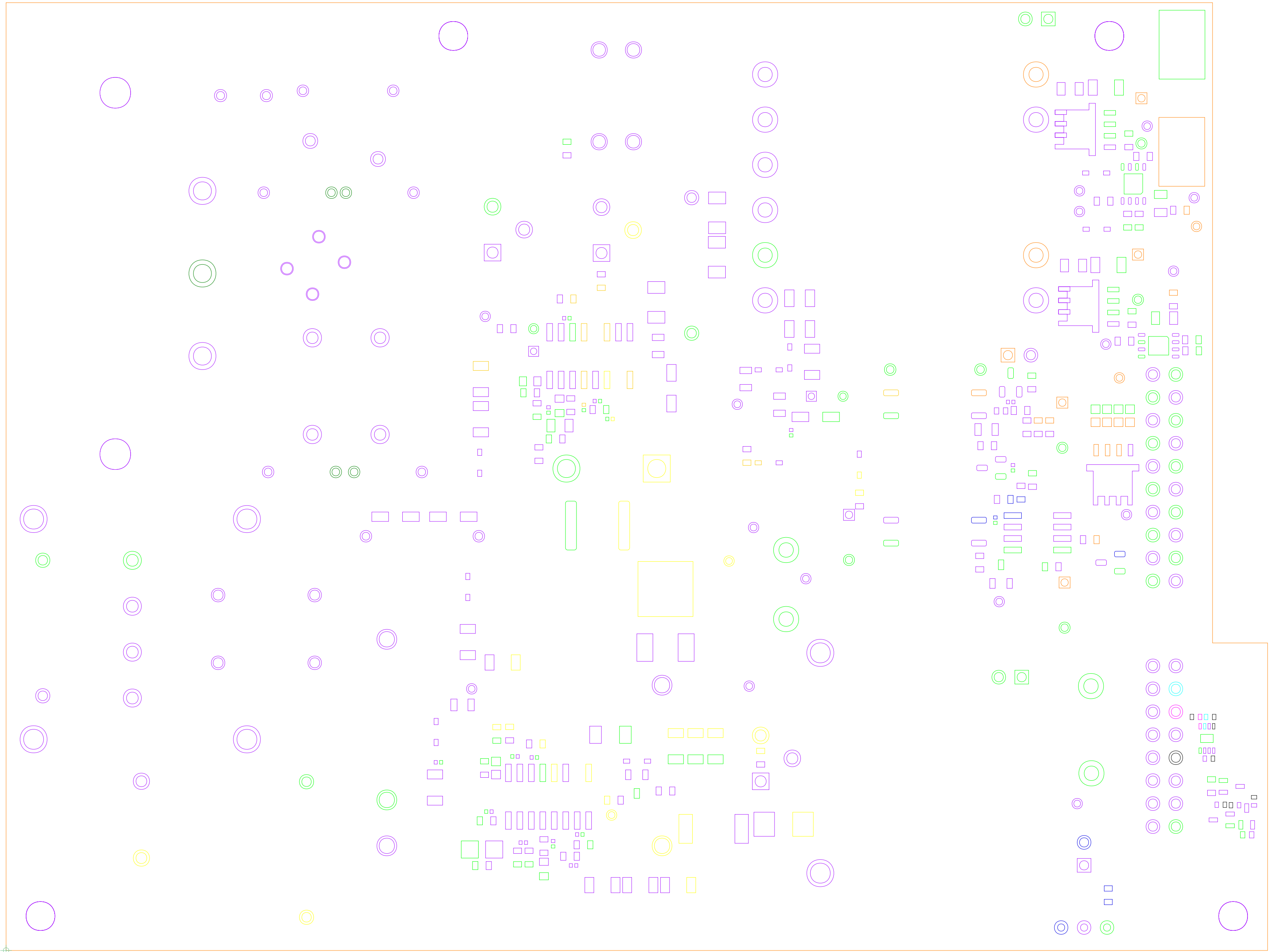
200W LLC W/ PFC

SIZE: D | REVISION: REV1 | DWG NO: ONSEC-18-022

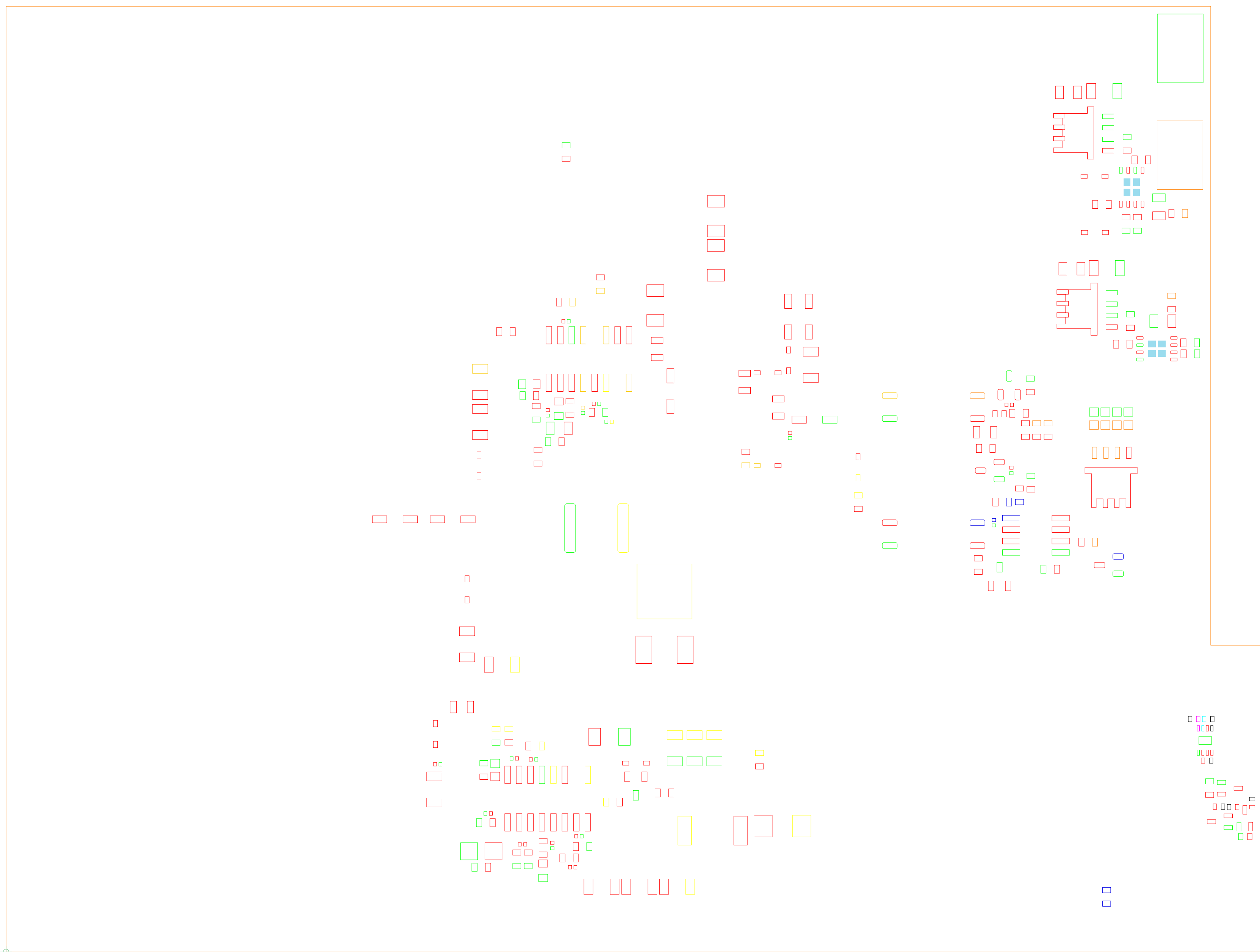
SCALE: 1/1 | DRAWING: FABRICATION | SHEET: 1 OF 3

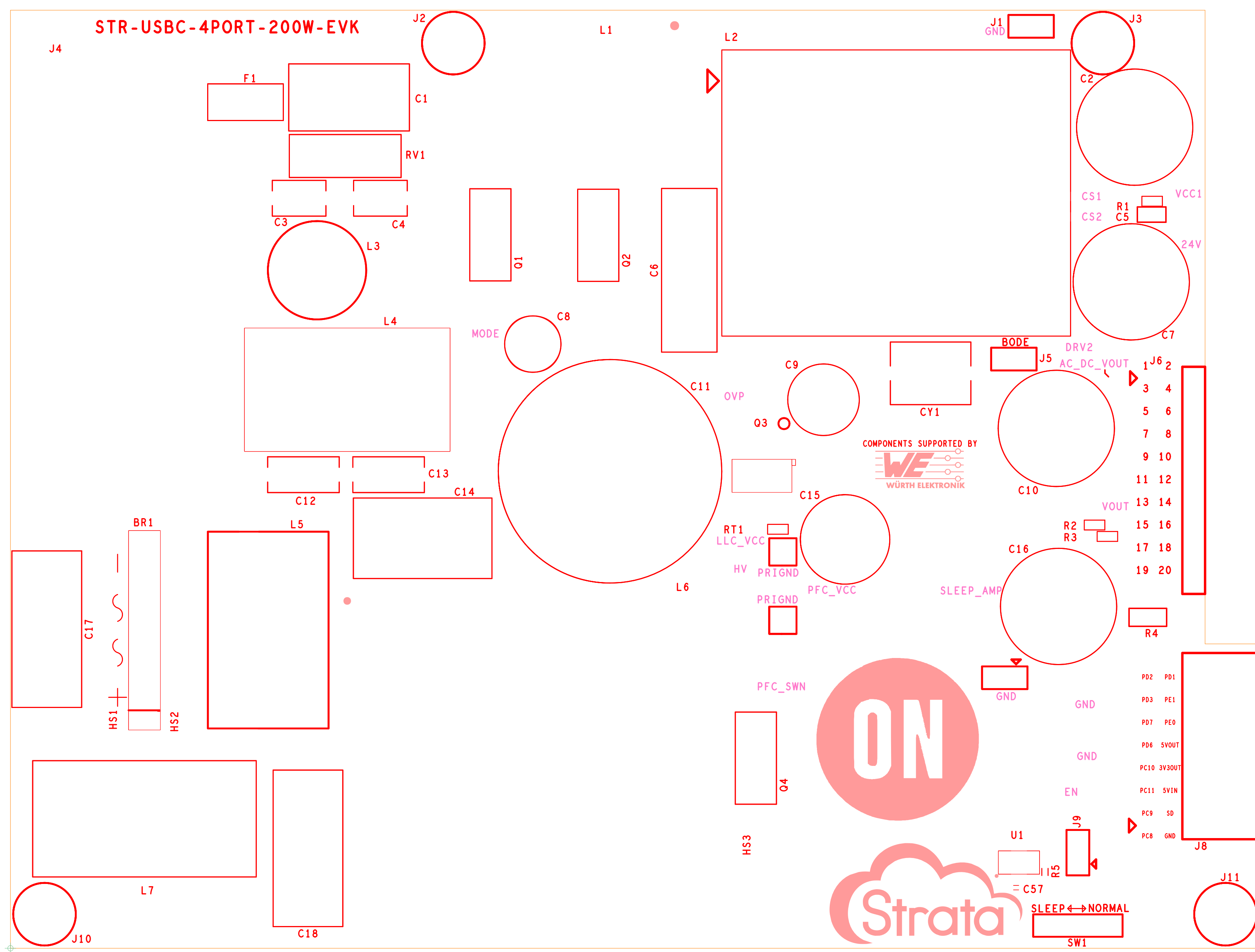


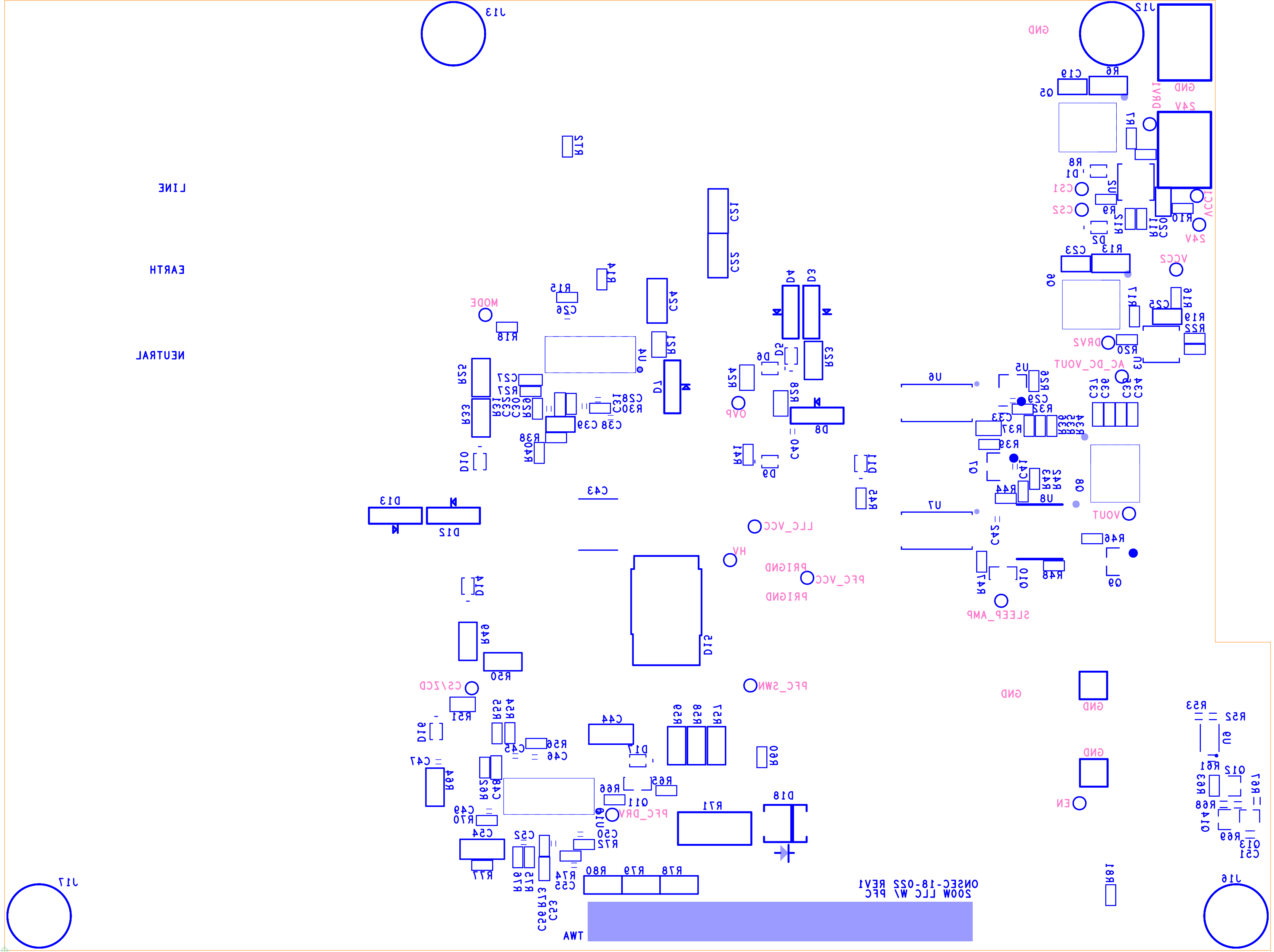
ART FILM - SMASKTOP

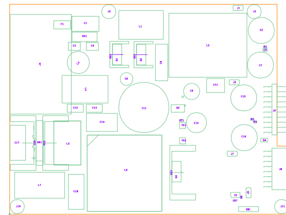


ART FILM - SMASKBOT



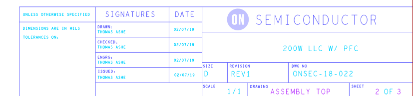

STR-USBC-4PORT-200W-EVK
J4
F1
C1
RV1
J2
L1
L2
J1
GND
J3
C2
C3
C4
L3
Q1
Q2
C6
CS1
CS2
R1
C5
VCC1
24V
L4
MODE
C8
C7
BODE
J5
DRV2
AC_DC_VOUT
J6
C9
C11
OVP
Q3
CY1
C10
COMPONENTS SUPPORTED BY
WÜRTH ELEKTRONIK
C12
C13
C14
C15
BR1
L5
RT1
LLC_VCC
HV
PRIGND
PFC_VCC
VOUT
R2
R3
C16
L6
SLEEP_AMP
R4
C17
HS1
HS2
PFC_SWN
GND
PD2 PD1
PD3 PE1
PD7 PE0
PD6 5VOUT
PC10 3V3OUT
PC11 5VIN
PC9 SD
PC8 GND
EN
Q4
ON
HS3
U1
J9
R5
C57
J8
L7
C18
J10
J11
Strata
SLEEP NORMAL
SW1





ASSEMBLY TOP NOTES (UNLESS OTHERWISE SPECIFIED):

1. ASSEMBLE AND INSPECT PER IPC-A-610 CLASS 3.
2. SOLDER, FLUX, AND ROHS TYPES SHOULD BE DEFINED IN QUOTATION FROM MANUFACTURER.
3. IF BARE BOARDS ARE SUPPLIED BY ON SEMICONDUCTOR THEY WILL BE AN <ARRAY OR INDIVIDUAL PEICES>.
4. ONLY PARTS CONTAINED IN BILL OF MATERIALS SHALL USED FOR TURN-KEY ASSEMBLY UNLESS EQUIVALENT PART APPROVED BY ON SEMICONDUCTOR.
5. REMOVE ANY KAPTON TAPE COVERING COMPONENTS EXCEPT FOR IMAGE SENSORS WHERE IT SHOULD ONLY BE REMOVED IF LENS OR LENS HOLDER INTERFERE WITH KAPTON TAPE REMOVAL.
6. "DNI" REFERENCE IN BILL OF MATERIALS MEANS DO NOT INSTALL AND THESE PARTS ARE NOT REQUIRED FOR BOARD BUILD.
7. RETURN ALL CONSIGNED AND TURN-KEY UNASSEMBLED OR EXTRA COMPONENTS WITH ASSEMBLED PCBS.
8. REFLOW HEAT PROFILE IS REQUIRED BY ASSEMBLER TO ENSURE PROPER SOLDER ATTACH.
9. HIDDEN PINS SUCH AS BGA PACKAGES ARE REQUIRED TO BE X-RAY'ED FOR PROPER SOLDER ATTACH.
10. NO ARRAY MOUSE BITES ARE ALLOWED ON EDGE OF FINISHED PCB. USE PLUNGE ROUTER TO REMOVE AFTER ASSEMBLY.
11. SOLDERMASK BARREL RELIEF TO AVOID ASSEMBLY ISSUES ON LARGE SURFACE MOUNT PADS IS ACCEPTABLE.
12. IF ASSEMBLY BOTTOM NOTES ARE NOT FOUND USE TOP NOTES.
13. PLACE HEAT SINKS FOR BR1 THEN FASTEN TO BR1 BEFORE PLACING L5
14. PLACE BR1 BEFORE OTHER THROUGH HOLE PARTS - REQUIRED FOR HEATSINK SPACING
15. Q1 AND Q2 USE PROVIDED HEATSINKS, NOT LISTED IN BOM - PLEASE MOUNT THESE TO THE TO220 PACKAGE
16. L6 REQUIRES PIN 12 TO BE REMOVED BEFORE PLACING



ASSEMBLY BOTTOM NOTES (UNLESS OTHERWISE SPECIFIED):

1. USE ASSEMBLY TOP NOTES.

ON SEMICONDUCTOR

200W LLC W/ PFC

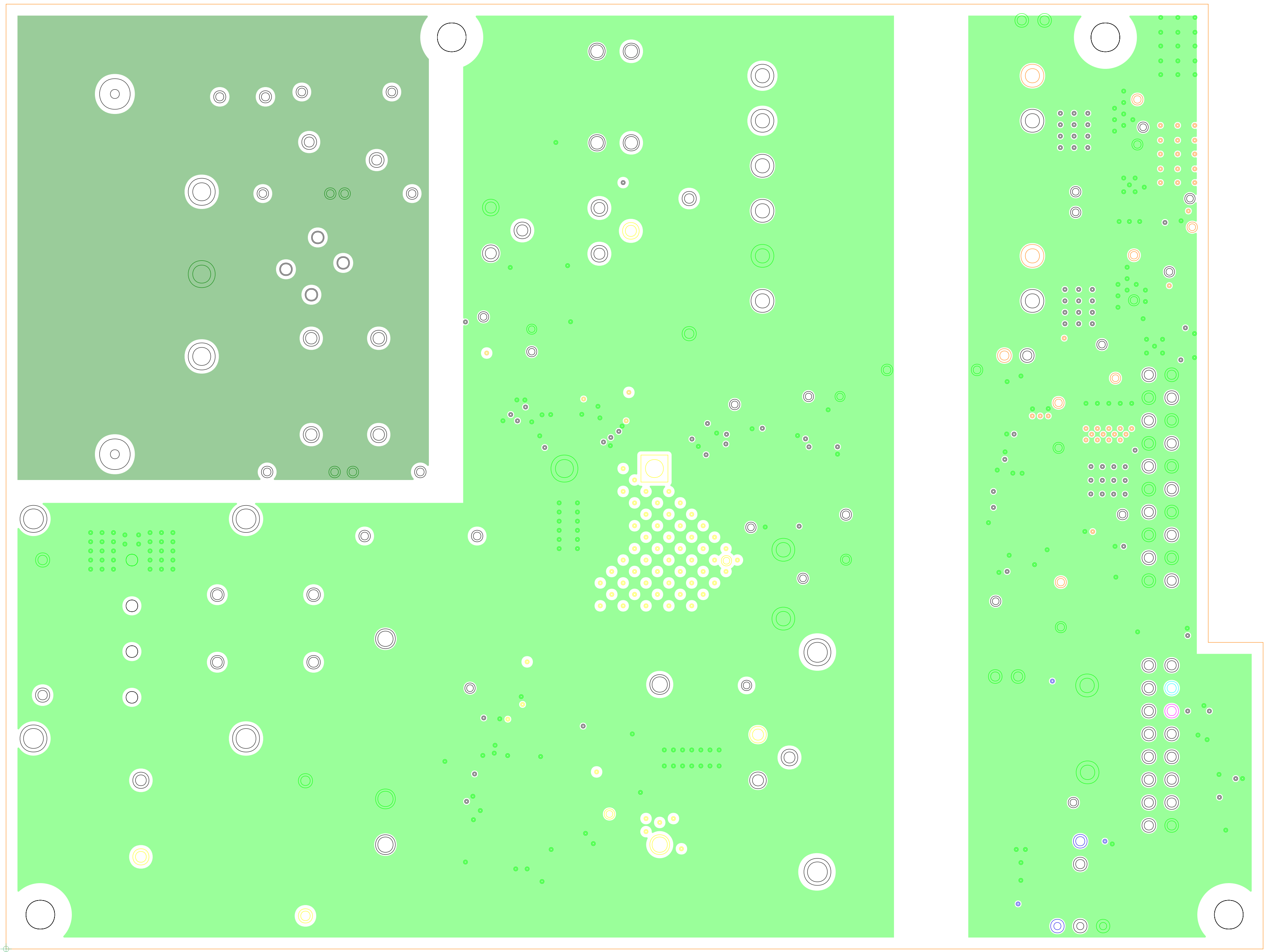
DWG NO	ONSEC-18-022
REVISION	REV1
SIZE	D
SHEET	3 OF 3
DRAWING	ASSEMBLY BOTTOM
SCALE	1/1

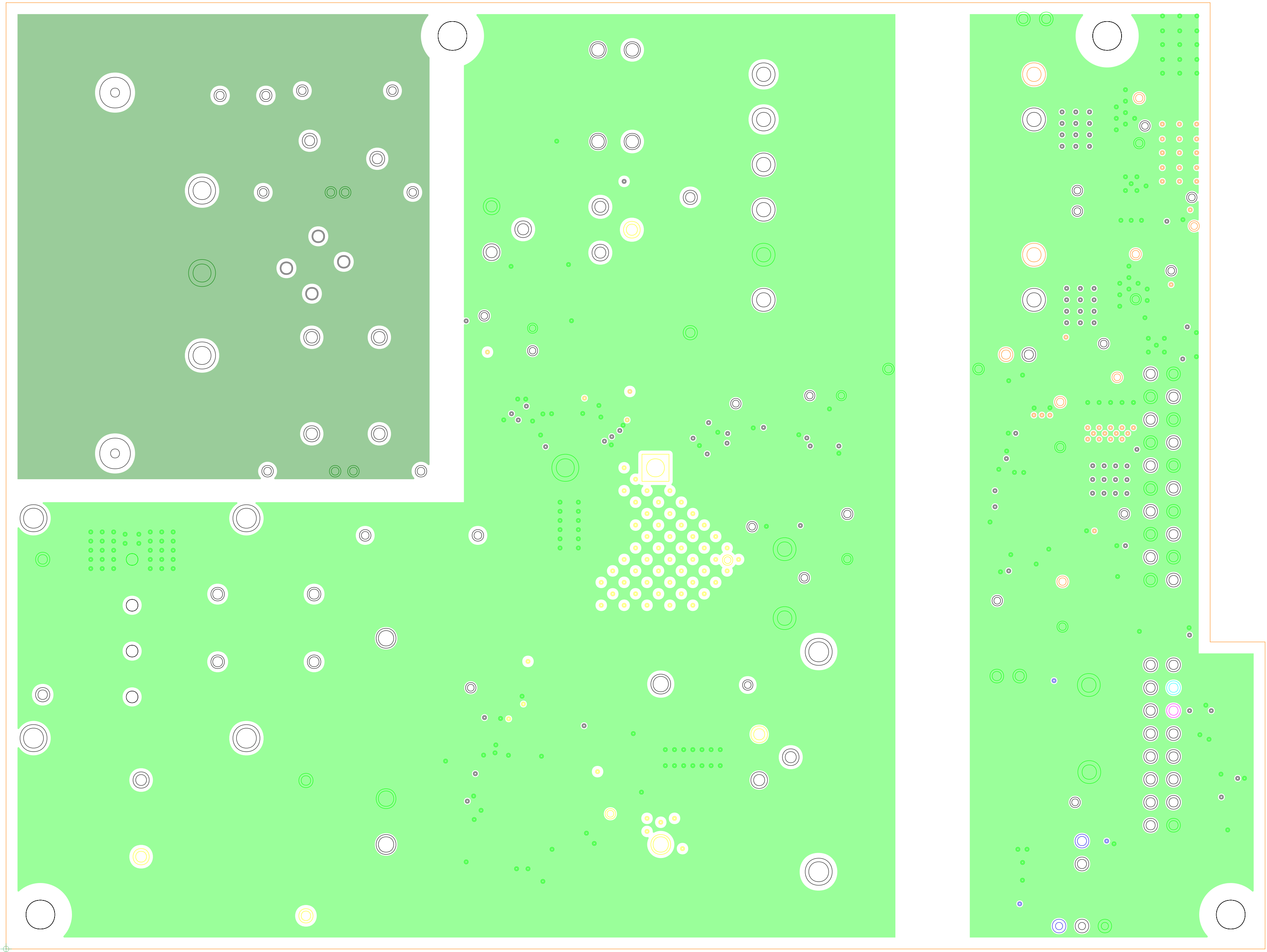
DATE	SIGNATURES
02/07/19	DRAWN: THOMAS ASHE
02/07/19	CHECKED: THOMAS ASHE
02/07/19	ENGRG: THOMAS ASHE
02/07/19	ISSUED: THOMAS ASHE

UNLESS OTHERWISE SPECIFIED

DIMENSIONS ARE IN MILS

TOLERANCES ON:





ART FILM - L3