AK5406

80MSPS Triple ADC for Displays

General Description

The AK5406 is an RGB Graphic & D-terminal Signal Process Device in which integrates 10-Bit 80Mhz AD Converters.
The Device has On-Chip 3 Channels ADCs, Voltage Reference circuit, Programmable Gain Offset Amplifiers and Black Loop Function which automatically sustains Clamp Level to an arbitrarily set value.

Features

- ADCs 80 MSPS max. (Internally 10-bit, Output is reduced to 8-bit)
- 0.5V ~ 1.0V input signal range
- Black Loop (Automatic Offset adjust) function
- Low Clock Jitter
- On-Chip SYNC Separation function
- Pedestal Clamp and Mid-Point Clamp function
- Power Down function
- Low Power Dissipation
- 3.3V ± 0.3V power supply
- CMOS
- -40℃ to 85℃
- Package 80-LQFP

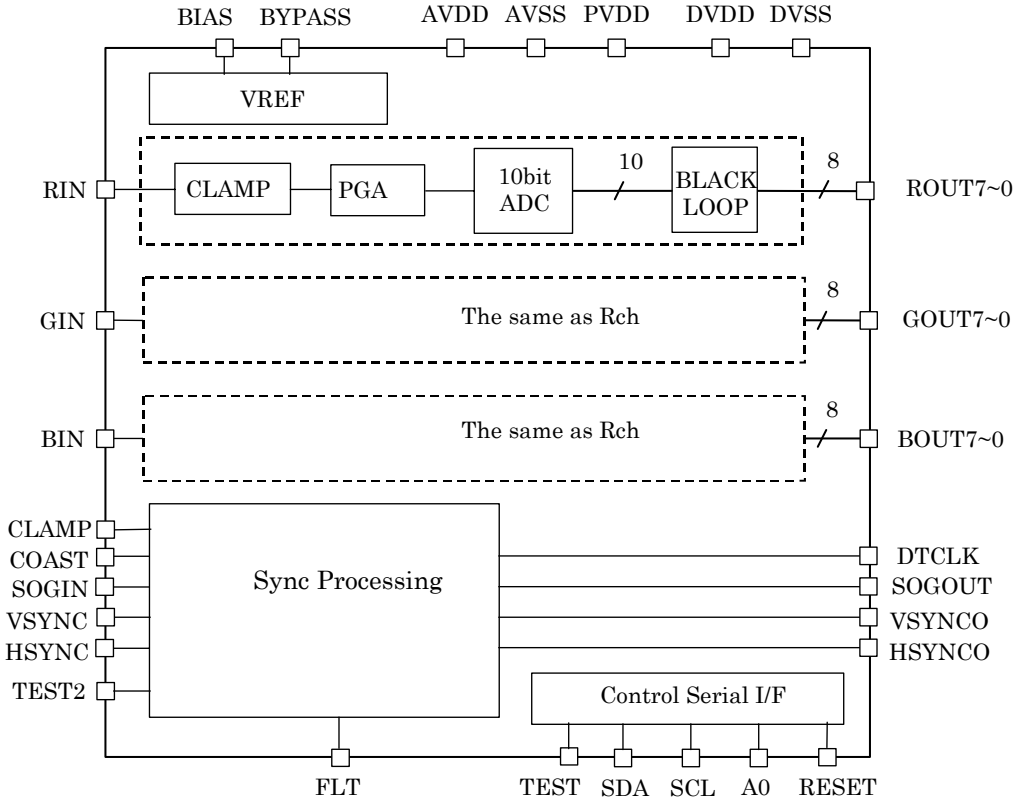


Fig. 1 Block Diagram

■ Functional Block Description

Table 1 : Block Description

block	Function	
CLAMP	To Clamp Pedestal level of input signal during Clamp period.	
PGA	Programmable Gain Amplifier. It has 8-bit resolution. Full-scale input range of ADC can be pre-set from 0.5V to 1V.	
ADC	10-bit 80 MSPS AD Converter.	
BLACK LOOP	A loop to settle Pedestal level to the Black set value. Can be disable by register setting.	
VREF	To generate internal reference voltage.	
Control Serial I/F	Control register with I²C Interface (400KHz).	
Sync Processing	To generate timing signals such as ADC operating clock, from Horizontal / Vertical SYNC signal inputs.	
	SLICER	Comparator to slice SYNC signal part in SYNC-ON-Green signal.
	PLL	PLL to generate Pixel Clock from Horizontal SYNC signal
	COAST GEN	To generate Coast signal from VSYNC.
	CLAMP GEN	To generate Clamp signal from HSYNC.
	CLP COAST	To execute Coast processing on Clamp signal.
	SYNC SEP	To separate VSYNC from Slicer output.

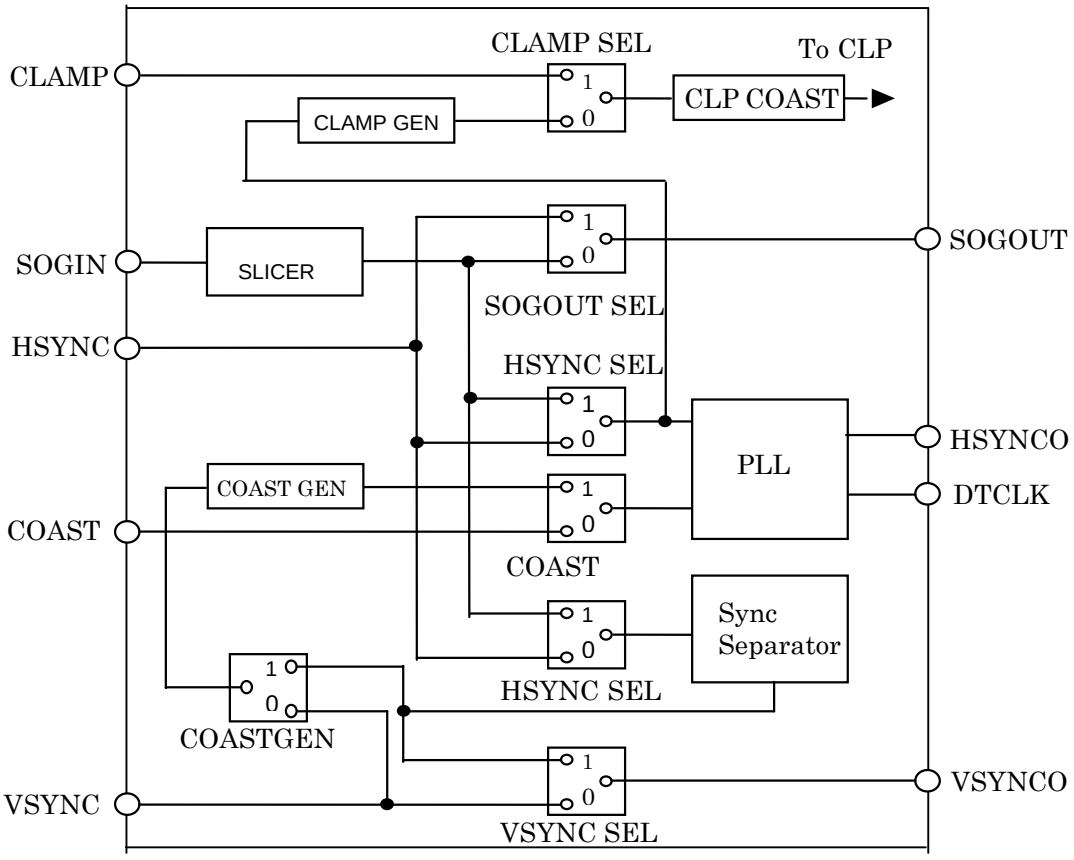
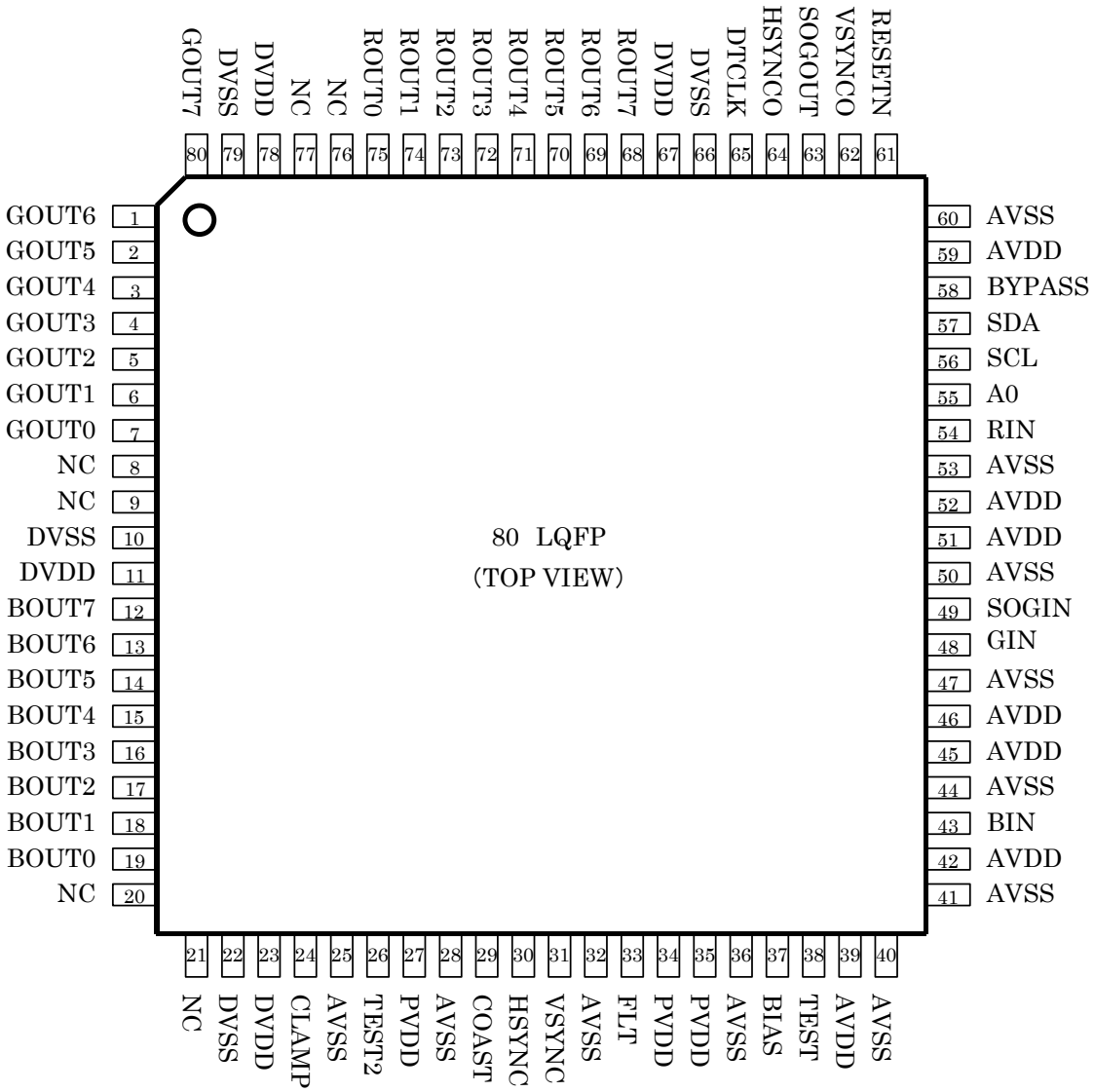


Fig. 2 Sync Processing

■ Pin Allocations



■ Pin Functions

Table 2 : Pin Functions

	Pin name	I/O	Functions
Output Pins			
64	HSYNCO	DO	Horizontal SYNC output. HSYNC output which is re-configured HSYNC input signal by internal timing. It is phase-synchronized with DTCLK. When phase of DTCLK is modified by Clock Phase Adjust register setting, this output phase also changes in sync with it.
62	VSYNCO	DO	Vertical SYNC output. Either VSYNC input or Sync Separator could be output.
63	SOGOUT	DO	Sync-On-Green Slice comparator output.
Serial Interface (I²C) Pins			
57	SDA	DI/ DO	Data I/O pins
56	SCL	DI	Clock
55	AO	DI	Address
61	RESETN	DI	Register initialization signal input (active low).
Data Pins			
68 ~75 80, 1~7 12 ~19	ROUT7 ~ROUT0 GOUT7 ~GOUT0 BOUT7 ~BOUT0	DO	RED channel ADC outputs GREEN channel ADC outputs BLUE channels ADC outputs Bit 7 is the MSB. They are output in sync with DTCLK. When DTCLK phase is modify by Clock Adjust register setting, these output phases also change in sync with it.
Data Clock Pins			
65	DTCLK	DO	Strobe clock for Data and HSYNCO. It is generated by PLL and synchronized with internal ADC sampling clock. Its phase changes in accordance with Clock Phase Adjust register setting. It is phase-synchronized with HSYNCO and Data.
Input Pins			
54 48 43	RIN GIN BIN	AI	RED channel analog input. GREEN channel analog input. BLUE channel analog input. 0.5V~1.0V full scale input. Each input signal is AC-coupled to each pin and clamp operation is executed.
30	HSYNC	DI	Horizontal SYNC input. Reference Clock input to generate DTCLK clock by the on-chip PLL (it is also possible to input Sync-On-Green signal on SOGIN pin as Reference Clock). Active polarity of input signal is selectable by register setting. Leading edge is used for this and trailing edge is ignored.
31	VSYNC	DI	Vertical SYNC input.
49	SOGIN	AI	Sync-On-Green input. Comparator input pin to extract SYNC signal from Sync-On-Green signal. Comparator threshold level is adjustable by register setting (10 ~ 320mV / step). When this pin is not used, connect to AVDD directly or connect to AVSS via a 1nF capacitor.

38	TEST	DI	Test pin. Connect to AVSS. This pin has an on-chip pull-down resistor.
29	COAST	DI	Clock control coast input. Upon application of this Coast input, PLL stops to synchronize with Horizontal SYNC signal and starts to self-run the oscillation. It is also possible to use internally generated timing from VSYNC, without using this pin. Connect to AVSS when not used.
24	CLAMP	DI	External Clamp input. Input pin to select timing in order to clamp Video input to an internal, pre-set value.
26	TEST2	DI	Test pin. Connect to PVDD through MOS SW internally.
Decoupling capacitor etc. connection pins			
58	BYPASS	AO	Bypass capacitor connection pin for Reference Voltage. Connect a 0.1uF capacitor between this pin and AVSS.
37	BIAS	AO	Bias Current pin for internal Analog circuit. Connect a 6.8kΩ ±1% resistor between this pin and AVSS.
33	FLT	AO	External Filter connection pin for PLL. This pin is internally fixed to PVDD at power-down mode.
Power Supply pins			
39 42 45 46 51 52 59	AVDD	PWR	Analog power supply pins.
11 23 67 78	DVDD	PWR	Digital power supply pins.
27 34 35	PVDD	PWR	Power supply pins for PLL.
25 28 32 36 40 41 44 47 50 53 60	AVSS	PWR	Analog ground pins.
10,22 66,79	DVSS	PWR	Digital ground pins.
NC Pins			
8,9, 20,21 76,77	NC	NC	NC pins. Left open.

AI : Analog Input pin, AO : Analog Output pin
DI : Digital Input pin, DO : Digital Output pin, PWR : Power Supply / Ground pin
DI pins be free from Hi-Z input.
DO pins set to be Hi-Z output state by register setting.

■ Absolute Maximum Ratings

Table 3 : Absolute Maximum Ratings (AVSS, DVSS = 0V ; all voltages are referenced to ground level)

Item	Symbol	Min	Max	Unit	Note
Power Supplies Analog Digital PLL	 AVDD DVDD PVDD	 -0.3 -0.3 -0.3	 4.5 4.5 4.5	 V V V	
Input Current (excluding power supply pins)	IIN		±10	mA	
Analog Input Voltage	VINA	AVSS-0.3	AVDD+0.3	V	RIN, GIN, BIN, SOGIN
Digital Input Voltage	VINL	AVSS-0.3	AVDD+0.3	V	SDA, SCL, A0, RESETN
Digital Input Voltage	VINL2	AVSS-0.3	PVDD+0.3	V	VSYNC, HSYNC, CLAMP, COAST, TEST, TEST2
Input Voltage at Hi-Z condition (Data Output pin)	VONL	DVSS-0.3	DVDD+0.3	V	ROUT,GOUT,BOUT, HSYNCO, VSYNCO, SOGOUT, DTCLK
Storage Temperature	Tstg	-65	150	°C	

(note) Operation under a condition exceeding above limits may cause permanent damage to the device. Normal operation is not guaranteed under the above, extreme conditions.

■ Recommended Operating Conditions

At the power-up, the AK5406 device must be reset using RESETN pin.

Table 4 : Recommended Operating Conditions

(AVSS, DVSS = 0V ; all voltages are referenced to ground level)

Item	Symbol	Min	TYP	MAX	Unit	Note
Power Supplies Analog Digital PLL	 AVDD DVDD PVDD	 3.0 3.0 3.0	 3.3 3.3 3.3	 3.6 3.6 3.6	 V V V	
Operating Temperature Range	Ta	-40		85	°C	

■ Electrical Characteristics

1) Analog Characteristics

(AVDD = DVDD = PVDD = 3.3V, Ta = 25°C, sampling frequency at 80 MSPS, input signal frequency = 1MHz, input signal amplitude = -2 dBFS unless otherwise noted)

Table 5.

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Range						
at maximum gain	IRNG1				0.5	V
at minimum gain	IRNG2		1.0			V
Input Full Scale Matching	IRNGM	at minimum gain			10	%FS
Static Characteristics						
Differential Non-Linearity	DNL	(note 1)		±0.5	±1.0	LSB
Integral Non-Linearity	INL	(note 1)		±1.0	±3.0	LSB
Offset	VOF				±47	LSB
Dynamic Characteristics						
S/N	SNR			46		dB
Cross-Talk	CT	Input Frequency = 7.5MHz		55		dBc
PLL Jitter	TJ	(note 2)		300		ps rms
Power Dissipation						
Analog	IA			180		mA
Digital	ID	(note 3)		24		mA
PLL	IP			15		mA
Total	IT			219	290	mA
At Power-Down	IPD	(note 4)		1.5	2.6	mA

(note 1) Measured at gain = 80H (Address : 08H, 09H, 0AH)

(note 2) VCO range = 2H, charged pump current = 3H (Address : 05H), PLL Div : 2200(897H), fH=33.75kHz, CLK=74.25MHz

(note 3) Capacitive loadings

CL = 15pF (DTCLK pin)

CL = 5pF (ROUT, GOUT, BOUT, HSYNCO, VSYNCO pins)

(note 4) During power-down, SOG Slicer & Slicer VREF and I²C Control circuits are active.

2) Digital Input / Output DC Characteristics

Table 6 : Digital DC Characteristics
(AVDD = DVDD = PVDD = 3.0 ~ 3.6V, AVSS = DVSS= 0v, Ta = -40 ~ 85°C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
High Level Input Voltage	VIH	A0, RESETN pins	0.7AVDD			V
Low Level Input Voltage	VIL	A0, RESETN pins			0.3AVDD	V
High Level Input Voltage	VIHP	VSYNC, HSYNC, COAST, CLAMP pins	0.7PVDD			V
Low Level Input Voltage	VILP	VSYNC, HSYNC, COAST, CLAMP pins			0.3PVDD	V
Input Pin Leakage Current	ILIKG	HSYNC,VSYNC,CLAMP, COAST pins			±10	uA
High Level Output Voltage	VOH	ROUT, GOUT, BOUT, HSYNCO, VSYNCO, SOGOUT pins IOH=-1mA	DVDD-0.5			V
Low Level Output Voltage	VOL	ROUT, GOUT, BOUT, HSYNCO, VSYNCO, SOGOUT pins IOL=1mA			0.5	V
DTCLK pin High Level Output Voltage	VOHC	DTCLK pin IOH= -4mA	DVDD-0.5			V
DTCLK pin Low Level Output Voltage	VOLC	DTCLK pin IOL= 4mA			0.5	V
Hi-Z Leakage Current	IOZ	ROUT, GOUT, BOUT HSYNCO, VSYNCO, SOGOUT, DTCLK pins at Hi-Z output			±10	uA
I²C High Level Input Voltage	VIH2	SDA, SCL pins	0.7AVDD			V
I²C Low Level Input Voltage	VIL2	SDA, SCL pins			0.3AVDD	V
I²C Low Level Output Voltage	VOL2	SDA pin, IOL=3mA			0.4	V

3) Switching Characteristics

Table 7 : Switching Characteristics
(AVDD = DVDD = PVDD = 3.0 ~ 3.6V, AVSS = DVSS = 0V, Ta = -40 ~ 85°C, CL of DTCLK pin = 15pF, CL of ROUT, GOUT, BOUT, HSYNCO pins = 5pF)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Conversion Speed maximum minimum	 fsmax fsmin		 80		 9	 MSPS MSPS
DTCLK duty			42	50	58	%
Data Skew	tskw	Referenced to the Falling edge of DTCLK output (note 1)	-1.0		4.0	ns
HSYNC Input Frequency			15		110	kHz
Reset Timing	trst	After the power-up	1			us

(note 1) 1/2 of VDD referenced

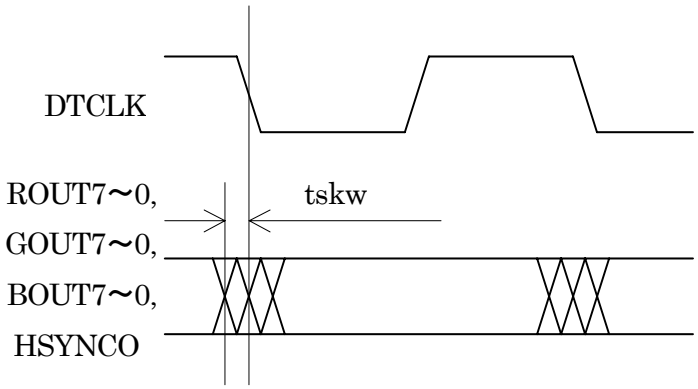


Fig. 4 Output Timing

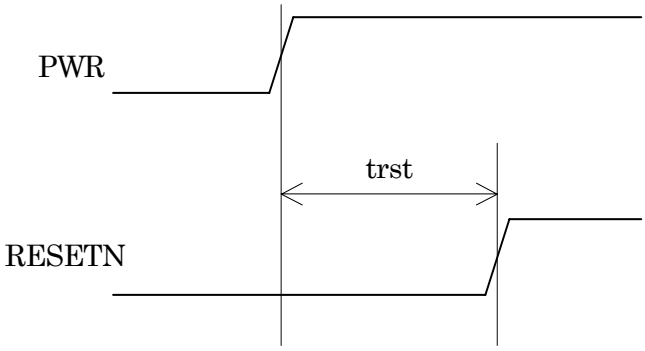


Fig. 5 Reset Timing

4) Serial I/F Switching Characteristics

Table 8 : Serial I/F Switching Characteristics
(AVDD = DVDD = PVDD = 3.0 ~ 3.6V, AVSS = DVSS = 0V, Ta = -40 ~ 85°C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Bus Free Time	t_{BUF}		1.3			us
Hold Time (Start Condition)	$t_{HD:STA}$		0.6			us
Clock Pulse Low Time	t_{LOW}		1.3			us
Input Signal Rise Time	t_R				300	ns
Input Signal Fall Time	t_F				300	ns
Setup Time (Start Condition)	$t_{SU:STA}$		0.6			us
Setup Time (Stop Condition)	$t_{SU:STO}$		0.6			us

The above I²C bus related timings are I²C Bus Specifications, and they are not the device limits.

For details, refer to I²C Bus Specifications.

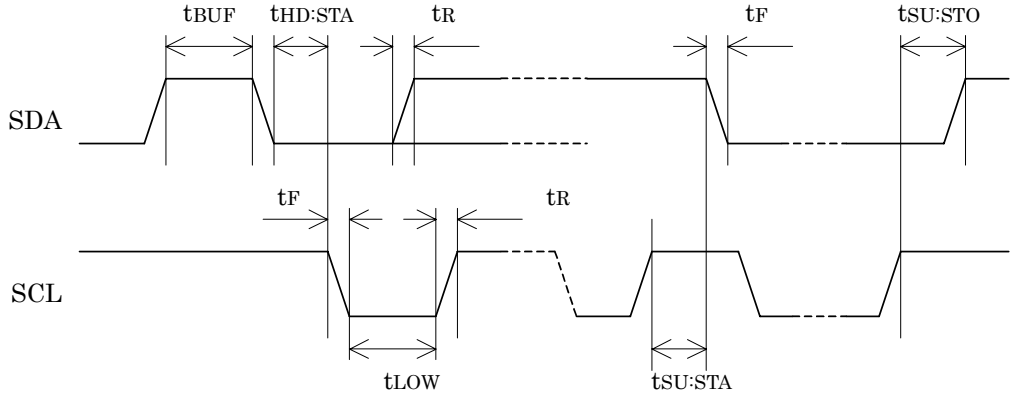


Fig. 6 Serial Control Timing

Table 9. (AVDD = DVDD = PVDD = 3.0 ~ 3.6V, AVSS = DVSS = 0V, Ta = -40 ~ 85°C)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Data Setup Time	$t_{SU:DAT}$		100 (note 1)			ns
Data Hold Time	$t_{HD:DAT}$		0.0		0.9 (note 2)	us
Clock Pulse High Time	t_{HIGH}		0.6			us

(note 1) when to use in I²C Bus Standard mode, $t_{SU:DAT} \geq 250$ns must be satisfied.
(note 2) when the AK5406 is used on non-extended t_{LOW} bus (used at t_{LOW} = minimum specification), this condition must be satisfied.

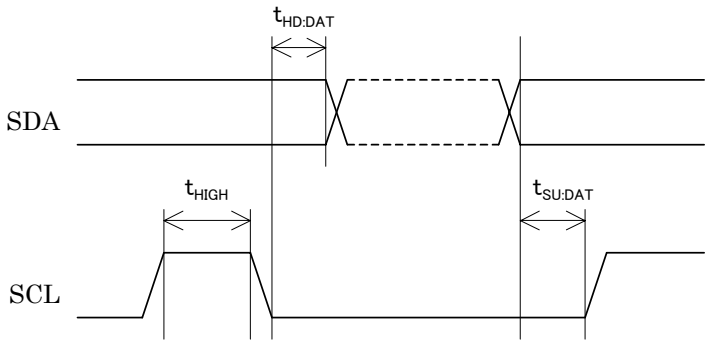


Fig. 7 Serial Control Timing (#2)

■ Functional Description

ADC

10-bit 80 MSPS A/D Converter, output is reduced to 8-bit.

Reset Operation

Reset Operation must be executed after the power-up.
Reset pulse can be fed in asynchronous fashion, with a pulse width of longer than 1 us.
Right after the reset operation, registers are set to their default.

PLL Function

The Pixel Clock is re-produced by PLL based on HSYNC to be input.
The AK5406 is corresponds from 9MHz to 80MHz of frequency by adjusting Charged Pump Current as PLL parameter.
The example of Charged Pump current calculation is shown below, and the closest value is setting to register (Address 0x03 bit 5:3).

AK5406 PLL Cpcurrent (CPI) calculation :

CPI = ((2pi*fH)/NFRatio)^2*C*N*P / Kvco;
fH : PLL reference signal (Horizontal SYNC signalin [Hz])
NFRatio : Set to each natural frequency
Reference signal is divided and set to 13.
C: 0.082uF
N: PLL divide ratio (Register Address 0x01, 0x02)
P: 4:<9-32MHz>, 2:<32-64MHz>, 1:<64-80MHz> Clock Frequency range.
Kvco: 130MHz

PLL Coast Funtion

The Pixel Clock is re-produced by PLL based on HSYNC to be input.
Coast mode is to cease its PLL tracking operation and to let VCO self-run.
There are 2 modes in Coast function –
One is HSYNC Pulse Duration Coast where the duration time is selected from Pre-VSYNC timing as start point and Post-VSYNC timing as stop point, and the other is to input directly on Coast pin a signal to notify its timing.
(refer to timing diagram 3) Coast Timing)

Clamp Function

This is a function to adjust reference level of AC-coupled input signal to match with the AK5406 internal reference level. It is required to specify a specific period where reference level of input signal is being input. It is selectable to specify the period by external CLAMP pin or by register setting. If the clamp period is specified by register, the position and the period from the trailing edge of HSYNC are set to the register. (refer to timing diagram 4) Clamp Timing #1)
During the clamp period the Analog Clamp circuit (Clamp Block) and the Black Loop circuit (Black Loop block) are operational at the same timing at the default setting. It is possible to set the Analog Clamp at the first half of clamp period and Black Loop at the other half during the clamp period by register setting. ((refer to timing diagram 5) Clamp timing #2) Clamp function can be coasted as in the case of PLL ((refer to timing diagram 6) Clamp Coast).
It is also possible by register setting to clamp the minimum value in accordance with RGB signals or to clamp the center value in accordance with YUV signals (refer to register address 10H).

Gain Adjust Function

ADC Full-Scale Input Range is adjustable within 0.5V ~ 1V by PGA (Programmable Gain Amplifier). PGA has an 8-bit resolution.

SYNC Separation Function

VSYNC is extracted from the internal Slicer output.

Black Loop Function, Offset Adjust Function

With a help of Black Loop operation during the Clamp period, offset of internal circuit can be eliminated and Clamp level is retained to the set value.
Black level is arbitrarily pre-settable for each of 3 channels independently, in the range from –4 to +20 by Black Loop Setting Value setting register.
In addition to enabling Black Loop function always during the Clamp period, it is also possible to control Black Loop function to operate or to hold the condition by register setting.
Black Loop function can be completely disabled.
Only in this case, each of channel offset adjust registers is valid and external offset adjustment is enabled.
Gain Offset Control diagram below shows its relation.

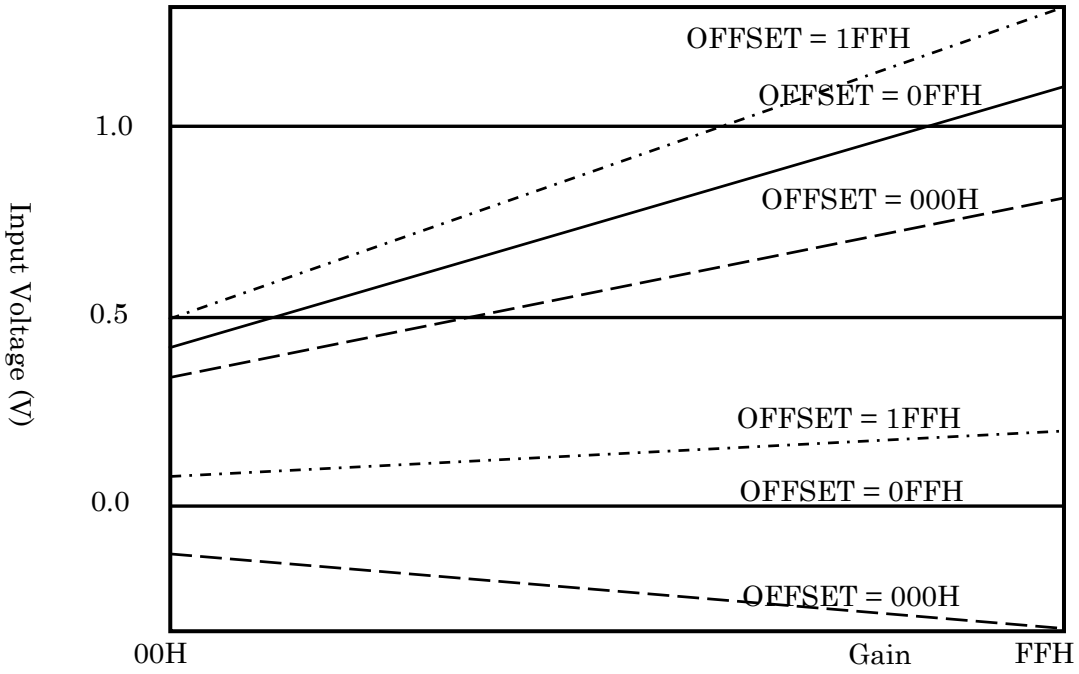


Fig. 8 Gain Offset Control

Control Serial I/F

This is a control register with I²C Serial Interface.
An external pull-up resistor should be connected on SDA pin.
Data on SDA line is captured at the rising edge of SCL.
Make certain that Data on SDA line changes state only during SCL at low condition.
When SDA changes state while SCL is at high condition, it is interpreted to be a Start condition if the change occurs at the falling transition, and it is to be a Stop condition if it occurs at the rising transition.

[I²C Slave Address]

I²C Slave Address is selectable to be either 1001100 or 1001101 by AO pin setting.

Table 10 : I²C Address

A0 pin	I²C Slave Address
LO	1001100
HI	1001101

[I²C Write Sequence]

When the Slave Address of the AK5406 Write Mode is received at the First Byte, Sub-Address at the Second Byte and Data at the Third & Succeeding Bytes are received.

There are 2 operations in Write sequence –

(a) Single Byte Write Sequence

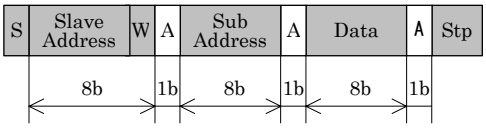


Fig. 9a Single Byte Write Sequence

(b) Multiple Byte (m bytes) Write Sequence (Sequential Write operation)

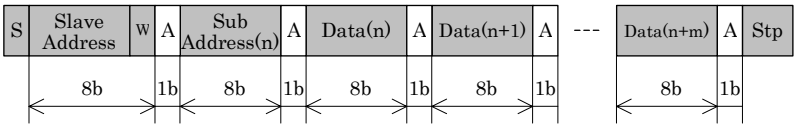


Fig. 9b Sequential Write

(c) Read Sequence

When the Slave Address of the AK5406 Read Mode is received at the First Byte, Data at the second & Succeeding Bytes transmitted from the AK5406.

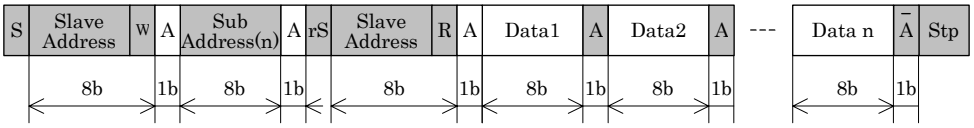


Fig. 9c Read Sequence

Abbreviation terms listed above mean :

S,rS	Start Condition	
A	0:Acknowledge	(SDA Low)
Ā	1:Not Acknowledge	(SDA High)
Stp	Stop Condition	
R/W	1:Read, 0:Write	
▭	To be controlled by the Master device. To be output by micro-computer normally.	
▭	To be controlled by the Slave device. To be output by the AK5406.	

■ Timing Charts

Reference register address
07H : (HSYNCO WIDTH)
0EH : HSYNC POL, HSYNCO POL

1) Output Timing

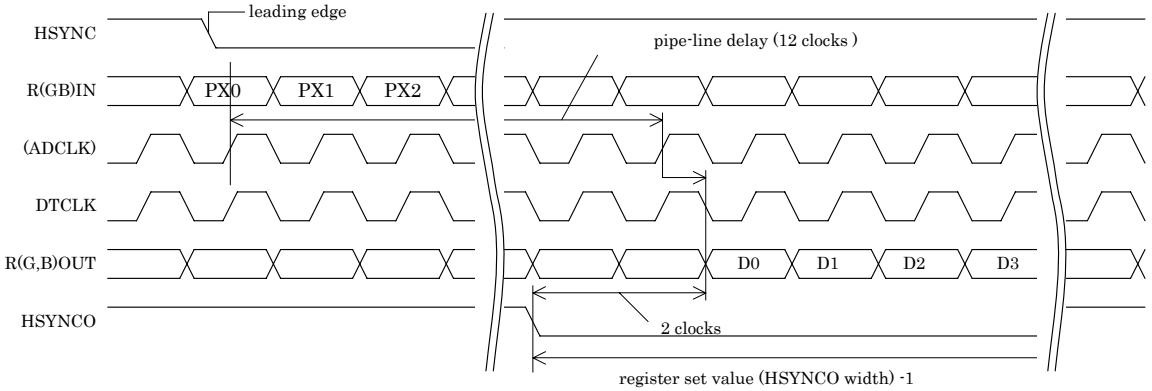


Fig. 10 Output Timing

2) 4 : 2 : 2 Output Mode Timing

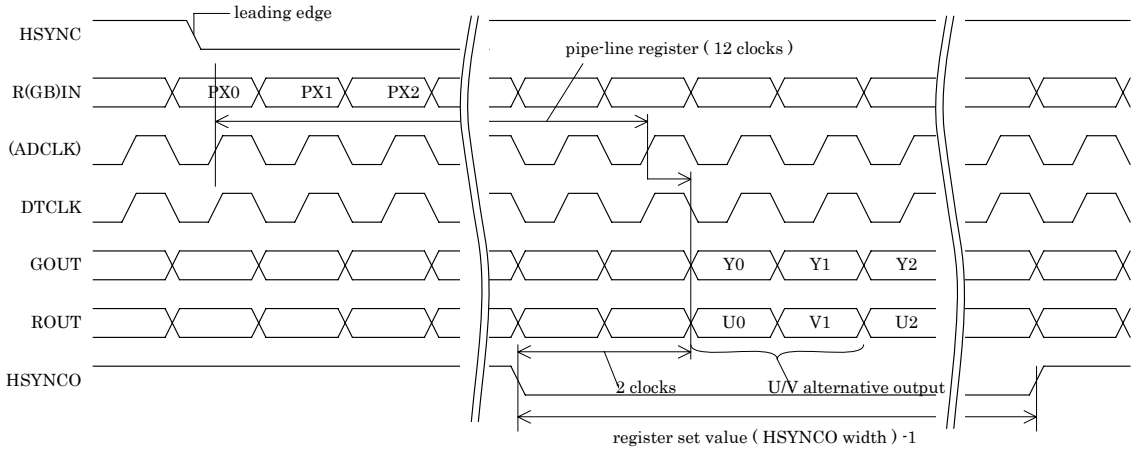


Fig. 11 4 : 2 : 2 Output Mode Timing

Reference register address
15H : Output Format

3) Coast Timing

Reference register address
0FH : COAST SEL, COAST POL
12H : PRE COAST
13H : POST COAST

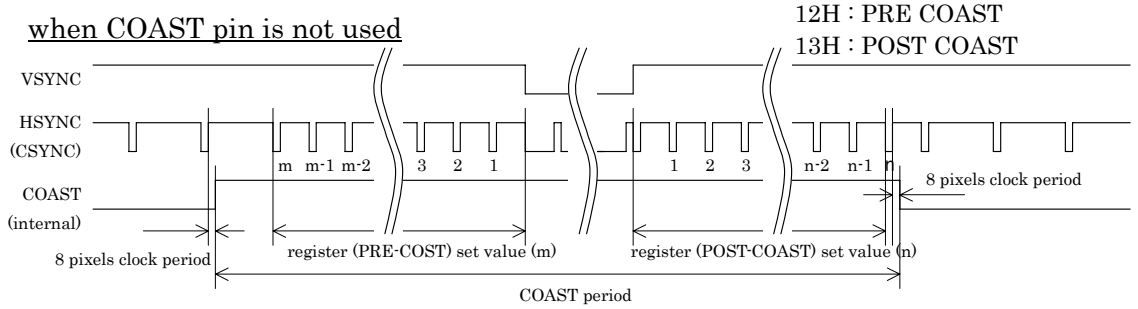


Fig. 13 COAST Timing

(note) Since PRE-COAST time is counted, based on # of lines in the previous Field, there is a case in the interlaced signal mode that COAST period may slightly differ between Odd Field case and Even Field case.

*525i Mode COAST example

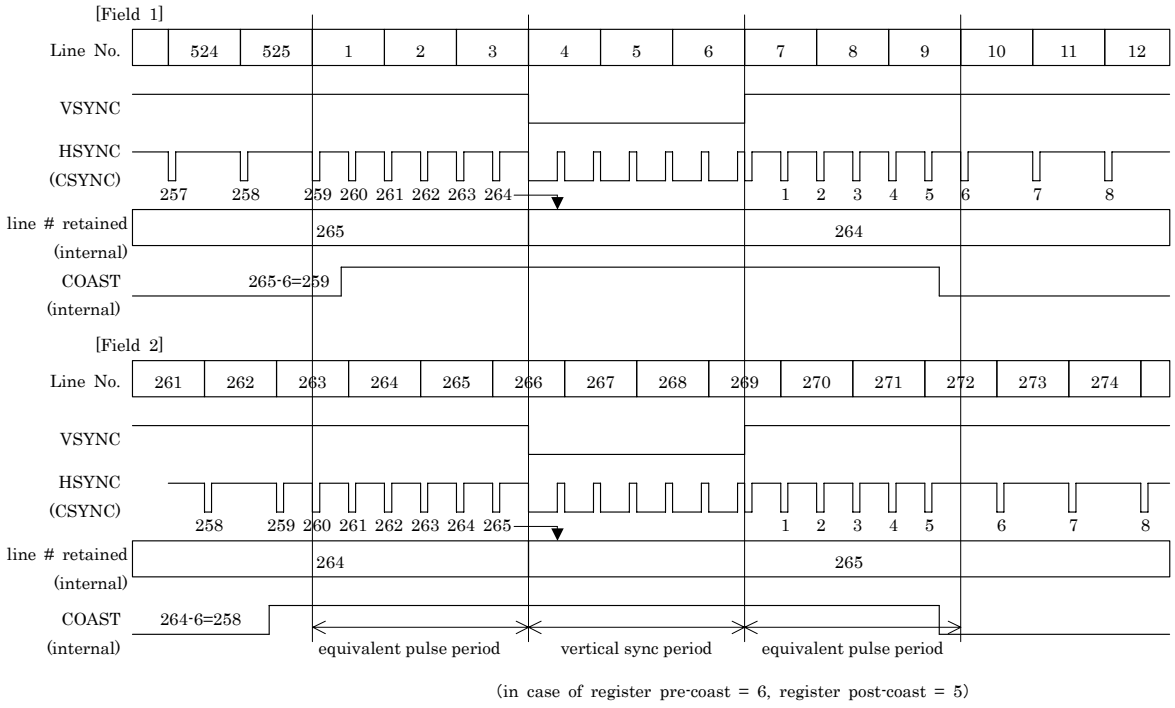


Fig. 14 COAST Timing (525i Mode Coast example)

when COAST pin is used

input signal fed on COAST pin is used as is, as internal coast signal.

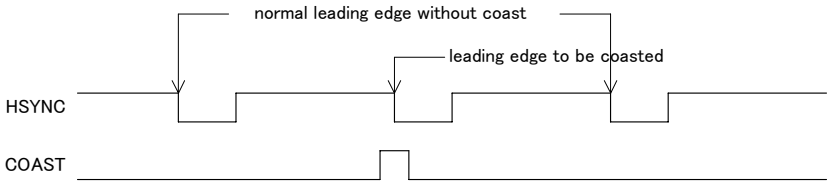


Fig. 15 COAST Timing (when COAST pin is used)

Reference register address
0FH : CLAMP SEL, CLAMP POL
05H : CLP PLACE
06H : CLP DURATION

4) Clamp Timing 1

when CLAMP pin is not used

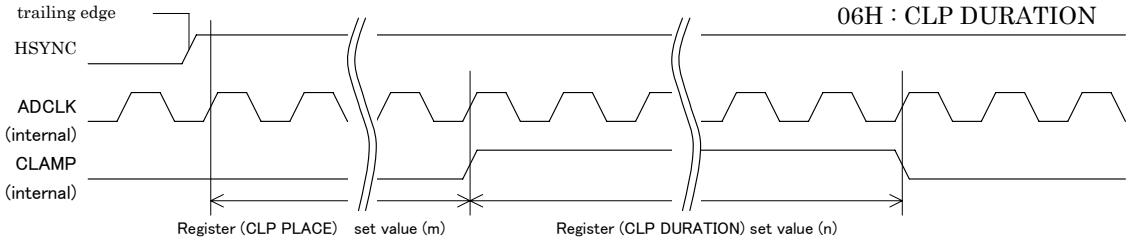


Fig. 16 Clamp Timing

when CLAMP pin is used

Externally feds clamp timing pulse from CLAMP pin.
Clamp timing pulse be sampled by ADCLK then used internally.

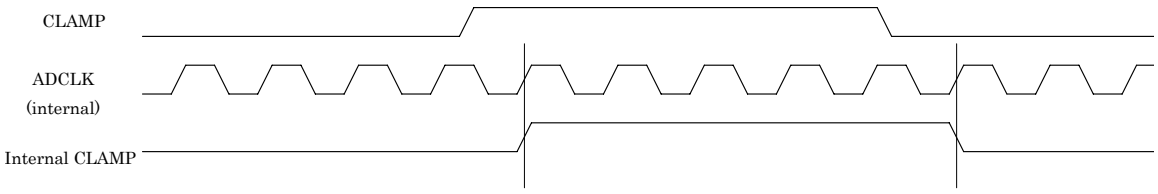


Fig. 17 Clamp Timing

5) CLAMP Timing 2

When register (LOOP DISABLE) is set to value (m) other than 0, the clamp period is divided into 2 half where it is possible that the Clamp Circuit operational at First half of the period (m pixels clock) and Black Loop at the other half.
When m = 0 (reset value), the Clamp Circuit and the Black Loop are operate at the same timing.

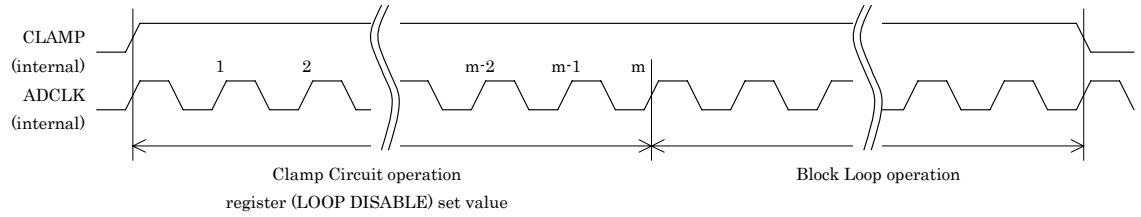


Fig. 18 Clamp Timing (#2)

Reference register address
26H : PRE CLPCOAST
27H : POST CLPCOAST

6) COAST Timing for Clamp

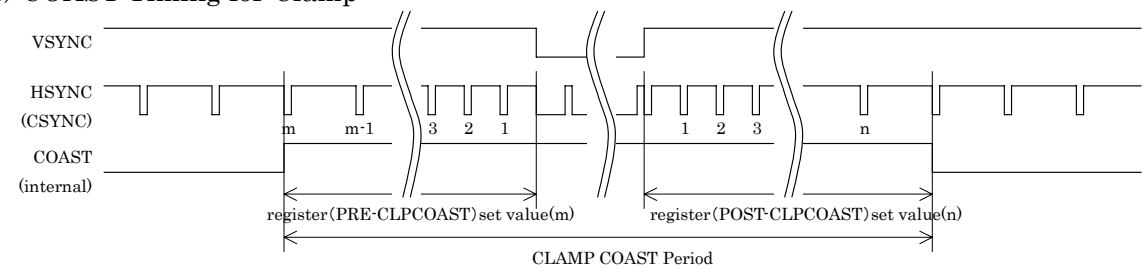


Fig. 19 Clamp Coast Timing

(note) Since PRE CLPCOAST time is counted, based on # of lines in the previous Field, there is a case in the interlaced signal mode that COAST period may slightly differ between Odd Field and Even Field case.
For details, refer to (3) COAST Timing section.

■ Control Register

Table 11 : Register map

Sub Adrs	R/W Or RO	Bits	Default Value	Register Name	Function
00H	RO	7:0	10101110	CHIPID	Device ID number
01H	R/W	7:0	01101001	PLL DIV (MSB)	Upper 8-bit PLL divider ratio[11:4]
02H	R/W	7:4	1101****	PLL DIV (LSB)	Lower 4-bit PLL divider ratio[3:0]
03H	R/W	7:6 5:3	01****** **001***	PLL VCO PLL CP	Bit [7:6] PLL VCO range Bit [5:3] PLL Charged Pump current
04H	R/W	7:3	10000***	PHADJ	Clock phase adjust (1LSB = T/32)
05H	R/W	7:0	10000000	CLP PLACE	Clamp position
06H	R/W	7:0	10000000	CLP DURATION	Clamp period
07H	R/W	7:0	00100000	HSYNCO WIDTH	HSYNCO pulse width
08H	R/W	7:0	10000000	RED GAIN	Red channel gain adjust
09H	R/W	7:0	10000000	GREEN GAIN	Green channel gain adjust
0AH	R/W	7:0	10000000	BLUE GAIN	Blue channel gain adjust
0B-0DH	RO	7:0	00000000		Reserved
0EH	R/W	6	*1******	HSYNC POL	Bit 6 : HSYNC input polarity setting (0 : Low 1 : Hi)
		5	**0*****	HSYNCO POL	Bit 5 : HSYNCO output polarity setting (0 : Hi 1 : Low)
		3	****0***	HSYNC SEL	Bit 3 : Hsync select (0 : HSYNC 1: Sync-on-Green)
		2	*****0**	VSYNC POL	Bit 2 : VSYNCO inversion (0 : INV 1 : No INV)
		0	*******0	VSYNC SEL	Bit 0 : VSYNC select (0 at power-down(PDN=0)) (0 : VSYNC 1 : Sync Separator Signal)
0FH	R/W	7	0*******	CLAMP SEL	Bit 7: Clamp signal select (0:HSYNC 1:CLAMP pin)
		6	*1******	CLAMP POL	Bit 6: Clamp polarity (0 : Hi 1 : Low)
		5	**0*****	COAST SEL	Bit 5: Coast select (0 : COAST Pin 1 : VSYNC)
		3	****1***	COAST POL	Bit 3: Coast polarity setting (0 : Low 1 : Hi)
		1	******1*	PDN	Bit 1: Power-down (0 : power-down 1 : normal operation)
10H	R/W	7:3	10111***	SOGTH	Sync-on- Green threshold level setting
		2	*****0**	RED CLP LVL	Bit 2: Red channel clamp level setting (0 : Minimum value 1 : Mid value)
		1	******0*	GREEN CLP LVL	Bit 1: Green channel clamp level setting (0 : Minimum value 1 : Mid value)
		0	*******0	BLUE CLP LVL	Bit 0: Blue channel clamp level setting (0 : Minimum value 1 : Mid value)

Sub Adrs	R/W Or RO	Bits	Default Value	Register Name	Function
11H	R/W	7:0	00100000	SSEPTH	Sync Separator threshold level setting
12H	R/W	7:0	00000000	PRE COAST	Pre-Coast
13H	R/W	7:0	00000000	POST COAST	Post-Coast
14H	RO	7:0	00000000	RESERVE	Reserved
15H	R/W	1	******1*	OUTPUT FORMAT	Bit1 : Output Format (0: 4:2:2, 1:4:4:4)
16H	R/W	7:0	********		Don't care
17H	R/W	0	*******1	RED OFFSET (MSB)	Red channel offset adjust (MSB)
18H	R/W	7:0	00000000	RED OFFSET (LSB)	Red channel offset adjust (LSB)
19H	R/W	0	*******1	GREEN OFFSET (MSB)	Green channel offset adjust (MSB)
1AH	R/W	7:0	00000000	GREEN OFFSET (LSB)	Green channel offset adjust (LSB)
1BH	R/W	0	*******1	BLUE OFFSET (MSB)	Blue channel offset adjust (MSB)
1CH	R/W	7:0	00000000	BLUE OFFSET (LSB)	Blue channel offset adjust (LSB)

Table 12 : Black Loop Registers

Sub Adrs	R/W Or RO	Bits	Default Value	Register Name	Function
1DH	R/W	0	*******0	RED BLK LVL (MSB)	RED channel black loop setting value (MSB)
1EH	R/W	7:0	00000000	RED BLK LVL (LSB)	RED channel black loop setting value (LSB)
1FH	R/W	0	*******0	GREEN BLK LVL (MSB)	GREEN channel black loop setting value (MSB)
20H	R/W	7:0	00000000	GREEN BLK LVL (LSB)	GREEN channel black loop setting value (LSB)
21H	R/W	0	*******0	BLUE BLK LVL (MSB)	BLUE channel black loop setting value (MSB)
22H	R/W	7:0	00000000	BLUE BLK LVL (LSB)	BLUE channel black loop setting value (LSB)
23H	R/W	7:5	000*****	LBW	Black Loop bandwidth
		4:3	***00***	LOOPOFFRNG	Black Loop coring bandwidth control
		2	*****0**	LOOPMODE	Black Loop mode (0 : loop enable 1 : loop disable)
		1	******0*	LOOPHOLD	retention of black loop condition
		0	*******0	VSYNC UPDATE	(0 : active 1 : condition retained) limit black level update frequency to every 64 VSYNC
24H	R/W	6	*0******	COASTGEN SEL	COASTGEN input setting (0: VSYNC 1 : SYNC SEP)
		5	**0*****	CLPBW	Clamp bandwidth setting
		4:3	***11***	Fixed Bit	Used in fixed condition. Write “11” when to write.
		2	*****0**	SOGOUT POL	SOGOUT polarity (0 : normal 1 : inverted)
		1	******0*	SOGOUT SEL	SOGOUT signal select (0 : SOG 1 : HSYNC)
		0	*******0	DOFIX	Output level at power-down mode (0 : fixed low 1 : fixed high)
25H	R/W	7:0	00000000	LOOP DISABLE	Black loop off period during Clamp period
26H	R/W	7:0	00000000	PRE CLPCOAST	Pre-Coast for clamp signal
27H	R/W	7:0	00000000	POST CLPCOAST	Post-Coast for clamp signal
28H	R/W	7:6	11******	DATA DRIVE	ROUT,GOUT,BOUT,HSYNCO,VSYNCO, SOGOUT pin drivability
		5:4	**11****	CLOCK DRIVE	DTCLK pin drivability
29H	R/W	7:6	10******	Reserved	reserved
		5:3	**101***	IN RANGE	accelerate range control of black loop setting
		2:1	*****00*	Reserved	Reserved
		0	*******0	Reserved	reserved Do not write value other than “0”
2AH	R/W	6:0	*0111001	Reserved	Reserved
2BH	R/W	3:0	******00		Reserved
2CH	RO	7:0	00000000		Reserved

TEST Register
AK5406 has test register address 0x20 ~ 0x30, which could be accessed in normal mode. Do not write without default.

2DH	R/W	7:0	00000000	TEST	Default Value : 0x00
2EH	R/W	7:0	00000000	TEST	Default Value : 0x00
2FH	R/W	7:0	00100000	TEST	Default Value : 0x20
30H	R/W	7:0	00000000	TEST	Default Value : 0x00

Default value of AK5406

Adr	R/W	default
00H	RO	AEH
01H	R/W	69H
02H	R/W	D0H
03H	R/W	48H
04H	R/W	80H
05H	R/W	80H
06H	R/W	80H
07H	R/W	20H
08H	R/W	80H
09H	R/W	80H
0AH	R/W	80H
0BH	RO	00H
0CH	RO	00H
0DH	RO	00H
0EH	R/W	40H
0FH	R/W	4AH
10H	R/W	B8H
11H	R/W	20H
12H	R/W	00H
13H	R/W	00H
14H	RO	00H
15H	R/W	02H
16H	R/W	00H
17H	R/W	01H
18H	R/W	00H
19H	R/W	01H
1AH	R/W	00H
1BH	R/W	01H
1CH	R/W	00H
1DH	R/W	00H
1EH	R/W	00H
1FH	R/W	00H

Adr	R/W	default
20H	R/W	00H
21H	R/W	00H
22H	R/W	00H
23H	R/W	00H
24H	R/W	18H
25H	R/W	00H
26H	R/W	00H
27H	R/W	00H
28H	R/W	F0H
29H	R/W	A8H
2AH	R/W	39H
2BH	R/W	00H
2CH	RO	00H

■ Description of Register Contents

Default value is meshed

Sub Address 00H CHIP ID

When it is read, device ID number (ADH) is returned.

Sub Address 01H ~ 02H PLL DIV Default : 69DH

01H [7:0]	02H [7:4]	Decimal notation of 01H [7:0]&02H [7:4]	PLL multiplier ratio
00H	0H	0	Inhibited
00H	1H	1	
:	:	:	
0DH	DH	221	
0DH	EH	222	223
0DH	FH	223	224
0EH	0H	224	225
:	:	:	:
FFH	FH	4095	4096

"set-value plus one" becomes multiplier ratio of PLL.

Write operation of MSB side bits (sub address 01H) does not initiate PLL operation, and after LSB side data (sub address 02H) is written, a multiplier ratio becomes valid and PLL operation is executed.

Sub Address 03H

[7:6] PLL VCO

[7:6]	PLL VCO operating range
00	9~32MHz
01	32~64MHz
10	64~80MHz
11	Inhibited

[5:3] PLL CP

[5:3]	PLL charge pump current
000	50uA
001	100uA
010	150uA
011	250uA
100	350uA
101	500uA
110	750uA
111	Inhibited

Sub Address 04H PHADJ

[7:3]	ADC sampling clock phase	
00H	-180°	advances ↑
01H	-168.75°	
:	:	
0EH	-22.5°	
0FH	-11.25°	
10H	standard	
11H	+11.25°	↓ delayed
12H	+22.5°	
:	:	
1EH	+157.5°	
1FH	+168.75°	

Each single step is equal to 11.25 degrees.
A larger number reflects direction of a bigger delay.

Sub Address 05H CLP PLACE Default : 80H
Sub Address 06H CLP DURATION Default : 80H

Clamp timing can be internally generated when CLAMP SEL is set to "0".
The periods of clamping is start from trailing edge of HSYNC after the delayed of CLP PLACE pixels and its continue according to the setting of CLP DURATION pixels value. (refer to timing chart 4)
Do not set CLP DURATION to "0" when CLP PLACE is set to "0","1","2" value.

Sub Address 07H HSYNCO WIDTH Default : 20H

This is to set the pulse width of Horizontal SYNC signal which is re-configured by PLL and is output on HSYNCO pin (refer to timing charts 1 & 2).
Do not write this register value to "0".

Sub Address 08H ~ 0AH RED (GREEN,BLUE) GAIN

[7:0]	Input range [Vpp]	Gain
00H	0.377	High gain ↑
01H	0.380	
02H	0.383	
:	:	
7FH	0.751	
80H	0.754	
81H	0.757	
:	:	↓ Low gain
FDH	1.123	
FEH	1.126	
FFH	1.129	

(note) PGA Gain is shown by 543/(128 + N) where (N = 0 ~ 255(DEC)).
PGA Gain is set until ADC input range becomes 1.6Vpp.

Sub Address 0EH

[6] HSYNC POL

[6]	HSYNC input pin polarity
0	Active low (leading edge to fall)
1	Active high (leading edge to rise)

[5] HSYNCO POL

[5]	HSYNCO output pin polarity
0	Active high (leading edge to rise)
1	Active low (leading edge to fall)

[3] HSYNC SEL

[3]	HSYNC signal to be input to PLL	Signal to be input to Sync Separator
0	HSYNC pin	HSYNC pin
1	Sync-On-Green SLICER output	Sync-On-Green SLICER output

[2] VSYNC POL

[2]	VSYNCO output pin polarity
0	Inverted VSYNC
1	Normal VSYNC

[0] VSYNC SEL

[0]	VSYNC select
0	VSYNC
1	Sync Separator signal

(note) Sync Separator circuit is in power down, when bit 1 of PDN register at Sub Address 0FH is "0".

Sub Address 0FH

[7] CLAMP SEL

[7]	Clamp signal to be used at CLP
0	Internally generated signal from HSYNC
1	CLAMP pin

[6] CLAMP POL

[6]	CLAMP input pin polarity
0	Active high
1	Active low

[5] COAST SEL

[5]	Signal to be used as PLL COAST
0	COAST pin
1	Internally generated signal from VSYNC

[3] COAST POL

[3]	COAST input pin polarity
0	Active low
1	Active high

[1] PDN

[1]	Power-down control	Operating functional blocks
0	Power-down	VREF Sync-On-Green SLICER
1	Normal operation	Total circuit

Sub Address 10H

[7:3] SOGTH **Default : 17H**

[7:3]	SOG SLICER threshold level (upward direction from SOG clamp level)
00H	320mV
01H	310mV
:	:
1EH	20mV
1FH	10mV

[2:0] RED(GREEN,BLUE) CLP LVL

	Input clamp level
0	Minimum level
1	Center level

Sub Address 11H SSEPTH

[7:0]	Sync Separator threshold level
FFH	Wider pulse width
FEH	↑
:	
20H	Standard
:	
01H	↓
00H	Narrower pulse width

Sub Address 12H PRE COAST
Sub Address 13H POST COAST

Parameters in order to internally generate PLL COAST signal from VSYNC are set.
It is valid only when the COAST SEL bit is "1".
In the PRE-COAST register, # of preceding HSYNC periods to be coasted prior to VSYNC signal, is set and in the POST COAST register, # of succeeding HSYNC periods to be coasted after VSYNC signal, is set (refer to timing chart 3).

Sub Address 15H
[1] OUTFORMAT

[4]	Output Format
0	4:2:2
1	4:4:4

Input & Output signals vs Channel relation is listed in the following table when 4:2:2 output format is selected (refer to timing chart 1 & 2).

Channel	Input signal	Output signal
Red	V	U/V
Green	Y	Y
Blue	U	Hi-Z

Sub Address 17H ~ 1CH RED(GREEN, BLUE)OFFSET

[0],[7:0]	OFFSET adjust (addition / subtraction) values
1FFH	-64 LSB
1FEH	-63.75 LSB
:	:
100H	-0.25 LSB
0FFH	0 LSB
0FEH	+0.25 LSB
:	:
001H	+63.5 LSB
000H	+63.75 LSB

OFFSET of each channel is adjusted in 9-bit resolution.
Its center value is 0FFH and it is adjusted in 1/4 LSB per single step.
OFFSET adjust is valid only when black loop is disable (LOOP MODE = 1).
Data Write of MSB bits does not affect the operation and Data value becomes valid when Data write of LSB bits is made.

Sub Address 1DH ~ 22H RED (GREEN, BLUE) BLK LVL

BLKLVL	Black Loop setting values	
[0], [7:0]	At minimum clamp level setting (CLP LVL = 0)	At center clamp level setting (CLP LVL=1)
011111111	Inhibited	Inhibited
011111110	Inhibited	Inhibited
:	:	:
001010001	Inhibited	:
001010000	20	:
001001111	19.75	:
	:	:
000011101	7.25	Inhibited
000011100	7	135
000011011	6.75	134.75
	:	:
000000010	0.5	128.5
000000001	0.25	128.25
000000000	0	128 (200H)
111111111	-0.25	127.75
111111110	-5	127.5
:	:	:
111110001	-3.75	124.25
111110000	-4	124
111101111	Inhibited	123.75
	:	:
111100001	:	120.25
111100000	:	120
111011111	:	Inhibited
	: :	:
100000001	Inhibited	Inhibited
100000000	Inhibited	Inhibited

Data Write of MSB bits does not affect operation, and Data value becomes valid when Data Write of LSB bits are made.

Sub Address 23H

[7:5] LOOPBW

LOOPBW	Black Loop bandwidth
011	FAST
010	↑
:	
001	
000	Standard
111	
:	
101	↓
100	SLOW

[4:3] LOOPOFFRNG

LOOPOFFRNG	Black level coring control
00	No coring
01	±0.25 LSB
10	±1.5 LSB
11	±1.0 LSB

[2] LOOPMODE

LOOPMODE	Black Loop mode
0	Black Loop enable (BLK LVL register valid)
1	Black Loop disable (OFFSET register valid)

[1] LOOPHOLD

LOOPHOLD	Black Loop condition
0	Black Loop operation
1	Hold of Black Loop condition

[0] VSYNC UPDATE

VSYNC UPDATE	Update timing of the Black loop Offset correction
0	Corrected value of Black Loop Offset is updated at every HSYNC timing
1	Corrected value of Black Loop Offset is updated at every 64 VSYNC timing

*OFFSET Integrator of the Black Loop is updated at every HSYNC timing, regardless of this bit setting.

Only the update timing of the Offset Correction amounts which is added or subtracted to/from the ADC output is altered by this bit.

Sub Address 24H

[6] COASTGEN SEL

COASTGEN SEL	COASTGEN input setting
0	VSYNC pin
1	Sync Separator output

(note) when COASTGEN SEL is set to "1", please select the Sync Separator signal for VSYNC SEL at Sub Address 0EH bit "0".

[5] CLPBW

CLP BW	Clamp input / output current	Clamp bandwidth
0	600uA	Standard
1	150uA	SLOW

[4:3] "1" is written to each of these 2 bits.

[2] SOGOUT POL

SOGOUT POL	Signal polarity to be output on SOGOUT pin
0	Non-inverted
1	Inverted

(note) Polarity of the selected signal by SOGOUT SEL register is altered when it is output on SOGOUT pin.

[1] SOGOUT SEL

SOGOUT SEL	Signal to be output on SOGOUT pin
0	SOG SLICER output
1	Input signal on HSYNC pin

[0] DOFIX

DOFIX	Output level at power-down
0	Fixed low
1	Fixed high

(note) Compatible pins : ROUT7-0, GOUT7-0, BOUT7-0, , HSYNCO, VSYNCO, SOGOUT, DTCLK.

Sub Address 25H LOOP DISABLE

When this register value(m) is set to value other than "0", it is possible to divide the clamp period into two half, where the First half is Clamp circuit operational (m pixels clock) and Black Loop operation in the other half. (refer to timing chart 5)
When set this register value, the value must be smaller than CLP DURATION value.

Sub Address 26H PRE CLPCOAST Default : 00H
Sub Address 27H POST CLPCOAST Default : 00H

Parameters to coast Clamp signal are set.
In the PRE COAST register, # of preceding HSYNC periods to be coasted after VSYNC signal, is set in the POST CLPCOAST register, # of succeeding HSYNC periods to be coasted after VSYNC signal, is set. (refer to timing chart 6)

Sub Address 28H

[7:6] DATA DRIVE

DATA DRIVE	ROUT, GOUT, BOUT, HSYNCO, VSYNCO, SOGOUT pin drivability
00	Hi-Z
01	Hi-Z
10	MAX x 1/4
11	MAX

[5:4] CLOCK DRIVE

CLOCK DRIVE	DTCLK pin drivability
00	Hi-Z
01	Hi-Z
10	MAX x 1/4
11	MAX

Sub Address 29H

[3:1] IN RANGE

IN RANGE	Accelerate range control of black loop setting
000	No acceleration
001	Non-boosted bandwidth when it settles within ±0.25 LSB
010	Non-boosted bandwidth when it settles within ±0.5 LSB
011	Non-boosted bandwidth when it settles within ±0.75 LSB
100	Non-boosted bandwidth when it settles within ±1 LSB
101	Non-boosted bandwidth when it settles within ± 2 LSB
110	Non-boosted bandwidth when it settles within ±3 LSB
111	Non-boosted bandwidth when it settles within ±4 LSB

Sub Address 2AH [6:0] Reserve 1 Default : 39H
Sub Address 2BH [3:0] Reserve 1 Default : 00H Reserved.

■ Recommended External Component Connection Examples (part 1)

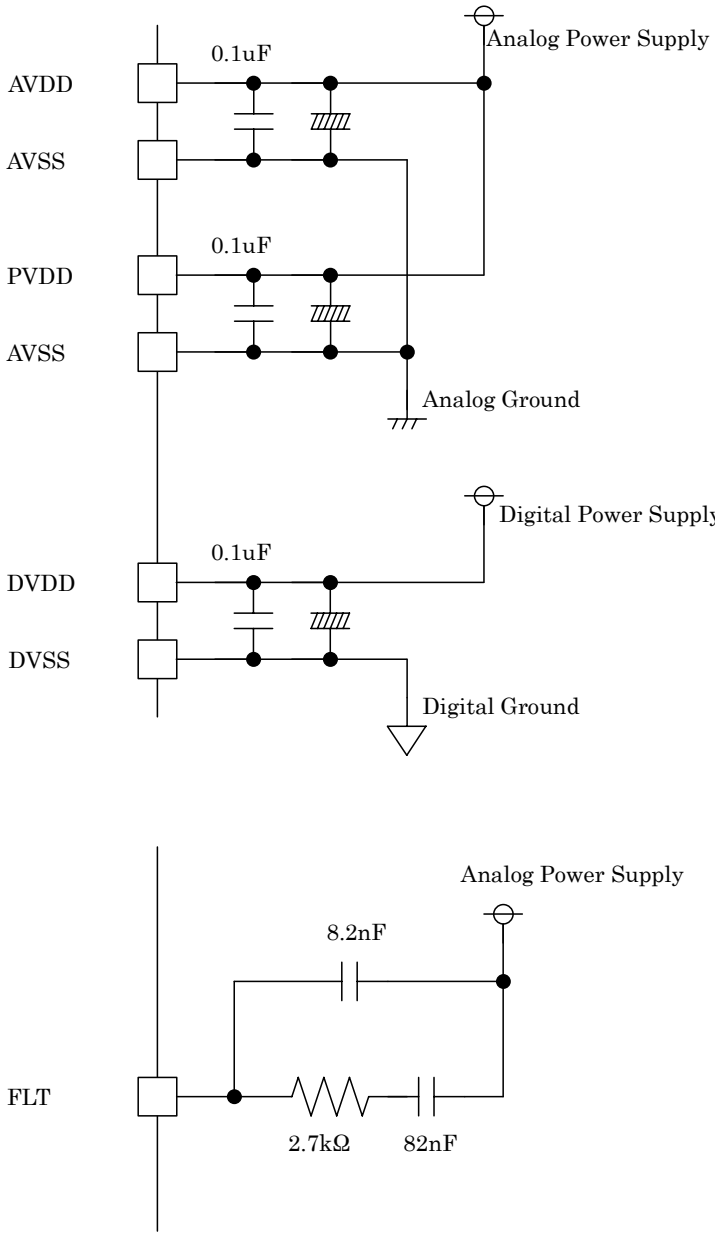


Fig. 17 Recommended External Component connection examples

■ Recommended External Component Connection Examples (part 2)

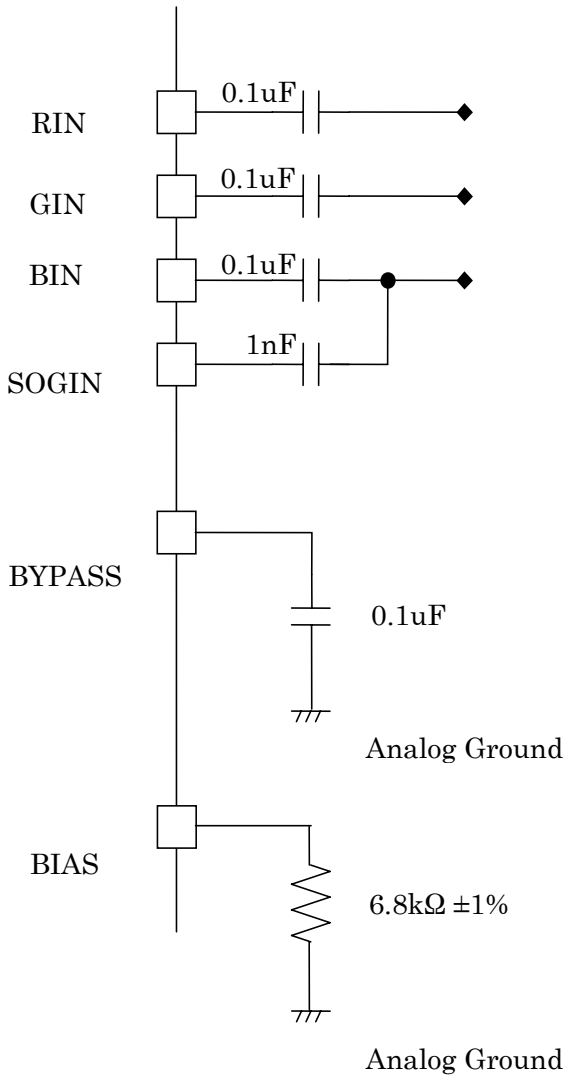
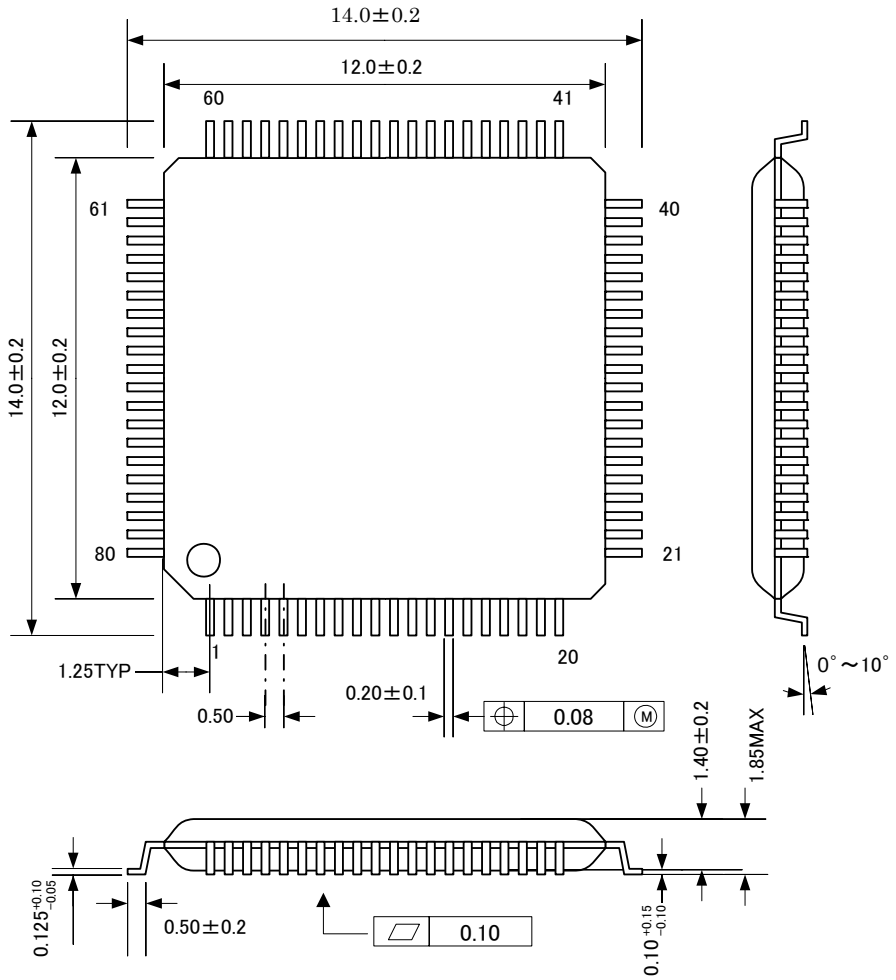


Fig. 18 Recommended External Component connection examples (part 2)

■ Package Marking

Contents of XXXXAAA
XXXX: Production date (numbers)
AAA : lot number (alphabet)

Package Outline Dimensions



IMPORTANT NOTICE

- These products and their specifications are subject to change without notice.
  When you consider any use or application of these products, please make inquiries the sales office of Asahi Kasei EMD Corporation (AKEMD) or authorized distributors as to current status of the products.
- AKEMD assumes no liability for infringement of any patent, intellectual property, or other rights in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKEMD products are neither intended nor authorized for use as critical components[Note1)] in any safety, life support, or other hazard related device or system[Note2)], and AKEMD assumes no responsibility for such use, except for the use approved with the express written consent by Representative Director of AKEMD. As used here:
  Note1) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
  Note2) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
- It is the responsibility of the buyer or distributor of AKEMD products, who distributes, disposes of, or otherwise places the product with a third party, to notify such third party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKEMD harmless from any and all claims arising from the use of said product in the absence of such notification.