CMX7146
BPSK Wireless Data Modulator

7146FI-1.x: BPSK Wireless Data Modulator

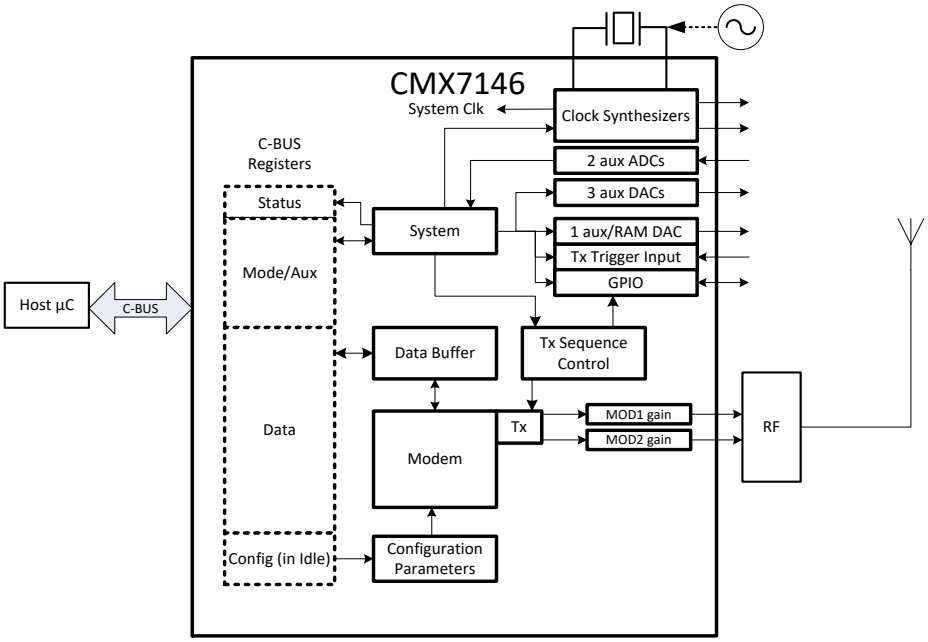
D/7146/3 December 2020 **DATASHEET** Advance Information

Features

- **Plain or differential BPSK encoding**
- **400, 600, 1200, 3600, 4800, 9600bps data rates**
- **Selectable RRC filter (α = 0.2, 0.3, 0.35)**
- **C-BUS serial interface to host µController**
- **C-BUS thru-port control of CMX971**
- **2 x Auxiliary ADCs and 4 x auxiliary DACs**
- **Auxiliary system clock outputs**
- **Low-power (3.0V to 3.6V) operation**
- **Available in 48-lead VQFN Package**

Applications

- **Marine emergency beacons**
- **IIoT transmitters**
- **CubeSat communications**



1 Brief Description

CMX7146 FI-1.x is a BPSK data modulator for use in wireless systems, with automatic control of transmit hardware including RAMDAC for PA ramping. Other features include two Auxiliary ADC channels with four selectable inputs and up to four auxiliary DAC outputs (with the optional RAMDAC on the first DAC output, to facilitate transmitter power ramping). The device has flexible powersaving modes and is available in a VQFN package.

The device utilises CML's proprietary *FirmASIC*® component technology. On-chip sub-systems are configured by a Function Image™: this is a data file that is uploaded during device initialisation and defines the device's function and feature set. The Function Image™ can be loaded automatically from an external EEPROM or from a host µController over the built-in C-BUS serial interface. The device's functions and features can be enhanced by subsequent Function Image™ releases, facilitating in-the-field upgrades.

This Datasheet is the first part of a two-part document comprising Datasheet and User Manual: the User Manual can be obtained by registering your interest in this product with your local CML representative.

CONTENTS

Section		Page
1	**Brief Description**	**1**
1.1	History	3
2	**Signal List**	**6**
3	**External Components**	**8**
4	**PCB Layout Guidelines and Power Supply Decoupling**	**10**
5	**General Description**	**11**
5.1	CMX7146 Features	11
6	**Detailed Descriptions**	**12**
6.1	Xtal Frequency	12
6.2	Host Interface	12
6.2.1	C-BUS Operation	12
6.3	Function Image Loading	13
6.3.1	FI Loading from Host Controller	13
6.3.2	FI Loading from Flash/EEPROM	15
6.4	Device Control	16
6.4.1	Device Configuration (using the Programming Register)	16
6.4.2	Device Configuration (using dedicated registers)	16
6.4.3	Interrupt Operation	17
6.4.4	Signal Routing	17
6.4.5	Loading Transmit Data	17
6.4.6	The Transmit Sequence	17
6.4.7	Other Modem Modes	18
6.4.8	Data Transfer	18
6.4.9	Raw Data Transfer	19
6.4.10	Pre-loading transmit data	19
6.4.11	Auxiliary clock rates	19
6.4.12	Auxiliary data	19
6.4.13	GPIO Pin Operation	20
6.4.14	Auxiliary ADC Operation	20
6.4.15	Auxiliary DAC / RAMDAC Operation	21
6.5	Digital System Clock Generators	22
6.5.1	System Clock Operation	23
6.6	Signal Level Optimisation	23
6.7	C-BUS Register Summary	23
7	**CMX7146 FI-1.x Features**	**25**
7.1	Modulation	25
7.2	Radio Interface	25
7.3	Transmit Performance	26
8	**Performance Specification**	**29**
8.1	Electrical Performance	29
8.1.1	Absolute Maximum Ratings	29
8.1.2	Operating Limits	30
8.1.3	Operating Characteristics	31
8.1.4	Parametric Performance	36
8.2	C-BUS Timing	37
8.3	Packaging	38
9	**Configuration Guide**	**3**
9.1	C-BUS Register Details	3
9.1.1	Reset Operations	3
9.1.2	General Reset - $01 write	3
9.1.3	Aux config - $A7 write	4
9.1.4	AuxDAC control / data - $A8 write	5
9.1.5	Aux data1 - $A9 read	5
9.1.6	Aux data2 - $AA read	6
9.1.7	System CLK 1 and 2 PLL data - $AB, $AD write	6

9.1.8 System CLK 1 and 2 REF - $AC and $AE write 6
9.1.9 Analogue Output Gain - $B0 write 7
9.1.10 Input Gain and Input/Output Signal Routing - $B1 write 7
9.1.11 TxData0 - $B5 write (plus TxData1-6) 7
9.1.12 TxData1 - $B6 write 8
9.1.13 TxData2 - $B7 write 8
9.1.14 TxData3 - $CA write 8
9.1.15 TxData4 - $CB write 8
9.1.16 TxData5 Write - $C2 write 8
9.1.17 TxData6 - $C7 write 8
9.1.18 Power Down Control - $C0 write 8
9.1.19 Modem Mode and Control - $C1 write 9
9.1.20 Status - $C6 read 10
9.1.21 Programming Register – $C8 write 11
9.1.22 AuxConfig2 - $CD write 11
9.1.23 Interrupt Mask - $CE write 12
9.2 Programming Register Operation 12
9.2.1 Programming Example 13
9.2.2 Program Block 1 – Burst Tx Sequence + GPIO configuration 14
9.2.3 Program Block 3 – AuxDAC, RAMDAC and Clock control 16
9.2.4 Program Block 4 – Modulation Setup: 17
10 Application Notes 19
10.1 Simple Tx signal test 19
10.2 Tx Data Burst 19

Table Page

Table 1 BOOTEN Pin States 13
Table 2 C-BUS Data Registers 18
Table 3 C-BUS Registers 23
Table 4 Reset Operations 3
Table 5 RAMDAC Values 16

Figure Page

Figure 1 Block Diagram 5
Figure 2 CMX7146 Recommended External Components 8
Figure 3 CMX7146 Power Supply and De-coupling 10
Figure 4 C-BUS Transactions 12
Figure 5 FI Loading from Host 14
Figure 6 FI Loading from EEPROM 15
Figure 7 Transmit Sequence 18
Figure 8 Digital Clock Generation Schemes 22
Figure 9 Modulation Process 25
Figure 10 Outline Radio Design CMX7146/CMX971 25
Figure 11 Outline Radio Design CMX7146/CMX993 26
Figure 12 Tx Modulation Spectra MOD1/MOD2 I/Q output to Sig Gen 4800 bps 27
Figure 13 TX Modulation output from CMX971 4800 bps 28
Figure 14 C-BUS Timing 37
Figure 15 Mechanical Outline of 48-pin VQFN (Q3) 38

It is recommended that you check for the latest product datasheet version from the CML website: [www.cmlmicro.com].

1.1 History

Version	Changes	Date
3	Figure 1 corrected to show BPSK modulation Section 8.1.4: Minimum modem symbol rate changed to 400	7th December 2020
2	Figure 11 added to show integration with CMX993	17th September 2019
1	Original document, prepared for first beta release of software.	1st August 2019

Note: This product is Advance information: Changes and additions will be made to this specification. Items marked TBD or left blank will be included in later issues.

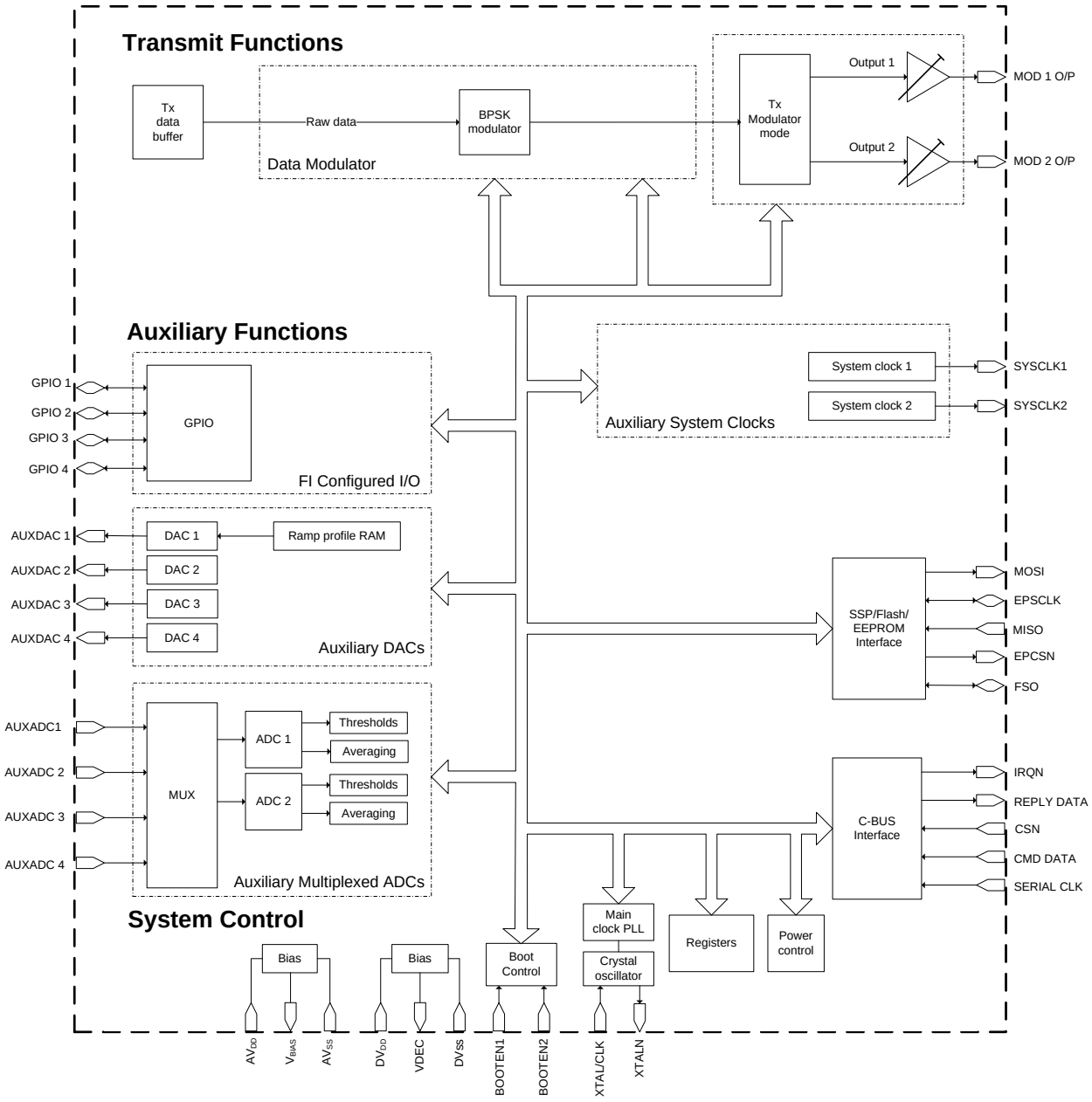


Figure 1 Block Diagram

2 Signal List

CMX7146 48-lead Q3	Signal Name	Type	Description
1	MOSI	OP	SPI bus Master Output
2	EPSCLK	BI	SPI bus Serial Clock
3	MISO	IP+PD	SPI bus Master Input
4	EPCSN	OP	Flash/EEPROM Chip Select
5	BOOTEN1	IP+PD	Used in conjunction with BOOTEN2 to determine the operation of the bootstrap program.
6	BOOTEN2	IP+PD	Used in conjunction with BOOTEN1 to determine the operation of the bootstrap program.
7	DVss	PWR	Digital Ground
8	IRQN	OP	C-BUS: A 'wire-ORable' output for connection to the Interrupt Request input of the host. Pulled down to VSS(D) when active and is high impedance when inactive. An external pull-up resistor (R1) is required.
9	VDEC	PWR	Internally generated 2.5V digital supply voltage. Must be decoupled to DVss by capacitors mounted close to the device pins. No other connections allowed, except for optional connection to RFVdd.
10	GPIO1	BI	General Purpose I/O pin
11	GPIO3	BI	General Purpose I/O pin
12	GPIO4	BI	General Purpose I/O pin
13	SYSCLK1	OP	Synthesized Digital System Clock Output 1
14	DVss	PWR	Digital Ground
15	GPIO2	BI	General Purpose I/O pin
16	NC	NC	Do not connect
17	NC	NC	Do not connect
18	NC	NC	Do not connect
19	NC	NC	Do not connect
20	NC	NC	Do not connect
21	NC	NC	Do not connect
22	AVss	PWR	Analog Ground
23	MOD1	OP	Modulator 1 output
24	MOD2	OP	Modulator 2 output
25	V_{BIAS}	OP	Internally generated bias voltage of about AVdd/2, except when the device is in 'Powersave' mode when VBIAS will discharge to AVss. Must be decoupled to AVss by a capacitor mounted close to the device pins. No other connections allowed.
26	AUDIO OUT	OP	Reserved for future use
27	AUXADC1	IP	Auxiliary ADC input 1
28	AUXADC2	IP	Auxiliary ADC input 2

CMX7146 48-lead Q3	Signal Name	Type	Description
29	AUXADC3	IP	Auxiliary ADC input 3
30	AUXADC4	IP	Auxiliary ADC input 4
31	AVdd	PWR	Analog +3.3V supply rail. Levels and thresholds within the device are proportional to this voltage. This pin should be decoupled to AVss by capacitors mounted close to the device pins.
32	AUXDAC1	OP	Auxiliary DAC output 1 / RAMDAC
33	AUXDAC2	OP	Auxiliary DAC output 2
34	AVss	PWR	Analog Ground
35	AUXDAC3	OP	Auxiliary DAC output 3
36	AUXDAC4	OP	Auxiliary DAC output 4
37	DVss	PWR	Digital Ground
38	VDEC	PWR	Internally generated 2.5V supply voltage. Must be decoupled to DVss by capacitors mounted close to the device pins. No other connections allowed, except for the optional connection to RFVdd.
39	XTAL / CLOCK	IP	input from the external clock source or Xtal
40	XTALN	OP	The output of the on-chip Xtal oscillator inverter. NC if external Clock used.
41	DVdd	PWR	Digital +3.3V supply rail. This pin should be decoupled to DVss by capacitors mounted close to the device pins.
42	COMMAND DATA	IP	C-BUS: Serial data input from the µC
43	REPLY DATA	TS OP	C-BUS: A 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC.
44	FSO	BI	SPI bus Chip Select
45	DVss	PWR	Digital Ground
46	SERIAL CLOCK	IP	C-BUS: The C-BUS serial clock input from the µC
47	SYSCLK2	OP	Synthesized Digital System Clock Output 2
48	CSN	IP	C-BUS: The C-BUS chip select input from the µC
EXPOSED METAL PAD	SUBSTRATE	~	On this device, the exposed central metal pad may be electrically unconnected or, alternatively, may be connected to Analogue Ground (AVss). **No other electrical connection is permitted.**

Notes:

IP	=	Input (+ PU/PD = internal pullup / pulldown resistor)
OP	=	Output
BI	=	Bidirectional
TS OP	=	3-state Output
PWR	=	Power Connection
NC	=	No Connection - should NOT be connected to any signal.

3 External Components

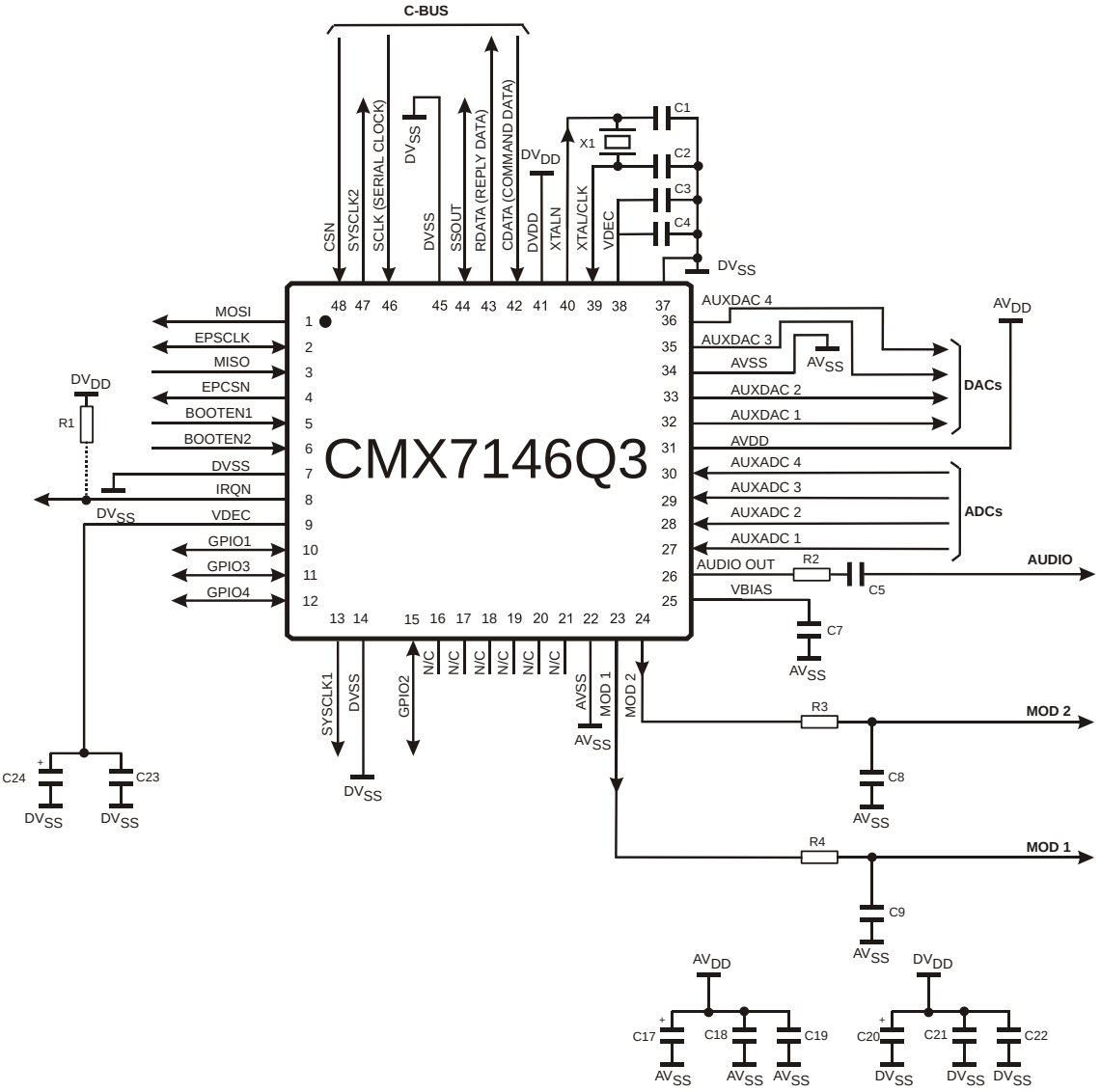


Figure 2 CMX7146 Recommended External Components

R1	100kΩ	C5	N/F	C19	10nF	X1	9.6 or 19.2MHz
R2	N/F	C6	N/F	C20	10µF		See note 1
R3	100kΩ	C7	100nF	C21	10nF		
R4	100kΩ	C8	100pF	C22	10nF		
C1	18pF	C9	100pF	C23	10nF		
C2	18pF	C10	*not used*	C24	10µF		
C3	10nF	C17	10µF	C25	10nF		
C4	10µF	C18	10nF	C26	10µF		

Resistors ±5%, capacitors and inductors ±20% unless otherwise stated.

Notes:

1. X1 can be a crystal or an external clock generator; this will depend on the application. The tracks between the crystal and the device pins should be as short as possible to achieve maximum stability and best start up performance. By default, 19.2 MHz external oscillator is assumed, other values could be used if the various internal clock dividers are set to appropriate values.

2. If any of the Channel inputs are not required, the respective pin should be connected to AVss.

3. A single 10µF electrolytic capacitor may be fitted in place of C4 and C24, providing the two V_{DEC} pins are connected together on the pcb with an adequate width power supply trace.

4 PCB Layout Guidelines and Power Supply Decoupling

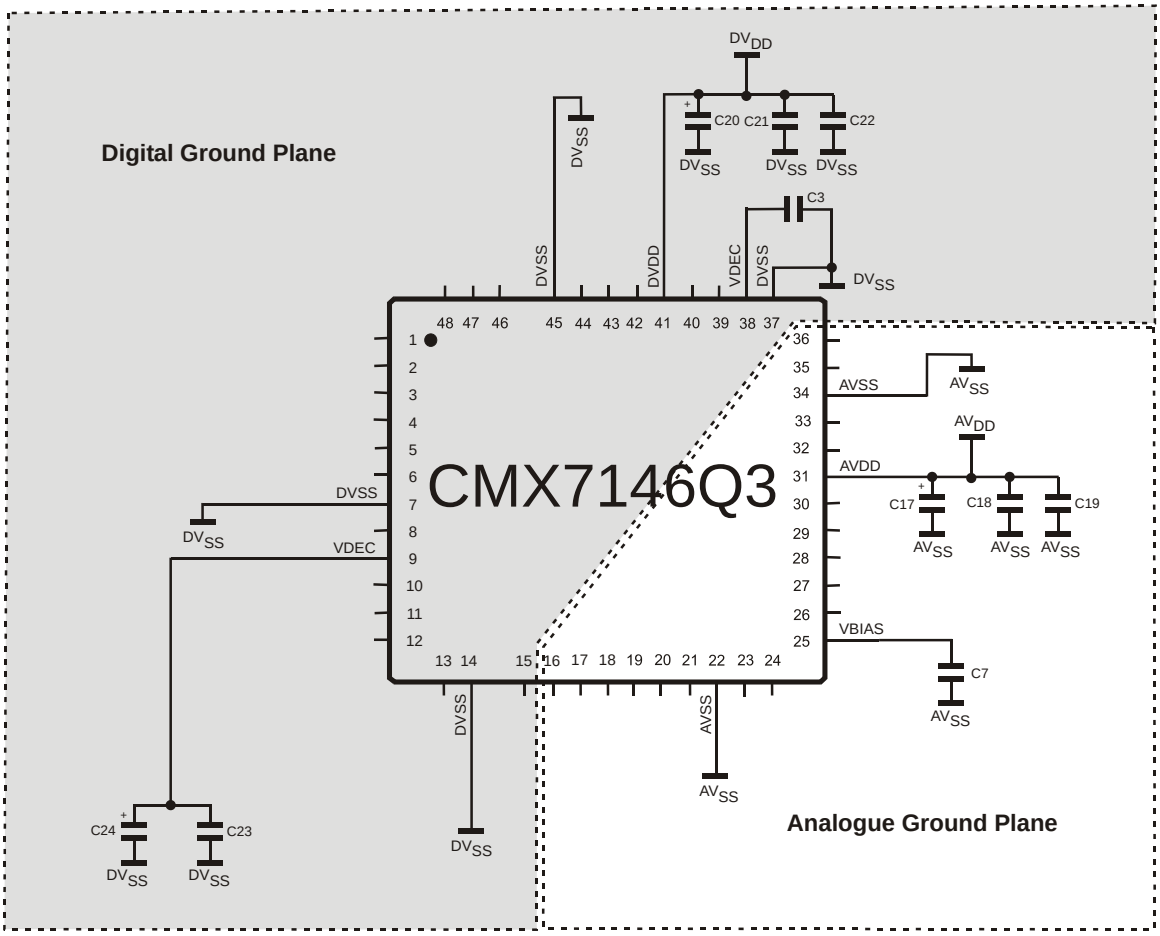


Figure 3 CMX7146 Power Supply and De-coupling

Component Values as per Figure 2.

Notes:

It is important to protect the analogue pins from extraneous in-band noise and to minimise the impedance between the CMX7146 and the supply and bias de-coupling capacitors. The de-coupling capacitors C3, C7, C18, C19, C21, C22, C24 and C25 should be as close as possible to the CMX7146. It is therefore recommended that the printed circuit board is laid out with separate ground planes for the AV_{SS} and DV_{SS} supplies in the area of the CMX7146 with provision to make links between them, close to the CMX7146. Use of a multi-layer printed circuit board will facilitate the provision of ground planes on separate layers.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity, so apart from the decoupling capacitor shown, no other loads should be connected. If V_{BIAS} needs to be used to set the discriminator mid-point reference, it must be buffered with a high input impedance buffer.

The crystal, X1, may be replaced with an external clock source.

5 General Description

5.1 CMX7146 Features

The CMX7146 is a transmit-only device for use in BPSK wireless data systems. A flexible power control facility allows the device to be placed in its powersave mode when not actively processing signals.

The device includes a crystal clock generator, with buffered output, to provide a common system clock if required.
A block diagram of the device is shown in Figure 1.

Tx Functions:

- Flexible Tx data transfer block size, up to 104bits
- Root raised cosine pulse-shape filtering
- RAMDAC capability for PA ramping control
- Tx burst sequence for automatic RAMDAC ramp and Tx hardware switching

Auxiliary Functions:

- 2 programmable system clock outputs
- 2 auxiliary ADCs with four selectable input paths
- 4 auxiliary DACs, one with built-in programmable RAMDAC

Interface:

- Adjustable I/Q modulation outputs to suit CMX971
- Optimised C-BUS (4 wire high speed synchronous serial command / data bus) interface to host for control and data transfer
- Open drain IRQ to host
- Four GPIO pins
- Flash/EEPROM boot mode
- C-BUS (host) boot mode

6 Detailed Descriptions

6.1 Xtal Frequency

The CMX7146 is designed to work with an external frequency source of 19.2MHz.

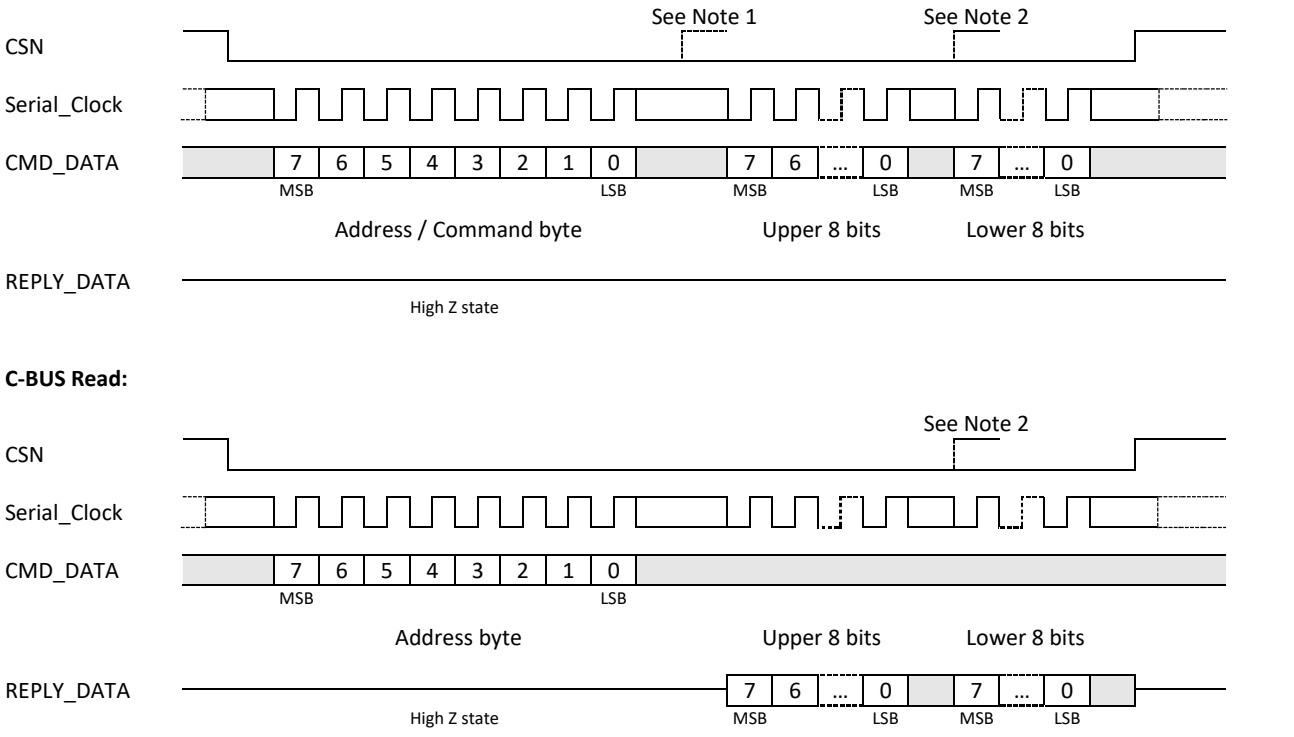
6.2 Host Interface

A serial data interface (C-BUS) is used for command, status and data transfers between the CMX7146 and the host µC; this interface is compatible with Microwire™, SPI™ and other similar interfaces. Interrupt signals notify the host µC when a change in status has occurred and the µC should read the status register across the C-BUS and respond accordingly. Interrupts only occur if the appropriate mask bit has been set, see section 6.4.3.

6.2.1 C-BUS Operation

This block provides for the transfer of data and control or status information between the CMX7146's internal registers and the host µC over the C-BUS serial interface. Each transaction consists of a single Address byte sent from the µC which may be followed by one or more Data byte(s) sent from the µC to be written into one of the CMX7146's Write Only Registers, or one or more data byte(s) read out from one of the CMX7146's Read Only Registers, as illustrated in Figure 4. Data sent from the µC on the Command Data line is clocked into the CMX7146 on the rising edge of the Serial Clock input. Reply Data sent from the CMX7146 to the µC is valid when the Serial Clock is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. The number of data bytes following an Address byte is dependent on the value of the Address byte. The most significant bit of the address or data are sent first. For detailed timings see section 8.2. Note that, due to internal timing constraints, there may be a delay of up to 250µs between the end of a C-BUS write operation and the device reading the data from its internal register.

C-BUS Write:



C-BUS Read:

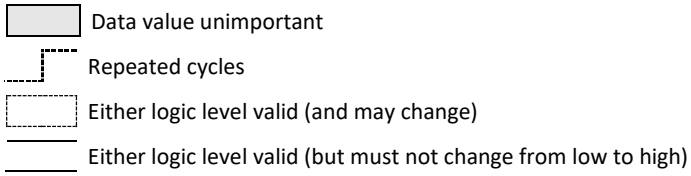


Figure 4 C-BUS Transactions

Notes:

1. For Command byte transfers only the first 8 bits are transferred ($01 = Reset).
2. For single byte data transfers only the first 8 bits of the data are transferred.
3. The CMD_DATA and REPLY_DATA lines are never active at the same time. The Address byte determines the data direction for each C-BUS transfer.
4. The Serial_Clock input can be high or low at the start and end of each C-BUS transaction.
5. The gaps shown between each byte on the CMD_DATA and REPLY_DATA lines in the above diagram are optional, the host may insert gaps or concatenate the data as required.

6.3 Function Image Loading

The Function Image™ (FI), which defines the operational capabilities of the device, may be obtained from the CML Technical Portal, following registration. This is in the form of a 'C' header file which can be included into the host controller software or programmed into an external EEPROM or Flash memory. The maximum possible size of Function Image™ is 46 kbytes, although a typical FI will be less than this. Note that the BOOTEN pins are only read at power-on or following a C-BUS General Reset and must remain stable throughout the FI loading process. Once the FI load has completed, the BOOTEN pins are ignored by the CMX7146 until the next power-up or C-BUS General Reset.

The BOOTEN pins are both fitted with internal low-current pulldown devices. For C-BUS load operation, both pins should be pulled high by connecting them to DV_{DD} either directly or via a 47k resistor (see Table 1).

For Flash/EEPROM load, only BOOTEN1 needs to be pulled high in a similar manner, however, if it is required to program the EEPROM or Flash memory in-situ from the host, either a jumper to DV_{DD} or a link to a host I/O pin should be provided to pull BOOTEN2 high when required (see Table 1).

Once the FI has been loaded, the CMX7146 performs these actions:-

(1) the product identification code ($7146) is reported in C-BUS register $C5
(2) the FI version code is reported in C-BUS register $C9
(3) the two 32-bit FI checksums are reported in C-BUS register pairs $A9, $AA and $B8, $B9
(4) the device waits for the host to load the 32-bit Device Activation Code to C-BUS register $C8
(5) once activated, the device initialises fully, enters idle mode and becomes ready for use.

The checksums can be verified against the published values to ensure that the FI has loaded correctly. Once the FI has been activated, the checksum, product identification and version code registers are cleared and these values are no longer available. If an invalid activation code is loaded, the device will report the value $DEAD in register $A9 and become unresponsive to all further host commands (including General Reset).

Both the Device Activation Code and the checksum values are available from the CML Technical Portal.

Table 1 BOOTEN Pin States

	BOOTEN2	BOOTEN1
C-BUS Host load	1	1
reserved	1	0
Flash/EEPROM load	0	1
No FI load	0	0

Note: In the rare event that a General Reset needs to be issued without the requirement to re-load the FI, the BOOTEN pins must both be cleared to '0' before issuing the Reset command. The Checksum values will be reported and the Device Activation code will need to be sent in a similar manner as that shown in Figure 6. There will not be any FI loading delay. This assumes that a valid FI has been previously loaded and that Vdd has been maintained throughout the reset to preserve the data.

6.3.1 FI Loading from Host Controller

The FI can be included into the host controller software build and downloaded into the CMX7146 at power-up over the C-BUS interface. The BOOTEN pins must be set to the C-BUS load configuration, the CMX7146 powered up and placed into Program Mode, the data can then be sent directly over the C-BUS to the CMX7146.

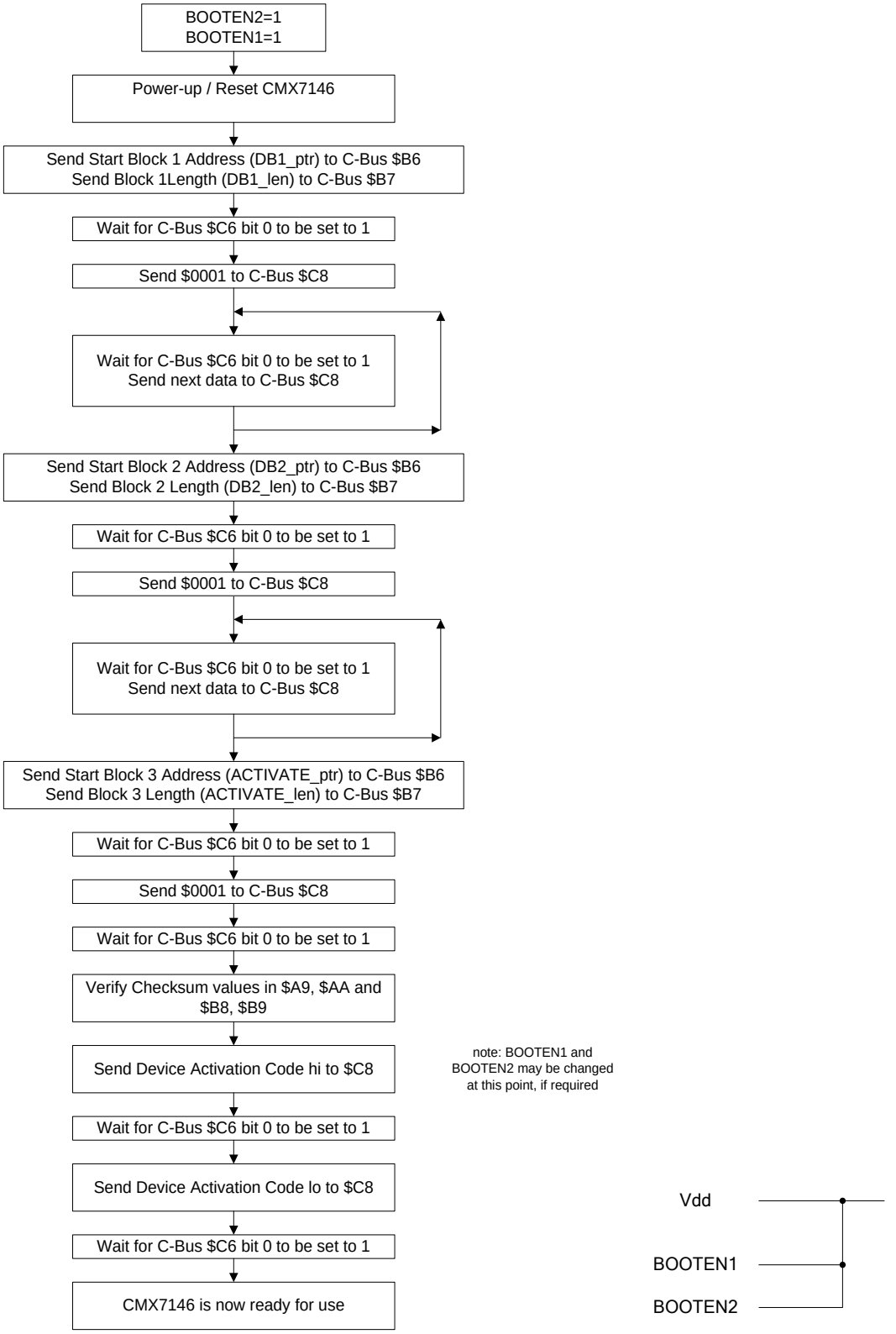


Figure 5 FI Loading from Host

The download time is limited by the clock frequency of the C-BUS, with a 5MHz SCLK, it should take less than 500ms to complete.

6.3.2 FI Loading from Flash/EEPROM

The FI must be converted into a format for the Flash/EEPROM programmer (normally Intel Hex) and loaded into the EEPROM or Flash memory either by the host or an external programmer. The CMX7146 needs to have the BOOTEN pins set to Flash/EEPROM load, and then on power-on, or following a C-BUS General Reset, the CMX7146 will automatically load the data from the EEPROM or Flash memory without intervention from the host controller.

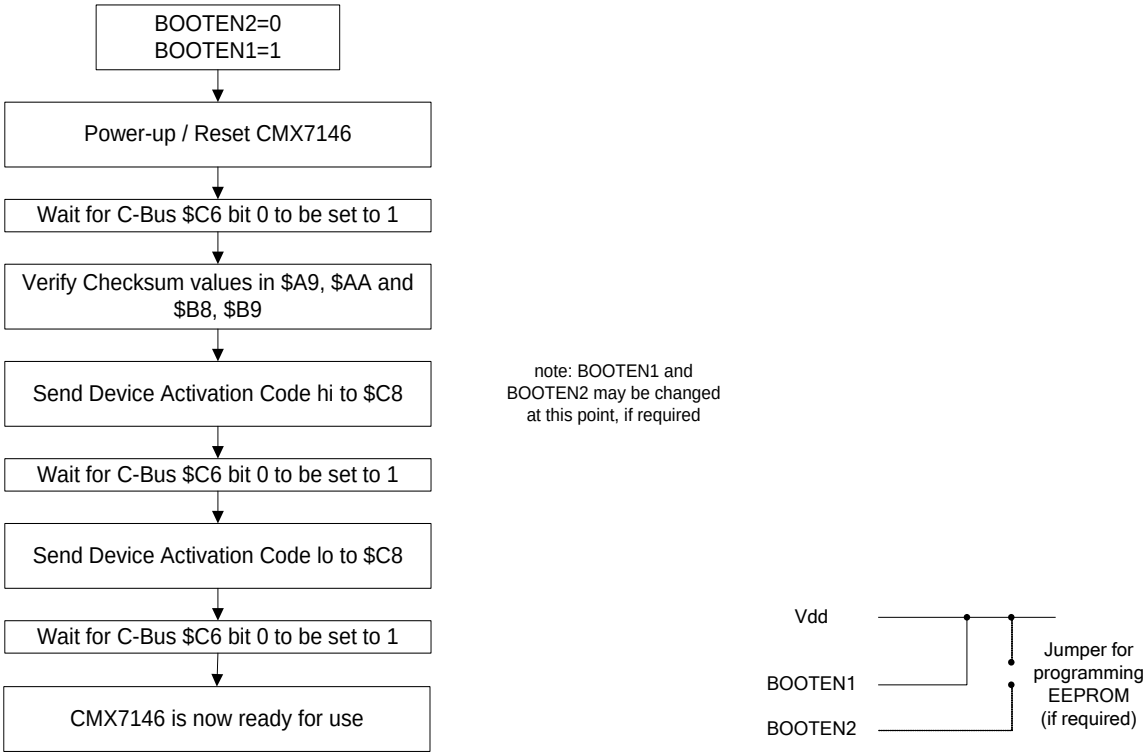


Figure 6 FI Loading from EEPROM

The CMX7146 has been designed to function with Atmel AT25HP512 serial EEPROM and the AT25F512 Flash EEPROM devices, however other manufacturers parts may also be suitable.

6.4 Device Control

Once the Function Image is loaded the CMX7146 can be set into one of two main operating modes using the Modem Mode and Control - $C1 write register:

- Idle mode – for powersave or device configuration
- Transmit mode – for transmission of data

These modes are described in the following sections. All control is carried out over the C-BUS interface: either directly to operational registers in Transmit mode or by using the Programming register ($C8) in Idle.

Additional Power-saving can be achieved in Idle mode by disabling unused hardware blocks, however care must be taken not to disturb any sections that are automatically controlled. Note that the BIAS block must be enabled to allow any of the Input or Output blocks to function.

When placed in an active Transmit mode the CMX7146 will begin by switching GPIO signals as configured by the transmit sequence. The RAMDAC can also be configured to ramp up at this point. Transmission begins with the data supplied by the host being encoded, filtered and output via MOD1 and MOD2. After all the data has been sent the burst ends with the RAMDAC ramping down and/or GPIO signals switching.

- Power Down Control - $C0 write
- Modem Mode and Control - $C1 write
- TxData0 - $B5 write (plus TxData1-6)
- Programming Register – $C8 write

6.4.1 Device Configuration (using the Programming Register)

While in Idle mode the programming register becomes active. The programming register provides access to the programming blocks which allow configuration of many device features including:

- Selection of baud rates, RRC filter bandwidth and data encoding method
- Selection of Automatic control of GPIO1-4 and the RAMDAC during transmission
- Configuration of RAMDAC profile
- Configuration of AuxADC and averaging
- Programming of input and output gains and offsets.

Full details of operation are given in section 9.2 in the User Manual.

6.4.2 Device Configuration (using dedicated registers)

Some features may be configured using dedicated registers which are available at all times including while in Transmit mode. These include:

- Auxiliary ADC detect thresholds
- Auxiliary ADC input selection and averaging mode
- Power down control
- Input gain and input/output signal routing

The registers that allow configuration of these features are:

- Aux config - $A7 write
- AuxConfig2 - $CD write
- Power Down Control - $C0 write
- AuxConfig2 - $CD write
- Input Gain and Input/Output Signal Routing - $B1 write

6.4.3 Interrupt Operation

The CMX7146 can produce an interrupt output to the host when various events occur. Each event has an associated status register bit and an interrupt mask register bit. The interrupt mask register is used to select which status events will trigger an interrupt on the IRQN line. Events can all be masked using the IRQ mask bit (bit 15) or individually masked using the interrupt mask register. Enabling an interrupt by setting a mask bit (0→1) after the corresponding Status register bit has already been set to 1 will also cause the an interrupt on the IRQN line. The IRQ bit (bit 15) of the status register reflects the IRQN line state.

All interrupt flag bits in the Status register, except the Programming Flag (bit 0), are cleared and the interrupt request is cleared following the command/address phase of a C-BUS read of the Status register. See:

- Interrupt Mask - $CE write
- Status - $C6 read

6.4.4 Signal Routing

The CMX7146 offers two modulator outputs MOD1 and MOD2 which provide I/Q output for in-phase and quadrature signals. Note that for BPSK modulation the signal is the same on both outputs. The analogue gain / attenuation of each output can be set individually, with additional Fine Attenuation control available via the Programming registers. See:

- Input Gain and Input/Output Signal Routing - $B1 write
- AuxConfig2 - $CD write

6.4.5 Loading Transmit Data

The first block of data MUST be loaded into the TxData registers BEFORE executing the Modem Mode change to transmit it.

The host should write the data block to the C-BUS TxData registers and then set modem control to the required transmit type with the Mode bits as Tx. As soon as the data has been read from the C-BUS TxData registers the DataRDY IRQ will be asserted. More data should be loaded into the TxData registers at this stage before data buffered in the CMX7146 runs out, otherwise the burst will end.

For precise control of the instant that transmission starts it is possible to trigger a transmission using GPIO1 as an input. In addition to triggering the modulation output, it is possible to define a transmission sequence with defined RAMDAC ramp up/down, and GPIO on/off events. The transmission sequence is configured using Program Block 1.

6.4.6 The Transmit Sequence

The CMX7146 is capable of being configured to provide the following features:

1. Selecting Tx mode results in transmission beginning directly on entry to Tx mode

2. Once started, transmission can be configured to be a simple modulation output or can include a programmable sequence of events including RAMDAC rampup/down and GPIO On/Off.

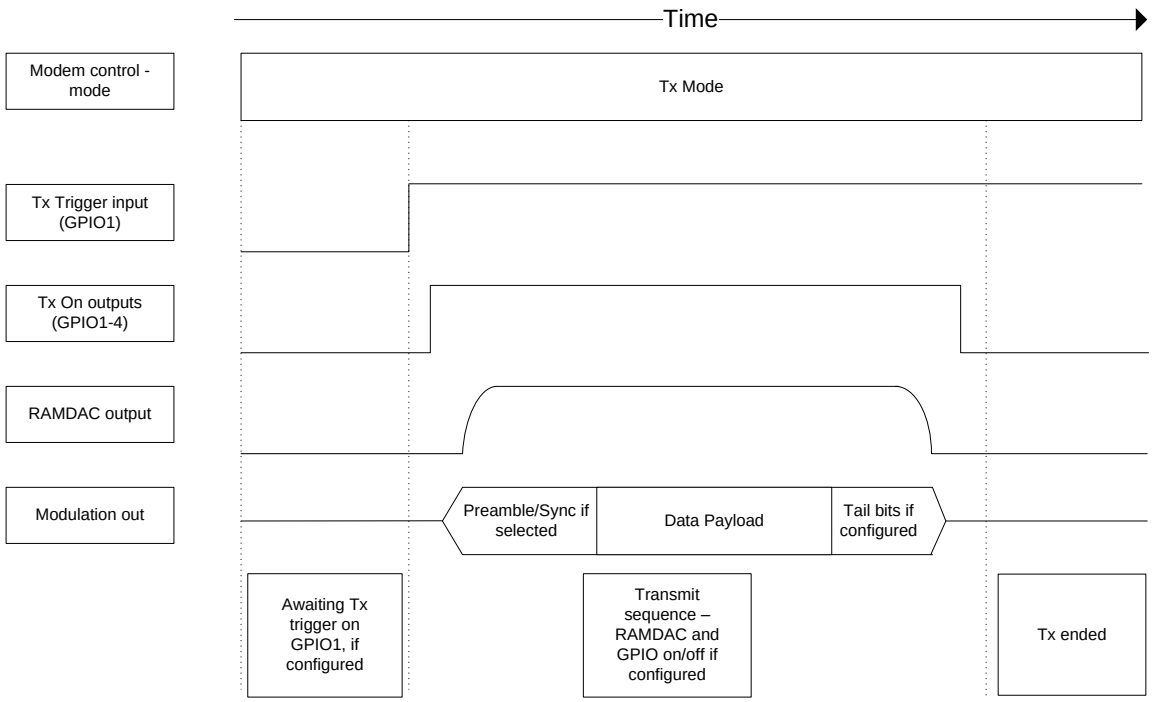


Figure 7 Transmit Sequence

6.4.7 Other Modem Modes

Tx PRBS mode transmits an internally generated pseudo-random data sequence for test and alignment.

6.4.8 Data Transfer

The payload data is transferred to and from the host via a block of seven Tx 16-bit C-BUS registers which allow up to 104 bits (13 bytes) of data to be transferred at once.

- Modem Mode and Control - $C1 write
- TxData0 - $B5 write containing control fields and data (and TxData 1-6 containing data only)

Table 2 C-BUS Data Registers

C-BUS Address	Function
$B5	Tx data 0-7 & control
$B6	Tx data 8-23
$B7	Tx data 24-39
$CA	Tx data 40-55
$CB	Tx data 56-71
$C2	Tx data 72-87
$C7	Tx data 88-103

TxData0 holds a Transaction Counter. This a two-bit counter which the host must increment (modulo 4) on every write to the TxData block. If the CMX7146 identifies that a block has been written out of sequence, the Event IRQ will be asserted. The device detects that new data from the host is available by the change in the value of the Transaction Counter, therefore the host should ensure that all the data is available in the TxData block before updating this register (ie, TxData0 should be the last register the host writes to in any block transfer).

6.4.9 Raw Data Transfer

When transferring raw data the lowest 8 bits of the TxData0 register is reserved for a Byte/Bit selector, Byte/Bit Counter and a Transaction Counter to allow the host to identify any data loss, and the remaining 104 bits hold the data to be transmitted. The byte count indicates how many bytes in the data block are valid and so reduces the need to perform a full 7 word C-BUS write if only small blocks of data need to be transferred. The Byte/Bit selector provides a bit transfer mode, which while less efficient (in terms of C-BUS accesses to transfer a quantity of data) provides a facility to transmit a burst of arbitrary length, not just a whole number of bytes. It is suggested that data is transferred in the maximum size blocks possible until the end of a burst - where the remaining bits, or bytes can be transferred in a single transaction of the required size.

6.4.10 Pre-loading transmit data

It is possible to pre-load a number of transactions in to the CMX7146 before transmission begins. To do this the host should load the first transaction into the TxData registers and then select transmit(idle) mode. The first transaction will be loaded into the CMX7146 but no transmission will begin. Further transactions may be loaded in, creating a larger buffer of data than the TxData registers can hold themselves. Once the buffer is full the CMX7146 will stop accepting transactions. Next, an active Tx mode should be selected by the host and the data in the buffer will be transmitted allowing the host to load further transactions, as the buffer becomes free. The buffer is cleared when the host changes the lower two bits of the modem control register.

6.4.11 Auxiliary clock rates

Auxiliary functions including carrier sensing, Aux ADC, DAC and GPIO updates operate on an internal clock. This rate will be referred to in describing these functions. The AuxClk speed is given by:

In Idle: AuxClk = Xtal Frequency / (P3.2 x (P3.3 – 128) x 8)
In Tx, if P3.7 less than 256: AuxClk = symbol rate x 5/4
In Tx, if P3.7 more than 256: AuxClk = symbol rate x 5/2

6.4.12 Auxiliary data

The CMX7146 provides 2 auxiliary data registers. These can each be independently configured to output the following information:

- Aux ADC 1 input data and threshold detect status
- Aux ADC 2 input data and threshold detect status
- The input on GPIO pins 1-4 if configured as inputs
- The RSSI of any signal, based on the selected RSSI input

The information is selected using the AuxConfig register. See:

- Aux config - $A7 write
- Aux data1 - $A9 read
- Aux data2 - $AA read

6.4.13 GPIO Pin Operation

The CMX7146 provides 4 GPIO pins, each pin can be configured independently as automatic/manual, input/output and rising/falling (with the exception of the combination automatic + input which is only allowed for GPIO1).

Pins that are automatic outputs become part of a transmit sequence and will automatically switch, along with the RAMDAC (if it is configured as automatic) during the course of a burst. Pins that are manual are under direct user control. When automatic a rising, or a falling event at the start or end of transmission will cause the specified GPIO to get switched high or low accordingly.

GPIO1 may be configured as an automatic input. This means that any attempted transmission will wait until GPIO1 input is high (if rising is selected) or low (if falling is selected).

See:

- Program Block 1 – Burst Tx Sequence + GPIO configuration
- Aux config - $A7 write
- Aux data1 - $A9 read
- Aux data2 - $AA read
- AuxConfig2 - $CD write

6.4.14 Auxiliary ADC Operation

The inputs to the two Auxiliary ADCs can be independently routed to any of the Signal Input pins under control of the Signal Routing register, $A7. Conversions will be performed as long as a valid input source is selected, to stop the ADCs, the input source should be set to “off”. BIAS in the Power Down Control - $C0 write register must be enabled for Auxiliary ADC operation.

Averaging can be applied to the ADC readings by selecting the relevant bits in the Signal Routing register, $A7, the length of the averaging is determined by the value in the Programming register (P3.0 and P3.1), and defaults to a value of 0. This is a rolling average system such that a proportion of the current data will be added to the last value. The proportion is determined by the value of the average counter in P3.0 and P3.1. For an average value of 0; 50% of the current value will be applied, for a value of 1 = 25%, 2 = 12.5% etc. The maximum useful value of this field is 8.

High and Low thresholds may be independently applied to both ADC channels (the comparison is applied after averaging, if this is enabled) and an IRQ generated as required (except in the case where the high threshold has been set below the low threshold). The thresholds are programmed via the AuxADC Threshold register, $CD.

Auxiliary ADC data is read back in the AuxADC Data registers ($A9 and $AA) and includes the threshold status as well as the actual conversion data (subject to averaging, if enabled).

The Aux ADC sample rate is affected by settings in Program Block 3 – AuxDAC, RAMDAC and Clock control. The rate will be the AuxClk rate, see 6.4.11 Auxiliary clock rates.

See:

- Aux config - $A7 write
- Aux data1 - $A9 read
- Aux data2 - $AA read
- AuxConfig2 - $CD write

6.4.15 Auxiliary DAC / RAMDAC Operation

The four Auxiliary DAC channels are programmed via the AuxDAC Control register, $A8. AuxDAC channel 1 may also be programmed to operate as a RAMDAC which will autonomously output a pre-programmed profile at a programmed rate. The RAMDAC may be configured as automatic or manual using Program Block 1 – Burst Tx Sequence + GPIO configuration. The AuxDAC Control register, $A8, with b12 set, controls the RAMDAC mode of operation when configured as a manually triggered RAMDAC.

The default profile is a raised cosine (see Table 5 in the user manual), but this may be over-written with a user defined profile by writing to Program Block 3. The RAMDAC operation is only available in Tx mode and, to avoid glitches in the ramp profile, it is important not to change to IDLE whilst the RAMDAC is still ramping. The AuxDAC outputs hold the user-programmed level during a powersave operation if left enabled, otherwise they will return to zero. Note that access to all four AuxDACs is controlled by the AuxDAC Control register, $A8, and therefore to update all AuxDACs requires four writes to this register. It is not possible to simultaneously update all four AuxDACs.

See:

- AuxDAC control / data - $A8 write

6.5 Digital System Clock Generators

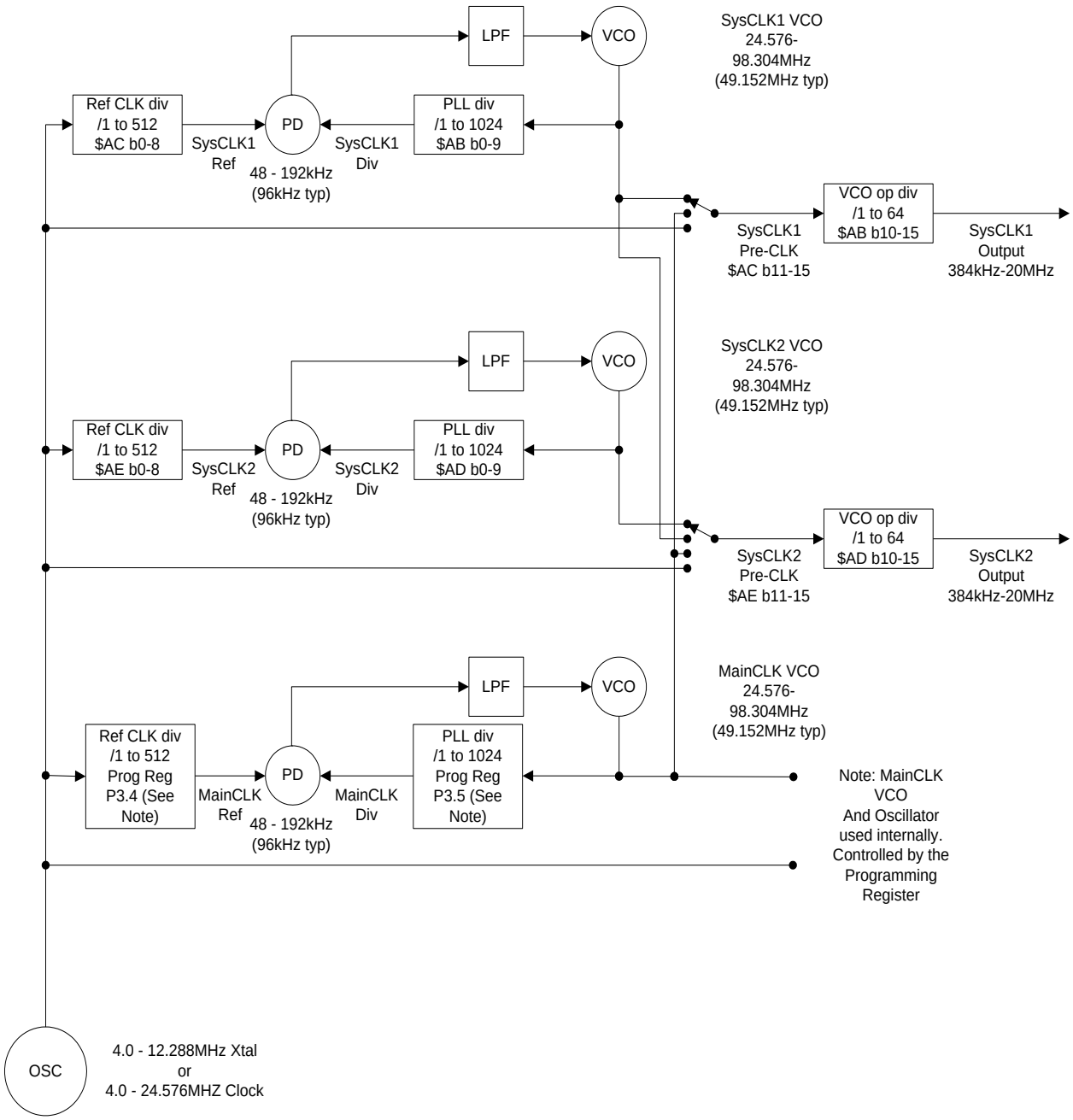


Figure 8 Digital Clock Generation Schemes

The CMX7146 includes a 2-pin crystal oscillator circuit. This can either be configured as an oscillator, as shown in section Xtal Frequency 6.1, or the XTAL input can be driven by an externally generated clock. In this implementation, the Xtal source frequency must be a 19.2 MHz oscillator.

6.5.1 System Clock Operation

Two System Clock outputs, SysClock1 Out and SysClock2 Out, are available to drive additional circuits, as required. These are digital phase locked loop (PLL) clocks that can be programmed via the System Clock registers with suitable values chosen by the user. The System Clock PLL Configure registers ($AB and $AD) control the values of the VCO Output divider and Main Divide registers, while the System Clock Ref. Configure registers ($AC and $AE) control the values of the Reference Divider and signal routing configurations. The PLLs are designed for a reference frequency of 96kHz. If not required, these clocks can be independently powersaved. The clock generation scheme is shown in the block diagram of Figure 8. Note that the output is inhibited until enabled by a host command over the C-BUS.

See:

- System CLK 1 and 2 PLL data - $AB, $AD write
- System CLK 1 and 2 REF - $AC and $AE write

6.6 Signal Level Optimisation

For the maximum signal out of the MOD1 and MOD2 attenuators, the signal level at the output of the Modem block is set to be 0dB, The Fine Output adjustment has a maximum attenuation of 1.8dB and no gain, whereas the Coarse Output adjustment has a variable attenuation of up to 44.8dB and no gain.

6.7 C-BUS Register Summary

Table 3 C-BUS Registers

ADDR. (hex)	R/W	REGISTER	Word Size (bits)
$01	W	C-BUS RESET	0
$A7	W	Aux Config	16
$A8	W	AuxDAC Data and Control	16
$A9	R	Aux Data1 and Status / Checksum 2 hi	16
$AA	R	Aux Data2 and Status / Checksum 2 lo	16
$AB	W	System Clk 1 PLL configure	16
$AC	W	System Clk 1 Ref configure	16
$AD	W	System Clk 2 PLL configure	16
$AE	W	System Clk 2 Ref configure	16
$AF		Reserved	
$B0		Reserved	
$B1	W	Input Gain and Signal Routing	16
$B2		Reserved	
$B3		Reserved	
$B4		Reserved	
$B5	W	TxData0	16
$B6	W	TxData1	16
$B7	W	TxData2	16
$B8	R	Checksum 1 hi	16
$B9	R	Checksum 1 lo	16
$BA		Reserved	16
$BB		Reserved	16
$BC		Reserved	16
$BD		Reserved	16
$BE		Reserved	
$BF		Reserved	
$C0	W	Power-Down Control	16
$C1	W	Modem Control	16
$C2	W	TxData5	16
$C3		Reserved	
$C5		Reserved	16
$C6	R	IRQ Status	16
$C7	W	TxData6	16
$C8	W	Programming Register	16
$C9		Reserved	16

ADDR. (hex)	R/W	REGISTER	Word Size (bits)
$CA	W	TxData3	16
$CB	W	TxData4	16
$CC		Reserved	16
$CD	W	GPIO write/AuxADC Thresholds	16
$CE	W	Interrupt Mask	16
$CF		Reserved	

All other C-BUS addresses (including those not listed above) are either reserved for future use or allocated for production testing and must not be accessed in normal operation.

7 CMX7146 FI-1.x Features

7.1 Modulation

The modulation process is shown in Figure 9. The data to be transmitted is optionally passed through a differential encoder and is then converted to NRZ symbol format. The symbol stream is interpolated and filtered using a Root Raised-Cosine (RRC) pulse-shaping filter with a selectable roll-off factor (alpha). The resulting baseband signal is duplicated on both I and Q outputs.

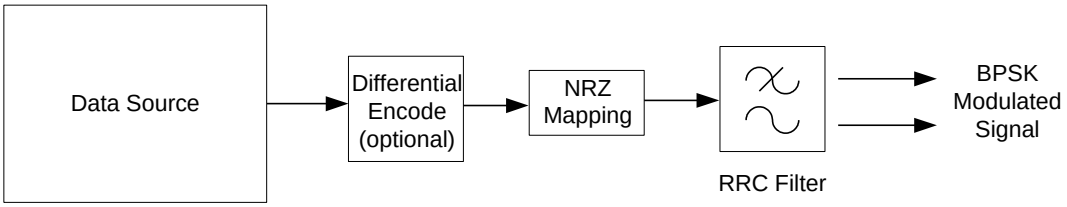


Figure 9 Modulation Process

7.2 Radio Interface

The CMX7146 should be configured to output I/Q modulation (Note: See section 7.1). An overview of how the CMX7146 might integrate into a transmitter, such as the CMX971, is shown in Figure 10. An alternative configuration showing the CMX7146 with the CMX993 is shown in Figure 11.

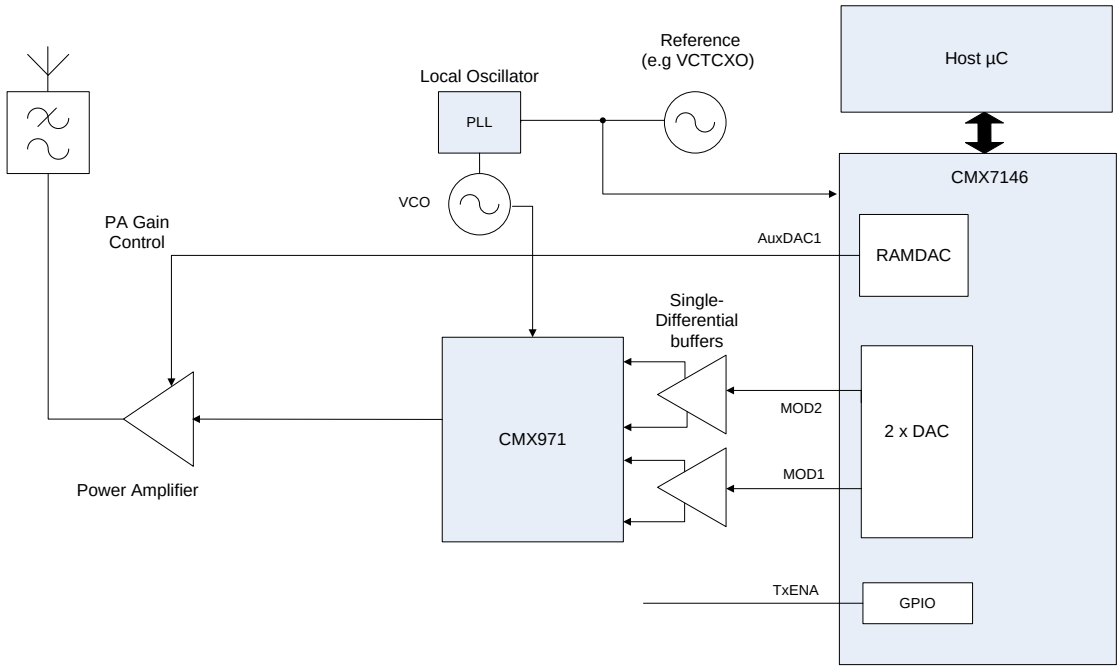


Figure 10 Outline Radio Design CMX7146/CMX971

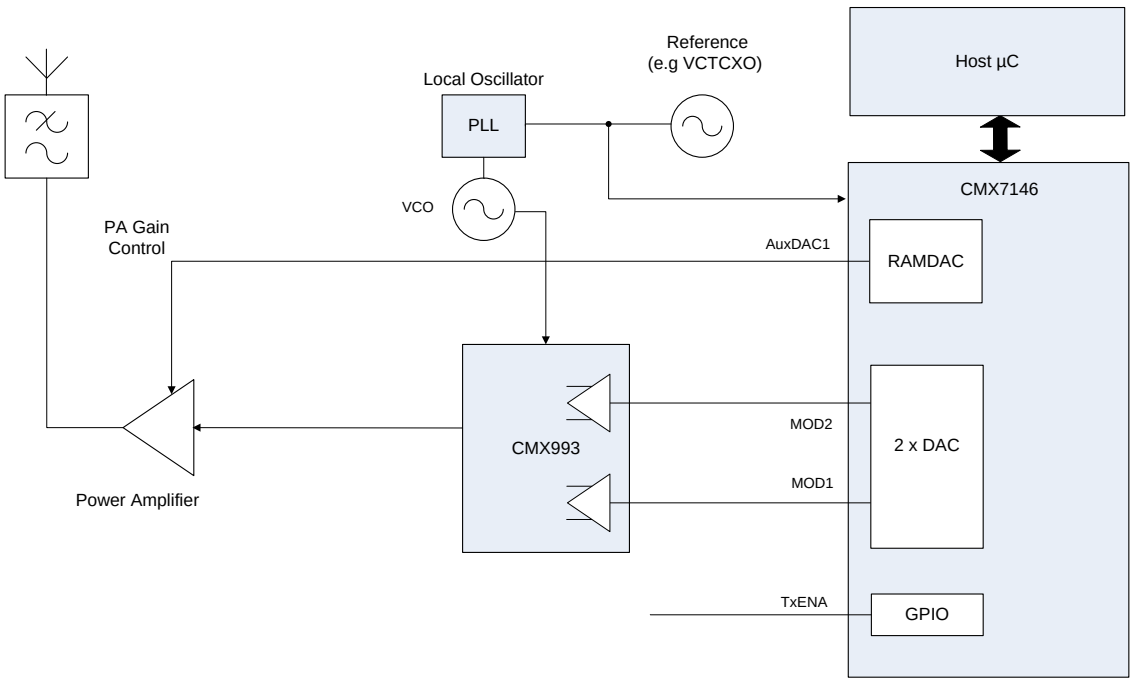
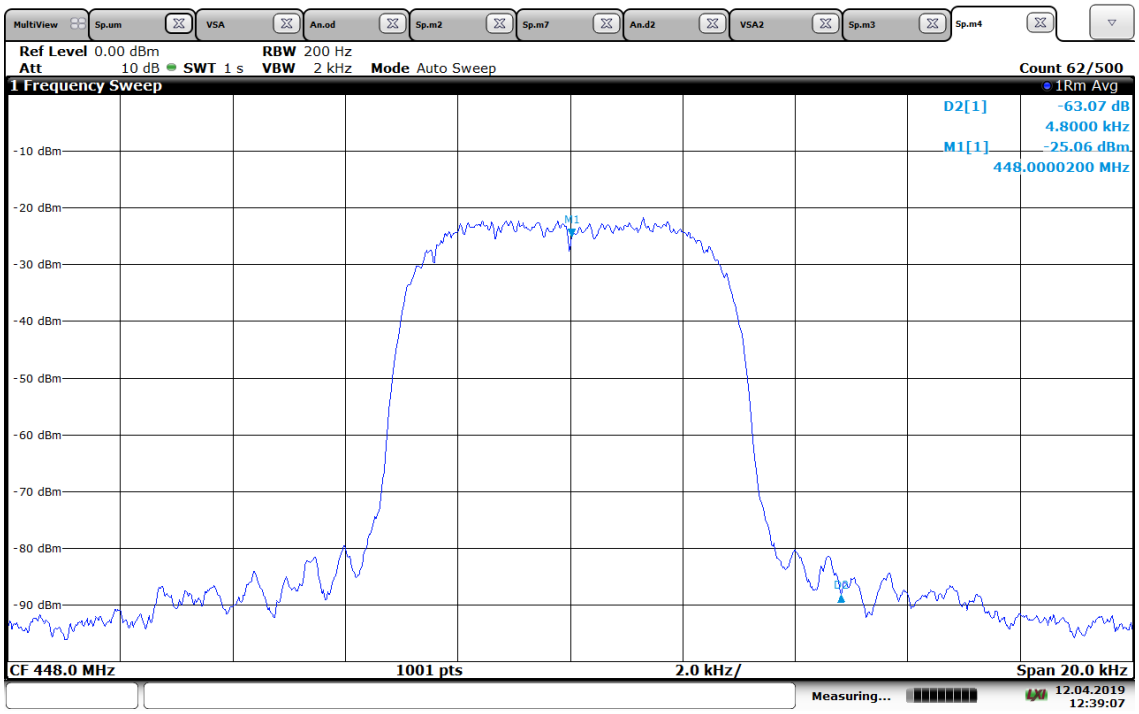


Figure 11 Outline Radio Design CMX7146/CMX993

7.3 Transmit Performance

The following figures show the Tx spectrum from the CMX7146. The results are measured on a spectrum/modulation analyser. The internal PRBS generator in the CMX7146 was used to generate the data using 4.8 kbps, Bt=0.3, $B0=$1100 to give a 200 mV pp I/Q output signal at MOD1 and MOD2. The resulting waveform exhibits a Peak-to-Mean ratio of 4.7 and it is essential that the following RF stages be configured so that they do not overload with the peak signal. It is also essential to minimise the Dc offsets from the MOD outputs through the single-to-differential converters to the I/Q inputs of the CMX971. These may be trimmed internally using P4.4 and P4.5. In this instance the CMX971 produced an output of -7.5 dBm mean / -3 dBm peak.



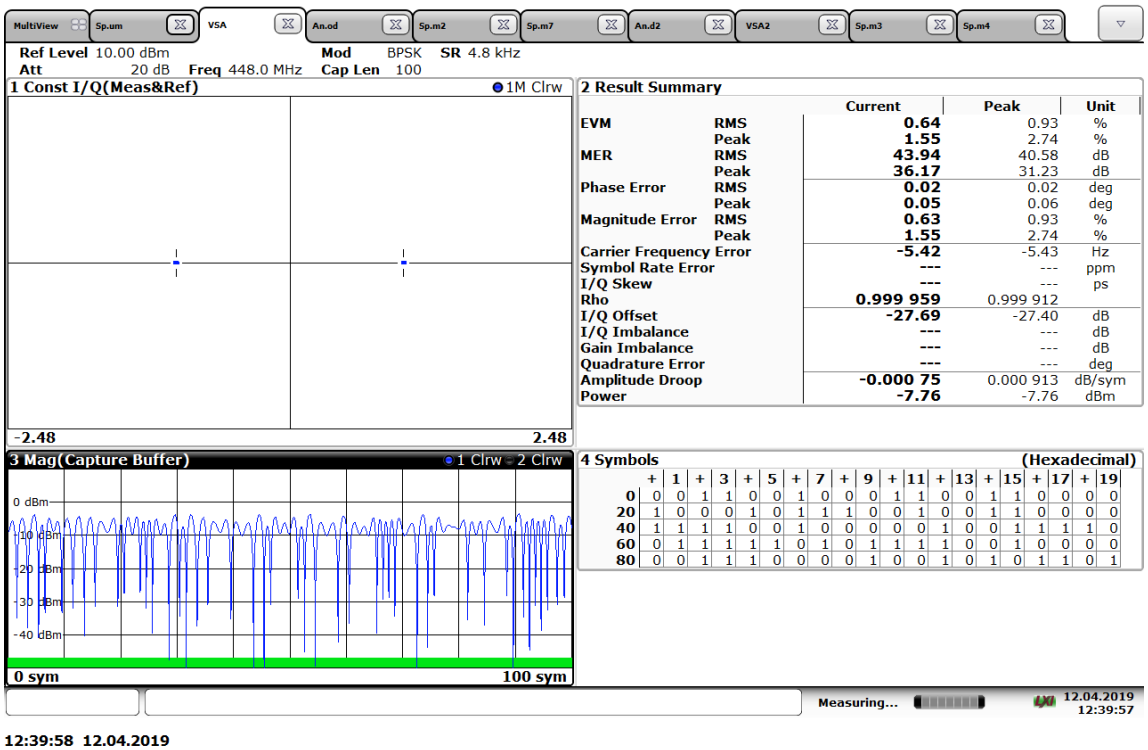


Figure 12 Tx Modulation Spectra MOD1/MOD2 I/Q output to Sig Gen 4800 bps

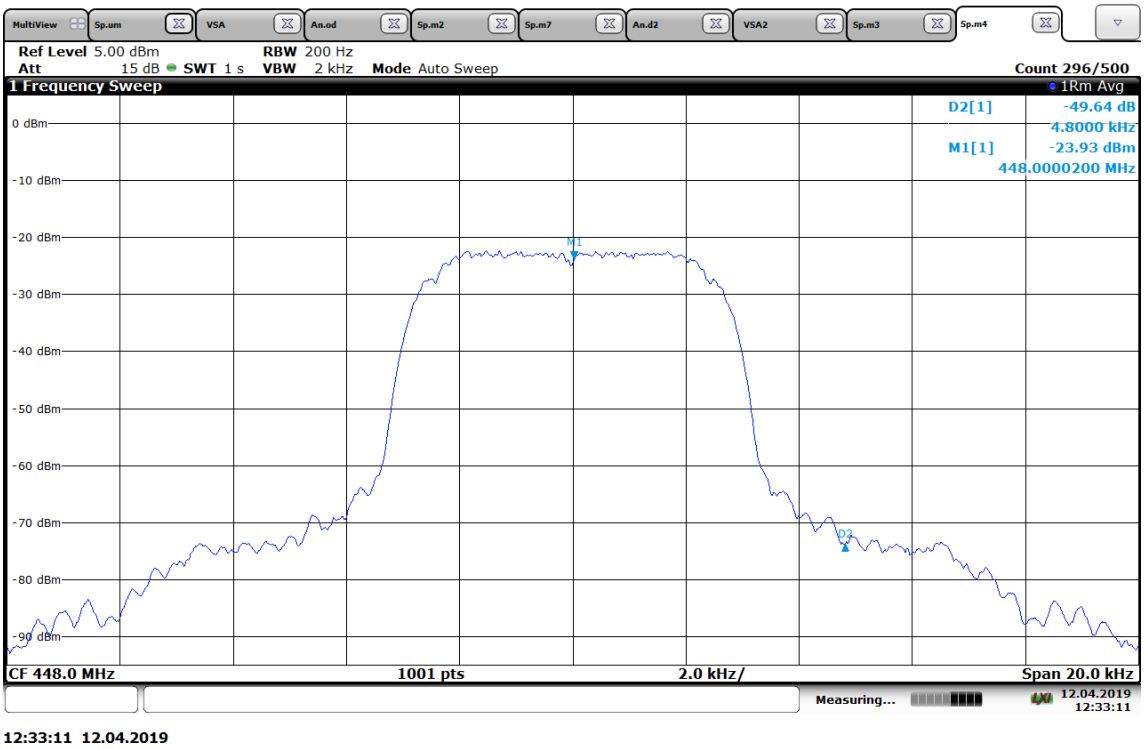


Figure 13 TX Modulation output from CMX971 4800 bps

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Unit
Supply: DV_{DD}- DV_{SS}	−0.3	4.5	V
AV_{DD}- AV_{SS}	−0.3	4.5	V
Voltage on any pin to DV_{SS}	−0.3	DV_{DD} + 0.3	V
Voltage on any pin to AV_{SS}	−0.3	AV_{DD} + 0.3	V
Current into or out of any power supply pin (excluding V_{BIAS}) (i.e. V_{DEC}, AV_{DD}, AV_{SS}, DV_{DD} or DV_{SS})	−30	+30	mA
Current into or out of any other pin	−20	+20	mA
Voltage differential between power supplies:			
DV_{DD} and AV_{DD}	0	0.3	V
DV_{SS} and AV_{SS}	0	50	mV

Q3 Package (48-pin VQFN)	**Min.**	**Max.**	**Unit**
Total Allowable Power Dissipation at Tamb = 25°C	–	1750	mW
... Derating	–	17.5	mW/°C
Storage Temperature	−55	+125	°C
Operating Temperature	−40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Unit
Supply Voltage:				
DV_{DD} – DV_{SS}		3.0	3.6	V
AV_{DD} – AV_{SS}		3.0	3.6	V
V_{DEC} – DV_{SS}	12	2.25	2.75	V
Operating Temperature		−40	+85	°C
XTAL/CLK Frequency (using an external clock)	11		19.2	MHz

Notes: 11 Nominal CLK frequency is 19.2 MHz

12 The VDEC supply is automatically derived from DVDD by the on-chip voltage regulator.

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Clk Frequency = 19.2 MHz±0.01% (100ppm); Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.3V.
V_{DEC} = 2.5V
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V.
Signal levels track with supply voltage, so scale accordingly.
Signal to Noise Ratio (SNR) in bit rate bandwidth.

Current consumption figures quoted in this section apply to the device when loaded with FI1.x only. The use of other Function Images™, can modify the current consumption of the device.

DC Parameters	Notes	Min.	Typ.	Max.	Unit
Supply Current	21				
All Powersaved					
DI_{DD}		–	8	100	µA
AI_{DD}		–	4	20	µA
IDLE Mode	22				
DI_{DD}		–	1.8	–	mA
AI_{DD}		–	4	–	µA
Tx Mode	22				
DI_{DD} (600 bps – I/Q)		–	3.8	–	mA
DI_{DD} (1200 bps – I/Q)		–	4.0	–	mA
DI_{DD} (2400 bps – I/Q)		–	4.6	–	mA
DI_{DD} (3600 bps – I/Q)		–	6.2	–	mA
DI_{DD} (4800 bps – I/Q)		–	8.0	–	mA
DI_{DD} (9600 bps – I/Q)		–	9.9	–	mA
AI_{DD} (600 bps – I/Q)		–	3.0	–	mA
AI_{DD} (1200 bps – I/Q)		–	3.1	–	mA
AI_{DD} (2400 bps – I/Q)		–	3.2	–	mA
AI_{DD} (3600 bps – I/Q)		–	3.3	–	mA
AI_{DD} (4800 bps – I/Q)		–	4.9	–	mA
AI_{DD} (9600 bps – I/Q)		–	5.0	–	mA
Additional current for each Auxiliary System Clock (output running at 4MHz)					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	250	–	µA
Additional current for each Auxiliary ADC					
DI_{DD} (DV_{DD} = 3.3V, V_{DEC} = 2.5V)		–	50	–	µA
Additional current for each Auxiliary DAC					
AI_{DD} (AV_{DD} = 3.3V)		–	200	–	µA

Notes:
21 Tamb = 25°C, not including any current drawn from the device pins by external circuitry.
22 System Clocks, Auxiliary circuits disabled, but all other digital circuits (including the Main Clock PLL) enabled. Active mode = TX raw with a repeating test signal.
$B1 = $0298
$B0 = $7700 (0dB MOD1 and MOD2)
$C0 = $0FC0 (DAC1, DAC2, MOD1, MOD2 enabled)
$CD = $8000 (0dB output gain)

DC Parameters (continued)		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK		25				
Input Logic '1'			70%	–	–	DV_{DD}
Input Logic '0'			–	–	30%	DV_{DD}
Input current (Vin = DV_{DD})			–	–	40	µA
Input current (Vin = DV_{SS})			–40	–	–	µA
C-BUS Interface and Logic Inputs						
Input Logic '1'			70%	–	–	DV_{DD}
Input Logic '0'			–	–	30%	DV_{DD}
Input Leakage Current (Logic '1' or '0')		21	–1.0	–	1.0	µA
Input Capacitance			–	–	7.5	pF
C-BUS Interface and Logic Outputs						
Output Logic '1'	(I_{OH} = 120µA)		90%	–	–	DV_{DD}
	(I_{OH} = 1mA)		80%	–	–	DV_{DD}
Output Logic '0'	(I_{OL} = 360µA)		–	–	10%	DV_{DD}
	(I_{OL} = -1.5mA)		–	–	15%	DV_{DD}
"Off" State Leakage Current		21	–	–	10	µA
IRQN	(Vout = DV_{DD})		–1.0	–	+1.0	µA
REPLY_DATA (output HiZ)			–1.0	–	+1.0	µA
V_{BIAS}		26				
Output voltage offset wrt $AV_{DD}/2$ (I_{OL} < 1µA)			–	±2%	–	AV_{DD}
Output impedance			–	22	–	kΩ

Notes:

25 Characteristics when driving the XTAL/CLK pin with an external clock source.

26 Applies when utilising V_{BIAS} to provide a reference voltage to other parts of the system. When using V_{BIAS} as a reference, V_{BIAS} must be buffered. V_{BIAS} must always be decoupled with a capacitor as shown in Figure 2.

AC Parameters		Notes	Min.	Typ.	Max.	Unit
XTAL/CLK Input						
'High' pulse width		31	15	–	–	ns
'Low' pulse width		31	15	–	–	ns
Input impedance (at 9.6MHz)						
Powered-up	Resistance		–	150	–	kΩ
	Capacitance		–	20	–	pF
Powered-down	Resistance		–	300	–	kΩ
	Capacitance		–	20	–	pF
Xtal start up (from powersave)			–	20	–	ms
Auxiliary System Clk 1/2 Outputs						
XTAL/CLK input to CLOCK_OUT timing:						
(in high to out high)		32	–	15	–	ns
(in low to out low)		32	–	15	–	ns
'High' pulse width		33	48	52.08	56	ns
'Low' pulse width		33	48	52.08	56	ns
V_{BIAS}						
Start up time (from powersave)			–	30	–	ms

Notes:
31 Timing for an external input to the XTAL/CLK pin.
32 XTAL/CLK input driven by an external source.
33 19.2 MHz Clk fitted and 19.2 MHz output selected.

AC Parameters	Notes	Min.	Typ.	Max.	Unit
Modulator Outputs 1/2 (MOD 1, MOD 2)					
Power-up to output stable	41	–	50	100	µs
Modulator Attenuators					
Attenuation (at 0dB)	43	−1.0	0	+1.0	dB
Cumulative Attenuation Error (wrt attenuation at 0dB)	43	−0.6	0	+0.6	dB
Output Impedance Enabled	42	–	600	–	Ω
Output Impedance Disabled	42	–	500	–	kΩ
Output current range (AV_{DD} = 3.3V)		–	–	±125	µA
Output voltage range	44	0.5	–	AV_{DD} –0.5	V
Load resistance		20	–	–	kΩ

Notes:

41 Power-up refers to issuing a C-BUS command to turn on an output. These limits apply only if V_{BIAS} is on and stable. At power supply switch-on, the default state is for all blocks, except the XTAL and C-BUS interface, to be in placed in powersave mode.

42 Small signal impedance, at AV_{DD} = 3.3V and Tamb = 25°C.

43 With respect to the signal at the feedback pin of the selected input port.

44 Centred about $AV_{DD}/2$; with respect to the output driving a 20kΩ load to $AV_{DD}/2$.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Auxiliary Signal Inputs (Aux ADC 1 to 4)					
Source Output Impedance	51	–	–	24	kΩ
Auxiliary 10 Bit ADCs					
Resolution		–	10	–	Bits
Maximum Input Level (pk-pk)	54	–	–	80%	AV_{DD}
Input impedance					
Resistance		–	10	–	MΩ
Capacitance		–	5	–	pF
Zero error (input offset to give ADC output = 0)		0	–	±10	mV
Integral Non-linearity		–	–	±3	LSBs
Differential Non-linearity	53	–	–	±1	LSBs
Auxiliary 10 Bit DACs					
Resolution		–	10	–	Bits
Maximum Output Level (pk-pk), no load	54	80%	–	–	AV_{DD}
Zero error (output offset from a DAC input = 0)		0	–	±10	mV
Resistive Load		5	–	–	kΩ
Integral Non-linearity		–	–	±4	LSBs
Differential Non-linearity	53	–	–	±1	LSBs

Notes:

51 Denotes output impedance of the driver of the auxiliary input signal, to ensure < 1 bit additional error under nominal conditions.

53 Guaranteed monotonic with no missing codes.

54 Centred about $AV_{DD}/2$.

8.1.4 Parametric Performance

For the following conditions unless otherwise specified:
External components as recommended in Figure 2.
Maximum load on digital outputs = 30pF.
Clk Frequency = 19.2 MHz ±0.01% (100ppm)); Tamb = −40°C to +85°C.
AV_{DD} = DV_{DD} = 3.0V to 3.6V.
Reference Signal Level = 308mV rms at 1kHz with AV_{DD} = 3.3V
Signal levels track with supply voltage, so scale accordingly.
Output stage attenuation = 0dB.

All figures quoted in this section apply to the device when loaded with FI1.x only. The use of other Function Images™, can modify the parametric performance of the device.

AC Parameters (cont.)	Notes	Min.	Typ.	Max.	Unit
Modem symbol rate		400		9600	sym s^{-1}
Modulation			BPSK		
Filter BT			Selectable: 0.2,0.3,0.35		
Tx mod accuracy			1		% RMS
Tx adjacent channel power (MOD1, MOD2, prbs)	65	70	74		dB

Notes:

64	Transmitting continuous default preamble
65	When used with CMX971

8.2 C-BUS Timing

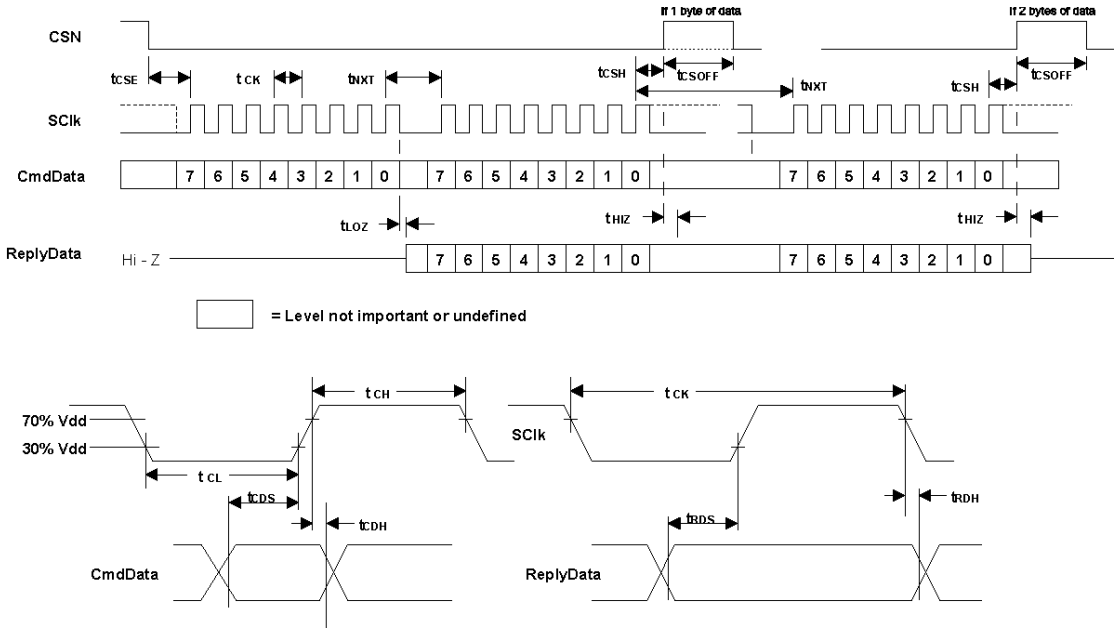


Figure 14 C-BUS Timing

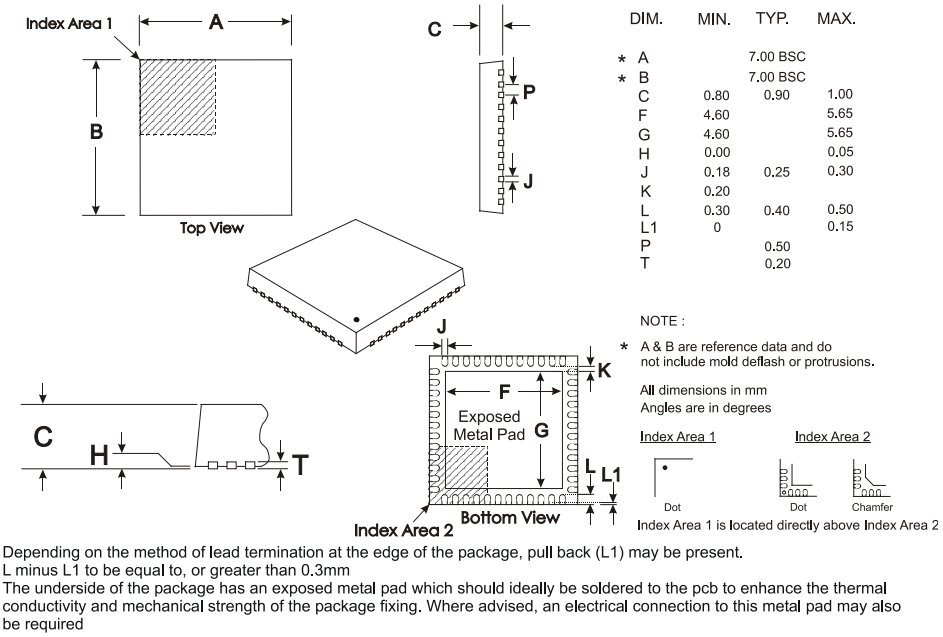
C-BUS Timing		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SClk high time		100	–	–	ns
t_{CSH}	Last SClk high to CSN high time		100	–	–	ns
t_{LOZ}	SClk low to ReplyData Output Enable Time		0.0	–	–	ns
t_{HIZ}	CSN high to ReplyData high impedance		–	–	1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0	–	–	µs
t_{NXT}	Inter-byte time		200	–	–	ns
t_{CK}	SClk cycle time		200	–	–	ns
t_{CH}	SClk high time		100	–	–	ns
t_{CL}	SClk low time		100	–	–	ns
t_{CDS}	Command Data setup time		75	–	–	ns
t_{CDH}	Command Data hold time		25	–	–	ns
t_{RDS}	Reply Data setup time		50	–	–	ns
t_{RDH}	Reply Data hold time		0	–	–	ns

Notes:

1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SERIAL_CLOCK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SERIAL_CLOCK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the latest version of C-BUS and allow faster transfers than the original C-BUS timing specification. The CMX7146 can be used in conjunction with devices that comply with the slower timings, subject to system throughput constraints.

8.3 Packaging



Depending on the method of lead termination at the edge of the package, pull back (L1) may be present.
L minus L1 to be equal to, or greater than 0.3mm
The underside of the package has an exposed metal pad which should ideally be soldered to the pcb to enhance the thermal conductivity and mechanical strength of the package fixing. Where advised, an electrical connection to this metal pad may also be required

Figure 15 Mechanical Outline of 48-pin VQFN (Q3)

Order as part no. CMX7146Q3

As package dimensions may change after publication of this datasheet, it is recommended that you check for the latest Packaging Information from the Datasheets page of the CML website: [www.cmlmicro.com].

About *FirmASIC*®

CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialisation. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

CML Microcircuits

United Kingdom	p: +44 (0) 1621 875500	e: sales@cmlmicro.com techsupport@cmlmicro.com
Singapore	p: +65 62888129	e: sg.sales@cmlmicro.com sg.techsupport@cmlmicro.com
United States	p: +1 336 744 5050 800 638 5577	e: us.sales@cmlmicro.com us.techsupport@cmlmicro.com

www.cmlmicro.com