Intel Agilex I-Series Transceiver-SoC Development Kit User Guide

Online Version
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1. Overview

Intel® Agilex™ I-Series Transceiver-SoC SI Development Kit is a complete design environment that includes both hardware and software you need to develop Intel Agilex I-Series FPGA designs. The board provides a wide range of peripherals and memory interfaces to facilitate the development of Intel Agilex I-Series Transceiver-SoC designs.

Table 1. Ordering Information

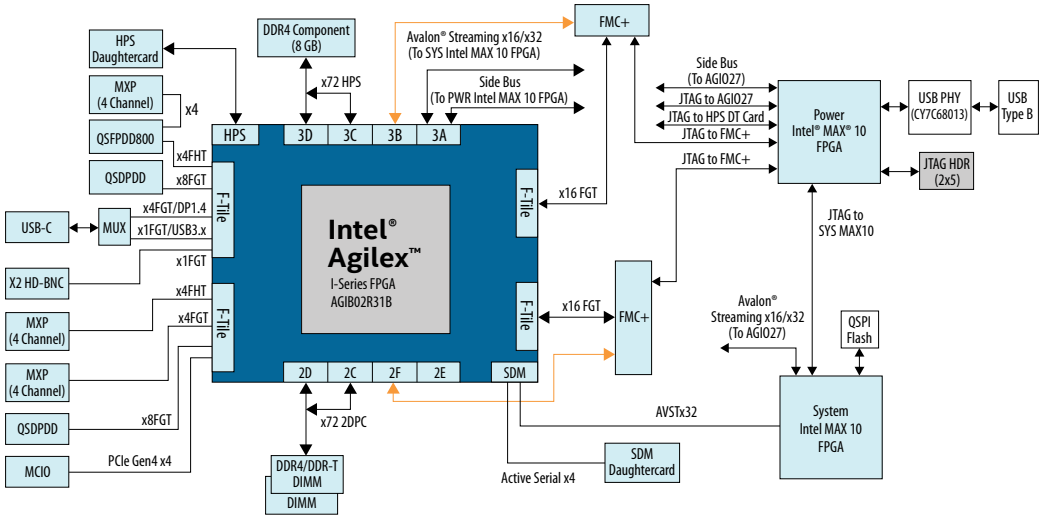
Development Kit Version	Ordering Code	Device Part Number	Serial Number Identifier
Intel Agilex I-Series Transceiver-SoC Development Kit (ES)	DK-SI-AGI027FES	AGIB027R31B1E2VR0	Under 500
Intel Agilex I-Series Transceiver-SoC Development Kit (ES)	DK-SI-AGI027FB	AGIB027R31B1E1VAA	Above 1000

For the board and FPGA capabilities, refer to the Intel Agilex FPGA and SoC page on the Intel website.

For more information about the *Intel Agilex Device Errata Sheet and User Guidelines (ES-1069)* and *Intel Agilex Known Issue List*, contact Intel Premier Support and quote ID #15011992053.

1.1. Block Diagram

Figure 1. Intel Agilex I-Series Transceiver-SoC Development Kit Block Diagram



1.2. Feature Summary

- Intel Agilex I-Series FPGA, 2.7M LE, 3184B package
- F-Tile 1 (13C)
  - 4 FHT transceiver channels fan out to Quad Small Form Factor Double Density 800 (QSFPDD800)
  - 8 FGT transceiver channels to Quad Small Form Factor Double Density connector
  - 2 FGT transceiver channels to HD-BNC for SDI
  - 4 FGT transceiver as DP2.0(1)
  - 1FGT transceiver for USB3.2(1)
- F-Tile 2 (13A)
  - 4 FHT transceiver channels (116G) to MXPM
  - 8 FGT transceiver channels (56G) to MXPM
  - 8 FGT transceiver channels to Quad Small Form Factor Double Density connector
  - 4 FGT transceiver channels to MCIO (PCIe*)
- F-Tile 3 (12C)
  - 16 FGT channels to FMC+
- F-Tile 4 (12A)
  - 16 FGT channels to FMC+
- SR DDR4 2666 (x72 w/ ECC), 16GB
- 8GB SR DDR4-2666 (x72 w/ ECC) component down (HPS)
- IO48 interface for HPS Out of Box Experience (OOBE) daughter cards

1.3. Box Contents

- Intel Agilex I-Series Transceiver-SoC Development Kit
- Single-rank DDR4 DIMM module
- QSPI flash daughter card
- HPS IO48 OOBE daughter card
- USB 2.0 Type B cable
- 240W power adapter and NA/EU/JP/UK cords

(1) Preliminary

1.4. Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Operating Condition	Range of Values
Ambient operating temperature range	0 °C to 30 °C
ICC load current	195 A
ICC load transient percentage	200 A/µs
FPGA maximum power supported by active heatsink/fan	220 W(2)

When handling the board, it is important to observe static discharge precautions.

Caution: Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the development kit.

Note: This development kit should not be operated in a vibration environment.

(2) 160W for core and 60W for FGT Transceiver

2. Getting Started

2.1. Intel Quartus® Prime Software and Driver Installation

Intel Quartus® Prime design software is a multiplatform design environment that easily adapts to your specific needs in all phases of FPGA, CPLD and SoC designs. The Intel Quartus Prime software delivers the highest performance and productivity for Intel FPGAs, CPLDs, and SoCs. Intel Quartus Prime Pro Edition software is optimized to support the advanced features in next-generation FPGAs and SoCs with the Intel Agilex, Intel Stratix® 10, Intel Arria® 10, and Intel Cyclone® 10 GX device families.

Intel Agilex I-Series Transceiver-SoC Development Kit includes on-board Intel FPGA Download Cable circuits for FPGA and system Intel MAX® 10 programming. However, for the host computer and board to communicate, you must install the Intel FPGA Download Cable driver on the host computer. Installation instructions for the Intel FPGA Download Cable driver for your operating system are available on the Intel website.

On the Intel website, navigate to the Cable and Adapter Drivers Information link to locate the table entry for your configuration and click the link to access the instructions.

The Intel SoC EDS is a comprehensive software tool suite for embedded software development on Intel SoC devices. It contains development tools, utility programs, run-time software, and application examples to expedite firmware and application software of SoC embedded systems.

As a part of the Intel SoC EDS, the Arm* Development Studio 5 (DS-5) Intel SoC FPGA Edition Toolkit provides a comprehensive set of embedded development tools for Intel's SoC FPGAs.

For more information and steps to install the Intel SoC EDS Tool Suite, refer to the links below.

Related Information

- Quick-Start for Intel Quartus Prime Pro Edition Software
- Intel Quartus Prime Pro Edition User Guide: Getting Started
- Arm DS-5 Intel SoC FPGA Edition Toolkit
- Intel SoC FPGA Embedded Development Suite User Guide

2.2. Design Examples

Unzip the install package which includes board design files, documents and examples directories. The table below lists the file directory names and a description of their contents.

Table 3. Installed Development Kit Directory Structure

Directory Name	Description of Directory Contents
board_design_files	Contains schematics, layout, assembly and bill of material board design files. Use these files as a starting point for a new prototype board design
documents	Contains the development kit documentation – quick start guides and user guide
examples	Contains: • Board Test System: BTS GUI, Power GUI, and Clock GUI • Golden Top project for pinout assignments management • Design Examples: Memory, XCVR, GPIO, PCIe Gen 4, System Intel MAX 10
factory_recovery	The original data programmed into flash U85 for AVST x32 configuration and System Intel MAX 10 before shipment. Use this data to restore the board with its original factory content.

3. Power Up the Development Kit

The instructions in this chapter explain how to setup the Intel Agilex I-Series Transceiver-SoC Development Kit for specific use cases.

3.1. Default Settings

The Intel Agilex I-Series Transceiver-SoC Development Kit ships with its board switches preconfigured to support the design examples in the kit. If you suspect your board might not be correctly configured with the default settings, follow the instructions in the factory default switch settings table to return to its factory settings before proceeding ahead.

Note: X refers to Don't Care in the table below.

Note: Don't set the switches when the power is on. Only set the switches after the power is off.

Table 4. Factory Default Switch Settings

Switch	Default Position	Default Function
S19 [1:4]	OFF/OFF/ON/ON	System Intel MAX 10 and FPGA selected in JTAG chain.
S20 [1:4]	ON/ON/ON/ON	Mode 1: On-board Intel download circuit act as the only JTAG master. Chained HPS with SDM nodes internally.
S9 [1:4]	ON/OFF/OFF/X	Configuration mode setting bits: AS - Fast mode
S10 [1:4]	ON/ON/ON/ON	SYS_SW[0:3] • SYS_SW[0]—Factory Loadn • '0'—Load image from Page 0 of the QSPI • SYS_SW[1]—MUX_SEL1 • SYS_SW[2]—MUX_SEL7 • SYS_SW[3]—MUX_SEL9

continued...

Switch	Default Position	Default Function
S15 [1:4]	ON/ON/ON/OFF	SYS_SW[4:7] • SYS_SW[4]—MUX_SEL_ZL • SYS_SW[5]—FMC-A PCIe RP/EP Select — "0": RP (Default) — "1": EP • SYS_SW[6]—FMC-B PCIe RP/EP Select — "0": RP (Default) — "1": EP • SYS_SW[7]—MCIO PCIe RP/EP Select — "0": RP — "1": EP (Default)
S1 [1:4]	OFF/OFF/OFF/OFF	User Switch [0:3]
S6 [1:4]	OFF/OFF/OFF/OFF	User Switch [4:7]
S22 [1:4]	ON/ON/ON/ON	MUX_DIP_SW[0:3] • MUX_DIP_SW0—MUX_SEL2 • MUX_DIP_SW1—MUX_SEL3 • MUX_DIP_SW2—MUX_SEL4 • MUX_DIP_SW3—MUX_SEL5 Set to "ON" by default to select on-board clock as input.
S23 [1:4]	ON/ ON / ON / ON	MUX_DIP_SW[4:7] • MUX_DIP_SW4—MUX_SEL10 • MUX_DIP_SW5—MUX_SEL11 • MUX_DIP_SW6—MUX_SEL12 • MUX_DIP_SW7—MUX_SEL14 Set "0"/closed by default for on-board clock as input.
S4 [1:4]	ON/ ON / ON / ON	MUX_DIP_SW[8:11] • MUX_DIP_SW8—MUX_SEL13 • MUX_DIP_SW9—MUX_SEL6 • MUX_DIP_SW10—MUX_SEL0 • MUX_DIP_SW11—MUX_SEL8 Set "0"/closed by default for on-board clock as input.

3.2. Power Up

To power up the development kit, follow these steps:

1. Use the provided 240 W power adapter to supply power through **J30**.
2. After power adapter is plugged into **J30** and switch **S18** is set to the **ON** position, **D22** LED illuminates, indicating that the board power up successfully. If the LED (**D22**) is not turned ON, it indicates that one or more power supply is incorrect.

3.3. Perform Board Restore

This development kit ships with GHRD design examples stored in the QSPI flash device and system Intel MAX 10 pre-programmed. You must perform board restore by using the following instructions through the Intel Quartus Prime Programmer GUI.

3.3.1. Restore Board System Intel MAX 10 with Default Factory Image

1. Set S19 or S20 switch to enable System Intel MAX 10 in JTAG chain, open the Intel Quartus Prime Programmer GUI, and detect the JTAG chain.
2. Attach System Intel MAX 10 image on System Intel MAX 10 part.
3. Select programming options and click program button.

   Note: Once you plug Intel FPGA Download Cable between **J11** and **PC**, the Intel on-board download cable circuit is disabled automatically.

3.3.2. Restore Board QSPI Flash with Default Factory Image

1. Ensure `MSEL[2:0]` are OFF (AvST x32 mode) before power up the board.
2. Open Intel Quartus Prime Programmer GUI, detect JTAG chain after System Intel MAX 10 is restored.
3. Attached AvST x32 image (`factory_recovery` folder) on QSPI flash which is under System Intel MAX 10 part.
4. Select programming options and click program button.

4. Board Test System

The Intel Agilex I-Series Transceiver and SoC Development Kit includes design examples and the board test system (BTS) GUI to test the functionality of this board. The BTS provides an easy-to-use interface to alter functional settings and observe results. You can use the BTS to test board components, modify functional parameters, observe performance, and measure power usage.

While using the BTS, you reconfigure the FPGA several times with test designs specific to the functionality that you are testing. The BTS is also useful as a reference for designing systems. The BTS communicates over the JTAG bus to a test design running in the Intel Agilex I-Series FPGA device.

The following figure shows the graphical user interface (GUI) of a board that is in factory configuration.

Figure 2. BTS GUI

4.1. Set Up BTS GUI Running Environment

To run BTS GUI, including Power Monitor and Clock Controller GUI, you need to download and install Java runtime including OpenJDK and OpenJFX on your systems and set up the running environment. This is a one-time procedure, so if you have already completed it before, you do not need to do it again unless the Java version upgrade is needed.

4.1.1. Download OpenJDK

To download the Temurin OpenJDK, follow these steps:

1. Download the Temurin OpenJDK using this link: https://adoptium.net/releases.html.
2. Select the Temurin 11 Long Term Support (LTS) version.

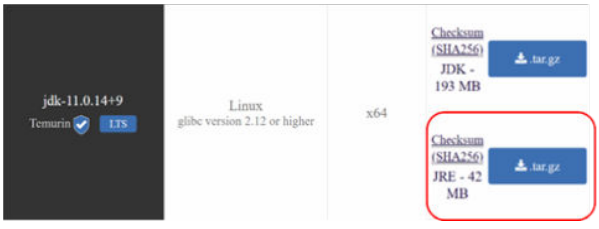
Figure 3. OpenJDK Version

3. On **Windows** system, choose the JRE zip format file.

Figure 4. Windows OpenJDK Version

4. On **Linux** system, choose the JRE tar.gz format file.

Figure 5. Linux OpenJDK Version



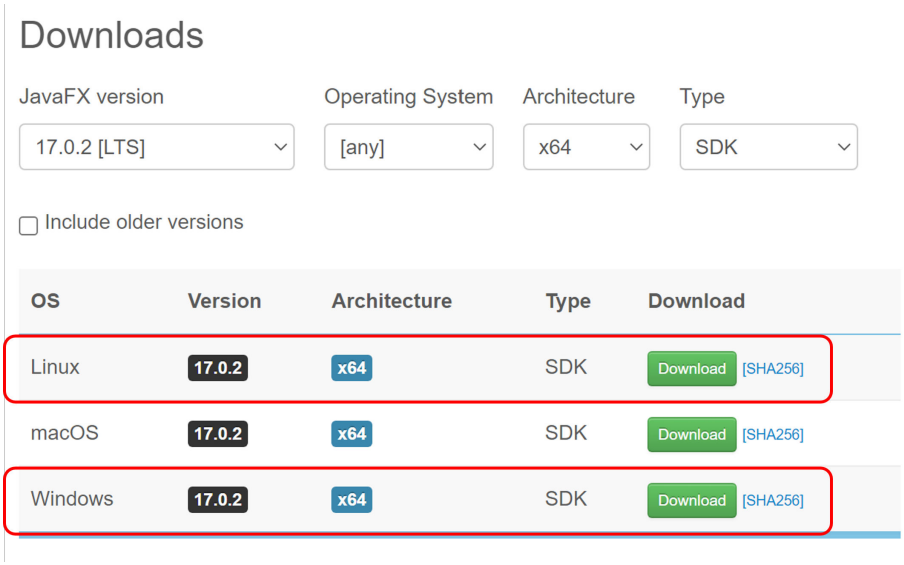
Note: The JDK version can be updated, download the latest version.

4.1.2. Download OpenJFX

To download the OpenJFX, follow these steps:

1. Download the OpenJFX using this link: https://gluonhq.com/products/javafx/.
2. Select JavaFX version 17.0.2 [LTS].
3. For the **Windows** system, download the JavaFX Windows x64 SDK.
4. For **Linux** system, download the JavaFX Linux x64 SDK.

Figure 6. JavaFX Version



4.1.3. Install OpenJDK and OpenJFX

You have two downloaded zip files, follow these steps to install them.

1. On **Windows** system, Intel recommends you to unzip the files and put them in the following directory:
   - C:\Program Files\Java\jre
   - C:\Program Files\Java\jfx

   Note: The unzipped folder name of JRE is `jdk-11.0.xx+x-jre` (for example, `jdk-11.0.14+9-jre`), you need to rename it to `jre`. The unzipped folder name of JFX is `javafx-sdk-17.0.2`, you need to rename it to `jfx`.
2. On **Linux** system, Intel recommends you to unzip the files and rename the folders using the following commands:

```
# unzip openjfx-17.0.2_linux-x64_bin-sdk.zip -d /opt/Java/
# tar zxvf OpenJDK11U-jre_x64_linux_hotspot_11.0.14_9.tar.gz -C /opt/Java/
# cd /opt/Java
# mv javafx-sdk-17.0.2 jfx
# mv jdk-11.0.14+9-jre jre
```

   You have the following two directories on your **Linux** system:
   - /opt/Java/jre

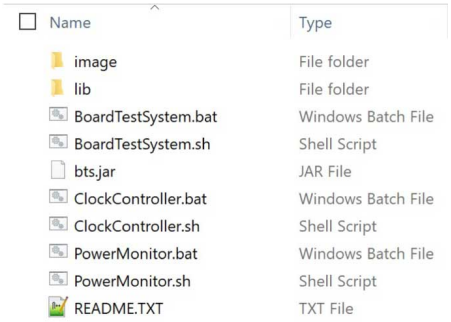
— /opt/Java/jfx

4.1.4. Run BTS GUI

Before powering up the development kit and running the BTS GUI, change the switch settings to the default settings. Refer to Factory Default Switch Settings.

The BTS release folder always includes the following files.

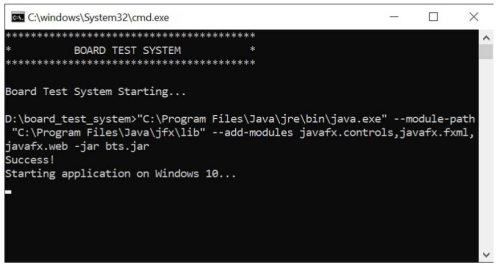
Figure 7. BTS Folder



You can run BTS GUI easily with the following scripts.

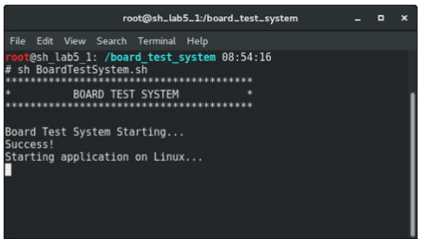
1. On **Windows** system, double click the .bat files to run BTS, Clock Controller, or Power Monitor GUI.

Figure 8. Windows Console



2. On **Linux** system, you need to run the shell script with root privilege.

Figure 9. Linux Console



Note: The .bat or shell script will check the Java environment settings, copy necessary files, and give some prompts if the environment is not set up correctly.

4.2. Test the Functionality of the Development Kit

This section describes each control in the BTS.

4.2.1. The Bottom Info Bar

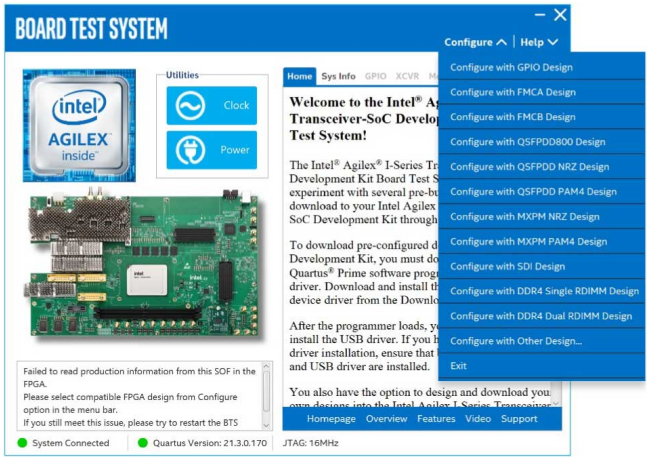
The bottom information bar shows the status of the system connection, the Intel Quartus Prime version and the JTAG clock.

- **System Connected/Disconnected**: Shows if the board is connected to the system. The green sign turns gray if the board becomes disconnected.
- **Intel Quartus Prime Version**: Displays the current Intel Quartus Prime version installed and active on your system. The text turns red if your version is older than the required version. Change the QUARTUS_ROOTDIR environment variable if you have installed the right version but the active version doesn't meet the requirement.
- **JTAG**: Displays the JTAG clock frequency.

4.2.2. The Configure Menu

Use the Configure Menu to select the design you want to use. Each design example tests different functionality that corresponds to one or more application tabs.

Figure 10. The Configure Menu



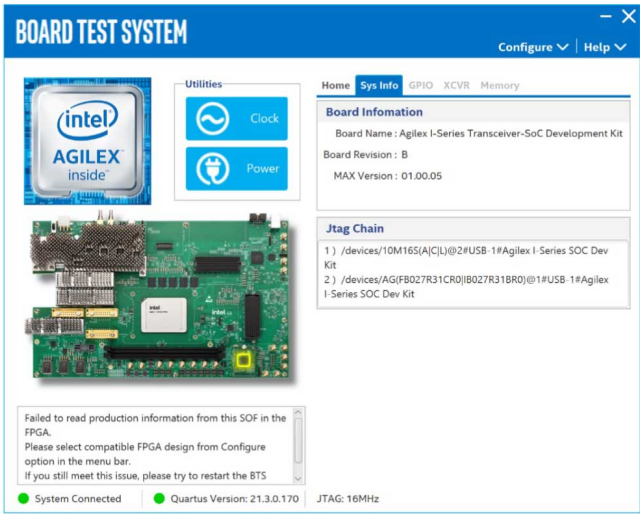
To configure the FPGA with a test system design, follow these steps:

1. On the **Configure** menu, click the **Configure** command that corresponds to the functionality you want to test.
2. In the dialog box that appears, click **Configure** to download the corresponding design's SRAM Object File (.sof) to the FPGA. The download process usually takes less than a minute.
3. When configuration finishes, the design begins running in the FPGA. The corresponding GUI application tabs that interface with the design are now enabled. If you use the Intel Quartus Prime Programmer for configuration, instead of the BTS GUI, you might need to restart the GUI.

4.2.3. The Sys Info Tab

The **Sys Info** tab shows information about the board's current configuration. The tab displays the board information, JTAG Chain devices and other details stored on the board.

Figure 11. The Sys Info Tab



The following sections describe the controls on the System Info tab.

Board Information

The board information control displays static information about your board.

- **Board Name**: Indicates the official name of the board given by the BTS.
- **Board Revision**: Indicates the revision of the board.
- **MAX Version**: Indicates the version of the system Intel MAX 10.

JTAG Chain

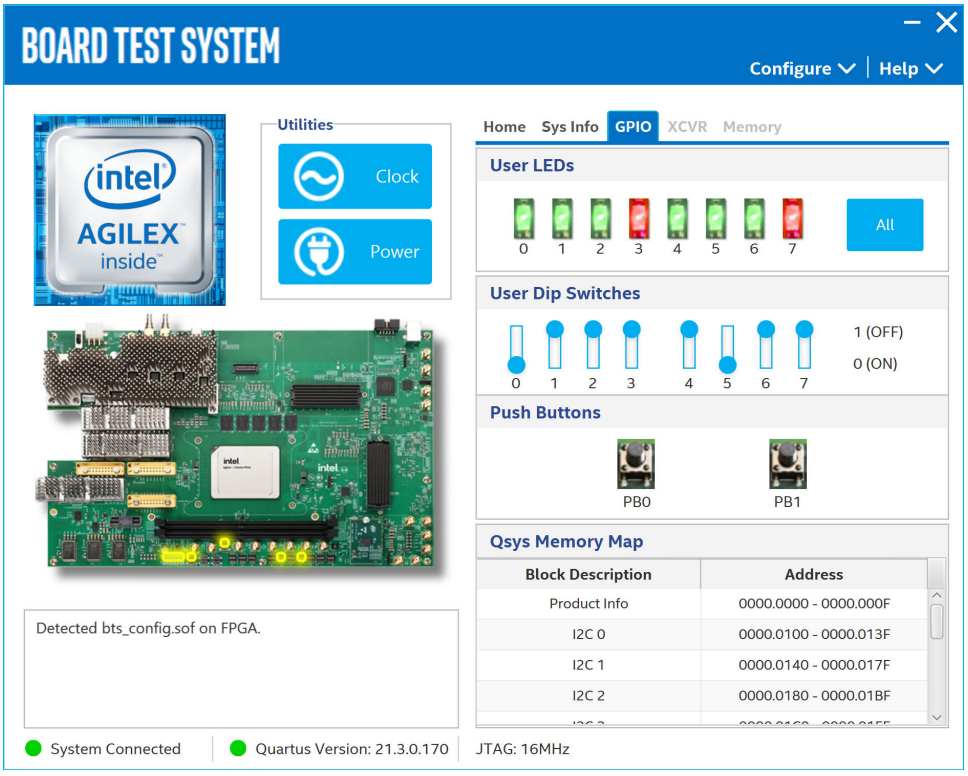
The JTAG chain control shows all the devices currently in the JTAG chain.

Note: System Intel MAX 10 and FPGA should all be in the JTAG chain when running the BTS GUI.

4.2.4. The GPIO Tab

The **GPIO** tab allows you to interact with all the general-purpose user I/O components on your board. You can turn LEDs on or off and see the status of push buttons and dip switches.

Figure 12. The GPIO Tab



The following sections describe the controls on the GPIO tab.

User LEDs

The User LEDs control displays the current state of the user LEDs. Toggle the LED buttons to turn the board LEDs on and off. Click the All button to reverse the state of all the LEDs.

User Dip Switches

The User Dip Switches control display the status of the USER_SW[0:3](S1) and USER_SW[4:7](S6).

Push Buttons

The Push Button control shows the status of PB0 and PB1.

Qsys Memory Map

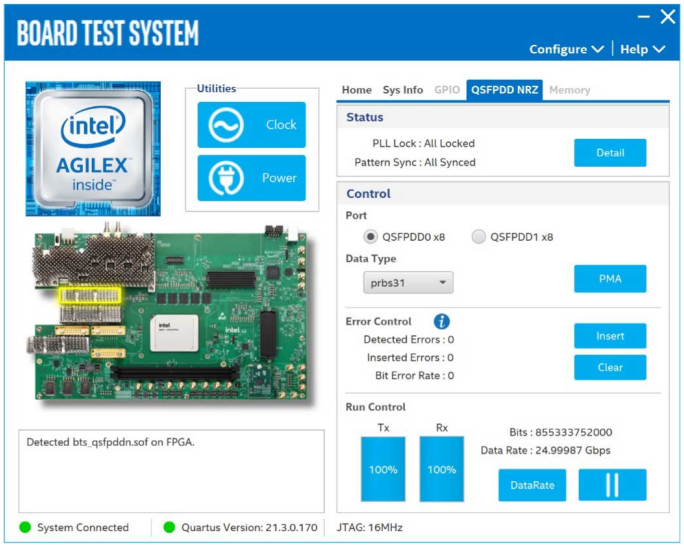
The Qsys Memory Map control shows the memory map of **bts_config.sof** design running on your board.

4.2.5. The XCVR Tab

The **XCVR** tab allows you to run transceiver tests on your board. You can run the test using either electrical loopback modules or optical fiber modules.

4.2.5.1. The QSFPDD NRZ Tab

Figure 13. The QSFPDD NRZ Tab



The following sections describe controls in the QSFPDD NRZ tab.

Status

The Status control displays the following status information during the loopback test:

- **PLL lock:** Shows the PLL locked or unlocked state.
- **Pattern Sync:** Shows the pattern synced or not state. The pattern is considered synced when the start of the data sequence is detected.
- **Detail:** Shows the PLL lock and pattern sync status of each channel. The number of the error bits of each channel can be found here.

Control

Use the following controls to select an interface to apply PMA settings, data type and error control:

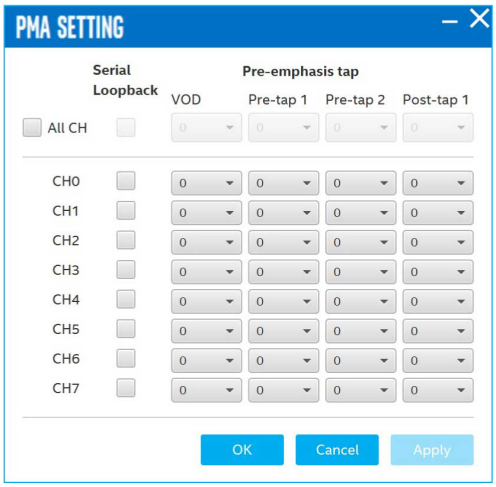
- **QSFPDD0 x8**
- **QSFPDD1 x8**

PMA Setting

Allows you to make changes to the PMA parameters that affect the active transceiver interface. The following settings are available for analysis:

- **Serial Loopback:** Displays the signal status between the transmitter and the receiver.
- **VOD:** Specifies the voltage output differential of the transmitter buffer.
- **Pre-emphasis tap:**
  - Pre-tap 1: Specifies the amount of pre-emphasis on the first pre-tap of the transmitter buffer.
  - Pre-tap 2: Specifies the amount of pre-emphasis on the second pre-tap of the transmitter buffer.
  - Post-tap 1: Specifies the amount of pre-emphasis on the post-tap of the transmitter buffer.

Figure 14. QSFPDD NRZ-PMA Setting



Data Type

The Data Type control specifies the type of data pattern contained in the transactions. Select the following available data types for analysis:

- **PRBS7:** pseudo-random 7-bit binary sequences
- **PRBS15:** pseudo-random 15-bit binary sequences
- **PRBS23:** pseudo-random 23-bit binary sequences
- **PRBS31:** pseudo-random 31-bit binary sequences (default)

Error Control

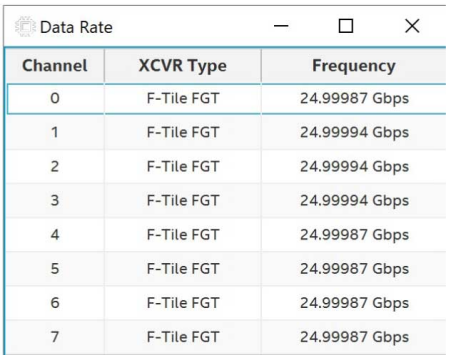
This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors:** Displays the number of data errors detected in the received bit stream.
- **Inserted Errors:** Displays the number of errors inserted into the transmit data stream.
- **Bit Error Rate:** Calculates the bit error rate of the transmit data stream.
- **Insert:** Insert a one-word error into the transmit data stream each time you click the button. Insert Error is only enabled during transaction performance analysis.
- **Clear:** Resets the Detected Errors counter and Inserted Errors counter to zeros.

Run Control

- **TX and RX performance bars:** Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Start:** This control initiates the loopback tests.
- **Data Rate:** Displays the XCVR type and data rate of each channel.

Figure 15. QSFPDD NRZ - Data Rate

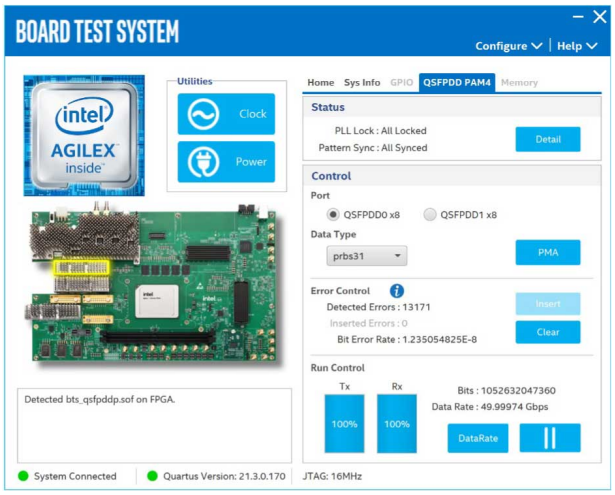


Channel	XCVR Type	Frequency
0	F-Tile FGT	24.99987 Gbps
1	F-Tile FGT	24.99994 Gbps
2	F-Tile FGT	24.99994 Gbps
3	F-Tile FGT	24.99994 Gbps
4	F-Tile FGT	24.99987 Gbps
5	F-Tile FGT	24.99987 Gbps
6	F-Tile FGT	24.99987 Gbps
7	F-Tile FGT	24.99987 Gbps

4.2.5.2. The QSFPDD PAM4 Tab

Similar control functions with the QSFPDD NRZ tab.

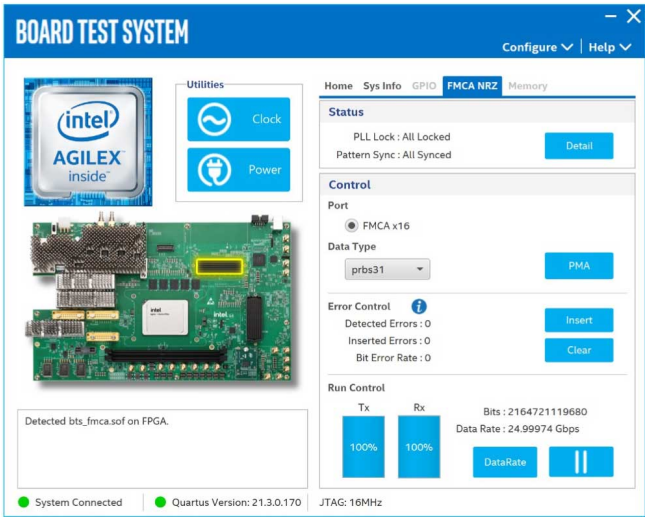
Figure 16. The QSFPDD PAM4 Tab



4.2.5.3. The FMCA NRZ Tab

Similar control functions with the QSFPDD NRZ tab except for the port selection.

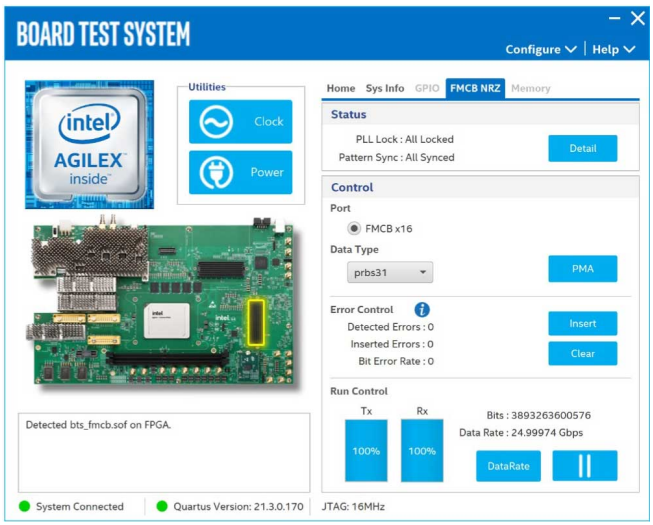
Figure 17. The FMCA NRZ Tab



4.2.5.4. The FMCB NRZ Tab

Similar control functions with the QSFPDD NRZ tab except for the port selection.

Figure 18. The FMCB NRZ Tab



4.2.5.5. The QSFPDD800 PAM4 Tab

Similar control functions with the QSFPDD NRZ tab.

Figure 19. The QSFPDD800 PAM4 Tab

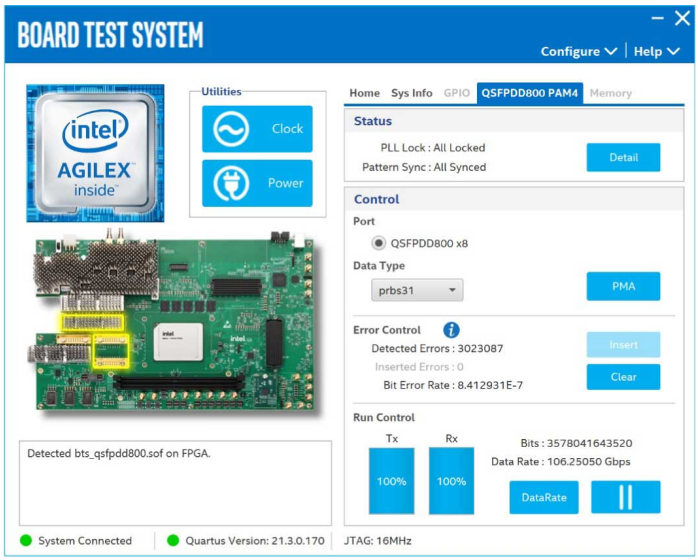
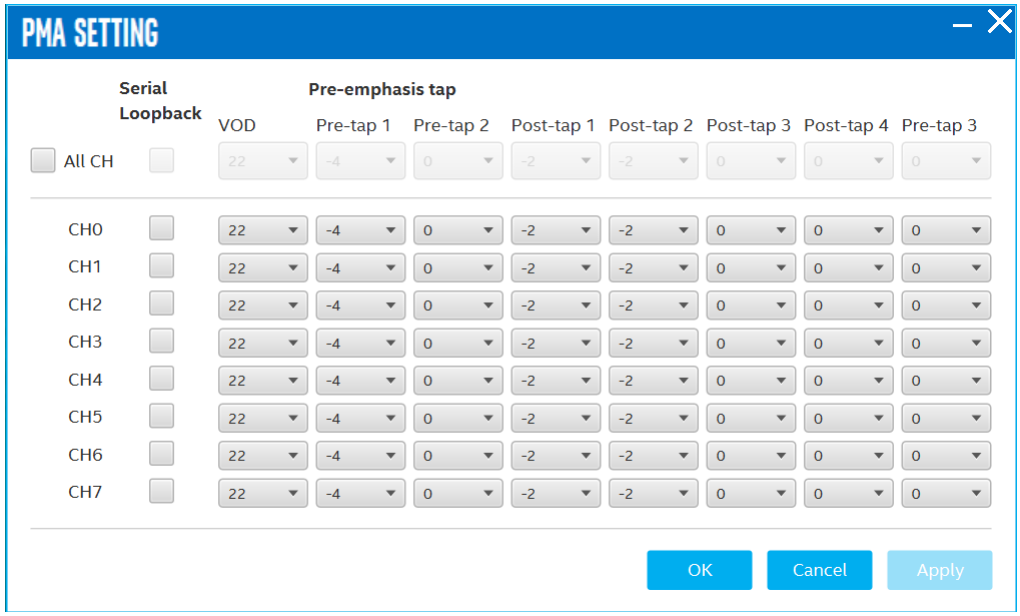


Figure 20. The QSFPDD800 PAM4 Tab - PMA Setting



PMA Setting

In addition to the PMA settings listed in Figure: *QSFPDD NRZ-PMA Setting*, additional settings are available for the F-tile FHT PMA. The PMA is set to the default values in the PAM4 designs.

- **Pre-emphasis tap:**
  - Post-tap 3: Specifies the amount of pre-emphasis on the third post-tap of the transmitter buffer.
  - Post-tap 4: Specifies the amount of pre-emphasis on the fourth post-tap of the transmitter buffer.
  - Pre-tap 3: Specifies the amount of pre-emphasis on the third pre-tap of the transmitter buffer.

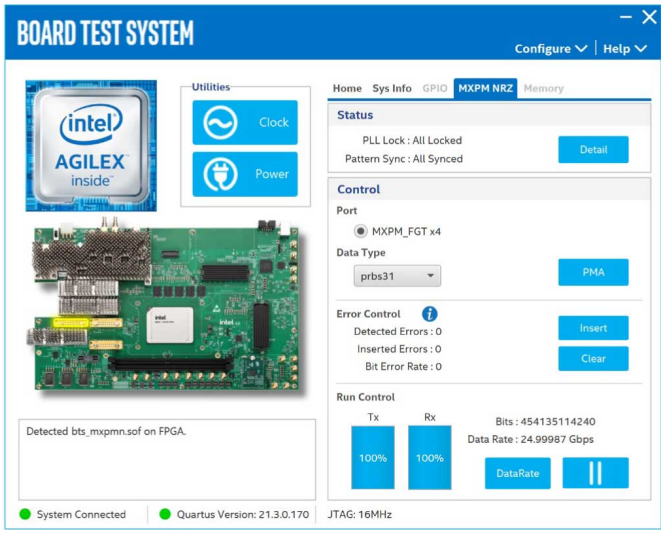
Related Information

The QSFPDD NRZ Tab on page 19

4.2.5.6. The MXPM NRZ Tab

Similar control functions with the QSFPDD NRZ tab except for the port selection.

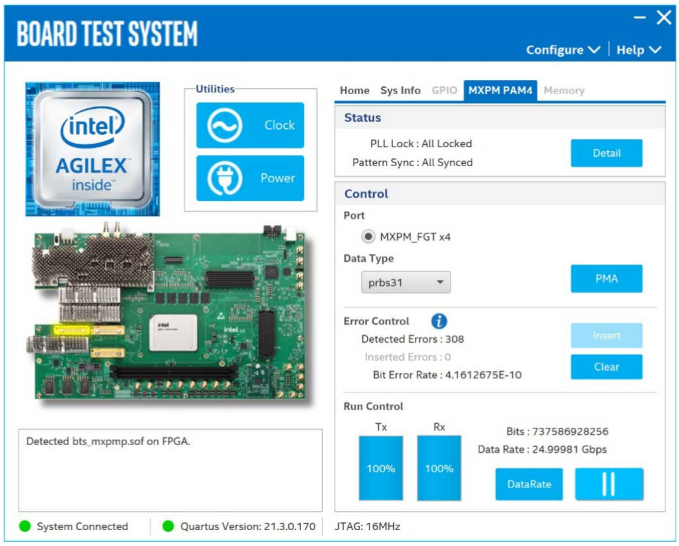
Figure 21. The MXPM NRZ Tab



4.2.5.7. The MXPM PAM4 Tab

Similar control functions with the QSFPDD NRZ tab.

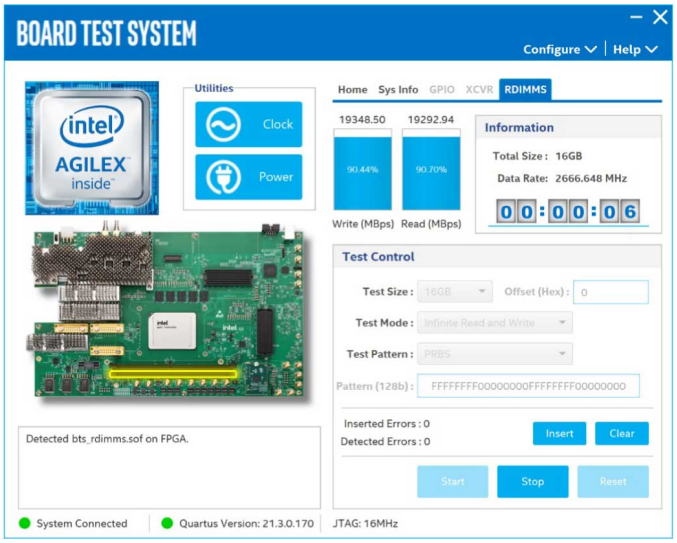
Figure 22. The MXPM PAM4 Tab



4.2.6. The Memory Tab

This tab allows you to read and write DDR4 DIMM-2A (DIMM-I) and DDR4 DIMM-2B (DIMM-II) memory on your board. RDIMMS only tests DIMM-II while RDIMMD tests DIMM-I and DIMM-II. Download the design through BTS Configure.

Figure 23. The RDIMMS Tab



The following sections describe controls on this tab.

Start

Initiates DDR4 memory transaction performance analysis.

Stop

Terminates transaction performance analysis.

Performance Indicators

These controls display current transaction performance analysis information collected since you last clicked **Start**:

- **Write and Read performance bars**: Show the percentage of maximum theoretical data rate that the requested transactions are able to achieve.
- **Write (MBps) and Read (MBps)**: Show the number of bytes analyzed per second.
- **Data Bus**: 72 bits (8 bits ECC) wide, reference clock is 166.666 MHz, and the frequency is 1333.33 MHz double data rate 2666.66 MT/s.

Test Control

- **Test Size**: You can choose the size of the memory to test. The available options are 64 KB, 256 KB, 1 MB, 16 MB, 64 MB, 256 MB, 1 GB, 4 GB, 8 GB, and 16GB (default).
- **Offset (Hex)**: You can define the memory start address to test.
- **Test Mode**: Infinite Read and Write (default), Single Read and Write.
- **Test Pattern**: PRBS (default), User Defined Constant, Walking '0', Walking '1'.

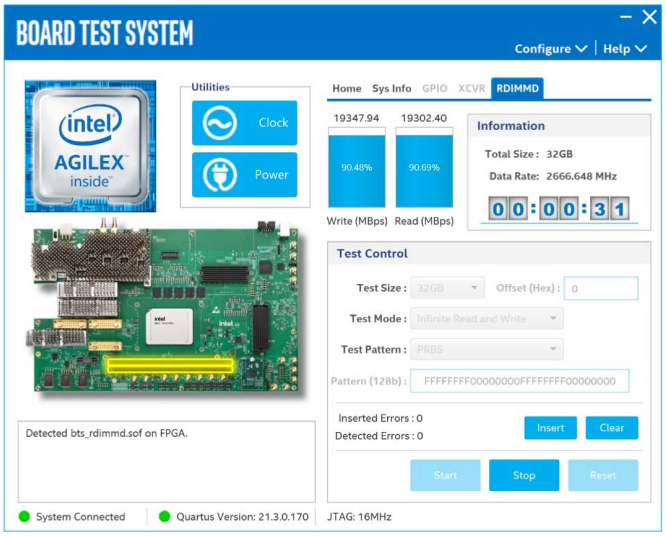
Error Control

This control displays data errors detected during analysis and allows you to insert errors:

- **Detected Errors**: Displays the number of data errors detected in the hardware.
- **Inserted Errors**: Displays the number of errors inserted into the transaction stream.
- **Bit Error Rate**: Calculates the bit error rate of the transmit data stream.
- **Insert**: Insert a one-word error into the transaction stream each time you click the button. Insert error is only enabled during transaction performance analysis.
- **Clear**: Resets the Detected Errors counter and Inserted Errors counter to zeros.

Figure 24. The RDIMMD Tab

Similar with RDIMMS. **Test Size** can be set to 32 GB with two RDIMMs.



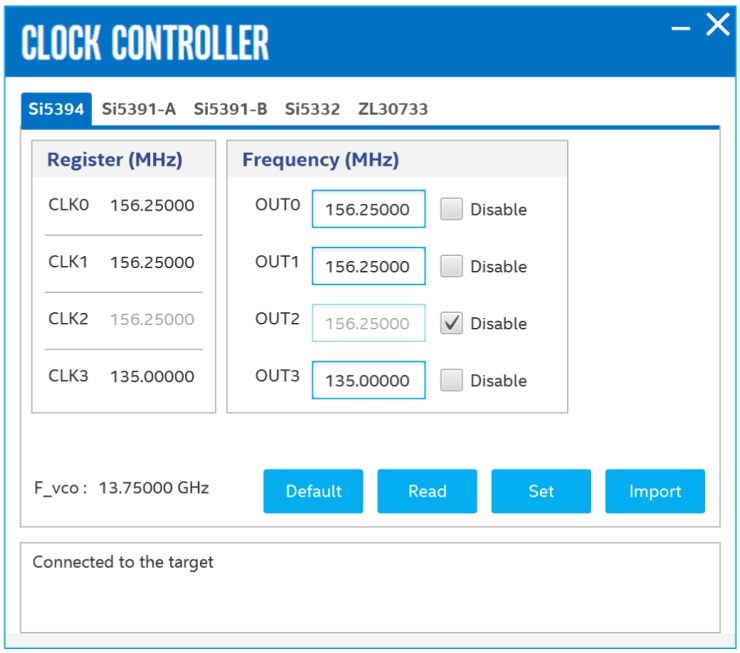
4.3. Control On-Board Clock through Clock Controller GUI

The Clock Controller GUI can change the on-board Si5394/Si5391-A/Si5391-B/Si5332/ZL30733 programmable PLLs to a large range of customized frequency. The instructions to run Clock Controller GUI are stated in the *Run BTS GUI* section. You can also start it using the BTS GUI icon "Clock".

The clock controller communicates with the system Intel MAX 10 device through a 10-pin JTAG header **J11** or USB port **J10**. Then, system Intel MAX 10 controls these programmable clock parts through a 2-wire I^2C bus.

Note: You cannot run the stand-alone Clock Controller GUI application when the BTS or Power Monitor GUI is running at the same time. ZL30733 can be controlled only when a design in which the I^2C interface is instantiated, such as the `bts_config.sof` under the `board_test_system\image\ES folder` has been downloaded to the FPGA.

Figure 25. Si5394



The following sections describe the Clock Controller buttons.

Read

Reads the current frequency setting for the oscillator associated with the active tab.

Default

Sets the frequency for the oscillator associated with the active tab back to its default value. This can also be accomplished by power cycling the board.

Set

Sets the programmable oscillator frequency for the selected clock to the value in the 0UTx output controls for Si5394. Frequency changes might take several milliseconds to take effect. You might see glitches on the clock during this time. Intel recommends resetting the FPGA logic after changing frequencies.

Import

Si5394 has a two-time rewritable non-volatile memory (NVM). You can generate the register list from the Clockbuilder Pro tool and import it into Si5394 to update the settings of the NVM. Register changes are volatile after power cycling.

Figure 26. Si5391-A

Similar control functions with Si5394.

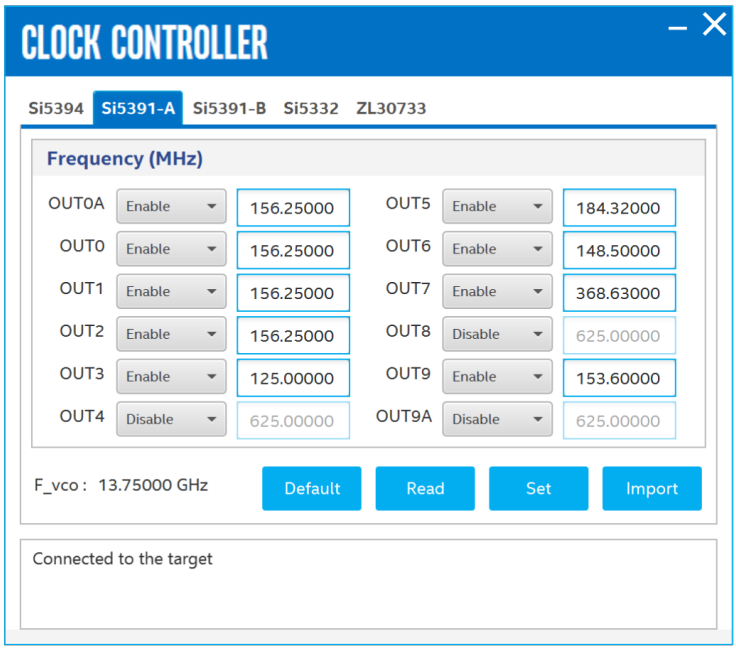


Figure 27. Si5391-B

Same with Si5391-A.

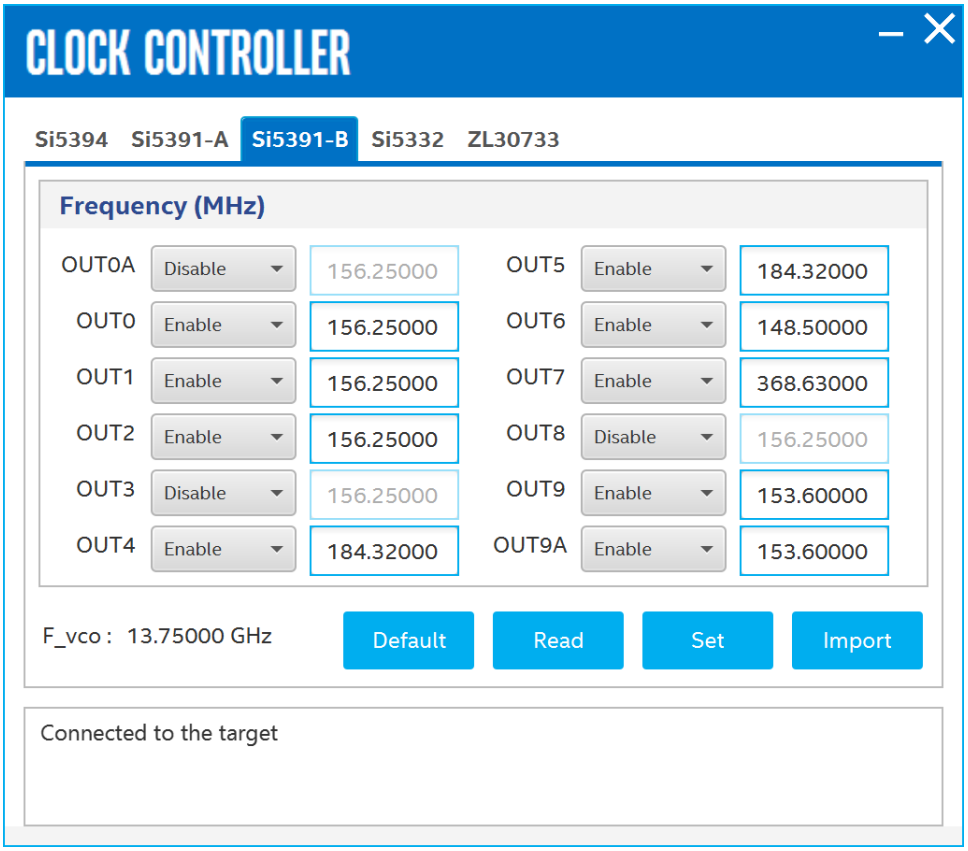


Figure 28. Si5332

Similar control functions with Si5394. There is no default button for this clock but you can use Import or power cycle the board to get default clock frequencies.

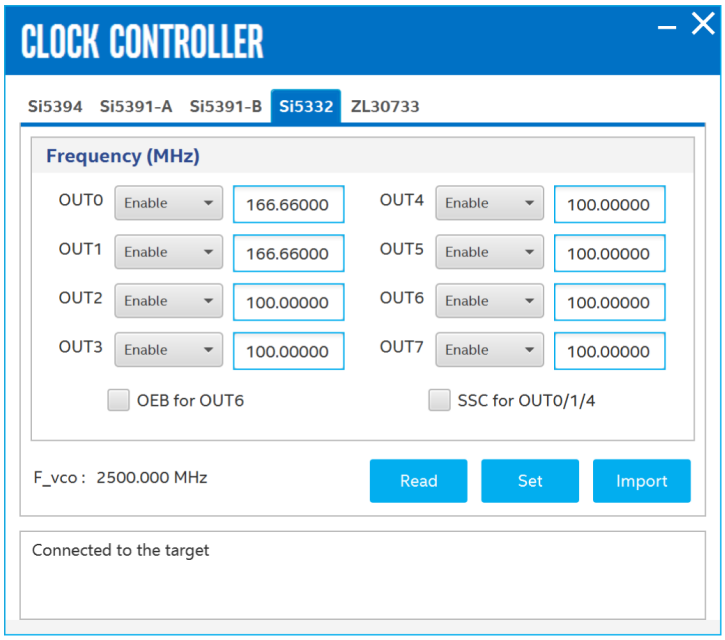
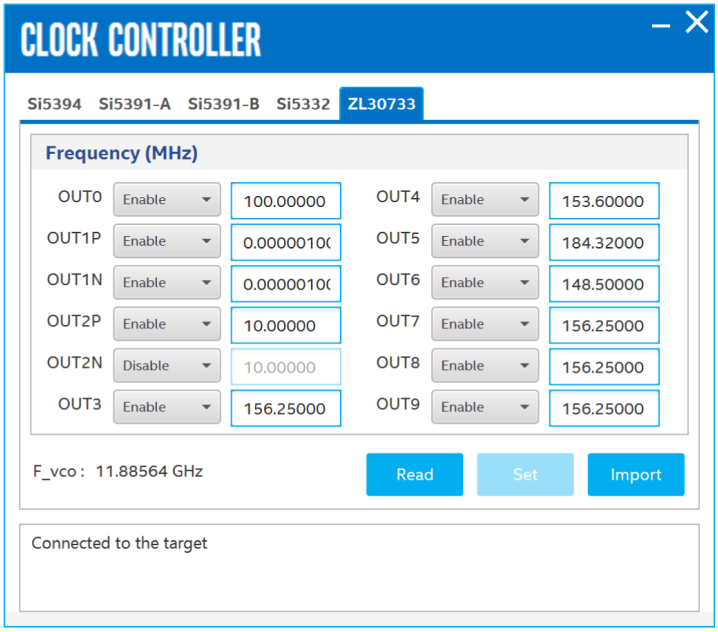


Figure 29. ZL30733

Similar control functions with Si5394. You can use Import to set the clock outputs. There is no default button for this clock, but you can use Import or power cycle the board to get default clock frequencies.



Related Information

Clockbuilder Pro Software on the Skyworks website

4.4. Monitor On-Board Power Regulator through Power Monitor GUI

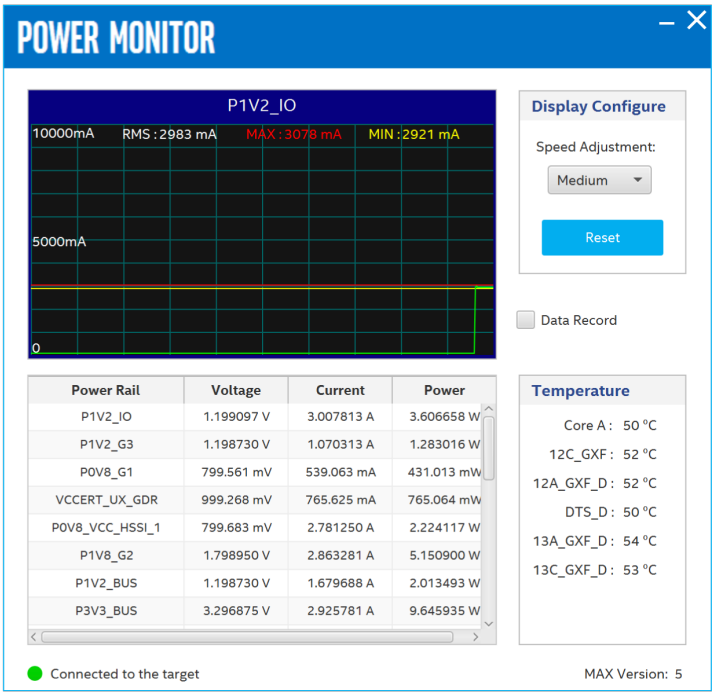
The Power Monitor GUI reports most power rails' voltage, current, and power information on the board. It also collects temperature from FPGA die, power modules, and diodes assembled on PCB.

The Power Monitor GUI communicates with System Intel MAX 10 through a 10-pin JTAG header **J11** or USB port **J10**. System Intel MAX 10 monitors and controls power regulator, temperature/voltage/current sensing chips through a 2-wire I^2C bus.

The instructions to run Power Monitor GUI are stated in the *Run BTS GUI* section. It can also be started with the BTS GUI icon "Power".

Note: You cannot run the stand-alone Power Monitor GUI when the BTS or the Clock Controller GUI is running at the same time.

Figure 30. Power Monitor GUI



The following sections describe the details of the Power Monitor GUI.

Display Configure

- Speed Adjustment: Adjusts the update rate of the current curve.
- Reset: Regenerates the graph.

Data Record

When the box is checked, the telemetry data of the selected power rail can be recorded. The data will be saved into a .csv file in the `log` directory.

Temperature

Reads the temperature data from FPGA die internal temperature sense diodes.

4.5. BTS Test Areas

BTS checks for hardware fault before you can use the board. If one or more BTS test items fail, it implies either a wrong hardware setting or hardware fault on specific interface.

4.6. Identify Test Pass or Fail-based on BTS GUI Test Status

QSFPDD0/QSFPDD1

Plug QSFPDD0/QSFPDD1 loopback module in **J27**/**J48** before you configure QSFPDD NRZ/PAM4 example build through BTS GUI.

QSFPDD800

Plug QSFPDD800 loopback module in **J22** and use the MXPM cable between MXPM_FHT connector **J2** and **J8** before you configure QSFPDD800 PAM4 example build through BTS GUI.

FMCA/FMCB

Plug FMCA/FMCB loopback module in **J7**/**J9** before you configure FMCA/FMCB NRZ example build through BTS GUI.

MXPM_FGT

Plug MXPM_FGT loopback module in **J28** before you configure MXPM NRZ/PAM4 example build through BTS GUI.

DDR4 DIMM

Plug the DIMM-I/II module which is shipped alone with this development kit in **J5**. The BTS GUI only supports fabric memory interfaces namely DDR4 DIMM-2A (DIMM-I) and DDR4 DIMM-2B (DIMM-II).

5. Development Kit Hardware and Configuration

The Intel Agilex I-Series Transceiver-SoC Development Kit can support multiple application scenarios and configuration modes. You need to change hardware setting and/or re-program system images for these cases.

Table 5. Supported Configuration Modes

S9 [1:4]	MSEL [2:0]	Configuration Mode
ON/OFF/OFF/X	001	AS – Fast mode (Default setting)
ON/ON/OFF/X	011	AS – Normal mode
ON/ON/ON/X	111	JTAG
OFF/ON/ON/X	110	Avalon®-ST x8
ON/OFF/ON/X	101	Avalon-ST x16
OFF/OFF/OFF/X	000	Avalon-ST x32

5.1. Configure FPGA and Access HPS Debug Access Port by JTAG

1. JTAG access does not rely on switch **S9** settings and system image.
2. Plug the USB cable to **J10** or Intel FPGA Download Cable to **J11**.
3. Open the Intel Quartus Prime Programmer, system console to configuration Intel Agilex FPGA SDM, system Intel MAX 10 and FMC JTAG nodes.
4. Open Arm Development Studio 5* (DS-5*) Intel SoC FPGA Edition to connect to and communicate with the HPS Debug Access Port (DAP) through the same JTAG interface.

5.2. Configure the FPGA Device Using the AS Mode (Default Mode)

1. Default **S9** setting and system Intel MAX 10 image support the active serial (AS) configuration mode.
2. Plug pre-programmed SDM QSPI flash daughter into **J3**.
3. Power on and observe FPGA user LED behavior.

5.3. Configure the FPGA Device Using the Avalon-ST Mode

1. Set **S9** to Avalon-ST x32 mode first.
2. Default system Intel MAX 10 image support the Avalon-ST x32 mode only. You should build a corresponding .POF image if you select Avalon-ST x8 or Avalon-ST x16 configuration mode.
3. Power on the board, use push button **S16** to choose page, and **S17** to configure the FPGA.
4. Default page depends on the setting of **S10.1**.

Table 6. Avalon-ST x32 LED Behavior

LED	Page0	Page1	Page2	Page3
LED_D9	ON	OFF	OFF	OFF
LED_D11	OFF	ON	OFF	ON
LED_D13	OFF	OFF	ON	ON
USER_LED0_D1	Blinking	Blinking	Blinking	Blinking
USER_LED1_D3	ON	ON	ON	ON
USER_LED2_D5	Blinking reversed	Blinking	Blinking	Blinking
USER_LED3_D7	ON	ON	ON	ON
USER_LED4_D2	ON	ON	Blinking reversed	Blinking
USER_LED5_D4	ON	Blinking reversed	Blinking	Blinking
USER_LED6_D6	ON	ON	ON	Blinking reversed
USER_LED7_D8	ON	ON	ON	ON

5.4. Daughter Cards

The Intel Agilex I-Series Transceiver-SoC Development Kit supports HPS OOBE daughter card. You can demonstrate HPS functions through these daughter cards and cables.

5.4.1. HPS Out of Box Experience (OOBE) Daughter Card

1. Plug HPS OOBE daughter card in **J4**.
2. To test HPS Ethernet capability, connect OOBE's **RJ45** port **J3** to internet.
3. To test HPS USB 2.0 capability, connect OOBE's **J4** port to USB cable.
4. To debug HPS from UART terminal applications, use USB cable to connect to OOBE's **J7**.
5. OOBE's MicroSD card is pre-programmed with GSRD and OS.
6. General I/O access is provided by push buttons and LED indicators.

6. Custom Projects for the Development Kit

6.1. Add SmartVID Settings in the Intel Quartus Prime QSF File

By default, the Intel Agilex silicon assembled on this development kit enables the SmartVID feature. To avoid the Intel Quartus Prime software from generating an error due to incomplete SmartVID settings, you must put constraints outlined below into the Intel Quartus Prime project QSF file.

Open your Intel Quartus Prime project QSF file, copy and paste the following constraint scripts into the file. Ensure there are no other similar settings with different values.

```
set_global_assignment -name USE_PWRMGT_SCL SDM_IO0
set_global_assignment -name USE_PWRMGT_SDA SDM_IO12
set_global_assignment -name USE_CONF_DONE SDM_IO16
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE ED8401
set_global_assignment -name NUMBER_OF_SLAVE_DEVICE 1
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS 62
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-13"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
```

6.2. Golden Top

You can use the Golden Top project as the starting point for your designs. It comes loaded with constraints, pin locations, defined I/O standard, direction, and general termination.

7. Revision History

Table 7. Revision History for the Intel Agilex I-Series Transceiver-SoC Development Kit User Guide

Document Version	Changes
2022.09.30	• Added UKCA in the *Safety and Regulatory Information* and *Compliance Information* sections. • Added the *Lithium Ion Battery Warnings* section. • Updated Table: *Ordering Information*. • Updated the *Perform Board Restore* section. • Updated step 3 in the *Restore Board QSPI Flash with Default Factory Image* section. • Updated the *Control On-Board Clock through Clock Controller GUI* section. • Updated step 1 and step 3 in the *Configure FPGA and Access HPS Debug Access Port by JTAG* section. • Updated the *System Management* section. • Updated the *Power Cord Requirements* section. • Updated the *Safety Cautions* section.
2022.04.07	Initial release.

A. Development Kit Components

A.1. System Management

Two Intel MAX 10 FPGAs (10M16SCU324C8G) are used for system management. System Intel MAX 10 acts as a system controller. It handles the FPGA Avalon-ST configuration, I^2C bus access, fan speed control, and system reset functions. The UB2/PWR Intel MAX 10 acts as the Power Manager and on-board JTAG controller. Refer to the following description for each function:

- **Power management:** Control systems and FPGA power-up and optional power-down sequence (PDS), supervise power regulators/switches status and manage power faults, supervise temperature analog-to-digital converter (ADC) interrupt signals and manage temperature faults.
- **JTAG controller:** Manage the JTAG chain topology, JTAG master source and JTAG slaves using **S19**/**S20**.

Table 8. JTAG Master Sources

Schematic Signal Name	Description
EXT_JTAG_TCK/TDO/TMS/TDI	JTAG header **J11** for Intel FPGA Download Cable
FX2_Dp/n	Input port **J10** for on-board Intel download circuit
HPS_GPIO[32:35]	Mictor 38-pin header on the OOBE daughter card

Table 9. JTAG Chain Topology Settings

Mode	S20 [4:2]	S19 [4] [3] [2] [1] ON: Bypass from chain OFF: Enable in chain	Function
000	ON/ON/ON (Default)	S19.1 (SDM+HPS) S19.2 (System Intel MAX 10) S19.3 (FMC_B) S19.4 (FMC_A)	Mode 1: On-board Intel download circuit act as the only JTAG Master. Chained HPS with SDM nodes **internally**. Mode 3: External Intel FPGA Download Cable act as the only JTAG Master. Chained HPS with SDM nodes **internally**.
001	ON/ON/OFF	SDM is always enabled in the JTAG chain. S19.1 (HPS) S19.2 (System Intel MAX 10) S19.3 (FMC_B) S19.4 (FMC_A)	Mode 2: On-board Intel download circuit act as the only JTAG Master. Chained HPS with SDM nodes **externally**.

continued...

Mode	S20 [4:2]	S19 [4] [3] [2] [1] ON: Bypass from chain OFF: Enable in chain	Function
			Mode 4: External Intel FPGA Download Cable act as the only JTAG Master. Chained HPS with SDM node **externally**.
100	OFF/ON/ON	S19.1 (SDM) S19.2 (System Intel MAX 10) S19.3 (FMC_B) S19.4 (FMC_A)	Mode 7: Both on-board Intel download circuit and OOBE act as JTAG Masters. Separated HPS and SDM JTAG **chains, OOBE only drive HPS**. Mode 8: Both external Intel FPGA Download Cable and OOBE JTAG act as JTAG Masters. Separated HPS and SDM JTAG **chains, OOBE only drive HPS**.
Others	N/A	N/A	Reserved

A.2. Power

Figure 31. Power Tree

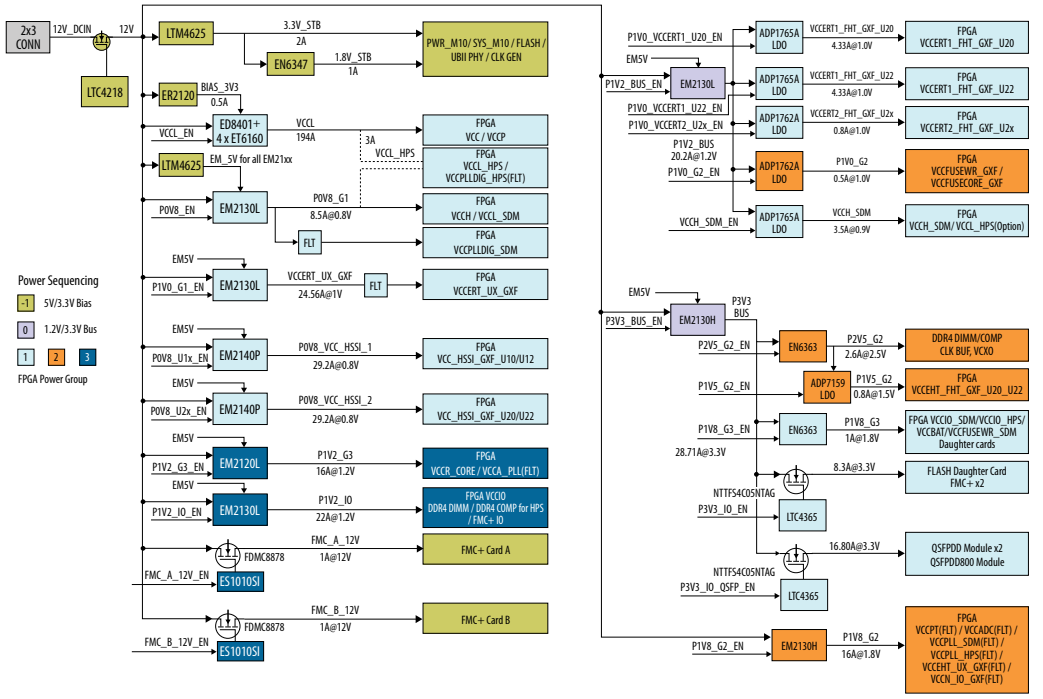
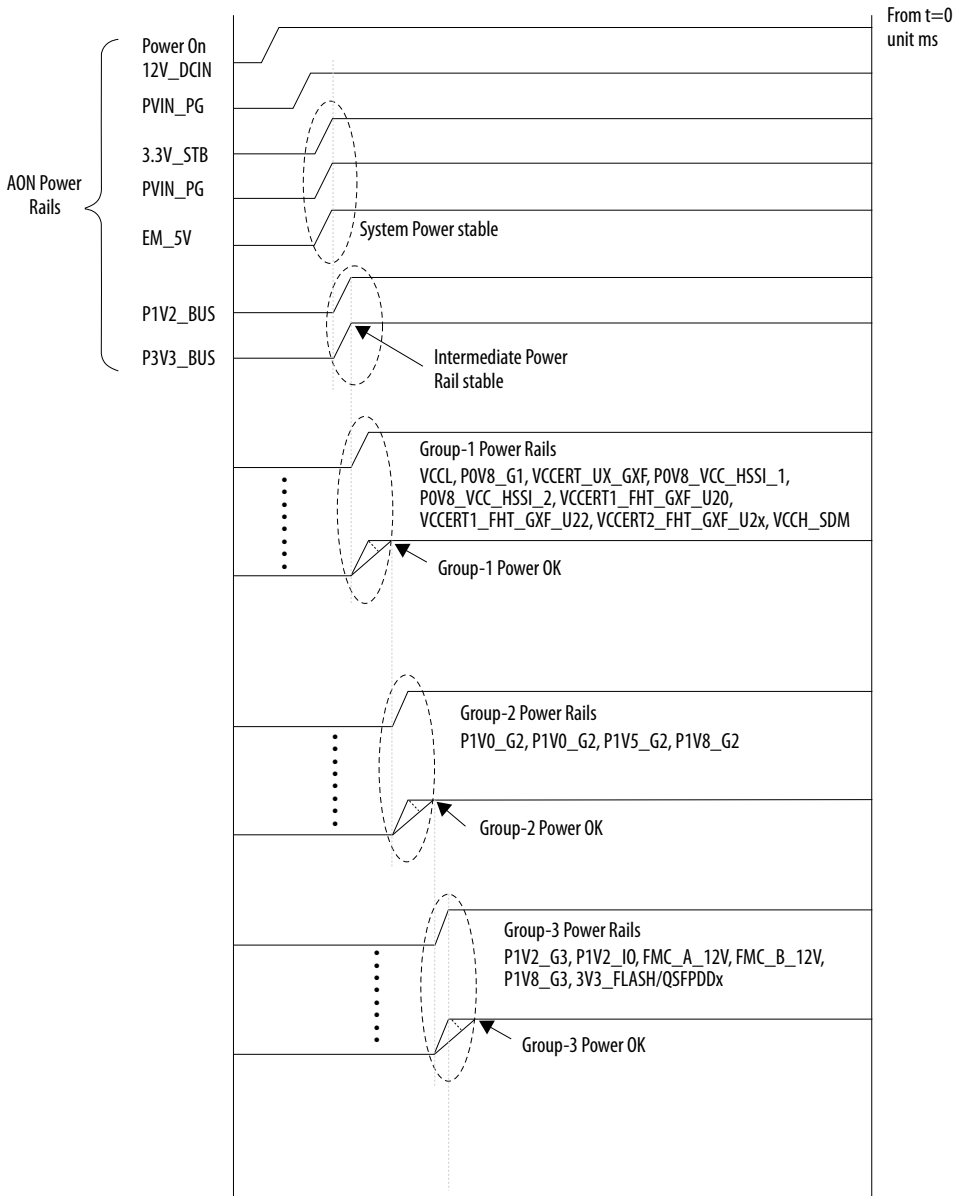


Figure 32. Power Sequence



Onboard hot-plug circuit shuts down all power rails when the total power is over 360 W (30 A).

UB2/PWR Intel MAX 10 shuts down significant power rails when one or more good power indicators is low due to a power fault.

UB2/PWR Intel MAX 10 also shuts down significant power rails when temperature cross the acceptable range.

A.3. Clocks

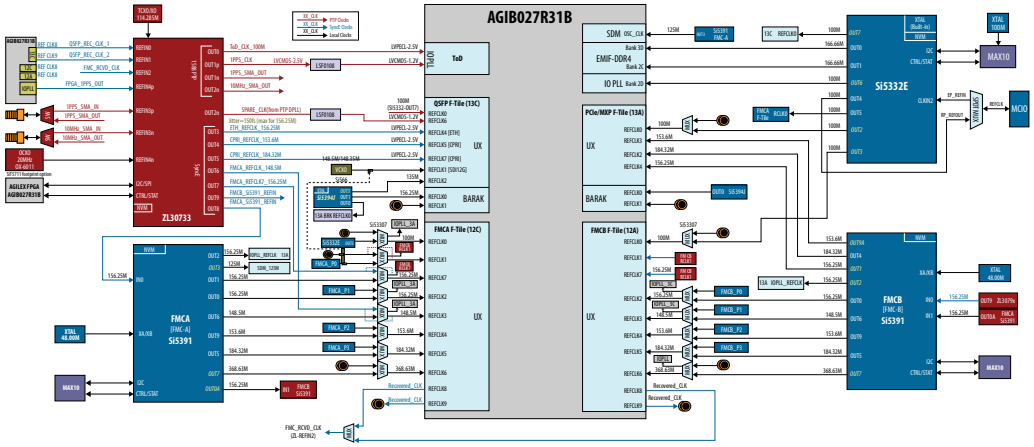
Table 10. Default Clock Frequency

Schematic Signal Name	Default Frequency
DDR4_HPS_REFCLKp/n	166.6M
DDR4_DIMM_2_REFCLKp/n	166.6M
Si5332_OUT2_P/N	100M
Si5332_OUT3_P/N	100M
PCIE_100M_REF_RP_AP/N	100M
Si5332_OUT5_P/N	100M
CLK_GPIO_P_4/N_4	100M
Si5332_OUT7_P/N	100M
Si5391_A_OUT_P0A/N0A	156.25M
Si5391_A_OUT_P0/N0	156.25M
Si5391_A_OUT_P1/N1	156.25M
Si5391_A_OUT_P5/N5	184.32M
Si5391_A_OUT_P6/N6	148.5M
Si5391_A_OUT_P7/N7	368.63M
Si5391_A_OUT_P9/N9	153.6M
Si5391_B_OUT_P0/N0	156.25M
CLK_13A_FGT_REFCLK4_P/N	156.25M
CLK_13A_FGT_REFCLK2_P/N	184.32M
Si5391_B_OUT_P5/N	184.32M
Si5391_B_OUT_P6/N6	148.5M
Si5391_B_OUT_P7/N7	368.63M
Si5391_B_OUT_P9/N9	153.6M
CLK_13A_FGT_REFCLK3_P/N	153.6M
CLK_FHT_13A_P_0/N_0	156.25M
CLK_FHT_13C_P_0/N_0	156.25M
CLK_FGT_13C_REFCLK_2P/N	135M
CLK_A_12C_FGT_P_0/N_0	100M
CLK_3A_GPIO_P_0/N_0	100M
CLK_A_12C_FGT_P_3/N_3	148.5M
CLK_3A_GPIO_P_2/N_2	148.5M
CLK_A_12C_FGT_P_2/N_2	156.25M
CLK_3A_GPIO_P_1/N_1	156.25M

continued...

Schematic Signal Name	Default Frequency
CLK_A_12C_FGT_P_4/N_4	156.25M
CLK_A_12C_FGT_P_6/N_6	368.63M
CLK_A_12C_FGT_P_5/N_5	184.32M
CLK_B_12A_FGT_P_0/N_0	100M
CLK_13A_FGT_REFCLK0_P/N	100M
CLK_B_12A_FGT_P_2/N_2	156.25M
CLK_3C_GPIO_P_1/N_1	156.25M
CLK_B_12A_FGT_P_3/N_3	148.5M
CLK_3C_GPIO_P_0/N_0	148.5M
CLK_B_12A_FGT_P_4	156.25M
CLK_B_12A_FGT_P_5	184.32M
CLK_B_12A_FGT_P_6	368.63M
ToD_CLK_100M_P/N	100M
ETH_REFCLK_156.25M_P/N	156.25M
CPRI_REFCLK_153.6M_P/N	153.6M
CPRI_REFCLK_184.32M_P/N	184.32M
FMCA_REFCLK_148.5M_P/N	148.5M
FMCA_REFCLK_156.25M_P/N	156.25M
Si5391_A_156.25M_REFIN_P/N	156.25M
Si5391_B_156.25M_REFIN_P/N	156.25M
CLK_3C_GPIO_P_1/N_1	156.25M
CLK_B_12A_FGT_P_3/N_3	148.5M
CLK_3C_GPIO_P_0/N_0	148.5M
1PPS_FPGA_CLK	1PPS
1PPS_SMA_OUT	1PPS
10MHz_SMA_OUT	10M
ZL_SPARE_CLK_100M	100M

Figure 33. Clock Tree



A.4. General Input/Output

Table 11. Intel MAX 10 and FPGA

Schematic Signal Name	Description
F_GPIO0	The value of filtered user_pb[0]
F_GPIO1	The value of filtered user_pb[1]
F_GPIO2	MCIO_PERST in RP mode
F_GPIO3	FMC_A_PERST in RP mode
F_GPIO4	FMC_B_PERST in RP mode
F_GPIO5	Status of SYS_SW3 from Intel MAX 10
F_GPIO6	Reserved
F_GPIO7	Reserved
F_GPIO8	Reserved
F_GPIO9	Reserved
F_GPIO10	Reserved
F_GPIO11	Reserved
F_GPIO12	Reserved

Table 12. System Intel MAX 10

Schematic Signal Name	Description
SYS_LED0/D9	PGM_LED0 for Avalon-ST configuration
SYS_LED1/D11	PGM_LED1 for Avalon-ST configuration
SYS_LED2/D13	PGM_LED2 for Avalon-ST configuration
SYS_LED3/D15	MAX_ERROR for Avalon-ST configuration
SYS_LED4/D10	MAX_LOAD for Avalon-ST configuration

continued...

Schematic Signal Name	Description
SYS_LED5/D12	MAX_CONF_DONE for Avalon-ST configuration
SYS_LED6/D14	Reserved
SYS_LED7/D16	Reserved
SYS_PB0/S11	MAX_RESETn
SYS_PB1/S12	FPGA_RESETn
SYS_PB2/S13	HPS_COLD_RESETn
SYS_PB3/S14	Power recycle
SYS_PB4/S16	PGM_SEL for Avalon-ST configuration
SYS_PB5/S17	PGM_CFG for Avalon-ST configuration
clk_i2c_en0	Before power ok: 0 After power ok: S_control_gui[2], =1 by default
clk_i2c_en1	Stuck at GND
VCCL_I2C_EN	Before power ok: 0 After power ok: S_control_gui[1], =1 by default
dimm_io_en	Before power ok: 0 After power ok: 1
zl_i2c_en	Before power ok: 0 After power ok: S_control_gui[3], =0 by default
si5394_rstn	When input globe resetn active: 0 When input globe resetn release: S_control_gui[13], =1 by default
si5394_oe_n	Before power ok: 1 After power ok: S_control_gui[14], =0 by default
si5391_rstn	When input globe resetn active: 0 When input globe resetn release: S_control_gui[9], =1 by default
si5394_lol	Store in status_gui bit3
si5394_int_n	Store in status_gui bit2
si5391_oen	Before power ok: 1 After power ok: S_control_gui[10], =0 by default
si5391_b_rstn	When input globe resetn active: 0 When input globe resetn release: S_control_gui[11], =1 by default
si5391_b_oen	Before power ok: 1 After power ok: S_control_gui[12], =0 by default
usb2_resetn	Before power ok: 0 After power ok: S_control_gui[15], =1 by default
usb_mux_reset	Before power ok: 1 After power ok: S_control_gui[16], =0 by default
mux_sel0	system_info_slv_data_write_0[0]=1 : controlled by system_info_slv_data_write_1[0]

continued...

Schematic Signal Name	Description
	system_info_slv_data_write_0[0]=0 : controlled by MUX_DIP_SW10
mux_sel1	system_info_slv_data_write_0[1]=1 : controlled by system_info_slv_data_write_1[1] system_info_slv_data_write_0[1]=0 : controlled by SYS_SW1
mux_sel2	system_info_slv_data_write_0[2]=1 : controlled by system_info_slv_data_write_1[2] system_info_slv_data_write_0[2]=0 : controlled by MUX_DIP_SW0
mux_sel3	system_info_slv_data_write_0[3]=1 : controlled by system_info_slv_data_write_1[3] system_info_slv_data_write_0[3]=0 : controlled by MUX_DIP_SW1
mux_sel4	system_info_slv_data_write_0[4]=1 : controlled by system_info_slv_data_write_1[4] system_info_slv_data_write_0[4]=0 : controlled by MUX_DIP_SW2
mux_sel5	system_info_slv_data_write_0[5]=1 : controlled by system_info_slv_data_write_1[5] system_info_slv_data_write_0[5]=0 : controlled by MUX_DIP_SW3
mux_sel6	system_info_slv_data_write_0[6]=1 : controlled by system_info_slv_data_write_1[6] system_info_slv_data_write_0[6]=0 : controlled by MUX_DIP_SW9
mux_sel7	system_info_slv_data_write_0[7]=1 : controlled by system_info_slv_data_write_1[7] system_info_slv_data_write_0[7]=0 : controlled by SYS_SW2
mux_sel8	system_info_slv_data_write_0[8]=1 : controlled by system_info_slv_data_write_1[8] system_info_slv_data_write_0[8]=0 : controlled by MUX_DIP_SW11
mux_sel9	system_info_slv_data_write_0[9]=1 : controlled by system_info_slv_data_write_1[9] system_info_slv_data_write_0[9]=0 : controlled by SYS_SW3
mux_sel10	system_info_slv_data_write_0[10]=1 : controlled by system_info_slv_data_write_1[10] system_info_slv_data_write_0[10]=0 : controlled by MUX_DIP_SW4
mux_sel11	system_info_slv_data_write_0[11]=1 : controlled by system_info_slv_data_write_1[11] system_info_slv_data_write_0[11]=0 : controlled by MUX_DIP_SW5
mux_sel12	system_info_slv_data_write_0[12]=1 : controlled by system_info_slv_data_write_1[12]

continued...

Schematic Signal Name	Description
	system_info_slv_data_write_0[12]=0 : controlled by MUX_DIP_SW6
mux_sel13	system_info_slv_data_write_0[13]=1 : controlled by system_info_slv_data_write_1[13] system_info_slv_data_write_0[13]=0 : controlled by MUX_DIP_SW8
mux_sel14	system_info_slv_data_write_0[14]=1 : controlled by system_info_slv_data_write_1[14] system_info_slv_data_write_0[14]=0 : controlled by MUX_DIP_SW7
mux_sel_zl	system_info_slv_data_write_0[15]=1 : controlled by system_info_slv_data_write_1[15] system_info_slv_data_write_0[15]=0 : controlled by SYS_SW4
mcio_clk_enn	Before power ok: 1 After power ok: S_control_gui[7], =0 by default
mcio_clk_sel_epn	system_info_slv_data_write_0[16]=1 : controlled by S_control_gui[8], =0 by default system_info_slv_data_write_0[16]=0 : • =0 when AGIB027R31B is Endpoint • =1 when AGIB027R31B is Root port
si5332_1_in[1:0]	S_control_gui[5:4], =00 by default
si5332_1_in[2]	1'bZ
PTP_CLK_RST_n	Before power ok: 0 After power ok: S_control_gui[6], =1 by default
PTP_CLK_LOL	Store in status_gui bit1
gpio0_ac0_zl_intn	Store in status_gui bit0

Table 13. UB2/PWR Intel MAX 10

Schematic Signal Name	Description
FPGA_POK_LED	FPGA Power Good
SYS_PWR_RSV0	Reserved GPIO between System Intel MAX 10 and Power Intel MAX 10. Used as I^2C clock.
SYS_PWR_RSV1	Reserved GPIO between System Intel MAX 10 and Power Intel MAX 10. Used as I^2C data.
SYS_PWR_RSV2	Reserved GPIO between System Intel MAX 10 and Power Intel MAX 10. It is the status of SYS_PB3.
SYS_PWR_RSV3	Reserved GPIO between System Intel MAX 10 and Power Intel MAX 10

A.5. Memory Interfaces

FPGA Dedicated External Memory Interface (2DPC DDR4)

Intel Agilex I-Series Transceiver-SoC Development Kit supports 32 GB 2DPC DDR4 with ECC support (x72). Mechanically, the development kit provides 2 dual-in memory module slots for the same. This development kit also supports 16 GB 1DPC DDR4 with ECC support (x72). Mechanically, install one RDIMM module on **J5**.

FPGA and HPS Shared External Memory Interface (DDR4)

DDR4 component interface is a 72 bit, single rank configuration based on x16 component. It runs at 2666 Mbps. MT40A1G16RC-062E:B from Micron is soldered down on the development kit. Both Intel Agilex FPGA fabric and HPS can access this external memory interface. However, they cannot be accessed at the same time.

A.6. Communication Interfaces

MCIO Port

The MCIO slot is a PCIe Gen4 x4 port which fans out from Intel Agilex I-Series FPGA F-tile. This port is designed to meet the standard MCIO pinout. System Intel MAX 10 acts as the board management controller (BMC) of the development kit. It manages power-up reset for both PCIe root port and PCIe endpoint. PCIE_PERSTn_A signal can act as output and input respectively.

Table 14. MCIO Port

Schematic Signal Name	Description
PCIE_PERSTn_A	PCIe endpoint/root port reset
PCIE_ALERTn_A	PCIe Alert
PCIE_100M_REF_AP/AN	PCIe reference clock
PCIE_SCL_A/SDA_A	PCIe I^2C bus
PCIE_TX_P/N[0:3]	Transceiver TX
PCIE_RX_P/N[0:3]	Transceiver RX

MCIO x4 Connector

The recommended MCIO cable to use with MCIO connector (Uxx) is NOT included as part of the development kit and must be acquired directly from third party supplier (Amphenol p/n = HMC74-0631).

QSFPDD

Intel Agilex I-Series Development Kit supports 2x QSFPDD ports. QSFDD port fans out from Intel Agilex I-Series FPGA F-tile (FGT). All 8 channels per QSFPDD can run up to 32G NRZ and 58G PAM4.

Table 15. QSFPDD Connector 0 (13C/J27)

Schematic Signal Name	Description
QSFPDD0_3V3_MODPRS_L	Module present
QSFPDD0_3V3_RESET_L	Module reset
QSFPDD0_3V3_MODSEL_L	Mode select
QSFPDD0_3V3_LPMODE	Initial mode
QSFPDD0_3V3_INT_L	Interrupt
I2C_QSFPDD0_3V3_SCL	I^2C clock
I2C_QSFPDD0_3V3_SDA	I^2C data
QSFPDD0_TX_P/N[0:7]	Transceiver TX
QSFPDD0_RX_P/N[0:7]	Transceiver RX

Table 16. QSFPDD Connector 1 (13A/J48)

Schematic Signal Name	Description
QSFPDD1_3V3_MODPRS_L	Module present
QSFPDD1_3V3_RESET_L	Module reset
QSFPDD1_3V3_MODSEL_L	Mode select
QSFPDD1_3V3_LPMODE	Initial mode
QSFPDD1_3V3_INT_L	Interrupt
I2C_QSFPDD1_3V3_SCL	I^2C clock
I2C_QSFPDD1_3V3_SDA	I^2C data
QSFPDD1_TX_P/N[0:7]	Transceiver TX
QSFPDD1_RX_P/N[0:7]	Transceiver RX

QSFPDD800/MXP

Intel Agilex I-Series Development Kit supports 1x QSFPDD800 port. QSFDD800 port fans out from Intel Agilex I-Series FPGA F-tile (FHT). The FHT tile from bank 13A and 13C can run up to 116G PAM4. 4 FHT lanes from bank 13C is terminated directly to QSFPDD800 connector lanes [0:3] (**J22**).

Table 17. QSFPDD800 (13A)

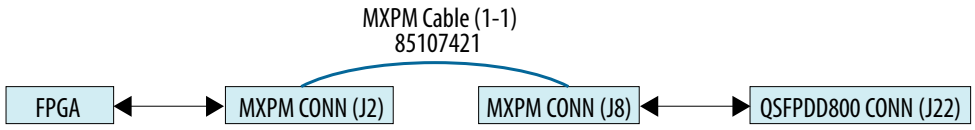
Schematic Signal Name	Description
QSFPDD800_3V3_MODPRS_L	Module present
QSFPDD800_3V3_RESET_L	Module reset
QSFPDD800_3V3_MODSEL_L	Mode select
QSFPDD800_3V3_LPMODE	Initial mode
QSFPDD800_3V3_INT_L	Interrupt
I2C_QSFPDD800_3V3_SCL	I^2C clock

continued...

Schematic Signal Name	Description
I2C_QSFPDD800_3V3_SDA	I^2C data
QSFPDD800_TX_P/N[0:3]	Transceiver TX
QSFPDD800_RX_P/N[0:3]	Transceiver RX

Four FHT lanes from bank 13A are terminated to MXPM connector (**J2**).Other lanes [4:7] of QSFPDD800 connector is terminated to MXPM connector (**J8**). For x8 QSFPDD800 topology, 1-1 cable between **J2** and **J8** need to be used.

Figure 34. MXPM Cable



MXP

MXP port fan out from Intel Agilex I-Series FPGA F-tile (13A). All four channels can run up to 32G NRZ and 58G PAM4.

Table 18. MXP

Schematic Signal Name	Description
FGT_MXPM_TX_P/N_[0:3]	Transceiver TX
FGT_MXPM_RX_P/N_[0:3]	Transceiver RX

FMC+ Connector

Intel Agilex I-Series Development Kit supports 2x FMC+ slots for functional expandability. The x16 FGT lanes from bank 12C and 12A are terminated to FMC-A (**J7**) and FMC-B (**J9**) connectors, respectively. Auxiliary signals are controlled by the system Intel MAX 10.

SDI Connector

1x FGT channel (13C/Q0/CH3) been terminated to the HD-BNC TX (**J1**) and RX (**J32**) connectors to support up to 12G SDI. System Intel MAX 10 acts as an I^2C master for both SDI driver and receiver, along with control signals.

USB Type-C Connector

Intel Agilex I-Series Development Kit has hardware support for the USB Type-C connector, which supports DP1.4 specification or USB 3.1 functionality through MUX (TUSB1146). This feature is yet to be validated and implemented.

Serial Buses

SDM I/Os (SDM_IO0/12) and Intel MAX 10 I/Os (VCCL_SDA/SCL) share the same I^2C bus which communicate with Intel Agilex FPGA core regulators. By default, SDM acts as SmartVID master and system Intel MAX 10 act as Power GUI master in this chain.

System Intel MAX 10 I/Os (PMB_SDA/SCL) manages the second I^2C bus which access all I^2C slave regulator except Intel Agilex FPGA core regulators.

System Intel MAX 10 supports I²C master dedicated to clock-related devices (CLK_I2C_SDA/SCL), which manages 3# clock devices and also connected to the HPS I/Os (HPS_GPIO30/31) through level translator.

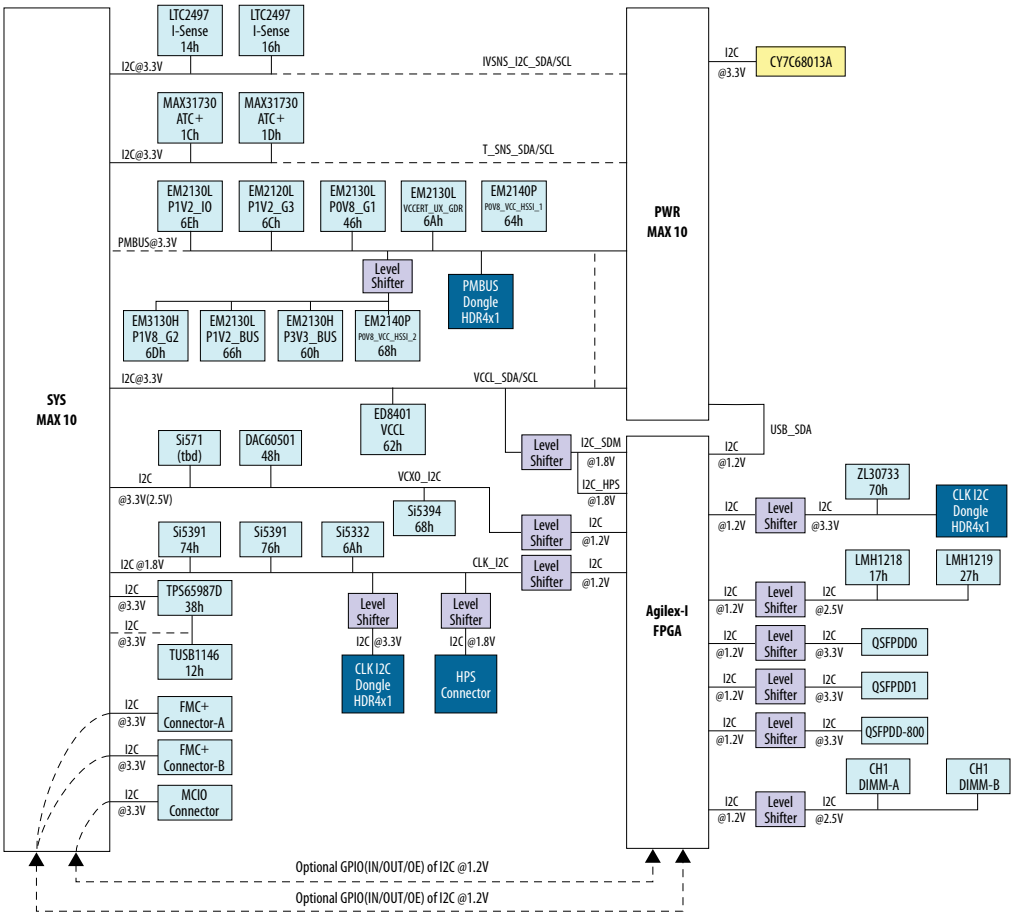
Another I²C master instance from system Intel MAX 10 (VCXO_I2C_SDA/SCL) controls the on board VCXO and Si5394 clock generator.

Intel Agilex FPGA also manages QSFPDD800, 2x QSFPDD, 2DPC DIMM I²C buses, SDI transceivers, and ZL30733 clock synthesizer device.

Table 19. I²C Debug Headers

Schematic Signal Name	Description
PMB_SCL/SDA	VRs I²C header **J41**
CLK_I2C_SDA/SCL_3V3	System Intel MAX 10 clock I²C bus header **J42**
ZL_I2C_SDA/SCL	ZL30733 I²C access header **J21**

Figure 35. I²C Serial Bus



A.7. Daughter Cards

HPS IO48 OOBE Daughter Card

- One RGMII 10/100/1000 Mbps Ethernet port: Standard RJ-45
- One UART port: Standard USB Mini-B Receptacle
- One Micro SD Card Connector: Standard Micro SD Card Socket
- One USB 2.0 port: Standard USB Micro-AB Receptacle
- One Mictor 38-pin connector (JTAG only without Trace signals)
- HPS dedicated JTAG pins are connected with both mother board JTAG chain and Mictor 38-pin header
- I^2C: HPS I^2C port
- GPIO
  - 2 Push buttons
  - 3 LEDs
  - 1 Ethernet Interrupt from Ethernet PHY
  - 1 USB over-current indicator
- HPS Clock: 25 MHz oscillator

256 MB QSPI Flash Daughter Card

This daughter card is pre-programmed with GHRD for AS configuration. It can be re-programmed by customer image. The part number is MT25QU02GCBB8E12-0SIT.

A.8. Connectors and Cables

Table 20. Connectors and Cables

Connectors and Cables	Part Number	Switch Reference	Notes
QSFPDD loopback module	NLNAMB0001 (Amphenol)	**J27** **J48** **J22** (for use up to 400 G)	—
QSFP-DD800 loopback type 1	ML4062-LB-112 (Multilane)	**J22**	For 800 G usage, connect 85107421 at **J2** and **J8**
MXMP breakout cable	85107421	**J2** – **J8**	Connect between **J2** and **J8**
MCIO cable	HMC74-0631	**J37**	—
HD-BNC Straight Plug to HD-BNC Straight Plug	095-850-214M100 (Amphenol)	**J1** **J32**	SDI loopback between **J1** and **J32**

B. Additional Information

B.1. Safety and Regulatory Information

ENGINEERING DEVELOPMENT PRODUCT - NOT FOR RESALE OR LEASE

This development kit is intended for laboratory development and engineering use only.

This development kit is designed to allow:

- Product developers and system engineers to evaluate electronic components, circuits, or software associated with the development kit to determine whether to incorporate such items in a finished product.
- Software developers to write software applications for use with the end product.

This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required Federal Communications Commission (FCC) equipment authorizations are first obtained.

Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference.

Unless the assembled kit is designed to operate under Part 15, Part 18 or Part 95 of the United States Code of Federal Regulations (CFR) Title 47, the operator of the kit must operate under the authority of an FCC licenseholder or must secure an experimental authorization under Part 5 of the United States CFR Title 47.

Safety Assessment and CE & UKCA mark requirements have been completed, however, other certifications that may be required for installation and operation in your region have not been obtained.

B.1.1. Safety Warnings

Power Supply Hazardous Voltage

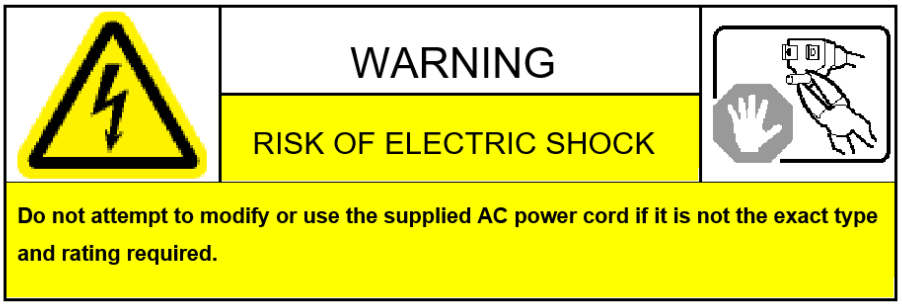
AC mains voltages are present within the power supply assembly. No user serviceable parts are present inside the power supply.

Power Connect and Disconnect

The AC power supply cord is the primary disconnect device from mains (AC power) and used to remove all DC power from the board/system. The socket outlet must be installed near the equipment and must be readily accessible.

System Grounding (Earthing)

To avoid shock, you must ensure that the power cord is connected to a properly wired and grounded receptacle. Ensure that any equipment to which this product is attached to is also connected to properly wired and grounded receptacles.



Power Cord Requirements

The plug on the power cord must be a grounding-type male plug designed for use in your region. It must have certification marks showing certification by an agency in your region. The connector that plugs into the appliance inlet of the power supply must be an IEC 320, sheet C13, female connector. If the power cord supplied with the system does not meet requirements for use in your region, discard the cord, and do not use it with adapters. Use only certified power supply cord with appropriate gauge, designed for use in your region.

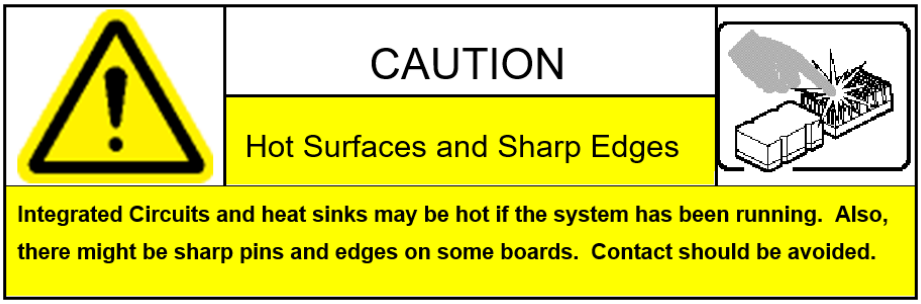
Lightning/Electrical Storm

Do not connect/disconnect any cables or perform installation/maintenance of this product during an electrical storm.

Risk of Fire

To reduce the risk of fire, keep all flammable materials a safe distance away from the boards and power supply. You must configure the development kit on a flame retardant surface.

B.1.2. Safety Cautions



Thermal and Mechanical Injury

Certain components such as heat sinks, power regulators, and processors may be hot. Heatsink fans are not guarded. Power supply fan may be accessible through guard. Care should be taken to avoid contact with these components.

Cooling Requirements

Maintain a minimum clearance area of 5 centimeters (2 inches) around the side, front and back of the board for cooling purposes. Do not block power supply ventilation holes and fan.

Electro-Magnetic Interference (EMI)

This equipment has not been tested for compliance with emission limits of FCC and similar international regulations. Use of this equipment in a residential location is prohibited. This equipment generates, uses and can radiate radio frequency energy which may result in harmful interference to radio communications. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment on and off, you are required to take measures to eliminate this interference.

Telecommunications Port Restrictions

The wireline telecommunications ports (modem, xDSL, T1/E1) on this product must not be connected to the Public Switched Telecommunication Network (PSTN) as it might result in disruption of the network. No formal telecommunication certification to FCC, R&TTE Directive, or other national requirements have been obtained.

Electrostatic Discharge (ESD) Warning

A properly grounded ESD wrist strap must be worn during operation/installation of the boards, connection of cables, or during installation or removal of daughter cards. Failure to use wrist straps can damage components within the system.

Attention: Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of this product in unsorted municipal waste.

Lithium Ion Battery Warnings

Lithium Battery: Risk of explosion if the lithium battery is replaced by an incorrect type. Risk of fire, explosion, or chemical burn if the battery is mistreated (punctured or crushed). Do not attempt to disassemble. Do not incinerate. Observe proper polarity when replacing battery. Do not dispose—the battery is intended to be serviced and disposed by qualified Intel service personnel only.

Perchlorate Material: Special handling may apply. For more details, refer to www.dtsc.ca.gov/hazardouswaste/perchlorate. This notice is required by California Code of Regulations, Title 22, Division 4.5, Chapter 33: Best Management Practices for Perchlorate Materials. This product includes a battery which contains perchlorate material.

Taiwan battery recycling:

(Translation - please recycle batteries)

Please return this product to Intel for proper disposition. If it is not returned, refer to local environmental regulations for proper recycling. Do not dispose of product in unsorted municipal waste.

B.2. Compliance Information

CE EMI Conformity Caution

This development board is delivered conforming to relevant standards mandated by Directive 2014/30/EU. Because of the nature of programmable logic devices, it is possible for the user to modify the development kit in such a way as to generate electromagnetic interference (EMI) that exceeds the limits established for this equipment. Any EMI caused as a result of modifications to the delivered material is the responsibility of the user of this development kit.