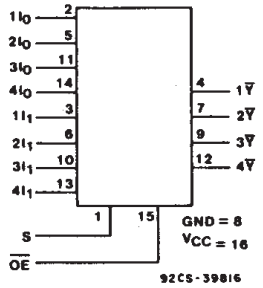
CD54/74HC258
CD54/74HCT258

File Number **1775**

High-Speed CMOS Logic

Data sheet acquired from Harris Semiconductor
SCHS276



FUNCTIONAL DIAGRAM

Quad 2-Input Multiplexer with 3-State Inverting Outputs

Type Features:

- *Buffered inputs*
- *Typical CD54/74HC258 propagation delay = 7 ns @ V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C*

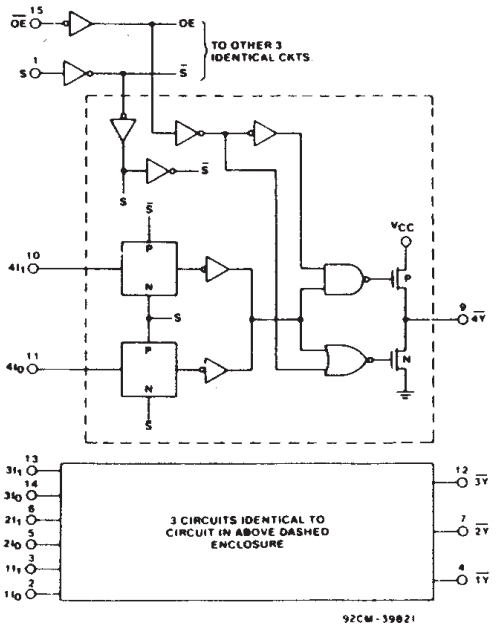
The RCA-CD54/74HC258 and CD54/74HCT258 are quad 2-input multiplexers which select four bits of data from two sources under the control of a common Select input (S). The Output Enable input ($\overline{OE}$) is active LOW. When $\overline{OE}$ is HIGH, all of the outputs ($\overline{1Y}$-$\overline{4Y}$) are in the high impedance state regardless of all other input conditions.

Moving data from two groups of registers to four common output busses is a common use of the 258. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator.

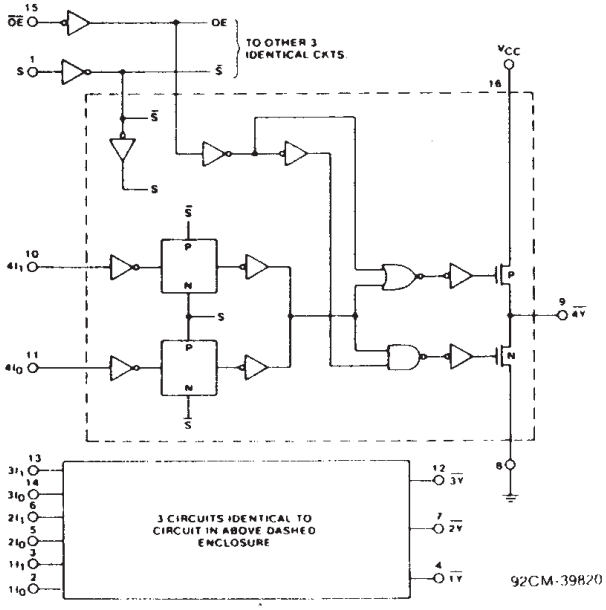
The CD54HC/HCT258 are supplied in 16-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC/HCT258 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT/HCU: -40 to +85°C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity:
  N_{IL} = 30%, N_{IH} = 30% of V_{CC}; @ V_{CC} = 5V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



CD54/74HC258 Logic Diagram



CD54/74HCT258 Logic Diagram

This data sheet is applicable to the CD74HC258 and CD54HCT258. The CD54HC258 was not acquired from Harris Semiconductor. See SCHS172 for information on the CD74HCT258.

CD54/74HC258
CD54/74HCT258

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to + 7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5V) ..... ±20mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5V) ..... ±20mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5\ V < V_O < V_{CC} + 0.5V$) ..... ±35mA
DC V_{CC} OR GROUND CURRENT (I_{CC}) ..... ±70mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -55 to +100°C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/°C to 300 mW
For T_A = -40 to +70°C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125°C
PACKAGE TYPE E, M ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300°C

RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

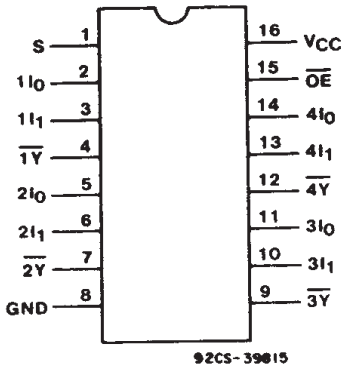
CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t_r, t_f			
at 2 V	0	1000	
at 4.5 V	0	500	ns
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.

FUNCTION TABLE

Output Enable	Select Input	Data Inputs		Output
$\overline{OE}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High level voltage
L = Low level voltage
X = Don't care.
Z = High impedance (off) state



TERMINAL ASSIGNMENT

CD54/74HC258
CD54/74HCT258

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC258/CD54HC258										CD74HCT258/CD54HCT258									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE		
	V_I V	I_O mA	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		V_I V	V_{CC} V	+25°C			-40/ +85°C		-55/ +125°C		
				Min	Typ	Max	Min	Max	Min	Max			Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9											
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	-6	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-7.8	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads (Bus Driver)	V_{IL} or V_{IH}	6	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		7.8	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Grid	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC}-2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA
3-State leakage current I_{OZ}	V_{IL} or V_{IH}	$V_O = V_{CC}$ or Gnd	6	—	—	±0.5	—	±5	—	±10	V_{IL} or V_{IH}	5.5	—	—	±0.5	—	±5	—	±10	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT Input Loading Table

Input	Unit Loads*
Data	0.5
S	1.5
$\overline{OE}$	1.5

*Unit Load is ΔI_{CC} limit specified in Static Characteristic Chart, e.g., 360 μA max. @ 25°C.

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SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL HC	TYPICAL HCT	UNITS
nI_O, nI_I, to $\overline{Y}$	t_{PHL} t_{PLH}	15	7	11	ns
$\overline{OE}$ to $\overline{Y}$	t_{PZL} t_{PZH}	15	11	11	ns
	t_{PLZ} t_{PHZ}	15	12	12	ns
S to $\overline{Y}$	t_{PHL} t_{PLH}	15	11	14	ns
Power Dissipation Capacitance*	C_{PD}	—	49	49	pF

*C_{PD} is used to determine the dynamic power consumption, per multiplexer.
$P_D = V_{CC}^2 fi (C_{PD} + C_L)$ where: fi = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		V_{CC}	25°C HC Min.	25°C HC Max.	25°C HCT Min.	25°C HCT Max.	-40°C to +85°C 74HC Min.	-40°C to +85°C 74HC Max.	-40°C to +85°C 74HCT Min.	-40°C to +85°C 74HCT Max.	-55°C to +125°C 54HC Min.	-55°C to +125°C 54HC Max.	-55°C to +125°C 54HCT Min.	-55°C to +125°C 54HCT Max.	UNITS
Propagation Delay,	t_{PLH}	2	—	95	—	—	—	120	—	—	—	145	—	—	
nI_O, nI_I, to $\overline{Y}$	t_{PHL}	4.5	—	19	—	27	—	24	—	34	—	29	—	41	ns
(Fig. 2)		6	—	15	—	—	—	20	—	—	—	25	—	—	
Propagation Delay		2	—	140	—	—	—	175	—	—	—	210	—	—	
S to $\overline{Y}$	t_{PLH}	4.5	—	28	—	34	—	35	—	43	—	42	—	51	ns
(Fig. 3)	t_{PHL}	6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay		2	—	140	—	—	—	175	—	—	—	210	—	—	
$\overline{OE}$ to Y	t_{PZL}	4.5	—	28	—	28	—	35	—	35	—	42	—	42	ns
(Fig. 4)	t_{PZH}	6	—	24	—	—	—	30	—	—	—	36	—	—	
Propagation Delay	t_{PLZ}	2	—	150	—	—	—	190	—	—	—	225	—	—	
$\overline{OE}$ to Y		4.5	—	30	—	30	—	38	—	38	—	45	—	45	ns
(Fig. 4)	t_{PHZ}	6	—	26	—	—	—	33	—	—	—	38	—	—	
Output Transition	t_{TLH}	2	—	60	—	—	—	75	—	—	—	90	—	—	
Time	t_{THL}	4.5	—	12	—	12	—	15	—	15	—	18	—	18	ns
(Fig. 2)		6	—	10	—	—	—	13	—	—	—	15	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF
3-State Output Capacitance	C_O		—	20	—	20	—	20	—	20	—	20	—	20	pF

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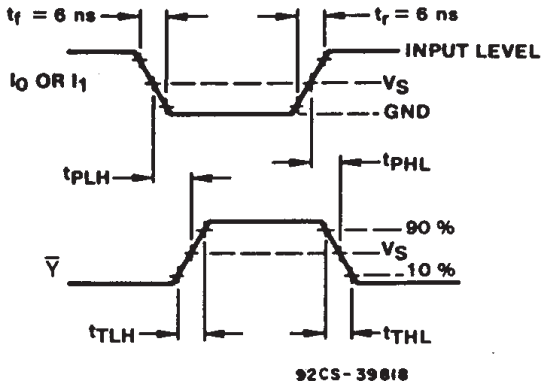

Fig. 2 - Select to output delays.

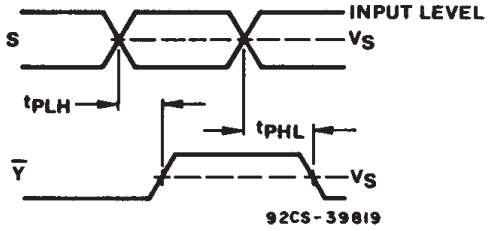

Fig. 3 - Select to output propagation delays.

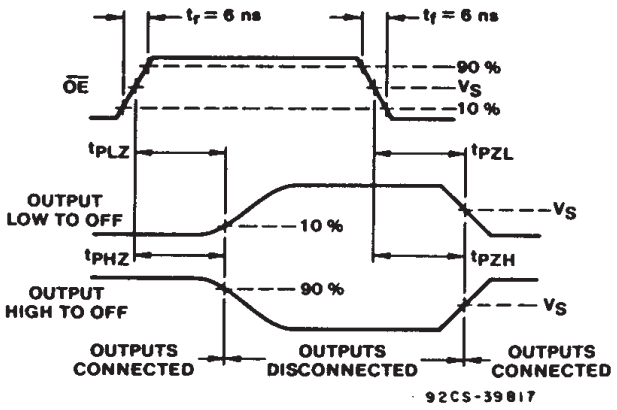

Fig. 4 - Output Enable to output propagation delays.

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3 V

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