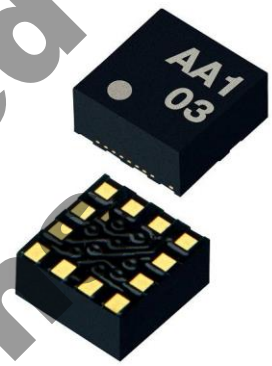
Kionix®	**± 2g / 4g / 8g / 16g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX003-1077 Rev. 2.0 05-Oct-2018**

Product Description



The KX003-1077 is a tri-axis ±2g, ±4g, ±8g, or ±16g silicon micromachined accelerometer. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning and digital communications. The accelerometer is delivered in a 2 x 2 x 0.9 mm LGA plastic package operating from a 1.71V – 3.6V DC supply. Voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics over the range of input supply voltages and virtually undetectable ratiometric error. The I^2C digital protocol is used to communicate with the chip to configure the part and monitor outputs.

Features

- Small footprint: 2 x 2 x 0.9 mm LGA 12-pin package
- Low current consumption: 0.9 µA in standby, 10 µA in Low Power, and 155 µA in High Resolution modes
- Extended user-configurable g-ranges: ±2g, ±4g, ±8g, ±16g
- 8-bit, 12-bit, and 14-bit resolution modes
- Wide supply voltage range: 1.71V – 3.6V with internal voltage regulator
- High resolution Wake-Up function with threshold configurable down to 3.9 mg
- User-configurable Output Data Rates from 0.781Hz to 1600Hz
- I^2C digital communication interface up to 3.4MHz
- Highly configurable interrupt control
- Embedded Low Pass filter
- Improved design to virtually eliminate post reflow offset and sensitivity shifts
- Improved noise performance
- Stable performance over temperature
- High shock survivability
- Self-test function
- RoHS / REACH compliant

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Kionix®	**± 2g / 4g / 8g / 16g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX003-1077 Rev. 2.0 05-Oct-2018**

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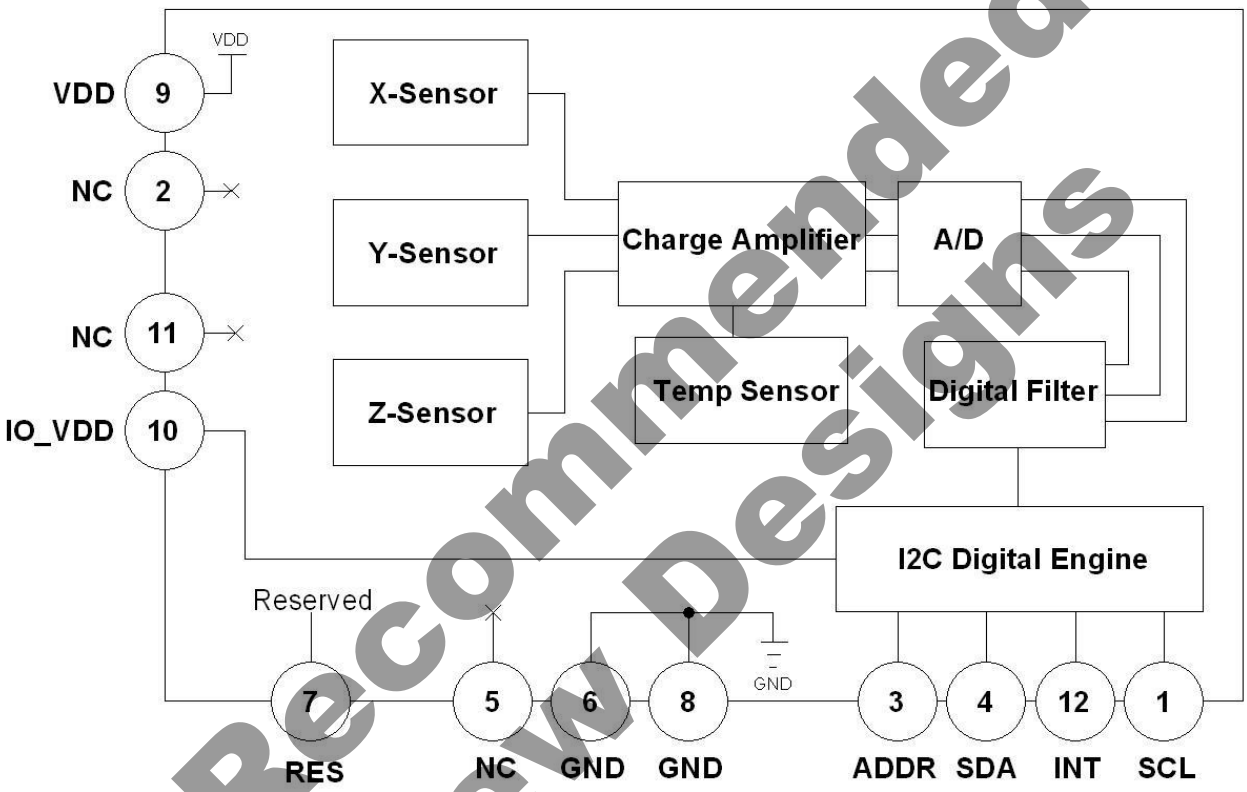
Functional Diagram



Kionix®	**± 2g / 4g / 8g / 16g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER: KX003-1077 Rev. 2.0 05-Oct-2018**

Product Specifications

Mechanical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		°C	-40	-	+85
Zero-g Offset		mg		±25	
Zero-g Offset Variation from RT over Temp.		mg/ºC		0.2	
Sensitivity (14-bit)[1,2]	± 8g	counts/g		1024	
	± 16g			512	
Sensitivity (12-bit)[1]	± 2g	counts/g		1024	
	± 4g			512	
	± 8g			256	
	± 16g			128	
Sensitivity (8-bit)[1]	± 2g	counts/g		64	
	± 4g			32	
	± 8g			16	
	± 16g			8	
Sensitivity Variation from RT over Temp.		%/°C		0.01	
Positive Self-Test Output change on Activation[3]		g		0.5 (x) -0.5 (y) 0.5 (z)	
Non-Linearity		% of FS		0.6	
Cross Axis Sensitivity		%		2	
Noise[4]	RMS Noise	mg		0.7	
	Noise Density	µg / √Hz		150	

Table 1: Mechanical Specifications

Notes:

1. Resolution and acceleration ranges are user selectable via I²C and via CTRL_REG1 register.
2. 14-bit Resolution is only available for registers 0x06 – 0x0B in the ±8g or ±16g High Resolution mode
3. Self-test can be exercised by setting STPOL bit = 1 in INT_CTRL_REG1 register, then writing 0xCA to the SELF_TEST register.
4. Noise is measured in High Resolution mode (RES = 1 in CTRL_REG1 register) at 50Hz ODR.

Electrical

(specifications are for operation at 2.5V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Operating	V	1.71	2.5	3.6
I/O Pads Supply Voltage (IO_VDD)		V	1.7		3.6
Current Consumption	High Resolution Mode (RES=1)	µA		155	
	Low Power Mode[1] (RES=0)			10	
	Disabled			0.9	
Output Low Voltage (V_{OL}) (IO_VDD < 2V)[2]		V	-	-	0.2 * IO_VDD
Output Low Voltage (V_{OL}) (IO_VDD ≥ 2V)[2]		V	-	-	0.4
Output High Voltage (V_{OH})		V	0.8 * IO_VDD	-	-
Input Low Voltage (V_{IL})		V	-	-	0.2 * IO_VDD
Input High Voltage(V_{IH})		V	0.8 * IO_VDD	-	-
Start Up Time[3]		ms		~1/ODR	
Power Up Time[4]		ms		12	30
I²C Communication Rate		MHz			3.4
I²C Slave Address (7-bit)[5]				0x0E / 0x0F	
Output Data Rate (ODR)[6]		Hz	0.781	50	1600
Output Signal Bandwidth (-3dB)[7]	High Resolution Mode (RES=1)	Hz		ODR/2	
	Low Power Mode (RES=0)			800	

Table 2: Electrical Specifications

Notes:

1. Current varies with Output Data Rate (ODR). See *Current Profile* section for details.
2. For I²C communication, this assumes a minimum 1.5kΩ pull-up resistor on SCL and SDA pins.
3. Start up time is from PC1 bit set to 1 in CTRL_REG1 register to valid outputs. Time varies with Output Data Rate (ODR) and power mode (RES bit setting in CTRL_REG1 register). See *Figure 1* for details.
4. Power up time is from VDD and IO_VDD valid to device boot completion.
5. User selectable with ADDR pin. See *Digital Interface* section for details.
6. User selectable through I²C. The shown values are typical.
7. User selectable and dependent on ODR setting in DATA_CTRL_REG register and RES bit setting in CTRL_REG1 register.

Start Up Time Profile

Typical Start Up Time (msec)		
ODR (Hz)	High Resolution RES = 1	Low Power RES = 0
0.781	1281	2
1.563	641	2
3.125	321	2
6.25	161	2
12.5	81	2
25	41	2
50	21	2
100	11	2
200	6	2
400	4	N/A
800	3	N/A
1600	2	N/A

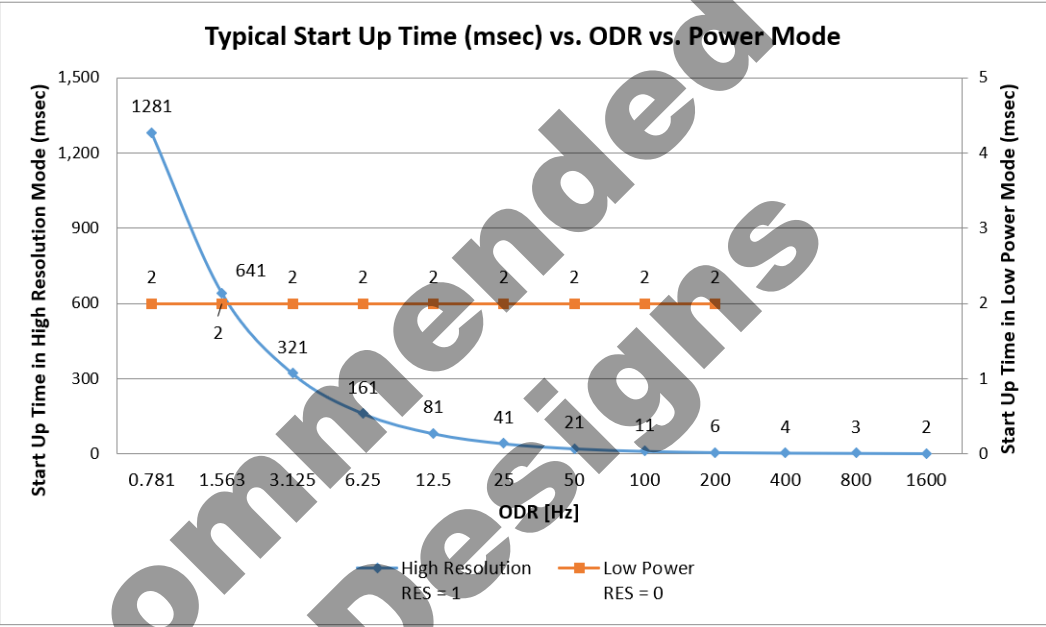


Figure 1: Typical Start Up Time

Current Profile

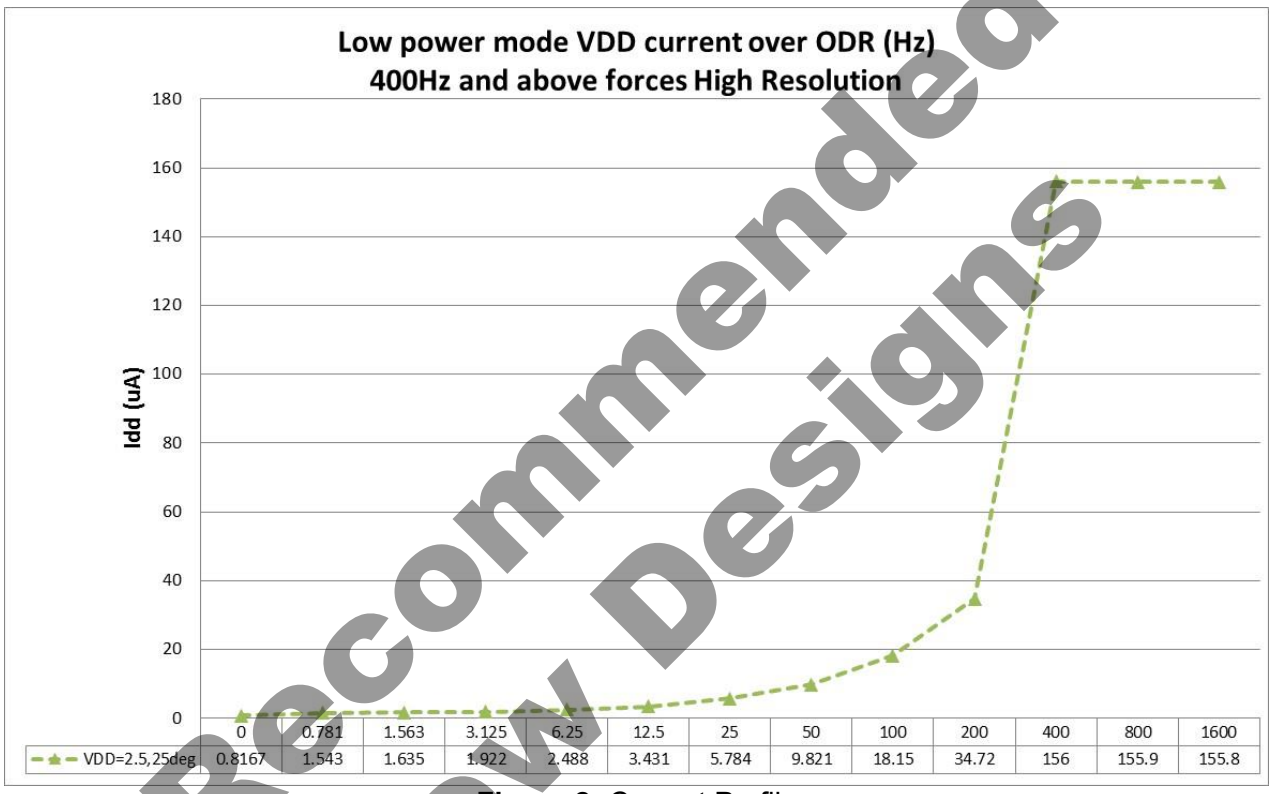


Figure 2: Current Profile

Power-On Procedure

Proper functioning of power-on reset (POR) is dependent on the specific **VDD, VDD_{LOW}**, **T_{VDD}** (rise time), and **T_{VDD_OFF}** profile of individual applications. It is recommended to minimize **VDD_{LOW}**, and **T_{VDD}**, and maximize **T_{VDD_OFF}**. It is also advised that the **VDD** ramp up time **T_{VDD}** be monotonic. Note that the outputs will not be stable until **VDD** has reached its final value.

To assure proper POR, the application should be evaluated over the customer specified range of VDD, VDD_{LOW}, T_{VDD}, T_{VDD_OFF} and temperature as POR performance can vary depending on these parameters.

Please refer to Technical Note ***TN017 Power-On Procedure*** for more information.

Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (VDD)	Absolute Limits	V	-0.5	-	3.63
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Table 3: Environmental Specifications

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

HF

This product is in conformance with RoHS directive, REACH regulation, and is Halogen-Free. For the current certificate of compliance, visit www.kionix.com website.

Handling, Mounting, Soldering

For package handling, mounting, and soldering guidelines, see TN007 Package Handling, Mounting, and Soldering Guidelines technical note.

Floor Life

Factory floor life exposure of the KX003 reels removed from the moisture barrier bag should not exceed a maximum of 168 hours at 30C/60%RH. If this floor life is exceeded, the parts should be dried per the IPC/JEDEC J-STD-033D standard (or latest revision).

Terminology

g

A unit of acceleration equal to the acceleration of gravity at the earth's surface.

$$1g = 9.8\frac{m}{s^2}$$

One thousandth of a g (0.0098 m/ s^2) is referred to as 1 milli-g (1 mg).

Sensitivity

The sensitivity of an accelerometer is the change in output per unit of input acceleration at nominal VDD and temperature. The term is essentially the gain of the sensor expressed in counts per g (counts/g) or LSB's per g (LSB/g). Occasionally, sensitivity is expressed as a resolution, i.e. milli-g per LSB (mg/LSB) or milli-g per count (mg/count). Sensitivity for a given axis is determined by measurements of the formula:

$$Sensitivity = \frac{(Output@+1g - Output@-1g)}{2g}$$

The sensitivity tolerance describes the range of sensitivities that can be expected from a large population of sensors at room temperature and over life. When the temperature deviates from room temperature (25ºC), the sensitivity will vary by the amount shown in Table 1.

Zero-g offset

Zero-g offset or 0-g offset describes the actual output of the accelerometer when no acceleration is applied. Ideally, the output would always be in the middle of the dynamic range of the sensor (content of the XOUT, YOUT, ZOUT registers = 0x00, expressed as a 2's complement number). However, because of mismatches in the sensor, calibration errors, and mechanical stress, the output can deviate from 0x00. This deviation from the ideal value is called 0-g offset. The zero-g offset tolerance describes the range of 0-g offsets of a population of sensors over the operating temperature range.

Self-test

Self-test allows a functional test of the sensor without applying a physical acceleration to it. When activated, an electrostatic force is applied to the sensor, simulating an input acceleration. The sensor outputs respond accordingly. If the output signals change within the amplitude specified in Table 1, then the sensor is working properly, and the parameters of the interface chip are within the defined specifications.

Functionality

Sense element

The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. This process technology allows Kionix to create mechanical silicon structures which are essentially mass-spring systems that move in the direction of the applied acceleration. Acceleration sensing is based on the principle of a differential capacitance arising from the acceleration-induced motion. Capacitive plates on the moving mass move relative to fixed capacitive plates anchored to the substrate. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit.

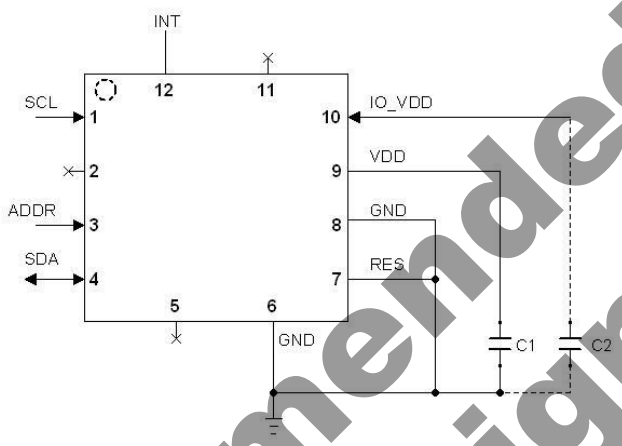
ASIC interface

A separate ASIC device packaged with the sense element provides all of the signal conditioning and communication with the sensor. The complete measurement chain is composed by a low-noise capacitance to voltage amplifier which converts the differential capacitance of the MEMS sensor into an analog voltage that is sent through an analog-to-digital converter. The acceleration data may be accessed through the I^2C digital communications provided by the ASIC. In addition, the ASIC contains all of the logic to allow the user to choose data rates, g-ranges, filter settings, and interrupt logic.

Factory calibration

Kionix trims the offset and sensitivity of each accelerometer by adjusting gain (sensitivity) and 0-g offset trim codes stored in non-volatile memory (OTP). Additionally, all functional register default values are also programmed into the nonvolatile memory. Every time the device is turned on or a software reset command is issued, the trimming parameters and default register values are downloaded into the volatile registers to be used during active operation. This allows the device to function without further calibration.

Application Schematic



Pin Description

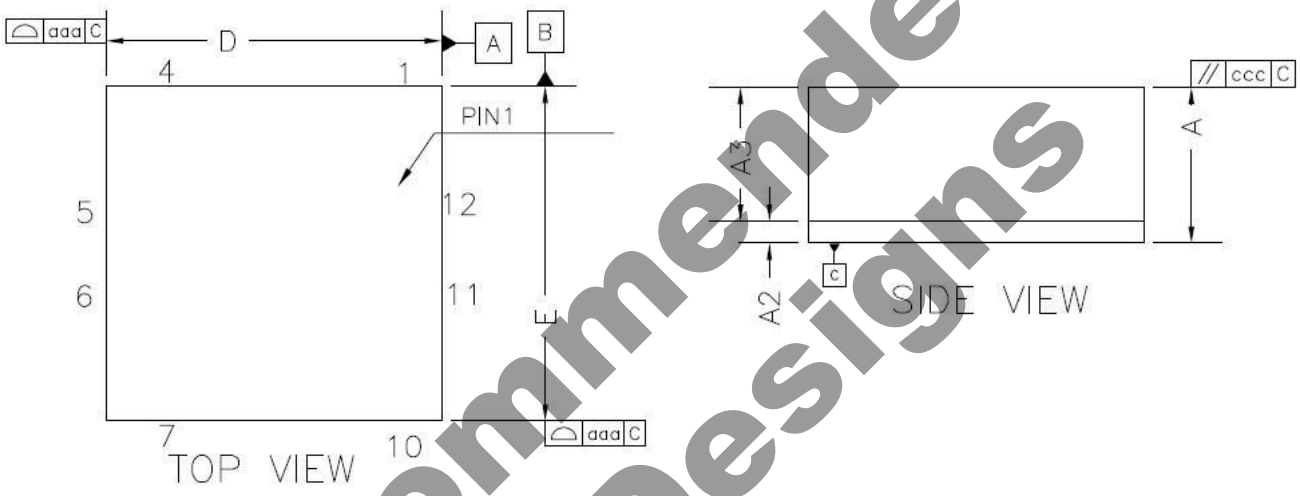
Pin	Name	Description
1	SCL	I2C Serial Clock
2	NC	Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.
3	ADDR	I2C Address pin. This pin must be connected to IO_VDD or GND to determine the I2C Device Address.
4	SDA	I2C Serial Data
5	NC	Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.
6	GND	Ground. (Internally tied to Pin 8)
7	RES	Reserved. Connect to GND. Optionally, can be connected to IO_VDD or VDD. Do not leave floating.
8	GND	Ground. (Internally tied to Pin 6)
9	VDD	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
10	IO_VDD	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor
11	NC	Not Internally Connected - Can be connected to VDD, IO_VDD, GND or leave floating.
12	INT	Physical Interrupt pin (Push-Pull). Leave floating if not used.

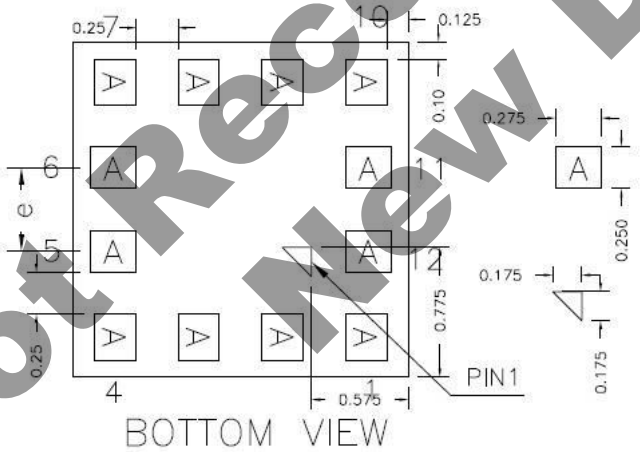
Table 4: Pin Description

Package Dimensions and Orientation

Dimensions

2 x 2 x 0.9 mm LGA





MILLIMETER			
SYMBOL	MIN	NOR	MAX
A	0.86	0.93	1.00
A2	0.10	0.13	0.16
A3	0.76	0.80	0.84
D	1.95	2.00	2.05
E	1.95	2.00	2.05
e	BSC 0.50		
aaa	0.10		
ccc	0.05		

PO-WJA220012-S7_01

All dimensions and tolerances conform to ASME Y14.5M-1994

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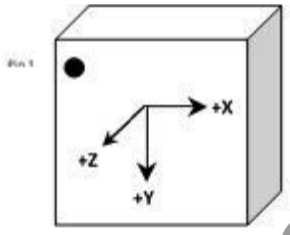
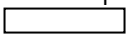
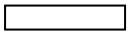
Orientation

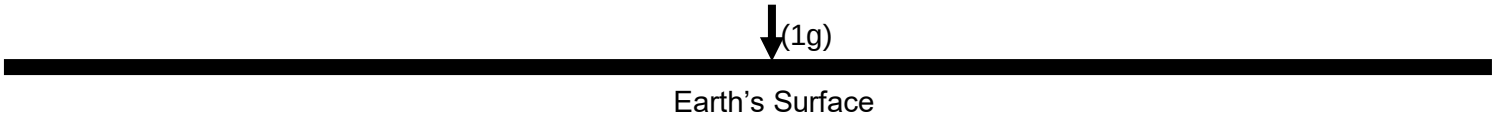


When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

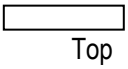
GSEL1=0, GSEL0=0, EN16G=0 (±2g)

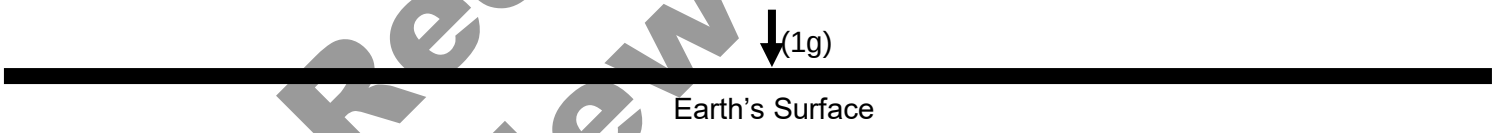
Position	1		2		3		4		5		6	
Diagram									 Top Bottom		 Bottom Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	+1024	+64	0	0	-1024	-64	0	0	0	0
Y (counts)	-1024	-64	0	0	+1024	+64	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+1024	+64	-1024	-64
X-Polarity	0		+		0		-		0		0	
Y-Polarity	-		0		+		0		0		0	
Z-Polarity	0		0		0		0		+		-	



Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1, EN16G=0 (±4g)

Position	1		2		3		4		5		6	
Diagram									 Top Bottom		 Bottom Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	+512	+32	0	0	-512	-32	0	0	0	0
Y (counts)	-512	-32	0	0	+512	+32	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	+512	+32	-512	-32
X-Polarity	**0**		**+**		**0**		**-**		**0**		**0**	
Y-Polarity	**-**		**0**		**+**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0, EN16G=0 (±8g)
GSEL1=1, GSEL0=1, EN16G=0 (±8g)[1]

Position	1			2			3			4			5			6		
Diagram													Top / Bottom			Bottom / Top		
Resolution (bits)	14	12	8	14	12	8	14	12	8	14	12	8	14	12	8	14	12	8
X (counts)	0	0	0	+1024	+256	+16	0	0	0	-1024	-256	-16	0	0	0	0	0	0
Y (counts)	-1024	-256	-16	0	0	0	+1024	+256	+16	0	0	0	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	0	0	0	0	+1024	+256	+16	-1024	-256	-16
X-Polarity	**0**			**+**			**0**			**-**			**0**			**0**		
Y-Polarity	**-**			**0**			**+**			**0**			**0**			**0**		
Z-Polarity	**0**			**0**			**0**			**0**			**+**			**-**		

(1g)

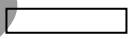
Earth's Surface

Notes:

1. This is applicable for 14-bit mode only in High Resolution mode

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0, EN16G=1 (±16g)
GSEL1=0, GSEL0=1, EN16G=1 (±16g)
GSEL1=1, GSEL0=0, EN16G=1 (±16g)
GSEL1=1, GSEL0=1, EN16G=1 (±16g)[1]

Position	1			2			3			4			5			6		
Diagram													Top  Bottom			Bottom  Top		
Resolution (bits)	14	12	8	14	12	8	14	12	8	14	12	8	14	12	8	14	12	8
X (counts)	0	0	0	+512	+128	+8	0	0	0	-512	-128	-8	0	0	0	0	0	0
Y (counts)	-512	-128	-8	0	0	0	+512	+128	+8	0	0	0	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	0	0	0	0	+512	+128	+8	-512	-128	-8
X-Polarity	**0**			**+**			**0**			**-**			**0**			**0**		
Y-Polarity	**-**			**0**			**+**			**0**			**0**			**0**		
Z-Polarity	**0**			**0**			**0**			**0**			**+**			**-**		

(1g)

Earth's Surface

Notes:

1. This is applicable for 14-bit mode only in High Resolution mode

Digital Interface

The Kionix KX003 digital accelerometer has the ability to communicate on the I²C digital serial interface bus. This allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers.

The serial interface terms and descriptions as indicated in Table 5 will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 5: Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KX003 has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KX003 always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held LOW by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are HIGH.

The I²C interface is compliant with high-speed mode, fast mode and standard mode I²C standards.

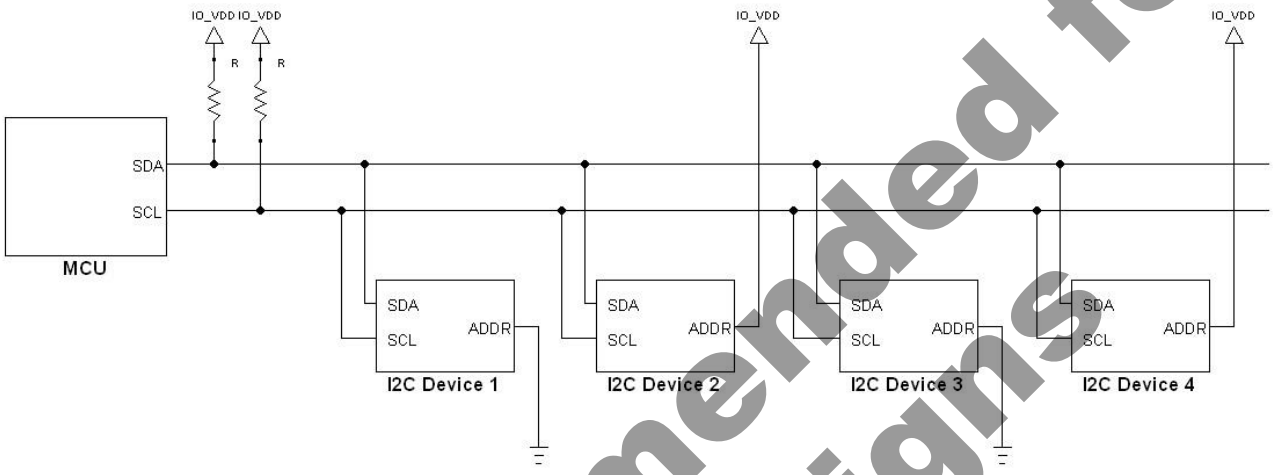
I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The Slave Address associated with the KX003 is 00011YX, where the user programmable bit X, is determined by the assignment of ADDR pin to GND or IO_VDD. Also, the factory programmable bit Y is set at the factory. For KX003-1077, the factory programmable bit Y is fixed to 1 (contact your Kionix sales representative for list of available devices). Table 6 lists possible I²C addresses for KX003-1077. It is possible to have up to four accelerometers on a shared I²C bus as shown in Figure 3 (i.e. two KX003-1077 accelerometers and two additional accelerometers with the factory programmable bit Y set to 0).

									Y	X	
Description	**Address Pad**	**7-bit Address**	**Address**	**<7>**	**<6>**	**<5>**	**<4>**	**<3>**	**<2>**	**<1>**	**<0>**
I2C Wr	GND	0x0E	0x1C	0	0	0	1	1	1	0	0
I2C Rd	GND	0x0E	0x1D	0	0	0	1	1	1	0	1
I2C Wr	IO_VDD	0x0F	0x1E	0	0	0	1	1	1	1	0
I2C Rd	IO_VDD	0x0F	0x1F	0	0	0	1	1	1	1	1

Table 6: I²C Slave Addresses for KX003-1077

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line LOW so that it remains stable LOW during the HIGH period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from LOW to HIGH while SCL is HIGH. The I²C bus is now free. Note that if the KX003 is accessed through I²C protocol before the startup is finished a NACK signal is sent.



I²C Device	Part Number	ADDR Pin	Slave Address	Bit Y (Bit 1 in 7-bit address)
1	KX003-1077	GND	0x0E	Factory Set to 1
2	KX003-1077	IO_VDD	0x0F	Factory Set to 1
3	*KXMMM	GND	0x0C	Factory Set to 0
4	*KXMMM	IO_VDD	0x0D	Factory Set to 0

* KXMMM – contact Kionix sales representative for list of compatible devices

Figure 3: Multiple KX003 Accelerometers on a Shared I²C Bus

Writing to an 8-bit Register

Upon power up, the Master must write to the KX003's control registers to set its operational mode. Therefore, when writing to a control register on the I²C bus, as shown Sequence 1 below, the following protocol must be observed: After a start condition, SAD+W transmission, and the KX003 ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KX003 to which 8-bit register the Master will be writing the data. Since this is I²C mode, the MSB of the RA command should always be zero (0). The KX003 acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KX003 acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KX003 is now stored in the appropriate register. The KX003 automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

****Note**** If a STOP condition is sent on the least significant bit of write data or the following master acknowledge cycle, the last write operation is not guaranteed and it may alter the content of the affected registers.

Reading from an 8-bit Register

When reading data from a KX003 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KX003 acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KX003 again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KX003 with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data but transmits a stop condition to end the data transfer. Note that the KX003 automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4. The 8-bit register data is transmitted using a left-most format, first bit shifted/clocked out being the MSB bit. If a receiver cannot transmit or receive another complete byte of data until it has performed some other function, it can hold SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases SCL.

****Note**** Accelerometer's output data should be read in a single transaction using the auto-increment feature to prevent output data from being updated prior to intended completion of the read transaction.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I²C bus and how the Master and Slave interact during these transfers. Table 7 defines the I²C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 7: I²C Terms

Sequence 1: The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2: The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3: The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4: The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

HS-mode

To enter the 3.4MHz high speed mode of communication, the device must receive the following sequence of conditions from the master: a Start condition followed by a Master code (00001XXX) and a Master Non-acknowledge. Once recognized, the device switches to HS-mode communication. Read/write data transfers then proceed as described in the sequences above. Devices return to the FS-mode after a STOP occurrence on the bus.

Sequence 5: HS-mode data transfer of the Master writing multiple bytes to the Slave.

Speed	FS-mode			HS-mode									FS-mode
Master	S	M-code	NACK	Sr	SAD + W		RA		DATA		P		
Slave						ACK		ACK		ACK			

n bytes + ack.

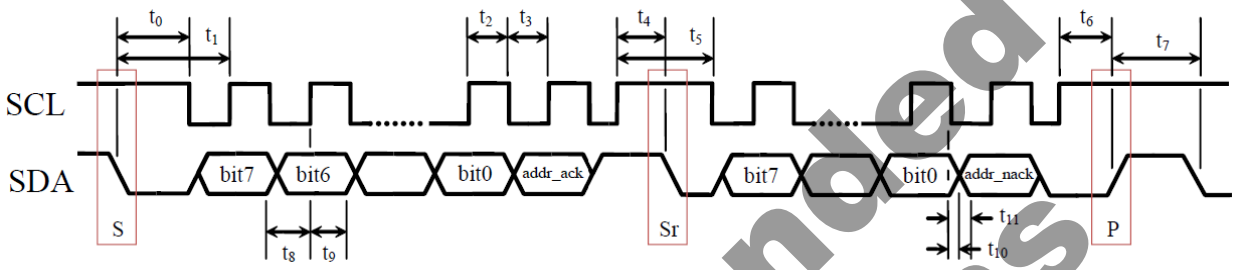
Sequence 6: HS-mode data transfer of the Master receiving multiple bytes of data from the Slave.

Speed	FS-mode			HS-mode				
Master	S	M-code	NACK	Sr	SAD + W		RA	
Slave						ACK		ACK

Speed	HS-mode								FS-mode
Master	Sr	SAD + R					NACK	P	
Slave			ACK	DATA	ACK	DATA			

(n-1) bytes + ack.

I²C Timing Diagram



Number	Description	MIN	MAX	Units
t_0	SDA LOW to SCL LOW transition (Start event)	50	-	ns
t_1	SDA LOW to first SCL rising edge	100	-	ns
t_2	SCL pulse width: HIGH	100	-	ns
t_3	SCL pulse width: LOW	100	-	ns
t_4	SCL HIGH before SDA falling edge (Start Repeated)	50	-	ns
t_5	SCL pulse width: HIGH during a S/Sr/P event	100	-	ns
t_6	SCL HIGH before SDA rising edge (Stop)	50	-	ns
t_7	SDA pulse width: HIGH	25	-	ns
t_8	SDA valid to SCL rising edge	50	-	ns
t_9	SCL rising edge to SDA invalid	50	-	ns
t_{10}	SCL falling edge to SDA valid (when slave is	-	100	ns
t_{11}	SCL falling edge to SDA invalid (when slave is	0	-	ns
Note	Recommended I²C CLK	2.5	-	µs

Table 8: I²C Timing (Fast Mode)

Embedded Registers

The KX003 has 20 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and describes bit functions of each register.

Register Name	Type (R/W)	Register Address (Hex)
Kionix Reserved	-	0x00 – 0x05
XOUT_L	R	0x06
XOUT_H	R	0x07
YOUT_L	R	0x08
YOUT_H	R	0x09
ZOUT_L	R	0x0A
ZOUT_H	R	0x0B
DCST_RESP	R	0x0C
Kionix Reserved	-	0x0D – 0x0E
WHO_AM_I	R	0x0F
Kionix Reserved	-	0x10 – 0 x15
INT_SOURCE1	R	0x16
INT_SOURCE2	R	0x17
STATUS_REG	R	0x18
Kionix Reserved	-	0x19
INT_REL	R	0x1A
CTRL_REG1*	R/W	0x1B
Kionix Reserved	-	0x1C
CTRL_REG2*	R/W	0x1D
INT_CTRL_REG1*	R/W	0x1E
INT_CTRL_REG2*	R/W	0x1F
Kionix Reserved	-	0x20
DATA_CTRL_REG*	R/W	0x21
Kionix Reserved	-	0x22 – 0x28
WAKEUP_COUNTER*	R/W	0x29
NA_COUNTER*	R/W	0x2A
Kionix Reserved	-	0x2B – 0x39
SELF_TEST*	W	0x3A
Kionix Reserved	-	0x3B – 0x69
WAKEUP_THRESHOLD_H*	R/W	0x6A
WAKEUP_THRESHOLD_L*	R/W	0x6B

Table 9: Register Map

* Note: When changing the contents of these registers, the PC1 bit in CTRL_REG1 must first be set to “0”

Register Descriptions

Accelerometer Outputs

These registers contain up to 14-bits of valid acceleration data for each. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Table 10 below. The register acceleration output binary data is represented in 2's complement format. For example, if N = 14 bits, then the Counts range is from -8192 to 8191, if N = 12 bits, then the Counts range is from -2048 to 2047, and if N = 8 bits, then the Counts range is from -128 to 127.

14-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = ±2g	Range = ±4g	Range = ±8g	Range = ±16g
00011111111111	8191	Not available	Not available	+7.999g	+15.998g
00011111111110	8190	Not available	Not available	+7.998g	+15.996g
…	…	…	…	…	…
00000000000001	1	Not available	Not available	+0.00098g	+0.00195g
00000000000000	0	Not available	Not available	0.000g	0.000g
11111111111111	-1	Not available	Not available	-0.00098g	-0.00195g
…	…	…	…	…	…
11100000000001	-8191	Not available	Not available	-7.999g	-15.998g
11100000000000	-8192	Not available	Not available	-8.000g	-16.000g

12-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = ±2g	Range = ±4g	Range = ±8g	Range = ±16g
0111 1111 1111	2047	+1.999g	+3.998g	+7.996g	+15.992g
0111 1111 1110	2046	+1.998g	+3.996g	+7.992g	+15.984g
…	…	…	…	…	…
0000 0000 0001	1	+0.001g	+0.002g	+0.0039g	+0.0078g
0000 0000 0000	0	0.000g	0.000g	0.0000g	0.0000g
1111 1111 1111	-1	-0.001g	-0.002g	-0.0039g	-0.0078g
…	…	…	…	…	…
1000 0000 0001	-2047	-1.999g	-3.998g	-7.996g	-15.992g
1000 0000 0000	-2048	-2.000g	-4.000g	-8.000g	-16.000g

8-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = ±2g	Range = ±4g	Range = ±8g	Range = ±16g
0111 1111	127	+1.984g	+3.969g	+7.938g	+15.875g
0111 1110	126	+1.969g	+3.938g	+7.875g	+15.75g
…	…	…	…	…	…
0000 0001	1	+0.016g	+0.031g	+0.0625g	+0.125g
0000 0000	0	0.000g	0.000g	0.000g	0.000g
1111 1111	-1	-0.016g	-0.031g	-0.0625g	-0.125g
…	…	…	…	…	…
1000 0001	-127	-1.984g	-3.969g	-7.938g	-15.875g
1000 0000	-128	-2.000g	-4.000g	-8.000g	-16.000g

Table 10: Acceleration (g) Calculation

XOUT_L

X-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R	Resolution
XOUTD5	XOUTD4	XOUTD3	XOUTD2	XOUTD1	XOUTD0	X	X	14-bit
XOUTD3	XOUTD2	XOUTD1	XOUTD0	X	X	X	X	12-bit
X	X	X	X	X	X	X	X	8-bit
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					Address: 0x06			

XOUT_H

X-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R	Resolution
XOUTD13	XOUTD12	XOUTD11	XOUTD10	XOUTD9	XOUTD8	XOUTD7	XOUTD6	14-bit
XOUTD11	XOUTD10	XOUTD9	XOUTD8	XOUTD7	XOUTD6	XOUTD5	XOUTD4	12-bit
XOUTD7	XOUTD6	XOUTD5	XOUTD4	XOUTD3	XOUTD2	XOUTD1	XOUTD0	8-bit
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					Address: 0x07			

YOUT_L

Y-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R	Resolution
YOUTD5	YOUTD4	YOUTD3	YOUTD2	YOUTD1	YOUTD0	Y	Y	14-bit
YOUTD3	YOUTD2	YOUTD1	YOUTD0	X	X	X	X	12-bit
X	X	X	X	X	X	X	X	8-bit
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					Address: 0x08			

YOUT_H

Y-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R	Resolution
YOUTD13	YOUTD12	YOUTD11	YOUTD10	YOUTD9	YOUTD8	YOUTD7	YOUTD6	14-bit
YOUTD11	YOUTD10	YOUTD9	YOUTD8	YOUTD7	YOUTD6	YOUTD5	YOUTD4	12-bit
YOUTD7	YOUTD6	YOUTD5	YOUTD4	YOUTD3	YOUTD2	YOUTD1	YOUTD0	8-bit
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					Address: 0x09			

ZOUT_L

Z-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R	Resolution
ZOUTD5	ZOUTD4	ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	Y	Y	14-bit
ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	X	X	X	X	12-bit
X	X	X	X	X	X	X	X	8-bit
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					Address: 0x0A			

ZOUT_H

Z-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R	Resolution
ZOUTD13	ZOUTD12	ZOUTD11	ZOUTD10	ZOUTD9	ZOUTD8	ZOUTD7	ZOUTD6	14-bit
ZOUTD11	ZOUTD10	ZOUTD9	ZOUTD8	ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4	12-bit
ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4	ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	8-bit
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
					Address: 0x0B			

DCST_RESP

This register can be used to verify proper integrated circuit functionality. It always has a byte value of 0x55 unless the DCST bit in CTRL_REG2 is set. At that point this value is set to 0xAA. The byte value is returned to 0x55 after reading this register.

R	R	R	R	R	R	R	R	
DCSTR7	DCSTR6	DCSTR5	DCSTR4	DCSTR3	DCSTR2	DCSTR1	DCSTR0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01010101
					Address: 0x0C			

WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x3F.

R	R	R	R	R	R	R	R	
WIA7	WIA6	WIA5	WIA4	WIA3	WIA2	WIA1	WIA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
					Address: 0x0F			

Interrupt Source Registers

These two registers report interrupt state changes. This data is updated when a new interrupt event occurs and each application's result is latched until the interrupt release register is read. The programmable interrupt engine can be configured to report data in an unlatched manner via the interrupt control registers.

INT_SOURCE1

This register reports which function caused an interrupt. Reading from the interrupt release register *(INT_REL)* will clear the entire contents of this register.

R	R	R	R	R	R	R	R
0	0	0	DRDY	0	0	WUFS	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Address: 0x16		

DRDY *– indicates that new acceleration data (0x06 to 0x0B) is available. This bit is cleared when acceleration data is read or the interrupt release register (INT_REL) is read.*
0 = New acceleration data not available
1 = New acceleration data available

WUFS *– Wake-up has occurred. This bit is cleared when the interrupt source latch register (INT_REL) is read (see Table 15 for details).*
0 = No motion
1 = Motion has activated the interrupt

INT_SOURCE2

This register reports the axis and direction of detected motion per Table 11. This register is cleared when the interrupt source latch register *(INT_REL)* is read *(see Table 15 for details).*

R	R	R	R	R	R	R	R
0	0	XNWU	XPWU	YNWU	YPWU	ZNWU	ZPWU
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Address: 0x17		

Bit	Description
XNWU	X Negative (X-) Reported
XPWU	X Positive (X+) Reported
YNWU	Y Negative (Y-) Reported
YPWU	Y Positive (Y+) Reported
ZNWU	Z Negative (Z-) Reported
ZPWU	Z Positive (Z+) Reported

Table 11: Motion Reporting

STATUS_REG

This register reports the status of the interrupt.

R	R	R	R	R	R	R	R
0	0	0	INT	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Address: 0x18		

INT *– reports the combined (OR) interrupt information of DRDY and WUFS in the interrupt source register (INT_SOURCE1). This bit is cleared when acceleration data is read or the interrupt release register (INT_REL) is read (see Table 15 for details).*
0 = no interrupt event
1 = interrupt event has occurred

INT_REL

Latched interrupt source information (*INT_SOURCE1* and *INT_SOURCE2*) is cleared and physical interrupt latched pin (INT) is changed to its inactive state when this register is read (see Table 15 for details).

R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					Address: 0x1A		

CTRL_REG1

Read/write control register that controls the main feature set.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PC1	RES	DRDYE	GSEL1	GSEL0	EN16G	WUFE	0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x1B			

PC1 *– controls the operating mode of the KX003.*
0 = stand-by mode
1 = operating mode

RES *– determines the performance mode of the KX003. Note that to change the value of this bit, the PC1 bit must first be set to "0".*
0 = Low Power, 8-bit valid. Only available for ODR ≤ 200 Hz. Bandwidth (Hz) = 800.
1 = High Resolution, 12-bit or 14-bit valid. Bandwidth (Hz) = ODR/2

DRDYE *– enables the reporting of the availability of new acceleration data as an interrupt. Note that to change the value of this bit, the PC1 bit must first be set to "0".*
0 = availability of new acceleration data is not reflected as an interrupt
1 = availability of new acceleration data is reflected as an interrupt

GSEL1, GSEL0, EN16G *– selects the acceleration range of the accelerometer outputs per Table 12. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

GSEL1	GSEL0	EN16G	Range
0	0	0	±2g
0	1	0	±4g
1	0	0	±8g
1	1	0	±8g[1]
0	0	1	±16g
0	1	1	±16g
1	0	1	±16g
1	1	1	±16g[1]

Table 12: Selected Acceleration Range

WUFE *– enables the Wake-Up (motion detect) function. Note that to change the value of this bit, the PC1 bit must first be set to "0".*
0 = Wake-Up function disabled
1 = Wake-Up function enabled

[1] This is a 14-bit mode available only in High Resolution mode and only for Registers 0x06h-0x0Bh

CTRL_REG2

Read/write control register that provides more feature set control. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
SRST	Reserved	Reserved	DCST	Reserved	OWUFA	OWUFB	OWUFC	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x1D			

SRST *– initiates software reset, which performs the RAM reboot routine. This bit will remain 1 until the RAM reboot routine is finished. Please refer to Technical Note TN017 Power-On Procedure for more information on software reset.*

SRST = 0 – no action
SRST = 1 – start RAM reboot routine

Note: Setting SRST = 1 will NOT result in an ACK, since the part immediately enters the RAM reboot routine. NACK may be used to confirm this command.

Reserved – Care must be taken to not overwrite Reset Value of reserved bit(s)

DCST *– initiates the digital communication self-test function.*
DCST = 0 – no action
DCST = 1 – sets DCST_RESP register to 0xAA and when DCST_RESP is read, sets this bit to 0 and sets DCST_RESP to 0x55

OWUFA, OWUFB, OWUFC *– sets the Output Data Rate for the Wake-Up function (motion detection) per Table 13.*

OWUFA	OWUFB	OWUFC	Output Data Rate
0	0	0	0.781Hz
0	0	1	1.563Hz
0	1	0	3.125Hz
0	1	1	6.25Hz
1	0	0	12.5Hz
1	0	1	25Hz
1	1	0	50Hz
1	1	1	100Hz

Table 13: Output Data Rate for Wake-Up Function

INT_CTRL_REG1

This register controls the settings for the physical interrupt pin (INT). Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	IEN	IEA	IEL	0	STPOL	0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00010000
					Address: 0x1E			

IEN *– enables/disables the physical interrupt pin (INT)*
IEN = 0 – physical interrupt pin (INT) is disabled
IEN = 1 – physical interrupt pin (INT) is enabled

IEA *– sets the polarity of the physical interrupt pin (INT)*
IEA = 0 – polarity of the physical interrupt pin (INT) is active LOW
IEA = 1 – polarity of the physical interrupt pin (INT) is active HIGH

IEL *– sets the response of the physical interrupt pin (INT) (see Table 15 for details)*
IEL = 0 – the physical interrupt pin (INT) latches until it is cleared by reading INT_REL
IEL = 1 – the physical interrupt pin (INT) will transmit one pulse with a period of 0.03 - 0.05ms

STPOL *– Self-test polarity.*
STPOL = 0 – negative polarity (unsupported)
STPOL = 1 – positive polarity (supported)

INT_CTRL_REG2

This register controls which axis and direction of detected motion can cause an interrupt. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
ULMODE	0	XNWUE	XPWUE	YNWUE	YPWUE	ZNWUE	ZPWUE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
					Address: 0x1F			

ULMODE *– Unlatched mode motion interrupt (see Table 15 for details)*
ULMOD = 0 – Unlatched mode is disabled
ULMOD = 1 – Unlatched mode is enabled

XNWU *– x negative (x-): 0 = disabled, 1 = enabled*
XPWU *– x positive (x+): 0 = disabled, 1 = enabled*
YNWU *– y negative (y-): 0 = disabled, 1 = enabled*
YPWU *– y positive (y+): 0 = disabled, 1 = enabled*
ZNWU *– z negative (z-): 0 = disabled, 1 = enabled*
ZPWU *– z positive (z+): 0 = disabled, 1 = enabled*

DATA_CTRL_REG

Read/write control register that configures the acceleration outputs. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	OSAA	OSAB	OSAC	OSAD	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000010
					Address: 0x21			

OSAA, OSAB, OSAC, OSAD *– sets the output data rate (ODR) for the low-pass filtered acceleration outputs per Table 14.*

OSAA	OSAB	OSAC	OSAD	Output Data Rate	LPF Roll-Off
1	0	0	0	0.781Hz	0.3905Hz
1	0	0	1	1.563Hz	0.781Hz
1	0	1	0	3.125Hz	1.563Hz
1	0	1	1	6.25Hz	3.125Hz
0	0	0	0	12.5Hz	6.25Hz
0	0	0	1	25Hz	12.5Hz
0	0	1	0	50Hz	25Hz
0	0	1	1	100Hz	50Hz
0	1	0	0	200Hz	100Hz
0	1	0	1	400Hz	200Hz
0	1	1	0	800Hz	400Hz
0	1	1	1	1600Hz	800Hz

Table 14: Acceleration Output Data Rate (ODR) and LPF Roll-Off

Note: Output Data Rates ≥ 400Hz will force device into High Resolution mode

WAKEUP_COUNTER

This register sets the time motion must be present before a wake-up interrupt is set. Every count is calculated as 1/OWUF delay period. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to “0”. Valid entries are from 1 to 255, excluding the zero value.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
WUFC7	WUFC6	WUFC5	WUFC4	WUFC3	WUFC2	WUFC1	WUFC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x29			

NA_COUNTER

This register sets the non-activity time required before another wake-up interrupt can be set. Every count is calculated as 1/OWUF delay period. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to “0”. Valid entries are from 1 to 255, excluding the zero value.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
NAFC7	NAFC6	NAFC5	NAFC4	NAFC3	NAFC2	NAFC1	NAFC0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x2A			

SELF_TEST

When 0xCA is written to this register, the MEMS self-test function is enabled. Electrostatic-actuation of the accelerometer, results in a DC shift of the X, Y and Z axes outputs. Writing 0x00 to this register will return the accelerometer to normal operation. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to “0”.

W	W	W	W	W	W	W	W	
0	0	0	0	0	0	0	0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					Address: 0x3A			

WAKEUP_THRESHOLD

This register sets the threshold for wake-up (motion detect) interrupt is set. Data bytes are WAKEUP_THRESHOLD_H, WAKEUP_THRESHOLD_L. The KX003 will be shipped from the factory with this value set to correspond to a change in acceleration of 0.5g. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to “0”.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Address	Register	Reset Value
WUTH11	WUTH10	WUTH9	WUTH8	WUTH7	WUTH6	WUTH5	WUTH4	0x6A	WAKEUP_THRESHOLD_H	00001000
WUTH3	WUTH2	WUTH1	WUTH0	0	0	0	0	0x6B	WAKEUP_THRESHOLD_L	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0			

Embedded Applications

Motion Interrupt

Feature Description

KX003 features a threshold interrupts triggered by the internal digital wake-up engine. This engine allows the KX003 to trigger interrupt when accelerometer activity exceeds a threshold window (Wake-Up event). Note that this function only generates an interrupt and doesn't trigger any changes to the part configuration (e.g. power mode, ODR, etc.).

Enabling / Disabling

The Wake-up detection can be enabled/disabled using WUFE bit in CTRL_REG1 register and the direction of motion detection can be set for any axis in INT_CTRL_REG2 register. The sampling rate for the Wake-Up function is independent of the output data rate of the KX003 and is set by OWUF bits in CTRL_REG2.

Latched / Pulsed / Unlatched Interrupt Modes

The wake-up event can be programmed to be reported on physical interrupt pin INT. There are three supported modes that are configured using IEL bit in CTRL_REG2 register and ULMODE bit in INT_CTRL_REG2 register. The modes are Latched, Pulsed, and Unlatched. Depending on the interrupt mode, the behavior of the external interrupt pin INT, the wake-up function status bit WUFS in INT_SOURCE1 register, the interrupt report bit INT in STATUS_REG, and corresponding motion direction detection bit (XNWU / XPWU / YNWU / YPWU / ZNWU / ZPWU) in the INT_SOURCE2 registers will be different.

ULMODE	IEL	Interrupt Mode	External INT Pin	INT bit and WUFS bit	XNWU / XPWU / YNWU / YPWU / ZNWU / ZPWU
0	0	Latched	INT pin latches until INT_REL is read	INT and WUFS bit are 1 until INT_REL is read	The corresponding motion directions bit is set to 1 until INT_REL is read
0	1	Pulsed	INT pin is pulsed @ 0.03-0.05 ms	INT and WUFS bit are 1 until INT_REL is read	The corresponding motion directions bit is set to 1 until INT_REL is read
1	0	Unlatched	INT pin is pulsed and automatically cleared after 1/OWUF	INT bit and WUFS bit are 1 until auto-cleared after 1/OWUF	The corresponding motion directions bit is set to 1 until INT_REL is read
1	1	Pulsed	INT pin is pulsed @ 0.03-0.05 ms	INT bit and WUFS bit are 1 until auto-cleared after 1/OWUF	The corresponding motion directions bit is set to 1 until INT_REL is read

Table 15: Latched / Pulsed / Unlatched Interrupt Modes Configuration

Debounce Counter

The Wake-Up digital engine has an internal debounce counter to qualify motion status detection. The debounce counter function can be set using WUFC<7:0> bits in WAKEUP_COUNTER register. Note that each Wake-Up Function Counter (WUFC) count qualifies 1 (one) user-defined Wake-Up Function ODR period as set by OWUF<2:0> bits in CTRL_REG2 register. Equation 1 shows how to calculate the WAKEUP_COUNTER register value for a desired wake-up delay time.

WAKEUP_COUNTER (counts) = Wake-Up Delay Time (sec) x Wake-Up Function ODR (Hz)

Equation 1: Wake-Up Delay Time Calculations

Non-Activity Counter

The Non-Activity register sets the non-activity time required before another wake-up interrupt will be reported. The non-activity counter function can be set using NAFC7<7:0> bits in NA_COUNTER register. Note that each Non-Activity Function Counter (NAFC) count qualifies 1 (one) user-defined Wake-Up Function ODR period as set by OWUF<2:0> bits in CTRL_REG2 register. Equation 2 shows how to calculate the WAKEUP_COUNTER register value for a desired wake-up delay time.

NA_COUNTER (counts) = Non-Activity Time (sec) x Wake-Up Function ODR (Hz)

Equation 2: Non-Activity Counter Calculations

Threshold Resolution

The motion interrupt threshold values are set by WUTH<11:0> bits in the WAKEUP_THRESHOLD registers and are compared to the top 12 bits of the accelerometer 8g output value (regardless of GSEL<1:0> setting in CTRL_REG1 register). This results in threshold resolution of 256 counts/g or 3.9mg/count

Threshold Calculations

To calculate the desired wake-up threshold use Equation 3. Please note that the wake-up engine function is independent of the user selected g-range.

WAKEUP_THRESHOLD (counts) = Desired Threshold (g) x 256 *(counts/g)*

Equation 3: Wake-Up Threshold Calculations

Wake-Up Detection Example

The latched motion interrupt response algorithm works as following: while the part is in inactive state, the algorithm evaluates differential measurement between each new acceleration data point with the preceding one and evaluates it against the WAKEUP_THRESHOLD threshold. When the differential measurement is greater than WAKEUP_THRESHOLD threshold, the wakeup counter starts the count. Differential measurements are now calculated based on the difference between the current acceleration and the acceleration when the counter started. The part will report that motion has occurred at the end of the count assuming each differential measurement has remained above the threshold. If at any moment during the count the differential measurement falls below the threshold, the counter will stop the count and the part will remain in inactive state.

To illustrate how the algorithm works, consider the Figure 4 below that shows the latched response of the motion detection algorithm with WAKEUP_COUNTER set to 10 counts. Note how the difference between the acceleration sample marked in red and the one marked in green resulted in a differential measurement represented with orange bar being above the WAKEUP_THRESHOLD. At this point, the counter begins to count number of counts stored in WAKEUP_COUNTER register and the wakeup algorithm will evaluate the difference between each new acceleration measurement and the measurement marked in green that will remain a reference measurement for the duration of the counter count. At the end of the count, assuming all differential measurements were larger than WAKEUP_THRESHOLD, as is the case in the example showed in Figure 4, a motion event will be reported. Figure 4 below shows the latched response of the Wake-Up Function with WUF counter = 10 counts.

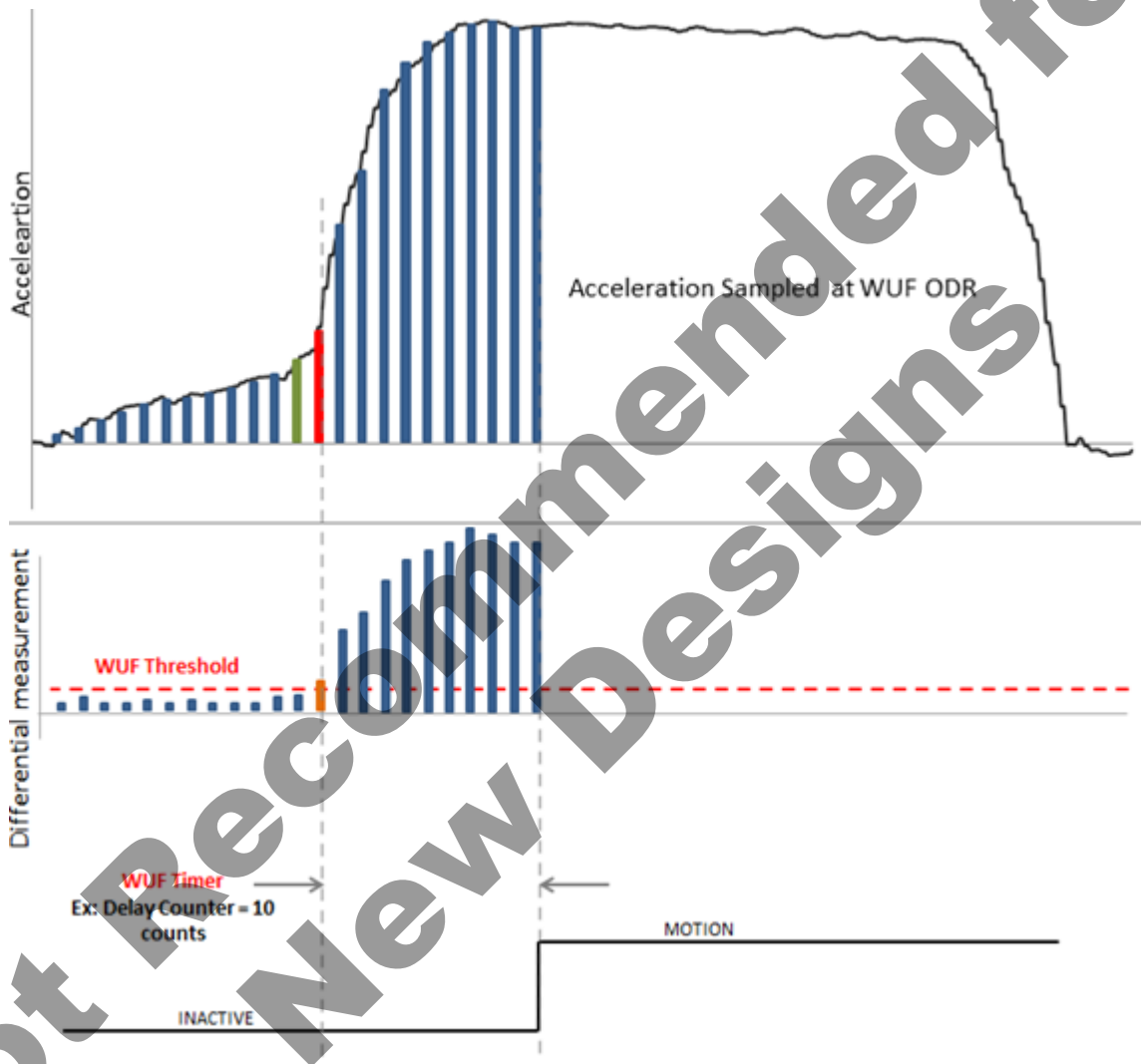


Figure 4: Latched Motion Interrupt Response

Revision History

Revision	Description	Date
1.0	Initial Release	24-May-2018
2.0	Removed Signal Bandwidth (-3dB) spec in Mechanical Specification. Updated I2C Operation section to add support for alternative I2C address. Updated Package Outline Drawing. Fixed Reg 0x6B name in Register Map (WAKEUP_THRESHOLD_L). Updated description of WUFS, INT, RES, SRST, IEL, ULMODE bits. Updated description of INT_SOURCE2, INT_REL, WAKEUP_THRESHOLD, SELF_TEST registers. Updated Embedded Wake-Up Function engine description.	05-Oct-2018

Appendix

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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