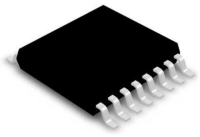
ADC1283

Datasheet

8 multiplexed channels, 50 ksps to 200 ksps, 12-bit SAR ADC

ADC1283



TSSOP-16

Maturity status link
ADC1283

Related products
ADC1281
ADC1282

Features

- 50 ksps to 200 ksps conversion rate
- 8-to-1-channel input MUX
- 2.7 V to 5.5 V digital I/Os supply voltage
- 2.7 V to 5.5 V analog supply voltage
- DNL (AVCC = DVCC = 5 V): +/- 0.9 LSB maximum
- INL (AVCC = DVCC = 5 V): +/- 1.2 LSB maximum
- Very low consumption: Pd = 3.2 mW typical @ 5 V supply
- Power-down mode
- Temperature range: -40 °C to 125 °C
- 4-wire SPI serial digital interface
- TSSOP-16 package

Applications

- Industrial process control
- Shunt resistor monitoring
- Data acquisition and instrumentation
- Test and measurement equipment
- Strain gauge sensing
- Telemetry

Description

The ADC1283 is a low-power, eight-channel pure CMOS 12-bit analog-to-digital converter specified for conversion from 50 ksps to 200 ksps, tested at 200 ksps (3.2 MHz clock frequency). The architecture is based on a successive-approximation register with an internal track-and-hold cell. The ADC1283 features 8 single-ended multiplexed inputs. The output serial data is straight binary and is SPI™ compatible.

The analog power supply operates from 2.7 V to 5.5 V. The digital power supply operates independently from analog supply from 2.7 V to 5.5 V. The power consumption at 5 V nominal supply is as low as 3.2 mW. The ADC1283 comes in a plastic TSSOP-16 package and can operate from -40 °C to +125 °C ambient temperature.

1 Block diagram and pin description

Figure 1. **Block diagram**

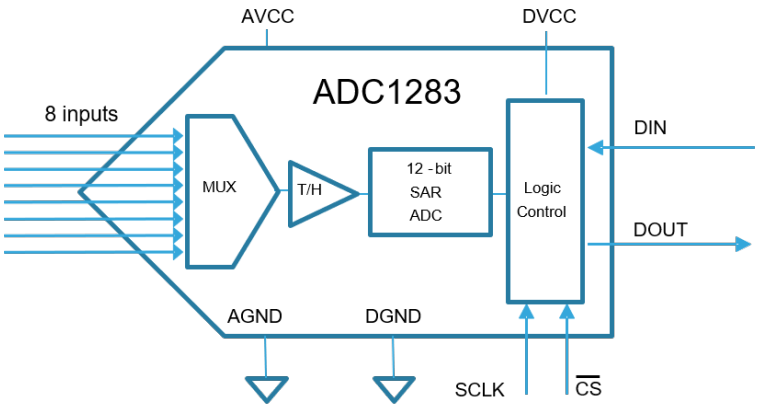


Figure 2. **Pin connection (top view)**

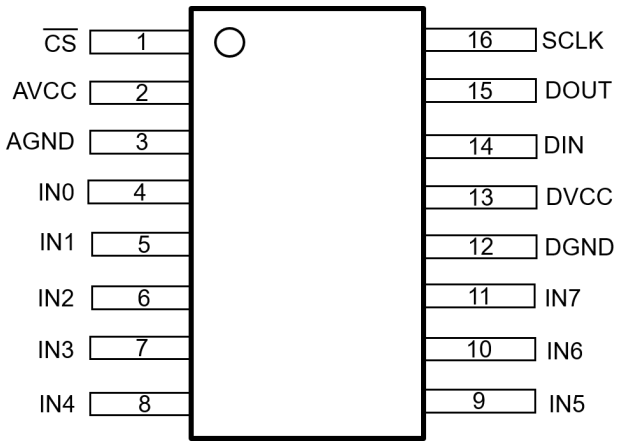


Table 1. **Pin description**

Pin n.	Pin name	Description
1	$\overline{CS}$	Chip select. Active low. Conversion starts on a falling edge of $\overline{CS}$
2	AVCC	Analog power supply. Used as reference voltage for inputs
3	AGND	Analog ground
4 - 11	IN0 – IN7	Single-ended analog inputs. Signals are referenced from 0 V to AVCC
12	DGND	Digital ground
13	DVCC	Digital power supply voltage
14	DIN	Digital data input. Used to address the control register
15	DOUT	Digital data output
16	SCLK	Clock input. Applied clock signal varies from 0.8 MHz to 3.2 MHz

2 Absolute maximum ratings and operating conditions

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
AVCC	Maximum analog supply voltage between AVCC and AGND	-0.3 to 7	V
DVCC	Maximum digital supply voltage between DVCC and DGND	-0.3 to 7	V
Tstg	Maximum storage temperature	-65 to 150	°C
Tj	Maximum Junction temperature	+150	°C
Rthja	Junction to ambient thermal resistance (for TSSOP-16)	95	°C/W
Rthjc	Junction to case thermal resistance (for TSSOP-16)	35	°C/W
Vi	Maximum applied voltage on any pin versus ground	-0.3 V to AVCC +0.3 V	V
Ii (1)	Maximum input current applied on any pin	±10	mA
ESD	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	1000	V

1. *When the input voltage at any pin exceeds the power supplies (that is VIN < AGND or VIN > AVCC or DVCC), the current at that pin should be limited to 10 mA. A limit of 2 pins can sustain such a condition, limiting the current to 20 mA for the whole device.*

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the devices. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating conditions. Exposure to the absolute maximum rating for extended periods may affect device reliability.

Table 3. Operating conditions

Symbol	Parameters	Min.	Unit
AVCC	Analog supply voltage	2.7 to 5.5	V
DVCC	Digital supply voltage	2.7 to 5.5	V
VINA	Analog input voltage	0 to AVCC	V
VIND	Digital input voltage	0 to DVCC	V
f_{SCLK}	Clock frequency	0.8 to 3.2	MHz
T	Ambient temperature range	-40 to +125	°C

Note: All voltages are related to GND = 0 V unless otherwise noted.

3 Electrical characteristics

Table 4. Electrical characteristics AGND = DGND = 0 V, f_{SCLK} = 3.2 MHz, f_{SAMPLE} = 200 ksps, C_L = 50 pF, Ta = 25 °C, all specifications T_{min} to T_{max} unless otherwise specified.

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
Static characteristics						
	Resolution with no missing codes	AVCC = DVCC = 2.7 V to 5.5 V			12	Bits
INL	Integral non-linearity (end point method)	AVCC = DVCC = 3.3 V	-1.2	±0.4	+1.2	LSB
		AVCC = DVCC = 5 V	-1.2	±0.4	+1.2	
DNL	Differential non-linearity	AVCC = DVCC = 3.3 V	-0.9	±0.4	+0.9	
		AVCC = DVCC = 5 V	-0.9	±0.4	+0.9	
VOFF	Offset error	AVCC = DVCC = 3.3 V	-2	±0.3	+2	
		AVCC = DVCC = 5 V	-2	±0.3	+2	
OEM	Offset error match	AVCC = DVCC = 3.3 V	-1.5	0	+1.5	
		AVCC = DVCC = 5 V	-1.5	0	+1.5	
FSE	Full scale error	AVCC = DVCC = 3.3 V	-2	±0.4	+2	
		AVCC = DVCC = 5 V	-2	±0.4	+2	
FSEM	Full scale error match	AVCC = DVCC = 3.3 V	-1.5	0	+1.5	
		AVCC = DVCC = 5 V	-1.5	0	+1.5	
Dynamic characteristics						
SINAD	Signal-to-noise plus distortion ratio (0 to Fs/2)	FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 3.3 V	69.2	73		dB
		FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 5 V	69.2	73		
SNR	Signal-to-noise ratio (0 to Fs/2)	FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 3.3 V	71	73		
		FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 5 V	71	73		
THD	Total harmonic distortion	FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 3.3 V		-88	-74	
		FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 5 V		-88	-74	
SFDR	Spurious-free dynamic range (0 to Fs/2)	FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 3.3 V	75	88		
		FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 5 V	75	89		
ENOB	Effective number of bits	FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 3.3 V	11.2	11.8		
		FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 5 V	11.2	11.8		
ISO	Channel-to-channel isolation	FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 3.3 V		90		dB
		FIN = 1.03 kHz, −0.02 dBFS AVCC = DVCC = 5 V		90		
IM2	2nd order intermodulation	FIN = 19.5 / 20.5 kHz, -0.02 dBFS AVCC = DVCC = 3.3 V		-99		dB
		FIN = 19.5 / 20.5 kHz, -0.02 dBFS AVCC = DVCC = 5 V		-99		

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
IM3	3rd order intermodulation	FIN = 19.5 / 20.5 kHz, -0.02 dBFS AVCC = DVCC = 3.3 V		-87		dB
		FIN = 19.5 / 20.5 kHz, -0.02 dBFS AVCC =^DVCC = 5 V		-88		
Analog input characteristics (AVCC = 2.7 V to 5.5 V)						
I_{DCL}	DC leakage current		-1	0.01	+1	µA
C_{INA}	Input capacitance	Track mode		33		pF
		Hold mode		4.5		pF
Digital input characteristics						
V_{IH}	Input high voltage	DVCC = 2.7 V to 5.5 V	0.7xDVCC			V
V_{IL}	Input low voltage	DVCC = 2.7 V to 5.5 V			0.3xDVCC	
V_{OH} (1)	Output high voltage	DVCC = 3.3 V, I_{source} = -1 mA	DVCC-0.5 V			V
		DVCC = 5 V, I_{source} = -1 mA	DVCC-0.5 V			
V_{OL} (1)	Output low voltage	DVCC = 3.3 V, I_{sink} = 1 mA			0.4	
		DVCC = 5 V, I_{sink} = 1 mA			0.4	
I_{IN}	Digital input current	V_{IN} = 0 V or DVCC	-1	0.01	1	µA
C_{IND}	Digital input capacitance	DVCC = 2.7 V to 5.5 V		3.5		pF
I_{OZH}, I_{OZL}	Hi-impedance output leakage current		-1	0.02	1	µA
C_{OUT}	Hi-impedance output capacitance			3.5		pF
Power supply characteristic						
I_{AVCC} + I_{DVCC}	Total supply current, normal mode (CS low)	AVCC = DVCC = 2.7 V to 5.5 V, f_S = 200 kSPS, F_{IN} = 40 kHz		0.64	0.8	mA
	Total supply current, shutdown mode (CS high)	AVCC = DVCC = 2.7 V to 5.5 V, f_S = 0, -40 °C < T < 85 °C		0.02	2	µA
		AVCC = DVCC = 2.7 V to 5.5 V, f_S = 0, 85 °C < T < 125 °C			10	
AC characteristics (AVCC = DVCC = 2.7 V to 5.5 V)						
f_S	Sample rate		50		200	ksps
$t_{CONVERT}$	Conversion (Hold) time				13	SCLK cycles
DC	SCLK duty cycle		40		60	%
t_{ACQ}	Acquisition (Track) time cycles	See Figure 4			3	SCLK cycles
	Throughput time	Acquisition time + Conversion time			16	SCLK cycles
t_{AD}	Aperture delay			4		ns
Timing specifications (AVCC = 2.7 V to 5.5 V) (1)(2)						
t_{CSH}	$\overline{CS}$ hold time after SCLK rising edge		10	0		ns
t_{CSS}	$\overline{CS}$ set-up time prior SCLK rising edge		10	4.5		ns
t_{EN}	$\overline{CS}$ falling edge to DOUT enabled			6	30	ns

Symbol	Parameters	Test conditions	Min.	Typ.	Max.	Unit
t_{DACC}	DOUT access time after SCLK falling edge			20	35	ns
t_{DHLD}	DOUT hold time after SCLK falling edge		7	13		ns
t_{DS}	DIN set-up time prior to SCLK rising edge		10			ns
t_{DH}	DIN hold time after SCLK rising edge		10			ns
t_{DIS}	$\overline{CS}$ rising edge to DOUT high-impedance	DOUT falling		12	20	ns
		DOUT rising		12	20	
t_{CH}	Min. SCLK high time			0.4 x t_{SCLK}		ns
t_{CL}	Min. SCLK low time			0.4 x t_{SCLK}		ns

1. *Datasheet minimum and maximum specification limits are specified by design, characterization or statistical analysis.*
2. *Timings are given with thresholds set to 50% of clock signals and 10% or 90% of data signals.*

4 Timing diagrams

Figure 3. **Operational timing diagram**

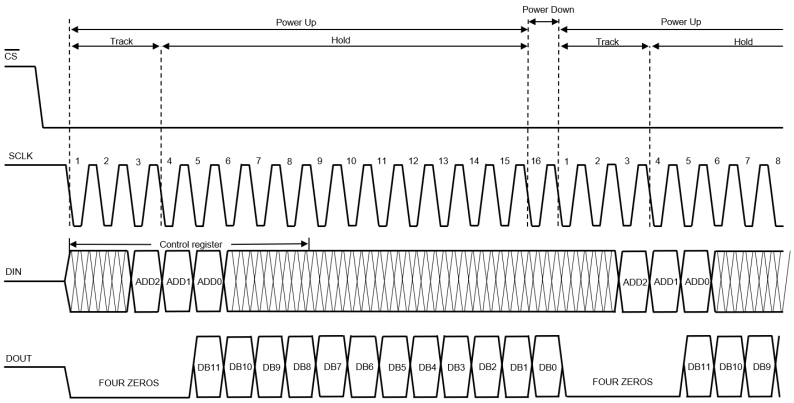


Figure 4. **Serial timing diagram**

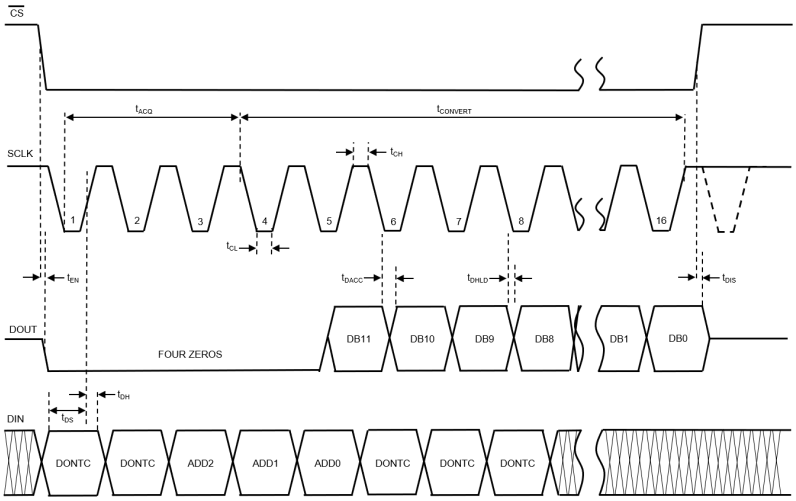
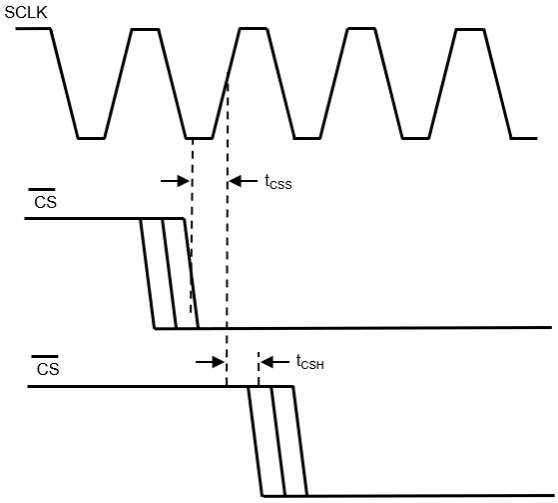


Figure 5. **SCLK and $\overline{CS}$ timing parameters**



5 Typical characteristics

T_A = 25 °C, f_{SAMPLE} = 200 ksps, f_{SCLK} = 3.2 MHz, F_{in} = 10 KHz unless otherwise stated.

Figure 6. DNL vs. output codes (AVCC = DVCC = 3 V)

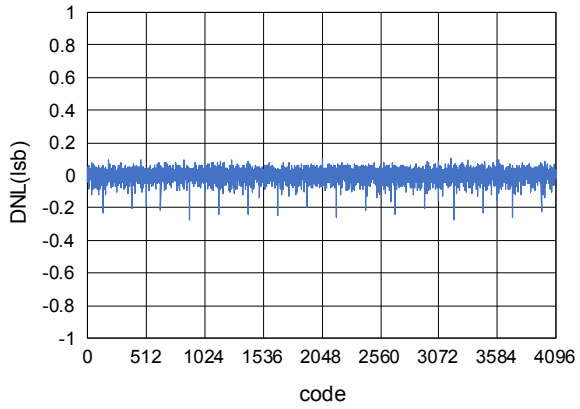


Figure 7. DNL vs. output codes (AVCC = DVCC = 5 V)

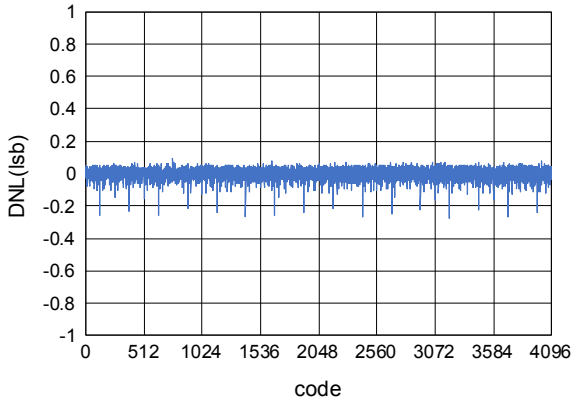


Figure 8. INL vs. output codes (AVCC = DVCC = 3 V)

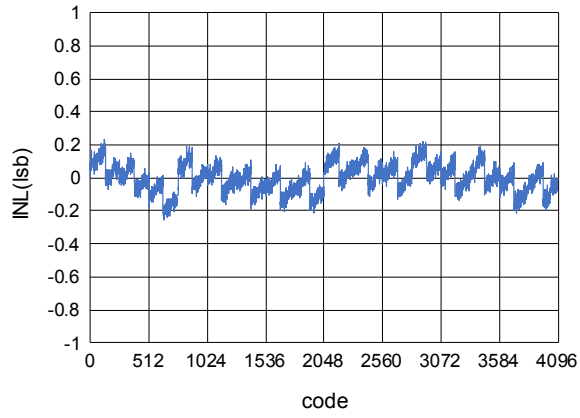


Figure 9. INL vs. output codes (AVCC = DVCC = 5 V)

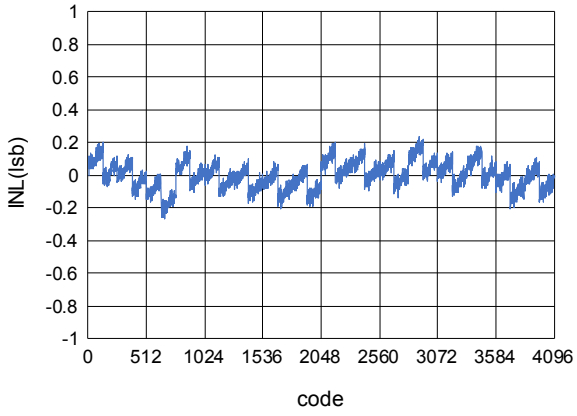


Figure 10. +/- DNL vs. AVCC = DVCC

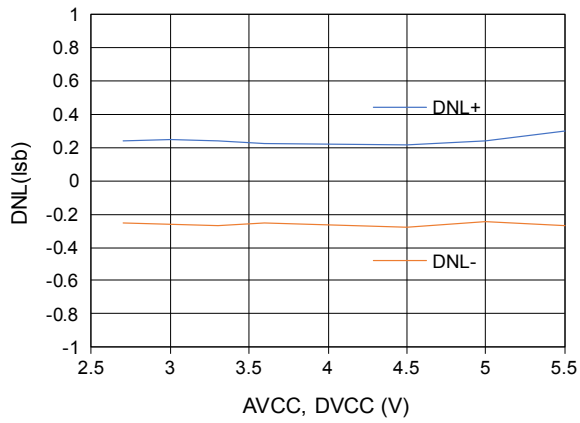


Figure 11. +/- INL vs. AVCC = DVCC

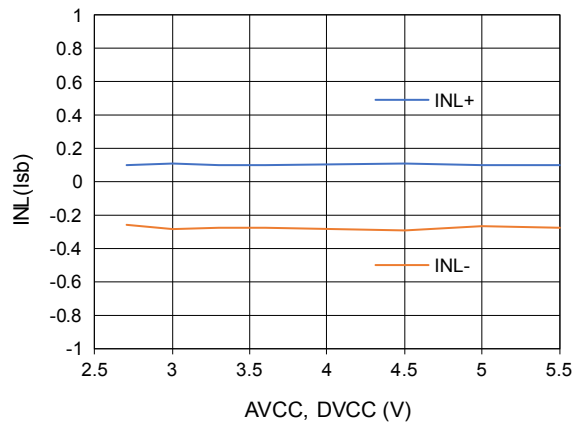


Figure 12. SNR vs. AVCC = DVCC

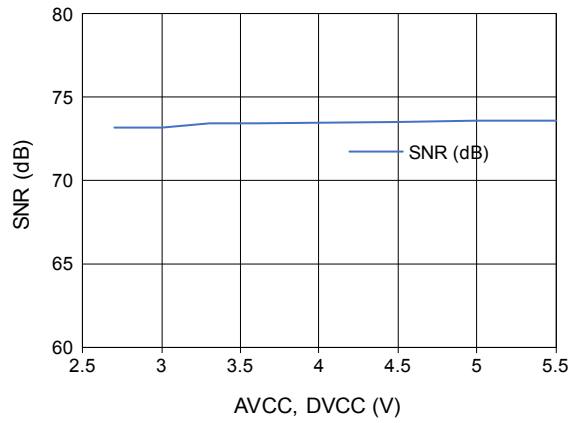


Figure 13. THD vs. AVCC = DVCC

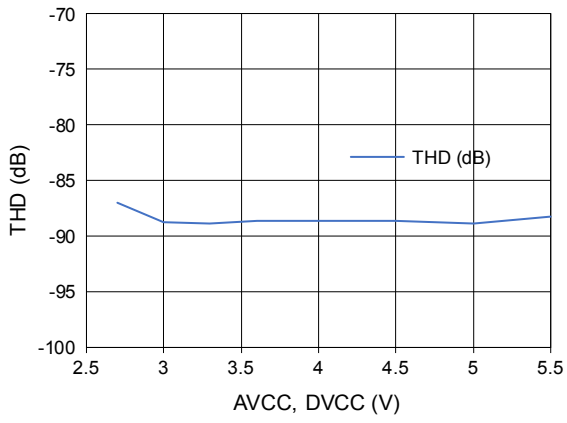


Figure 14. ENOB vs. AVCC = DVCC

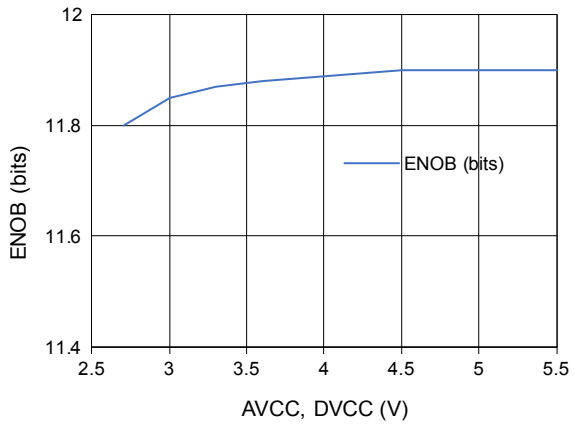


Figure 15. +/- DNL vs. DVCC with AVCC = 5 V

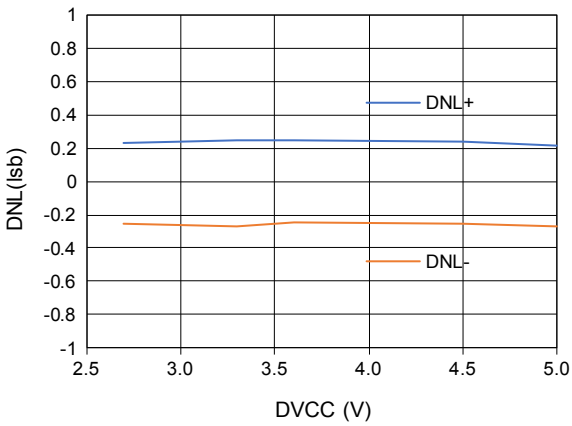


Figure 16. +/- INL vs. DVCC with AVCC = 5 V

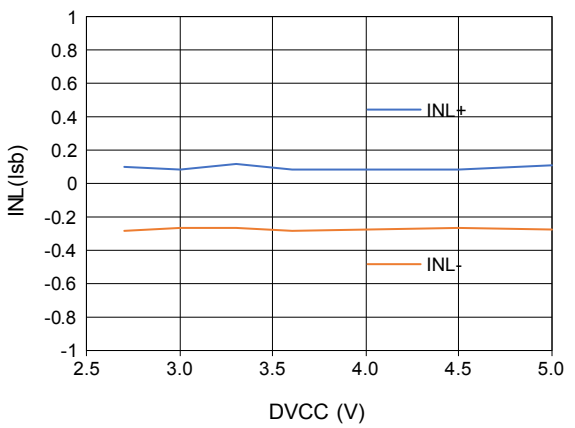


Figure 17. +/- DNL vs. SCLK duty cycle

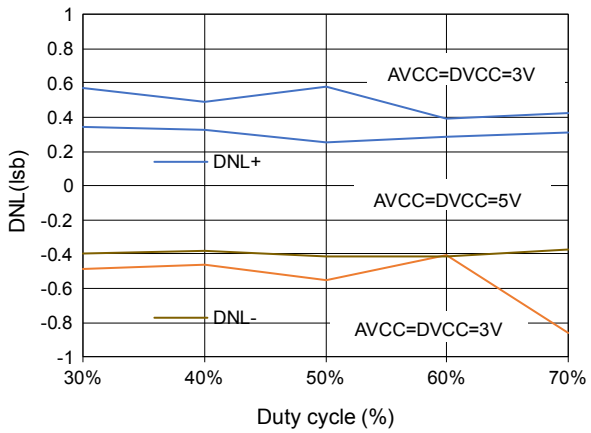


Figure 18. +/- INL vs. SCLK duty cycle

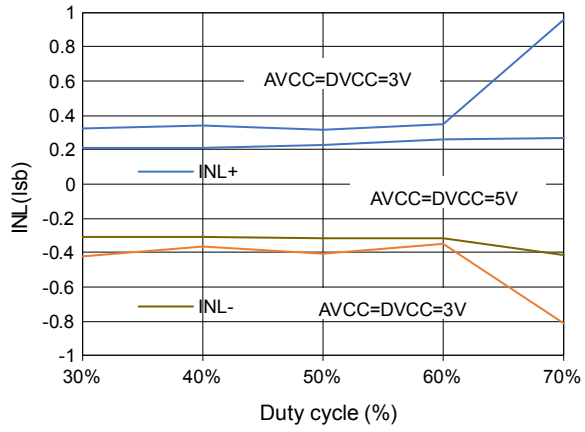


Figure 19. SNR vs. SCLK duty cycle

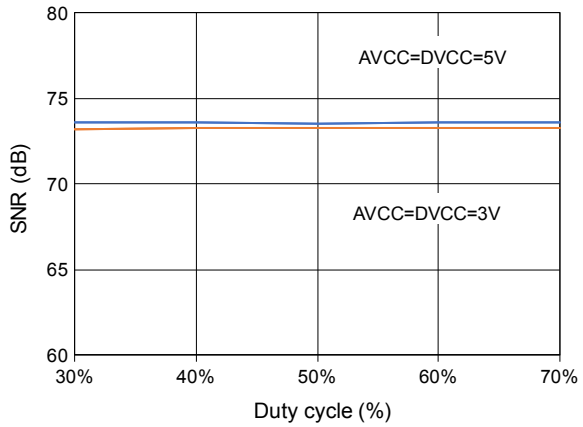


Figure 20. THD vs. SCLK duty cycle

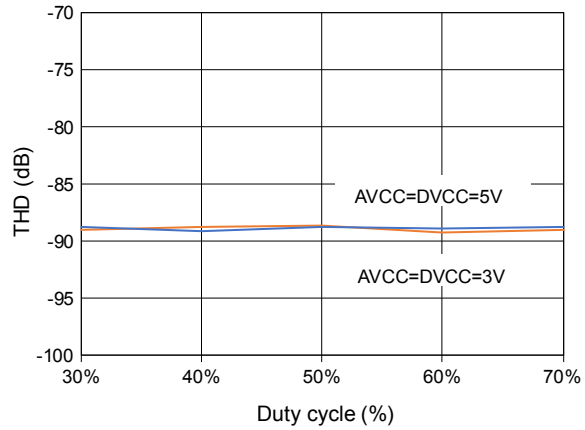


Figure 21. ENOB vs. SCLK duty cycle

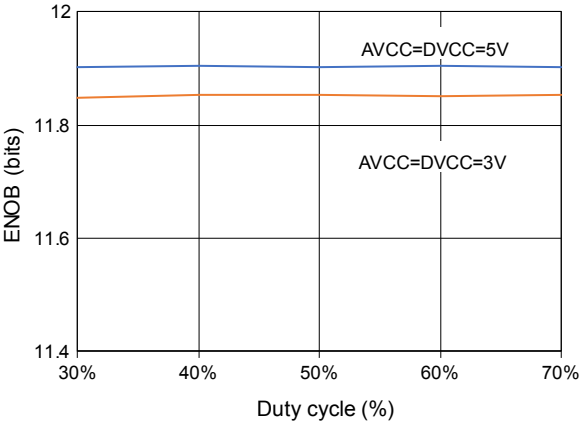


Figure 22. +/- DNL vs. SCLK

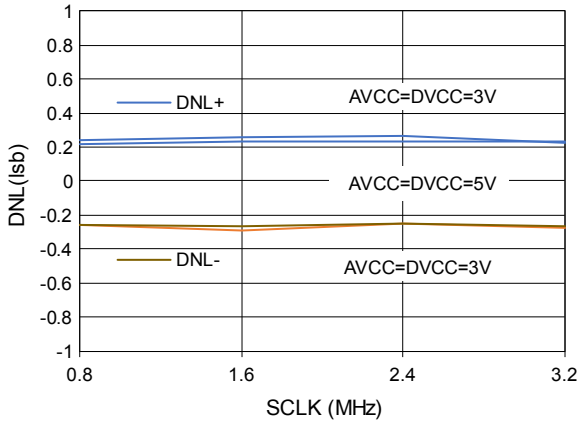


Figure 23. +/- INL vs. SCLK

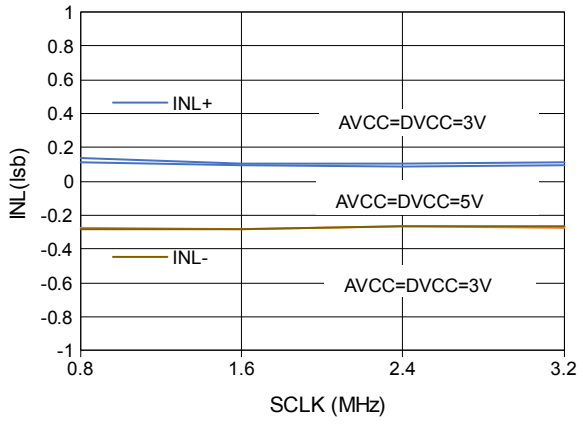


Figure 24. **SNR vs. SCLK**

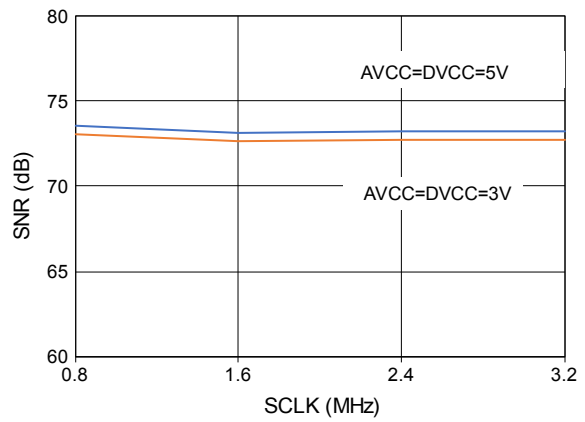


Figure 25. **THD vs. SCLK**

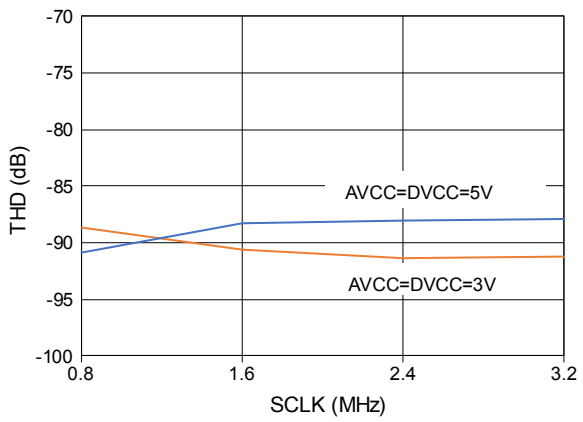


Figure 26. **ENOB vs. SCLK**

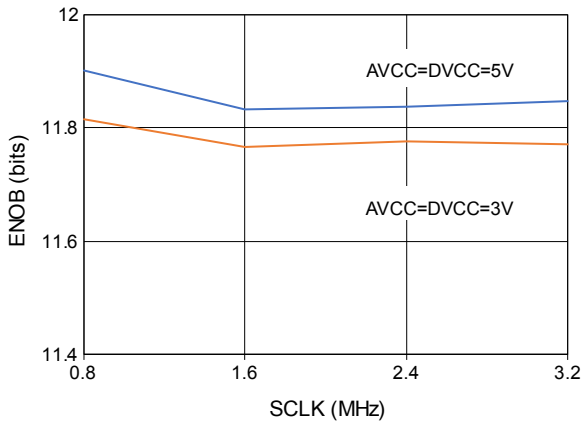


Figure 27. **+/- DNL vs. temperature**

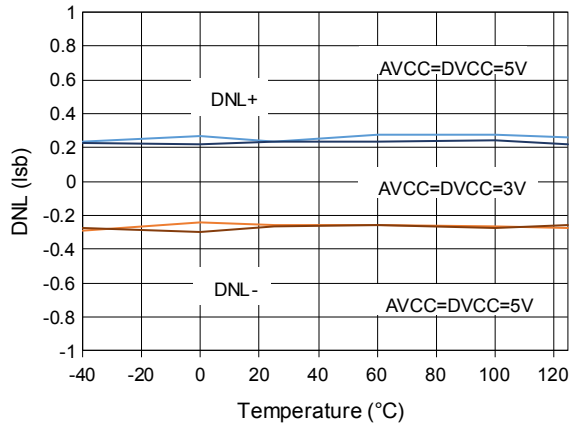


Figure 28. **+/- INL vs. temperature**

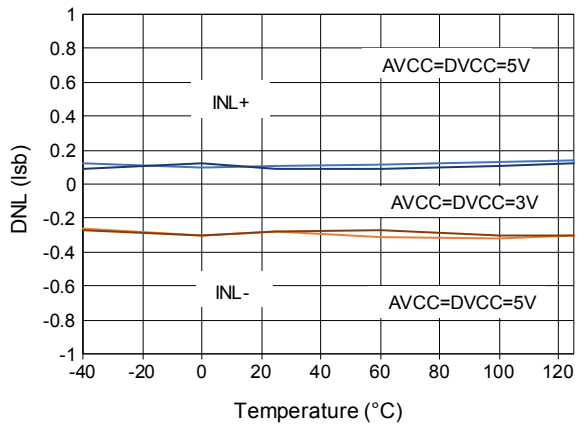


Figure 29. **SNR vs. temperature**

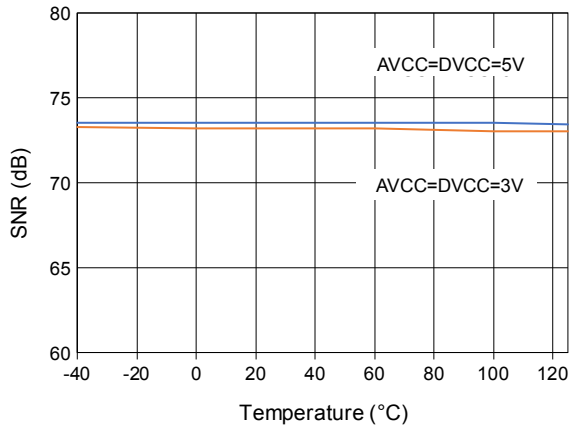


Figure 30. THD vs. temperature

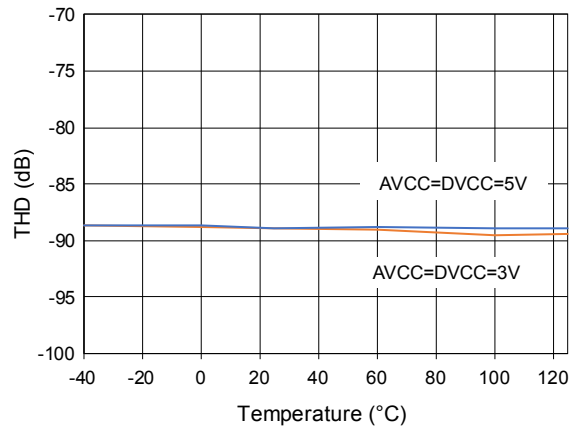


Figure 31. ENOB vs. temperature

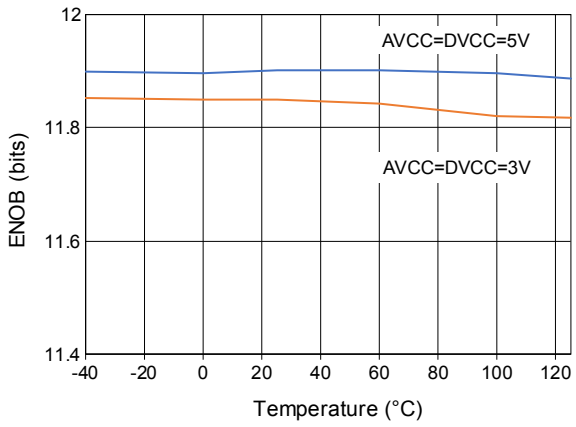


Figure 32. SNR vs. Fin

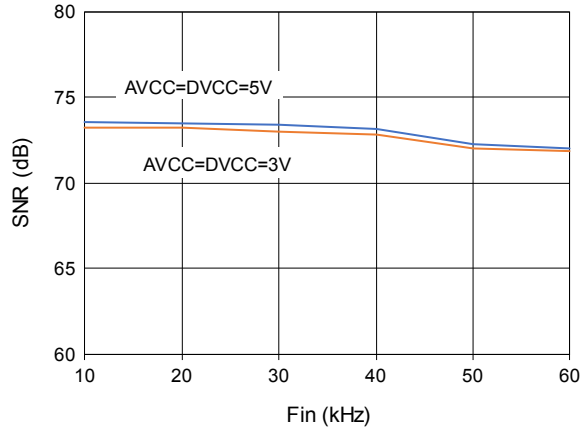


Figure 33. THD vs. Fin

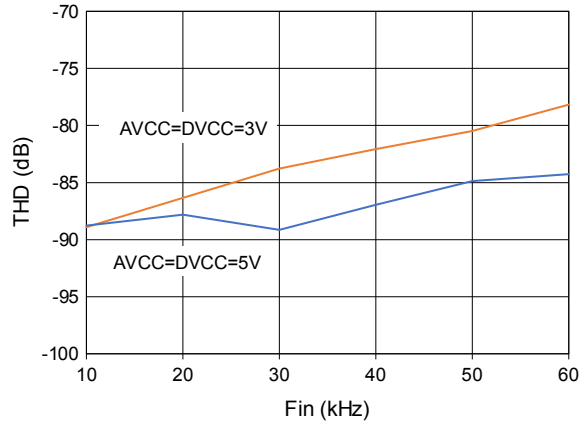


Figure 34. ENOB vs. Fin

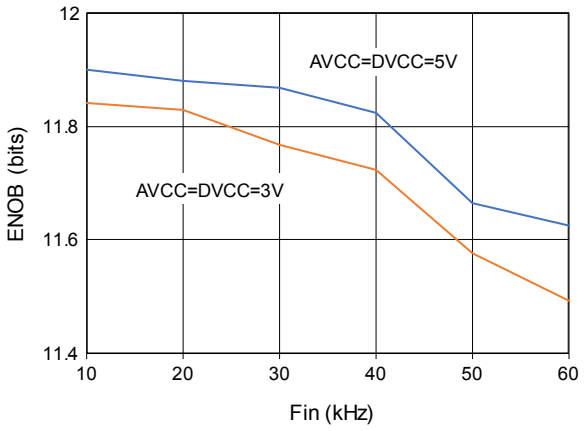


Figure 35. Power dissipation (mW) vs. SCLK

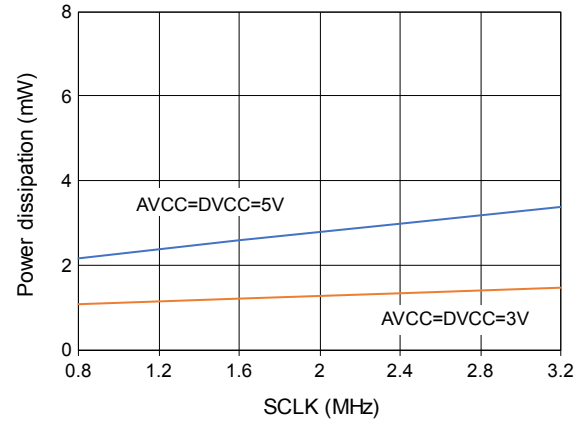
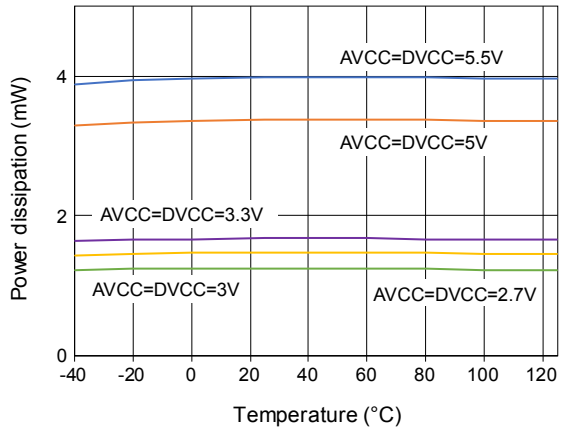


Figure 36. **Power dissipation (mW) vs. temperature**



6 Registers and input channel

Table 5. Control register bits

Bit #	7 (MSB)	6	5	4	3	2	1	0
Symbol	DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

Table 6. Control register bit description

Bit #	Symbol	Description
7, 6, 2, 1, 0	DONTC	Don't care
5	ADD2	These bits determine which input channel is converted, as per Table 7.
4	ADD1	
3	ADD0	

Table 7. Input channel description

ADD2	ADD1	ADD0	Address value (h)	Input channel
0	0	0	00	IN0
0	0	1	08	IN1
0	1	0	10	IN2
0	1	1	18	IN3
1	0	0	20	IN4
1	0	1	28	IN5
1	1	0	30	IN6
1	1	1	38	IN7

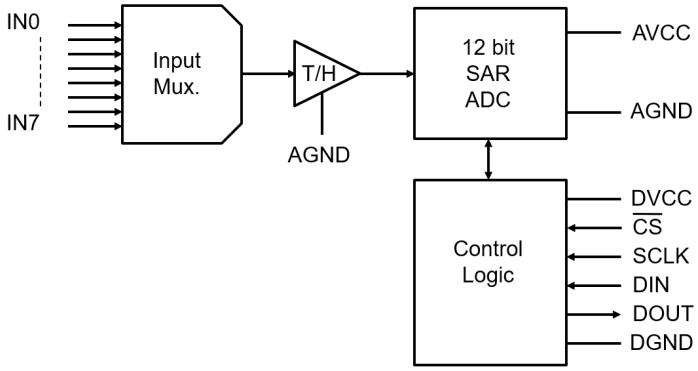
7 Application information

7.1 Functional description of the ADC1283

The ADC1283 implements a successive-approximation-register (SAR) structure to perform the conversion of analog signals into 12-bit pure binary digital outputs. As shown in the block diagram in Figure 37, it is made of capacitive Track and Hold, SAR ADC and control logic. The conversion circuit includes a fast settling time comparator to convey instruction into the register to store digital 0 or 1, and a redistribution DAC with logic control to have the ADC compare the track signal with a reference signal at each clock cycle.

The conversion is carried out in two phases. The sampling phase conveys the input signal through the capacitance array for the first 3 clock-cycles and the evaluation phase performs the conversion into digital 12-bit signal within 13 clock cycles. At each clock cycle of the evaluation phase, the hold signal is compared with a new value distributed by the DAC and the result is stored in the 12-bit register, MSB first. 13 clock cycles are necessary for this second step. So, a full conversion requires 16 clock cycles to generate a new 12-bit word on the DOUT pin.

Figure 37. Functional block diagram



7.2 Analog inputs

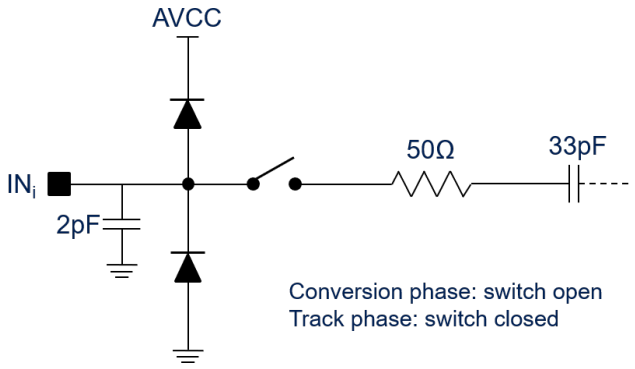
The inputs are single-ended and referenced from AVCC to AGND, since AVCC behaves as internal reference (refer to Table 1. Pin description). The dynamic range is AVCC and the LSB (Least Significant Bit) is:

$$LSB = \frac{AVCC}{2^{12}} \quad (1)$$

The capacitance seen on the input varies depending on conversion step. During the sampling phase, a 33 pF is seen from the input, thus care must be taken to the front-end driver to support this load.

The schematic below shows the equivalent input circuit.

Figure 38. Equivalent input circuit



To avoid aliasing of the input signals toward unwanted frequencies, it is recommended to insert a low-pass filter whose value is fixed depending on inputs frequency and sampling rate.

7.3 Interfacing the ADC1283

The conversion starts on a falling edge of $\overline{CS}$ and stops on a rising edge of $\overline{CS}$. An internal 8-bit register contains the address of the channel to be converted. 3 bits of this register are used to this purpose.

By default, if no value is written inside the register or if a wrong address is entered, channel 0 (IN0) is converted and outputted on DOUT after the first conversion cycle. This address register is reset to its default value (IN0) when ($\overline{CS}$) goes high.

At the start of the conversion, the first data present on DOUT after 16 clock cycles is always channel 0 (IN0). To get the information on another channel after starting conversion, 32 clock cycles are necessary (equivalent to two 12-bit words).

THE ADC1283 enters track mode under three different conditions. When ($\overline{CS}$) goes low with SCLK high, the ADC enters track mode on the first falling edge of SCLK. When ($\overline{CS}$) goes low with SCLK low, the ADC automatically enters track mode and the falling edge of ($\overline{CS}$) is seen as the first falling edge of SCLK. Finally, when ($\overline{CS}$) and SCLK go low simultaneously, the ADC enters track mode. While there is no timing restriction with respect to the rising edges of ($\overline{CS}$) and SCLK, see Figure 5 for set-up and hold time requirements for the falling edge of ($\overline{CS}$) with respect to the rising edge of SCLK.

3 clock cycles are necessary to charge the capacitance to memorize the level of the signal. The signal is then evaluated during 13 clock cycles. DOUT is always on the same format: four digital 0's followed by 12-bit signal (MSB first).

Conversion stops on ($\overline{CS}$) turning high but if ($\overline{CS}$) remains low, the ADC1283 continuously converts the analog signal on the selected channel.

For further information, please look at the Application Note related to the ADC1283.

8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 TSSOP-16 package information

Figure 39. TSSOP-16 package outline

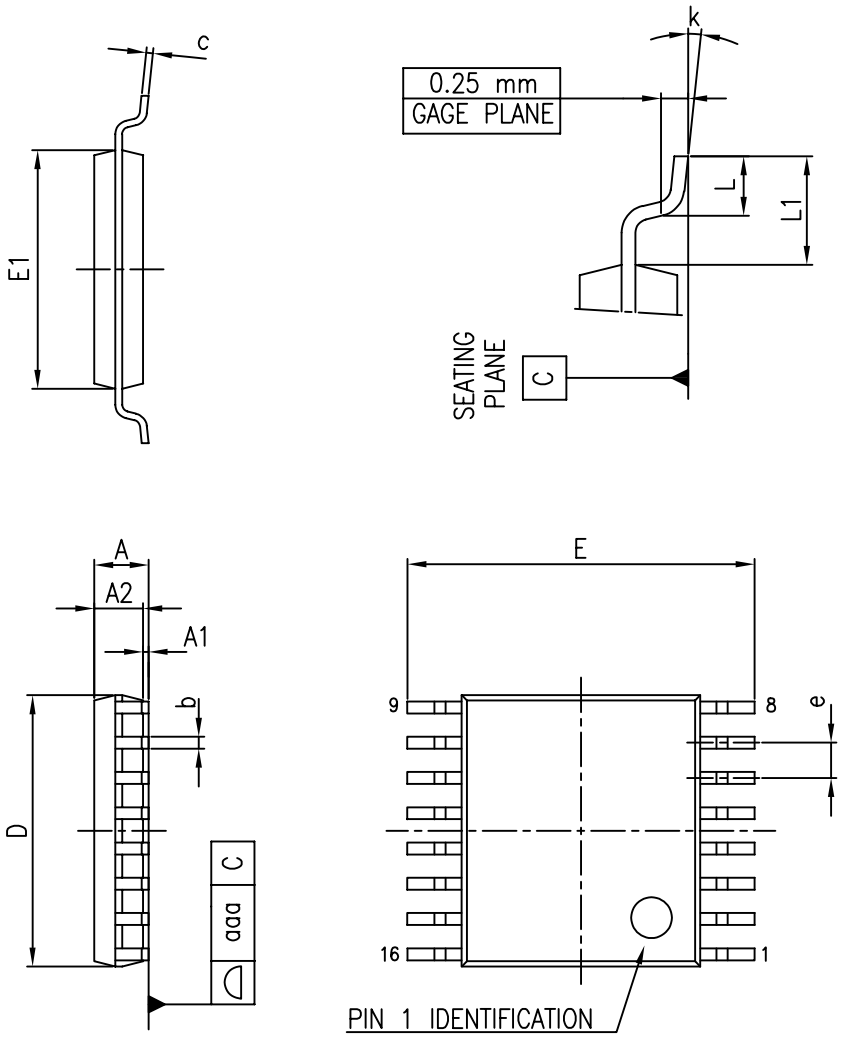


Table 8. **TSSOP-16 package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A			1.20
A1	0.05		0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65	
k	0°		8°
L	0.45	0.60	0.75
L1		1.00	
aaa			0.10

9 Ordering information

Table 9. **Order code**

Order code	Package	Temperature range	Marking
ADC1283IPT	TSSOP-16	- 40 °C to 125 °C	ADC1283

Revision history

Table 10. **Document revision history**

Date	Version	Changes
15-Mar-2022	1	Initial release.

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