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Chapter 1. Introduction

Growing popularity of standard USB PD3.0 chargers for mobile phone and notebook PC spurs the demand for leveraging standard PD 3.0 chargers to replace purposely and individually built chargers for any battery power electronic devices to reduce E-Waste.

AP33771 Evaluation Board (EVB) is intended to be used as an evaluation vehicle for charging applications between a Type C Connector-equipped Device (**TCD**, Energy Sink) and a Type C Connector-equipped PD Charger or Adaptor (**PDC**, Energy Source) through a Type C-to-C cable.

Figure 1 illustrates a TCD, embedded with PD3.0 Sink controller IC (i.e. AP33771), is physically connected to a PDC, embedded with USB PD3.0 decoder (e.g. AP43771) through a suitable Type C-to-Type C cable. Based on USB PD3.0 compliant firmware, AP33771 and AP43771 could go through the USB PD3.0 standard negotiation phase to establish suitable PD3.0 charging state.

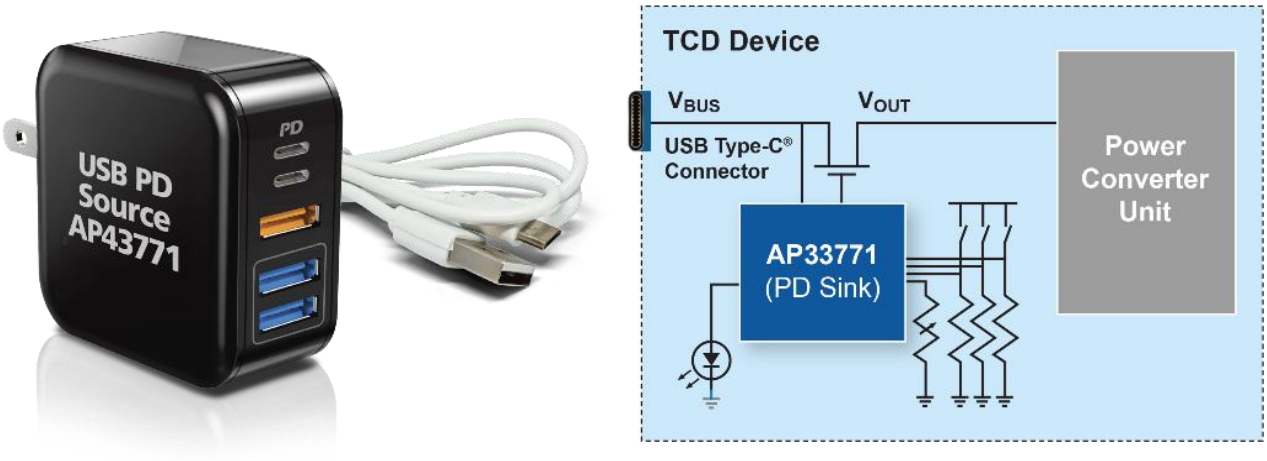


Figure 1 – A typical TCD with AP33771 PD3.0 Sink Controller to Request Input Voltage and Power from a USB PDC

To improve users' experiences in adoption of the AP33771 as USB Sink controller in TCDs, the AP33771 has built-in firmware to deal with automatic cable voltage drop compensation as well as legacy Type A charger charging through a Type A-to-C cable.

The AP33771 User's Guide of the Evaluation Board (EVB) explains a simple resistor-setting arrangement to request desired input voltage and input power for a typical TCD. The grant voltage and power back from a PDC for a successful match with source capability might be the exact the same or the lowest voltage and power sufficiency to cover the request, depending on the **PPS** (Programmable Power Supply) capability of the PDC.

Chapter 2. AP33771 Sink Controller

2.1 Package Outline

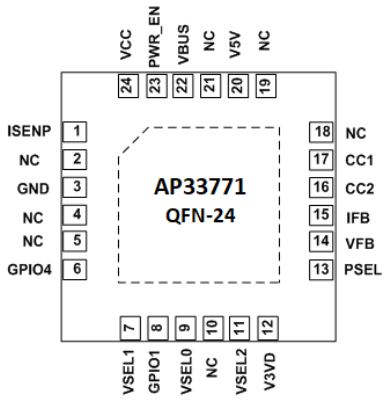


Figure 2 – Package Outline

2.2 Pin Descriptions

Pin No	Pin Name	Type (Note)	Pin Function
1	ISENP	AIO	Current Sense Positive Node.
2	NC	-	No Connection
3	GND	GND	Ground
4	NC	-	No Connection
5	NC	-	No Connection
6	GPIO4	DIO	General Purpose Input/Output pin, for LED usage.
7	VSEL1	DIO	For Voltage Select Pin1
8	GPIO1	DIO	General Purpose Input / Output
9	VSEL0	DIO	For Voltage Select Pin0
10	NC	-	No Connection
11	VSEL2	DIO	For Voltage Select Pin2
12	V3VD	DP	3.3V LDO Output. Power for Digital circuit and Digital I/O pins, with 0.1uF to Ground
13	PSEL	AIO	For Power Capability Selection.
14	VFB	AI	For Voltage Measurement.
15	IFB	AI	For Current Measurement, with 1nF to Ground
16	CC2	AIO	Type-C configuration channel 2
17	CC1	AIO	Type-C configuration channel 1
18	NC	-	No Connection
19	NC	-	No Connection
20	V5V	AP	5V LDO output. Power for Analog circuit and Analog I/O pins, with 0.1uF to Ground

21	**NC**	**-**	No Connection
22	**VBUS**	**AHV**	Terminal for Discharge Path.
23	**PWR_EN**	**AHV**	To control external NMOS switch ON (High) or OFF (Low).
24	**VCC**	**AHV**	The power supply of the IC, connected to a ceramic capacitor.
-	**EP**	**GND**	Exposed pad is connected to Ground

Table 1 –AP33771 Pin Number, Name, Type, and function

Note:
AHV– Analog High Voltage pin
AP – Power for Analog Circuit and Analog I/O pins, 5.0V operation
AI – Analog Input pin
DP – Power for Digital Circuit and I/O pins, 3.3V operation
AIO – Analog I/O pin.
DIO – Digital I/O pin.

Chapter 3. EVB Hardware Details

3.1 EVB TOP View

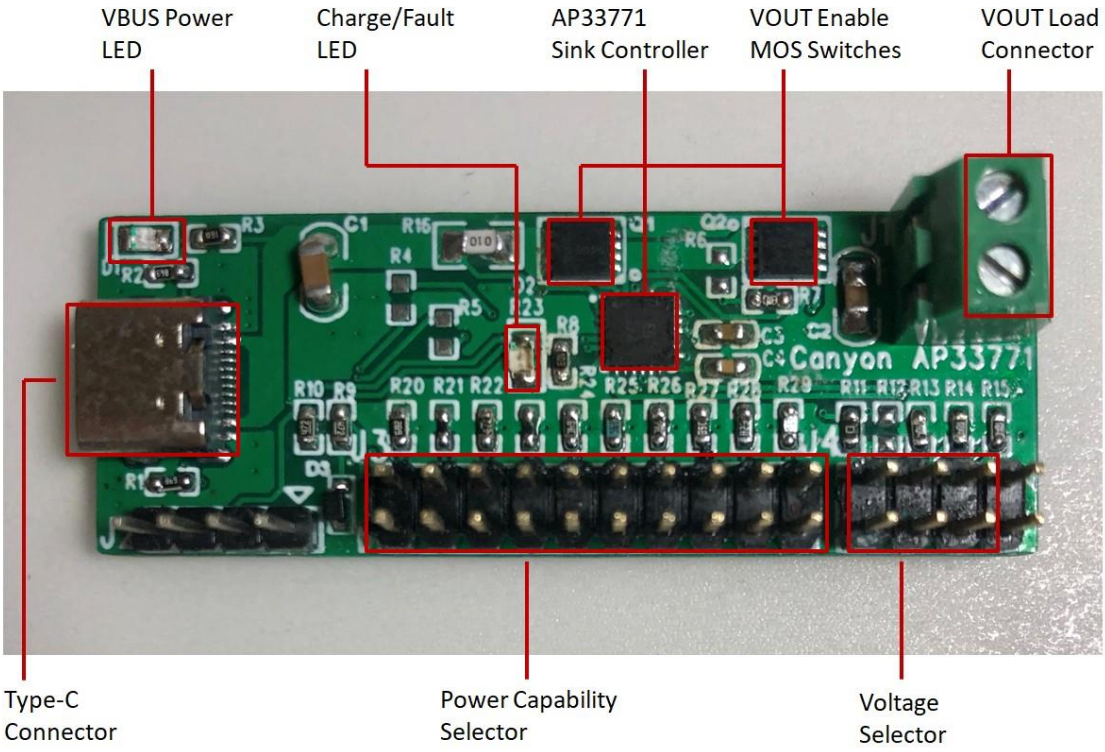


Figure 3 – AP33771 evaluation board top view and its key portions

3.2 EVB Block Diagram

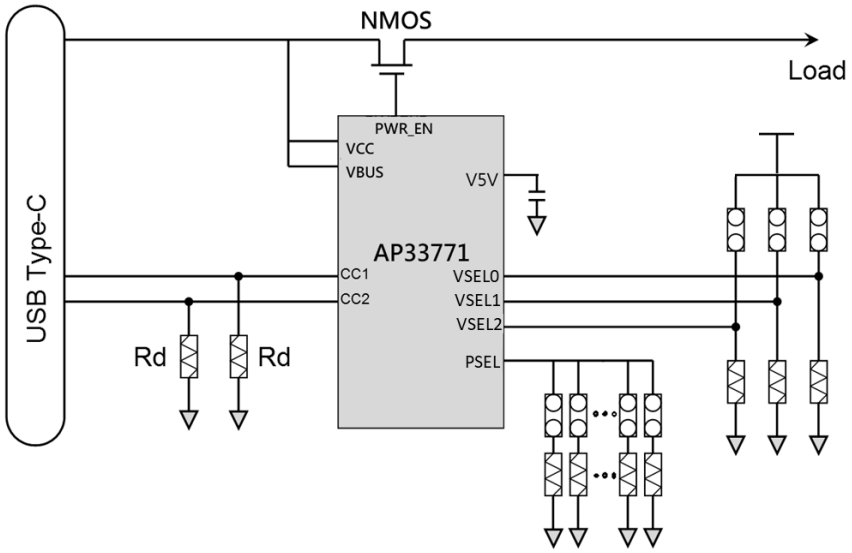
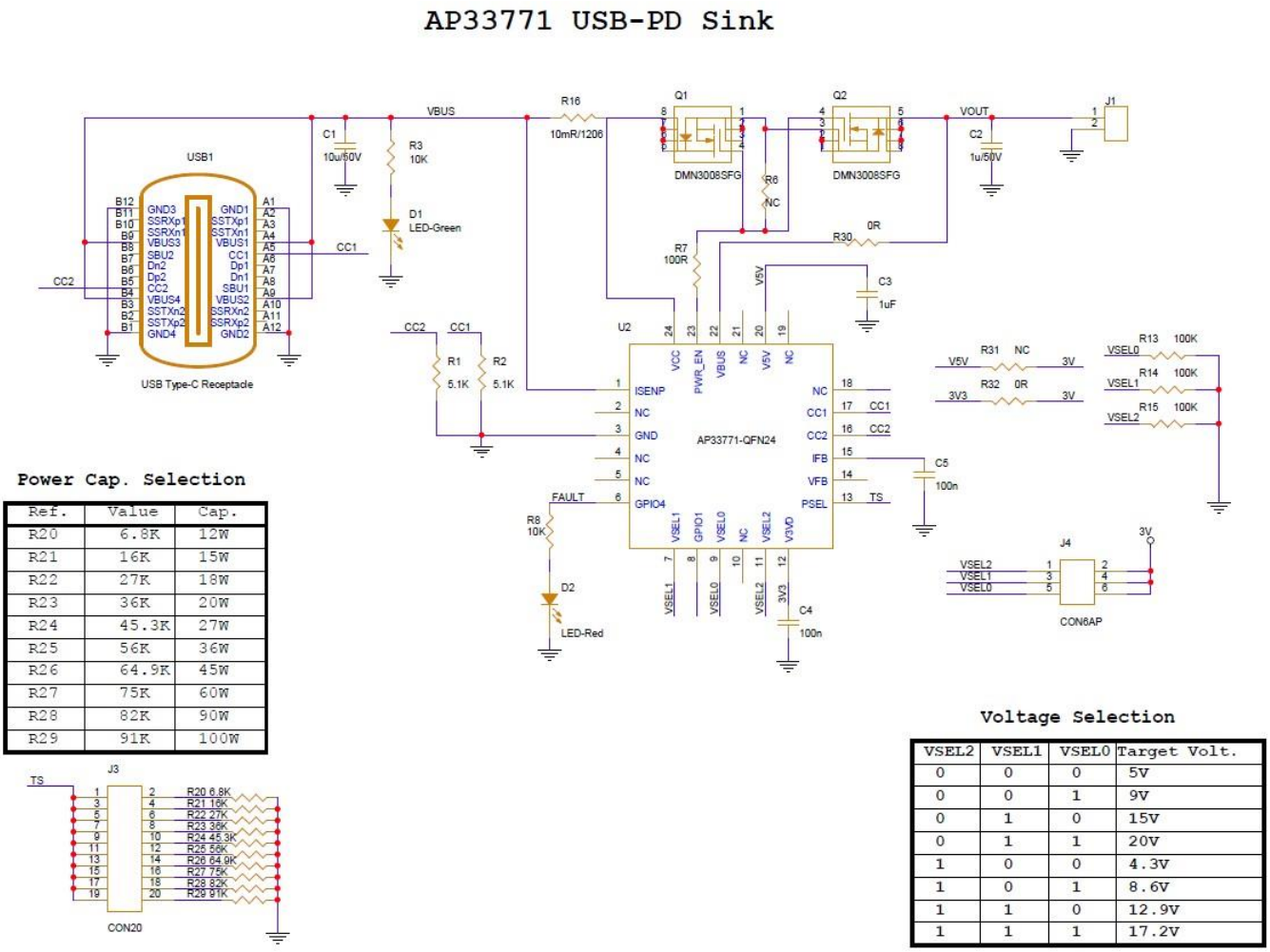


Figure 4 – Block diagram of the AP33771 evaluation board

3.3 EVB Schematics



Power Cap. Selection

Ref.	Value	Cap.
R20	6.8K	12W
R21	16K	15W
R22	27K	18W
R23	36K	20W
R24	45.3K	27W
R25	56K	36W
R26	64.9K	45W
R27	75K	60W
R28	82K	90W
R29	91K	100W

Voltage Selection

VSEL2	VSEL1	VSEL0	Target Volt.
0	0	0	5V
0	0	1	9V
0	1	0	15V
0	1	1	20V
1	0	0	4.3V
1	0	1	8.6V
1	1	0	12.9V
1	1	1	17.2V

Figure 5 –Schematics of the AP33771 Evaluation Board With Tables of PDO Selection and Power Capability

3.4 EVB System BOM

Item	Quantity	Reference	Part
1	1	C1	10u/50V
2	1	C2	1u/50V
3	1	C3	1uF
4	1	C4	100n
5	1	C5	100n
6	2	D1, D2	LED
7	2	Q1, Q2	DMN3008SFG
8	2	R1, R2	5.1K
9	1	R3	10K

10	1	R7	100
11	1	R8	10K
12	3	R13~ R15	100K
13	1	R16	10mR/1206
14	10	R20 ~R29	1% Accuracy. Select one for power capability
15	2	R30, R32	0
16	1	USB1	USB Type-C Receptacle
17	1	U1	AP33771-QFN24

Chapter 4. EVB Function Description

The AP33771 EVB provides users a simple resistor-setting to enable USB-PD negotiation between the TCD device and an external PDC. If the negotiation is successful, the PDC delivers the requested voltage and power to the TCD device through VBUS in Type-C cable. If negotiation is not successful, the PDC goes back to 5V PDO, and LED flickers with “Mismatch” pattern.

4.1 Board Outline

AP33771 EVB outline and floor plan is shown as Figure 6, where its connector and jumper location are listed in Table-2.

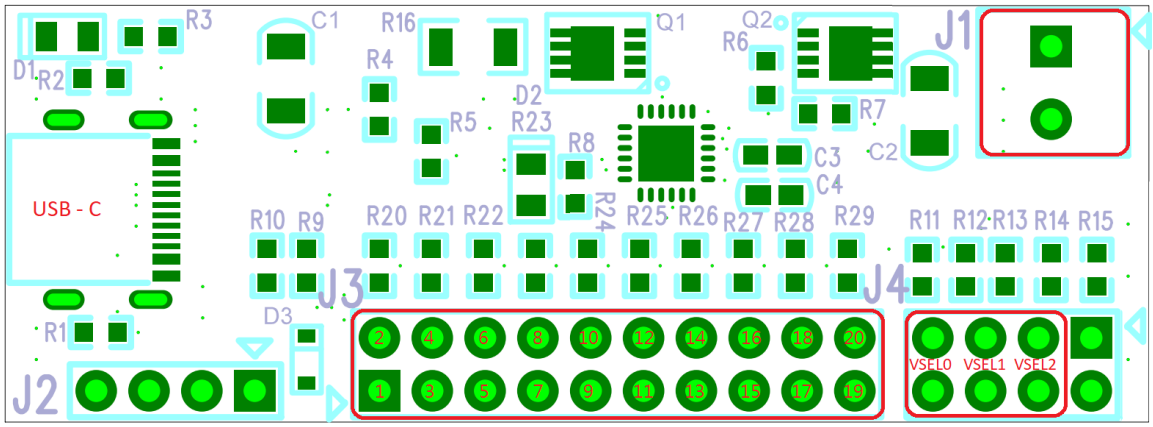


Figure 6 – Connector and jumper locations

Location	Function
J1	VOUT and Load Connector
J3	Power Selection
J4	Voltage Selection

Table 2 – Connectors and jumper names of the evaluation board

4.2 Voltage Selection

User can choose an appropriate set at J4 by jumpers to get a corresponding voltage according to Table-3. J4 is connected to VSEL2~VSEL0 pins, corresponding to relevant pins in the AP33771.

The top 4 rows of Table-3 map Selected Voltages into 4 standard Fixed PDO, 5V/9V/15V/20V. The bottom 4 rows of Selected Voltages, select 4.3V/8.6V/12.9V/17.2V, which match 1/2/3/4 cell(s) of typical Lithium-Ion battery for charger applications. Users can select appropriate resistor setting at J4 according to the desired voltage.

Selection No.	VSEL2	VSEL1	VSEL0	Selected Volt. (Target)	Grant Volt. (Source w/ PPS)	Grant Volt. (Source w/o PPS)
1	0	0	0	5V	5V	5V
2	0	0	1	9V	9V	9V
3	0	1	0	15V	15V	15V
4	0	1	1	20V	20V	20V
5	1	0	0	4.3V	4.3V	Mismatch (Note)
6	1	0	1	8.6V	8.6V	Mismatch (Note)
7	1	1	0	12.9V	12.9V	Mismatch (Note)
8	1	1	1	17.2V	17.2V	Mismatch (Note)

Note: If VSEL2 is ON (VSEL2 = 1) only source with PPS APDO are supported

Table 3 – Voltage selection through J4 connector setting

AP33771 will request the corresponding voltage from PDO capability of external PD Charger (PDC). During the voltage selection process of the AP33771, PPS Augmented PDO (APDO) has higher priority than Fixed PDO.

4.3 Power Capability Selection

The required power capability can be selected from the J3 connector, where a resister is connected to PSEL pin of the AP33771. With its constant current source output (20μA±3.0%) at the PSEL pin and an external resistor connected, the PSEL pin will show different voltage with different resistance. By measuring the voltage at the PSEL pin through internal ADC, the AP33771 will select the corresponding power capability. User can choose an appropriate resistor by a jumper to get a corresponding power capability according to Table-4.

The AP33771 also check whether source power is enough to meet the selected power which J3 Jumper has set. If the source power is smaller than the selected power, negotiation is completed with power mismatch, the AP33771 disables the MOS switch and LED flickers with “Mismatch” pattern.

For desired current capability greater then 3A, the user needs to use an e-Marker Type-C cable for the connection so that the PDO and APDO can follow the USB PD specification. According to USB PD protocol, PD source adapter checks the cable power capability which the e-Marker is used to report the cable parameters back to the source adapter.

Power Selection No.	Power Capability Selection	Real Resistance (kΩ)	Resistance Range (kΩ)	Power (W)
1	Short J3 pin 1 and 2	6.8	4 ~ 10	12
2	Short J3 pin 3 and 4	16	13 ~ 19	15
3	Short J3 pin 5 and 6	27	24 ~ 30	18
4	Short J3 pin 7 and 8	36	33 ~ 39	20
5	Short J3 pin 9 and 10	45	42 ~ 48	27
6	Short J3 pin 11 and 12	56	53 ~ 59	36
7	Short J3 pin 13 and 14	65	62 ~ 68	45
8	Short J3 pin 15 and 16	75	72 ~ 78	60
9	Short J3 pin 17 and 18	83	80 ~ 86	90
10	Short J3 pin 19 and 20	95	89 ~ 100	100

Table 4 – Power Capability Selection Table

The designers for TCDs are recommended to use the above real resistor with ±1% accuracy to connect to the PSEL pin.

Chapter 5. Built-In Application Firmware Features

5.1 Firmware Overview and LED Indication

The AP33771 has built-in firmware, which can intelligently handle various usage scenarios. Figure 7 shows the state transition diagram.

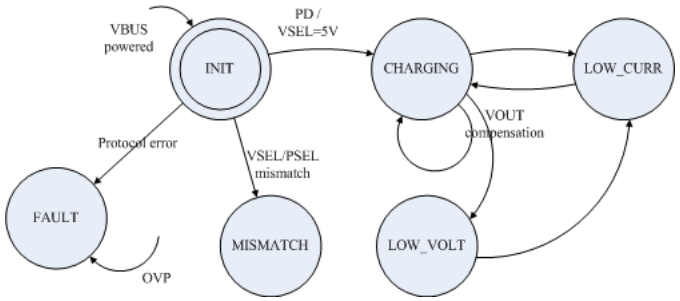


Figure 7 – AP33771 state diagram

The AP33771 controls LED lighting through GPIO4. Table 5 summarizes Transition conditions, LED indication and VOUT in each State.

State	Transition Conditions	LED Indication	VOUT	Comments
INIT (Initialization, PD Negotiation)	Protocol Errors, VSEL or PSEL Mismatch, PD and Non-PD 5V Charging	NA	OFF	VBUS/Rp attached and AP33771 initialization
CHARGING (Charging in progress)	Type C-to-C PD Voltage Drop Compensation, Non-PD 5V Charging Failure of Voltage Drop Compensation Type A-to-C, Trickle Charging Occurs	4-sec Breathing	ON	Successful negotiation/compensation and start charging
LOW_CURR	Resume normal charging	Full Light	ON	Charging current < 500mA
LOW_VOLT	Trickle charging	Half Light	ON	Voltage drop compensation failure
MISMATCH	Pending for User's Action	2-sec Flicker	OFF	Voltage or Power Mismatch
FAULT	Over Voltage Protection Occurs, Pending for User's Action	0.6-sec Flicker	OFF	OVP

Table 5 – LED Indication Table

5.2 PDO Selection Scheme

During the PD negotiation, the AP33771 evaluates all PDOs from PD Source capability discovery to find the right match with VSEL/PSEL according to Table 6. Subsequently, the AP33771 enables the associated MOS switches, and then VBUS is connected to VOUT when both voltage and power selection are matched.

If there are more than one PDO matched, the PPS PDO is higher priority over Fixed PDO.
If there are more than one PPS PDO matched, the lowest voltage PPS PDO takes precedence over other PDOs.
If there is no PDO matched, AP33771 requests the 1st PDO, 5V, and enters MISMATCH state.
If the source is not PD capable and VSEL is not 5V, AP33771 enters MISMATCH state. (Refer to Section 5.5)

Source PDO	Voltage Match Criteria	Power Match Criteria
Fixed PDO	$V_{VSEL} = V_{FIXED}$	$V_{FIXED} * I_{MAX} >= P_{PSEL}$
PPS PDO	$V_{PPSMIN} <= V_{VSEL} <= V_{PPSMAX}$	$V_{PROG} * I_{MAX} >= P_{PSEL}$

Table 6 – Voltage and Power Match Criteria

Note:

V_{VSEL} : Selected Voltage by VSEL
P_{PSEL} : Selected Power by PSEL
V_{FIXED} : Voltage of Fixed PDO
V_{PPSMIN} : Minimum Voltage of PPS PDO
V_{PPSMAX} : Maximum Voltage of PPS PDO
V_{PROG} : Nominal Voltage of PPS
I_{MAX} : Maximum Current of PDO/APDO

Table 7 shows the minimum and the maximum voltage for the Programmable Power Supply corresponding to the Nominal Voltage. (Extract from USB-PD Specification)

	Nominal Voltage			
	5V Prog	9V Prog	15V Prog	20V Prog
V_{PROG}	5V	9V	15V	20V
Maximum Voltage	5.9V	11V	16V	21V
Minimum Voltage	3.3V	3.3V	3.3V	3.3V

Table 7 – Nominal Voltage of PPS PDO

5.3 Over Voltage Protection (OVP)

The AP33771 triggers the OVP protection when VBUS voltage is higher than OVP threshold Voltage. Table 8 summarizes correspondence among VSEL Pin combination (VSEL2, VSEL1, VSEL0), V_{VSEL} Selected Voltage and OVP Threshold Voltage.

VSEL2	VSEL1	VSEL0	V_{VSEL} - Selected Voltage (V)	OVP Threshold Voltage (V)
0	0	0	5	7
0	0	1	9	11
0	1	0	15	17
0	1	1	20	22
1	0	0	4.3	6.3
1	0	1	8.6	10.6
1	1	0	12.9	14.9
1	1	1	17.2	19.2

Table 8 – OVP Threshold Voltage and Selected Voltage Correspondence

The OVP de-bounce time mechanism is to prevent mis-triggering by various spurious noises. The OVP de-bounce time is default to be 30ms. If VBUS voltage is larger than OVP threshold after the de bounce time limit (30ms), AP33771 enters FAULT state, the associated output enable MOS switches are turned off with LED flickering with the “Fault” pattern.

5.4 Automatic Type C-to-C Cable Voltage Drop Compensation

After the negotiation is completed and the MOS switch is enabled, the AP33771 monitors the VOUT voltage level. The VOUT voltage (V_{VOUT}) refers to the voltage on J1 Load Connector in Figure 6.

If the VOUT voltage fails to reach more than 6% below the V_{VSEL} Selected Voltage, the AP33771 only enables Automatic Type C Cable Voltage Drop Compensation mechanism for the combination where VSEL2 is 0. Table 9 shows the specification of Automatic Type C Cable Voltage Drop Compensation.

Source PDO	Compensation Criteria	Compensation Method	Voltage Compensation Upper Limit
Fixed PDO	$V_{VOUT} < V_{VSEL} * 0.94$ (3)	PDO Position +1 (next higher Voltage PDO)	4.0V (1)
PPS PDO	$V_{VOUT} < V_{VSEL} * 0.94$ (3)	Voltage + 0.1V each Voltage Drop Compensation iteration	1.3V (2)

Table 9 – Specification of Automatic Type C Cable Voltage Drop Compensation

Note:

1) Only allow PDO 5V to be raised to next PDO 9V, to prevent potential damage to subsequent circuit for battery charging by allowing next higher PDO (15V and 20V).
2) The Type C-to-C Compliance cables have typically end-to-end resistance of 250mΩ of any length. The maximum Voltage Drop compensation allowed is 1.3V - from source-end to sink-end of a Type C-to-C cable should be within 1.25V for maximum current of 5A.
3) AP33771 enables Voltage Drop Compensation when VSEL2 is 0 (V_{VSEL}=5V/9V/15V/20V) and V_{VOUT} < V_{VSEL} * (1 - 6%).

The criteria for enabling Voltage Drop Compensation mechanism will change with different V_{VSEL} Selected Voltage. Table 10 shows the correspondence between Selected Voltage and Compensation Criteria.

V_{VSEL} - Selected Voltage	Compensation Criteria
5V	V_{VOUT} < 4.7V
9V	V_{VOUT} < 8.46V
15V	V_{VOUT} < 14.1V
20V	V_{VOUT} < 18.8V
4.3V	Disable
8.6V	Disable
12.9V	Disable
17.2V	Disable

Table 10 – Correspondence between Selected Voltage and Compensation Criteria

According to the source PDO (Fixed PDO or PPS PDO), the AP33771 chooses different compensation method. Table 11 shows the examples of Type C-to-C Cable Voltage Drop Compensation situations.

Source PDO	V_{VSEL}	Before Compensation			After Compensation		
		Original Request Voltage	V_{VOUT}	State	Adjusted Request Voltage ($V_{ARequest}$)	V_{VOUT}	State
Fixed_5V	5V	Fixed_5V	< 4.7V	CHARGING	Fixed_5V	< 4.7V	LOW_VOLT
Fixed_5V / Fixed_9V	5V	Fixed_5V	< 4.7V	CHARGING	Fixed_9V	9V-Cable Voltage Drop (1)	CHARGING
Fixed_5V / Fixed_9V / PPS_3.3~11V	5V	PPS_5V	< 4.7V	CHARGING	PPS_5V+Voltage Drop (1.3V max) (2)	>= 4.7V	CHARGING
Fixed_5V / Fixed_9V / PPS_3.3~11V	5V	PPS_5V	< 4.7V	CHARGING	PPS_5V+1.3V	< 4.7V	LOW_VOLT

Table 11 – Example of Type C-to-C Cable Voltage Drop Compensation

Note: If the cable voltage drop from the source-end to the sink-end is 1.0V,

1) Adjusted $V_{ARequest}$ would be 9V and V_{VOUT} would be 8V
2) Adjusted $V_{ARequest}$ would be 5.7V for V_{VOUT} to reach 4.7V

If the Voltage Drop Compensation fails, it means that no suitable PDO is found or voltage compensation exceeds the upper limit. The AP33771 will be transitioned to the LOW_VOLT state.

5.5 Legacy Type A Charger with Type A-to-C Cable

When the energy source is from a legacy type A charger with Type A-to-C cable connection to the TCD, the AP33771 enters the Non-PD Mode after PD negotiation fails. Table 12 shows the Non-PD Mode state of AP33771 after PD negotiation and compensation.

If VSEL is 5V and VOUT voltage is higher than 4.7V, AP33771 enters CHARGING state.
If VSEL is 5V and VOUT voltage is lower than 4.7V, AP33771 enters LOW_VOLT state.
If VSEL is not 5V, AP33771 enters MISMATCH state.

Non-PD Mode State		
V_{VSEL}	V_{VOUT}	State
V_{VSEL} = 5V	V_{VOUT} >= 4.7V	CHARGING
V_{VSEL} = 5V	V_{VOUT} < 4.7V	LOW_VOLT
V_{VSEL} != 5V	NA	MISMATCH

Table 12 – The state of AP33771 connection to Type A legacy chargers

Chapter 6. USB Type C-to-C PD Sink-Source Application Examples

Usage cases 1 to 6 shows different scenarios and procedures between request power profile of a TCD and power source capability a PDC for establish charging states (Figure 8).

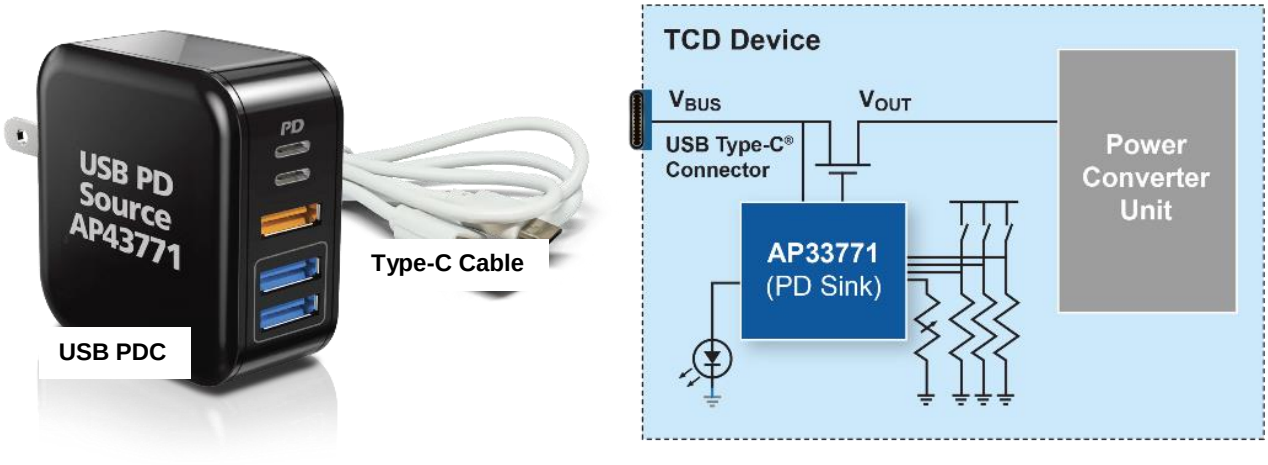


Figure 8 – Examples Based on a Typical TCD Application Scenario with an USB PDC

Case 1:	**PDC=36W**		**TCD = 15V and 36W**		
	PDO:	**APDO:**			
	5V/3A	**None**	**VSEL2 = 0**	**RPSEL= 56KΩ**	**VBUS = 15V**
	9V/3A		**VSEL1 = 1**		**VOUT = 15V**
	15V/2.4A		**VSEL0 = 0**		

A TCD request 15V and 36W from a given 36W PDC source with fixed PDOs: 5V/3A, 9V/3A, 15V/2.4A.

Step 1, set SEL2~SEL0 to be ”010” to get 15V, as Selection No. 3 in Table-3, and
Step 2, connect a resister with 56 KΩ and 1% accuracy to PSEL pin, as Selection No. 6 in Table-4.
Step 3, AP33771 starts to handshake with the powered PDC as soon as Type-C cable is connected.
Step 4, VBUS = 15V, because PDO 15V/2.4A is matched.
Step 5, VOUT = 15V, because Power and Voltage are all matched, then the MOS switches are enabled.

Case 2:	**PDC=36W**		**TCD = 15V and 45W**		
	PDO:	**APDO:**			
	5V/3A	**None**	**VSEL2 = 0**	**RPSEL= 65KΩ**	**VBUS = 15V**
	9V/3A		**VSEL1 = 1**		**VOUT = 0V**
	15V/2.4A		**VSEL0 = 0**		

TCD requests 15V and 45W from a given 36W PDC source with fixed PDOs: 5V/3A, 9V/3A, 15V/2.4A.

Step 1, set SEL2~SEL0 to be ”010” to get 15V, as Selection No. 3 in Table-3, and
Step 2, connect a resister with 65 KΩ and 1% accuracy to PSEL pin, as Selection No. 7 in Table-4.
Step 3, AP33771 starts to handshake with the powered PDC as soon as Type-C cable is connected.
Step 4, VBUS = 15V, because PDO 15V/2.4A is matched.
Step 5, VOUT = 0V, because Power and Voltage are not all matched, and so MOS switches are not enabled.

Case 3:	**PDC=36W**		**TCD = 15V and 36W**		
	PDO:	**APDO:**			
	5V/3A	**5V Prog/3A**	**VSEL2 = 0**	**RPSEL= 56KΩ**	**VBUS = 15V**
	9V/3A	**9V Prog/3A**	**VSEL1 = 1**		**VOUT = 15V**
	15V/2.4A	**15V Prog/2.4A**	**VSEL0 = 0**		

A TCD requests 15V and 36W from a given 36W PDC source with fixed PDOs and APDOs as above.

Step 1, set SEL2~SEL0 to be ”010” to get 15V, as Selection No. 3 in Table-3, and
Step 2, connect a resister with 56 KΩ and 1% accuracy to PSEL pin, as Selection No. 6 in Table-4.
Step 3, AP33771 starts to handshake with the powered PDC as soon as Type-C cable is connected.
Step 4, VBUS = 15V, because APDO 15V Prog/2.4A is matched. APDO has higher priority.
Step 5, VOUT = 15V, because Power and Voltage are all matched, and so MOS switches are enabled.

Case 4:	**PDC=36W**		**TCD = 12.9V and 36W**		
	PDO:	**APDO:**			
	5V/3A	**5V Prog/3A**	**VSEL2 = 1**	**R_{PSEL}= 56KΩ**	**VBUS = 12.9V**
	9V/3A	**9V Prog/3A**	**VSEL1 = 1**		**VOUT = 12.9V**
	15V/2.4A	**15V Prog/2.4A**	**VSEL0 = 0**		

A TCD requests 15V and 36W from a given 36W PDC source with fixed PDOs and APDOs as above.

Step 1, set SEL2~SEL0 to be ”110” to get 12.9V, as Selection No. 7 in Table-3, and
Step 2, connect a resister with 56 KΩ and 1% accuracy to PSEL pin, as Selection No. 6 in Table-4.
Step 3, AP33771 starts to handshake with the powered PDC as soon as Type-C cable is connected.
Step 4, VBUS = 12.9V, because APDO 15V Prog/2.4A is matched. APDO has higher priority.
Step 5, VOUT = 12.9V, because Power and Voltage are all matched, and so MOS switches are enabled.

Case 5:	**PDC=36W**		**TCD = 15V and 45W**		
	PDO:	**APDO:**			
	5V/3A	**5V Prog/3A**	**VSEL2 = 0**	**R_{PSEL}= 65KΩ**	**VBUS = 15V**
	9V/3A	**9V Prog/3A**	**VSEL1 = 1**		**VOUT = 0V**
	15V/2.4A	**15V Prog/2.4A**	**VSEL0 = 0**		

A TCD requests 15V and 45W from a given 36W PDC source with fixed PDOs and APDOs as above.

Step 1, set SEL2~SEL0 to be ”010” to get 15V, as Selection No. 3 in Table-3, and
Step 2, connected a resister with 65 KΩ and 1% accuracy to PSEL pin, as Selection No. 7 in Table-4.
Step 3, AP33771 starts to handshake with the powered PDC as soon as Type-C cable is connected.
Step 4, VBUS = 15V, because APDO 15V Prog/2.4A is matched. APDO has higher priority.
Step 5, VOUT = 0V, because Power and Voltage are not all matched, the MOS switches are not enabled.

Case 6:	**PDC=36W**		**TCD = 12.9V and 36W**		
	PDO:	**APDO:**			
	5V/3A	**None**	**VSEL2 = 1**	**R_{PSEL}= 56KΩ**	**VBUS = 5V**
	9V/3A		**VSEL1 = 1**		**VOUT = 0V**
	15V/2.4A		**VSEL0 = 0**		

A TCD requests 12.9V and 36W from a given 36W PDC source with fixed PDOs: 5V/3A, 9V/3A, 15V/2.4A.

Step 1, set SEL2~SEL0 to be ”110” to get 12.9V, as Selection No. 7 in Table-3, and
Step 2, connect a resister with 56 KΩ and 1% accuracy to PSEL pin, as Selection No. 6 in Table-4.
Step 3, AP33771 starts to handshake with the powered PDC as soon as Type-C cable is connected.
Step 4, VBUS = 5V, because no PDO can match to 12.9V request, and 5V is supported instead, according to PD rule.
Step 5, VOUT = 0V, because Power and Voltage are not all matched, the MOS switches are not enabled.

Chapter 7. Compliance test

The AP33771 EVB passes all test items in Ellisys USB-PD Compliance tester as below.

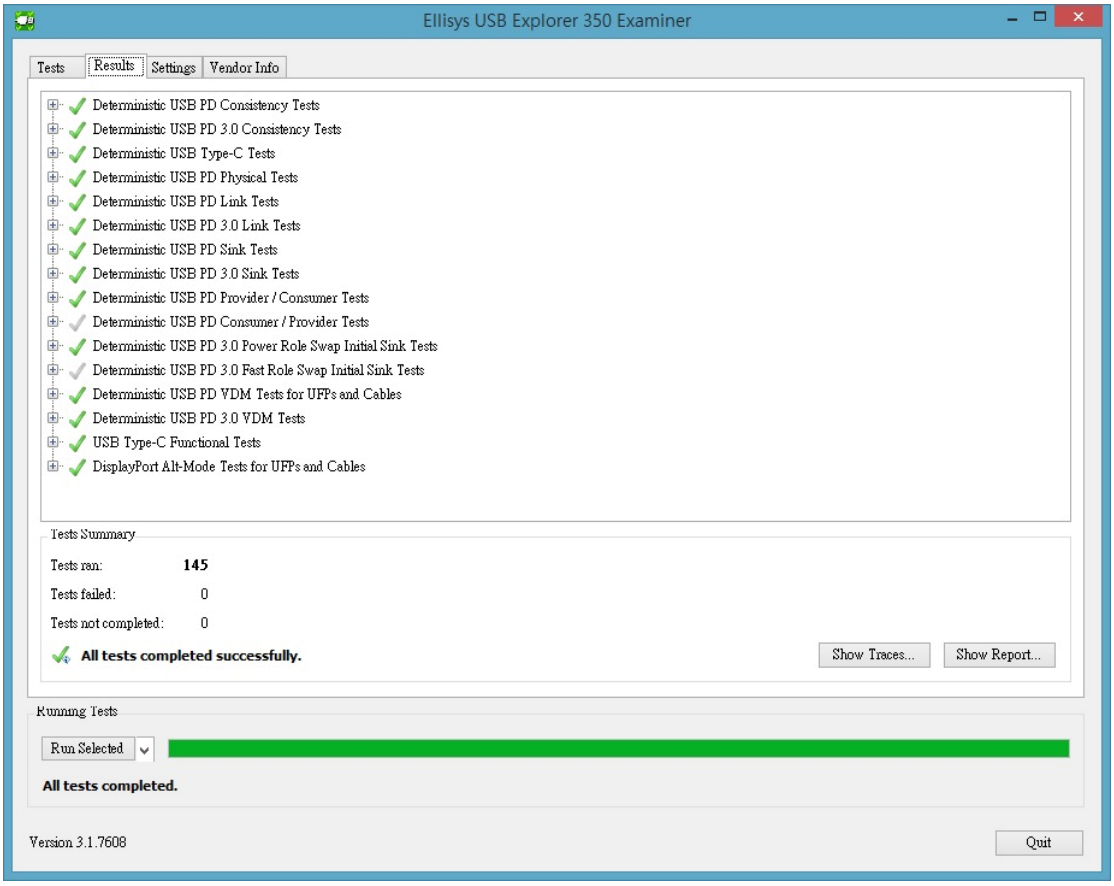


Figure 9 – Ellisys USB PD Test Environment and Test Item List

Chapter 8. Design Considerations

8.1 Termination of CC1/CC2 channels

Since the AP33771 has no internal Rd resistor embedded, designer must place 5.1K ohm resistor on both CC1 and CC2 to GND. Lack of any Rd will cause the AP33771 misrecognizing direction of CC and could not enter into PD negotiation process.

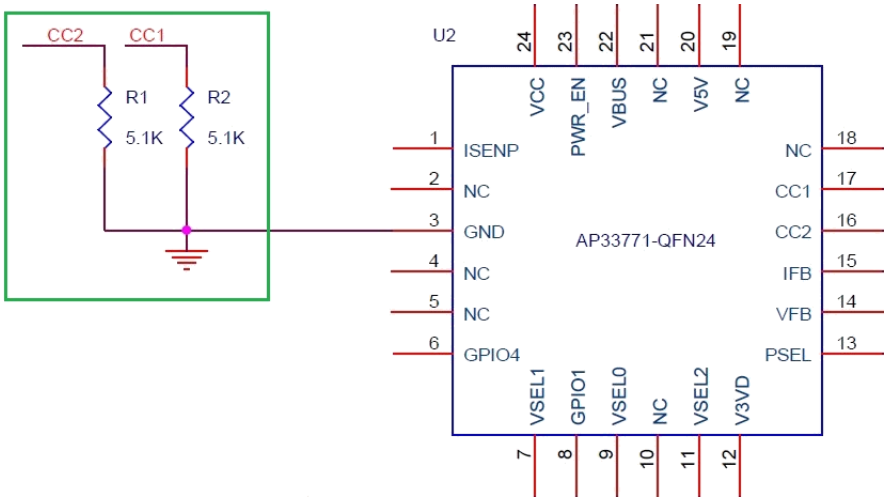


Figure 10 – Make sure the connection of external Rd resistors on CC1 and CC2

8.2 ESD Considerations

The AP33771 EVB is designed for functional evaluation; there is no ESD protection component on board. Do not use the AP33771 EVB to test ESD. For manufacturing, user must consider to add suitable ESD protection devices or to optimize their PCB design.

Chapter 9. Revision History

Revision	Issue Date	Comment	Author
1.0	1/13/2022	Initial Release	Joseph Liang
1.1	4/15/2022	Updated Figure 1 and Figure 8	Feng Zhao

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