



CUSTOMER ADVISORY

ADV2017

Intel® Stratix® 10 Device E-Tile Transceiver Update

Description:

Intel® is notifying customers of an important update to the Intel Stratix® 10 device E-Tile transceivers.

The Intel Quartus® Prime Settings File (QSF) assignment to preserve performance of unused transceiver channels is found not working as intended in versions of Intel Quartus Prime Pro Software prior to version 20.1.

Follow the recommended actions described in Table 1.

Recommended Actions:

Intel Stratix 10 device E-Tile customers who **do not** plan to preserve performance of unused Transceiver channel(s)/Tile(s) in future are not required to take any action, regardless of Intel Quartus® Prime Pro software version.

Intel Stratix 10 device E-Tile customers who **do** plan to preserve performance of unused Transceiver channel(s)/Tile(s) in future are requested to refer to Table 1 for recommended actions.

Table 1

Customer Design Version	Recommended Actions
Intel Quartus Prime Pro software v19.4	<ol style="list-style-type: none"><li data-bbox="488 363 1357 558">1. Upgrade design to Intel Quartus Prime Pro Software version 20.1 or later. You can find the Intel Quartus Prime Pro software version 20.1 here- https://fpgasoftware.intel.com/?edition=pro&platform=windows<li data-bbox="488 604 1365 846">2. Refer to section 3.1.10 of the updated E-Tile Transceiver PHY User Guide to note the preserve unused channel QSF assignment to be used based on design use case. You can find the updated E-Tile Transceiver PHY User Guide here- https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_etile_xcvr_phy.pdf<li data-bbox="488 892 1373 1134">3. Upon design compilation if you see the error shown below, add the following assignments to your .qsf file-<ul style="list-style-type: none"><li data-bbox="570 976 1357 1045">• set_instance_assignment -name HSSI_PARAMETER "refclk_divider_use_as_BTI_clock=TRUE"<li data-bbox="570 1056 1357 1125">• set_instance_assignment -name HSSI_PARAMETER "refclk_divider_input_freq=<frequency in Hz>" <p data-bbox="488 1178 1357 1581">Error (21636): QSF assignment PRESERVE_UNUSED_XCVR_CHANNEL has been specified to preserve unused transceiver channels in HSSI IO BANK 8B. However, no reference clock has been specified using the QSF assignments set_instance_assignment -name HSSI_PARAMETER "refclk_divider_use_as_BTI_clock=TRUE" and set_instance_assignment -name HSSI_PARAMETER "refclk_divider_input_freq=<frequency in Hz>". See E-tile User Guide for more information.</p>

Table 1 (continued)

Customer Design Version	Recommended Actions
Intel Quartus Prime Pro software v20.1	Refer to section 3.1.10 of the updated E-Tile Transceiver PHY User Guide to note the preserve unused channel QSF assignment to be used based on design use case. You can find the updated E-Tile Transceiver PHY User Guide here- https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_etile_xcvr_phy.pdf
Intel Quartus Prime Pro software versions excluding v19.4 & v20.1	<ol style="list-style-type: none"><li data-bbox="483 688 1352 884">1. Upgrade design to Intel Quartus Prime Pro Software version 20.1 or later. You can find the Intel Quartus Prime Pro software version 20.1 here- https://fpgasoftware.intel.com/?edition=pro&platform=windows<li data-bbox="483 932 1352 1171">2. Refer to section 3.1.10 of the updated E-Tile Transceiver PHY User Guide to note the preserve unused channel QSF assignment to be used based on design use case. You can find the updated E-Tile Transceiver PHY User Guide here- https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug_etile_xcvr_phy.pdf

Products Affected:

Selected Intel Stratix 10 TX, MX, and DX E-Tile devices.

The list of affected part numbers (OPNs) can be downloaded in Excel form:

<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2017-opn-list.xlsx>

Change Implementation:

Table 2

Milestone	Availability
Availability of Intel Quartus Prime software version 20.1	Now
Availability of updated E-Tile Transceiver PHY User Guide	Now

Contact:

For more information, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:

<https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html>

or submit a question to the Intel FPGA forum with ADV2017 in the title.

Customer Notifications Subscription:

Customers that subscribe to the Intel FPGA customer notification mailing list will receive the notifications automatically via email.

If you would like to receive Intel FPGA customer notifications by email, you can register to the Intel FPGA program and set up your subscription at:

<https://www.intel.com/content/www/us/en/programmable/my-intel/mail-emailsub/technical-updates.html>

Revision History

Date	Rev	Description
06/19/2020	1.0.0	Initial Release

©2020 Intel Corporation. All rights reserved. Intel, the Intel logo, Altera, Arria, Cyclone, Enpirion, Max, Nios, Quartus and Stratix words and logos are trademarks of Intel Corporation or its subsidiaries in the U.S. and/or other countries. Other marks and brands may be claimed as the property of others. Intel reserves the right to make changes to any products and services at any time without notice. Intel assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Intel. Intel customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.