

## 74VHC393 Dual 4-Bit Binary Counter

### Features

- High Speed:  $f_{MAX} = 170\text{MHz}$  (Typ.) at  $T_A = 25^\circ\text{C}$
- Low power dissipation:  $I_{CC} = 4\mu\text{A}$  (Max.) at  $T_A = 25^\circ\text{C}$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Power down protection is provided on all inputs
- Pin and function compatible with 74HC393

### General Description


The VHC393 is an advanced high speed CMOS 4-bit Binary Counter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. It contains two independent counter circuits in one package, so that counting or frequency division of 8 binary bits can be achieved with one IC. This device changes state on the negative going transition of the  $\overline{\text{CLOCK}}$  pulse. The counter can be reset to "0" ( $Q_0-Q_3 = \text{"L"}$ ) by a HIGH at the CLEAR input regardless of other inputs.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

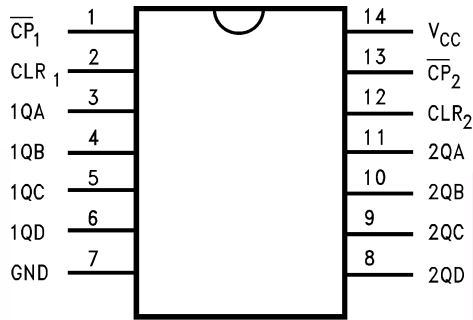
### Ordering Information

Order Number	Package Number	Package Description
74VHC393M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHC393SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC393MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

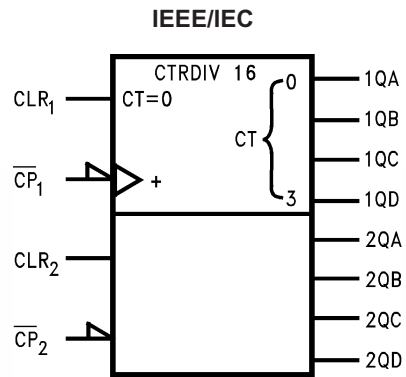
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

 All packages are lead free per JEDEC: J-STD-020B standard.

### Connection Diagram



### Logic Symbol/s



### Pin Descriptions

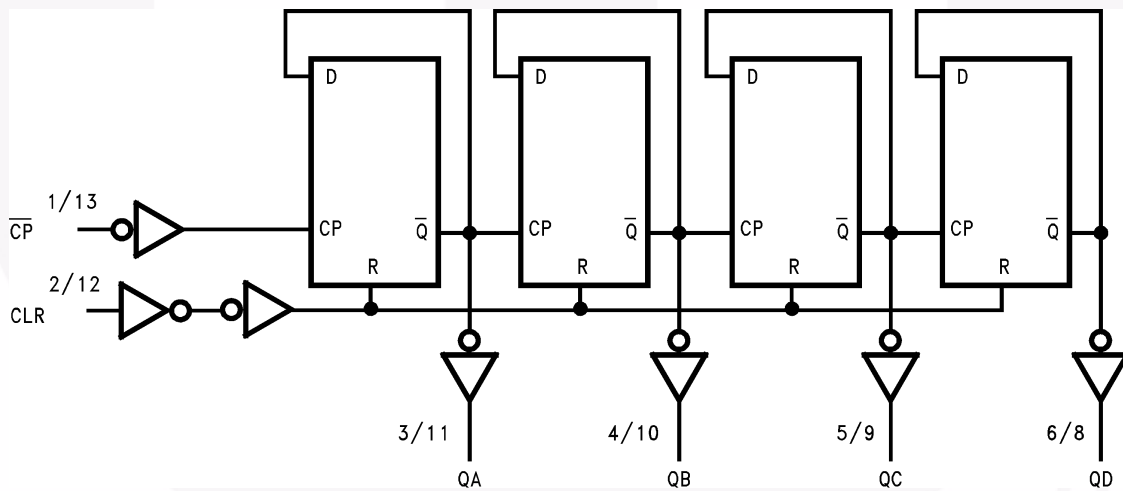
Pin Names	Description
CLR <sub>1</sub> , CLR <sub>2</sub>	Clear Inputs
$\overline{CP}_1$ , $\overline{CP}_2$	Clock Pulse Inputs
QA, QB, QC, QD	Outputs

### Truth Table

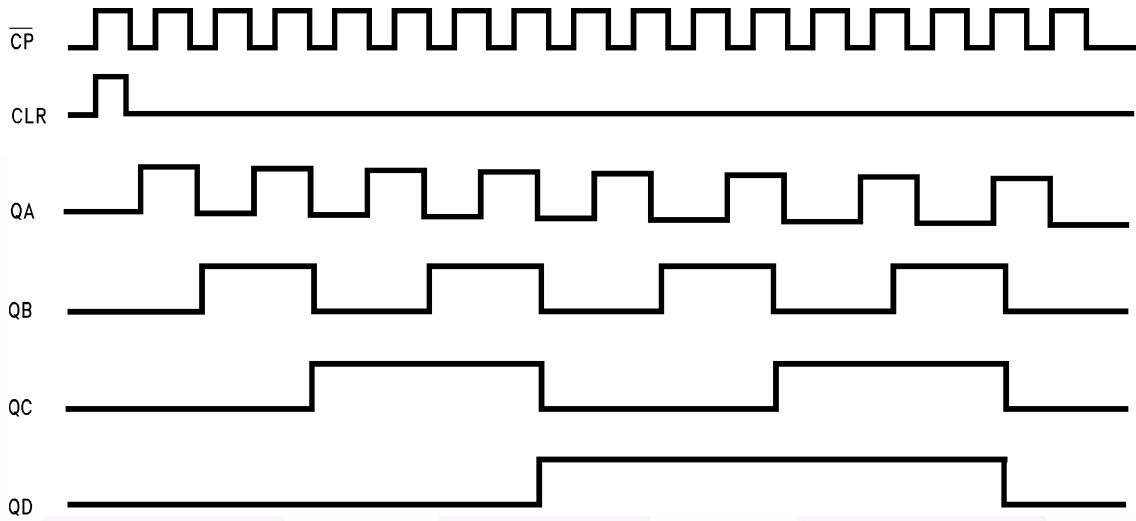
Inputs		Outputs			
$\overline{CP}$	CLR	QA	QB	QC	QD
X	H	L	L	L	L
$\overline{L}$	L	Count Up			
$\overline{H}$	L	No Change			

X: Don't Care

### System Diagram



### Timing Chart



## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	-0.5V to +7.0V
$V_{IN}$	DC Input Voltage	-0.5V to +7.0V
$V_{OUT}$	DC Output Voltage	-0.5V to $V_{CC} + 0.5V$
$I_{IK}$	Input Diode Current	-20mA
$I_{OK}$	Output Diode Current <sup>(4)</sup>	±20mA
$I_{OUT}$	DC Output Current	±25mA
$I_{CC}$	DC $V_{CC}$ /GND Current	±75mA
$T_{STG}$	Storage Temperature	-65°C to +150°C
$T_L$	Lead Temperature (Soldering, 10 seconds)	260°C

## Recommended Operating Conditions<sup>(1)</sup>

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
$V_{CC}$	Supply Voltage	2.0V to +5.5V
$V_{IN}$	Input Voltage	0V to +5.5V
$V_{OUT}$	Output Voltage	0V to $V_{CC}$
$T_{OPR}$	Operating Temperature	-40°C to +85°C
$t_r, t_f$	Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$ $V_{CC} = 5.0V \pm 0.5V$	0 ~ 100ns/V 0 ~ 20ns/V

### Note:

1. Unused inputs must be held HIGH or LOW. They may not float.

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$		Units	
				Min.	Typ.	Max.	Min.	Max.		
$V_{IH}$	HIGH Level Input Voltage	2.0		1.50			1.50		V	
		3.0 – 5.5		$0.7 \times V_{CC}$			$0.7 \times V_{CC}$			
$V_{IL}$	LOW Level Input Voltage	2.0				0.50		0.50	V	
		3.0 – 5.5				$0.3 \times V_{CC}$		$0.3 \times V_{CC}$		
$V_{OH}$	HIGH Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50\mu\text{A}$	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		$I_{OH} = -4\text{mA}$	2.58			2.48		V
		4.5		$I_{OH} = -8\text{mA}$	3.94			3.80		
$V_{OL}$	LOW Level Output Voltage	2.0	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50\mu\text{A}$		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		$I_{OL} = 4\text{mA}$			0.36		0.44	V
		4.5		$I_{OL} = 8\text{mA}$			0.36		0.44	
$I_{IN}$	Input Leakage Current	0 – 5.5	$V_{IN} = 5.5\text{V}$ or GND			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	
$I_{CC}$	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$ or GND			4.0		40.0	$\mu\text{A}$	

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	Conditions	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time (CP-QA)	3.3 ± 0.3	C <sub>L</sub> = 15pF		8.6	13.2	1.0	15.5	ns
			C <sub>L</sub> = 50pF		11.1	16.7	1.0	19.0	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		5.8	8.5	1.0	10.0	
			C <sub>L</sub> = 50pF		7.3	10.5	1.0	12.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time (CP-QB)	3.3 ± 0.3	C <sub>L</sub> = 15pF		10.2	15.8	1.0	18.5	ns
			C <sub>L</sub> = 50pF		12.7	19.3	1.0	22.0	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		6.8	9.8	1.0	11.5	
			C <sub>L</sub> = 50pF		8.3	11.8	1.0	13.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time (CP-QC)	3.3 ± 0.3	C <sub>L</sub> = 15pF		11.7	18.0	1.0	21.0	ns
			C <sub>L</sub> = 50pF		14.2	21.5	1.0	24.5	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		7.7	11.2	1.0	13.0	
			C <sub>L</sub> = 50pF		9.2	13.2	1.0	15.0	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time (CP-QD)	3.3 ± 0.3	C <sub>L</sub> = 15pF		13.0	19.7	1.0	23.0	ns
			C <sub>L</sub> = 50pF		15.5	23.2	1.0	26.5	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		8.5	12.5	1.0	14.5	
			C <sub>L</sub> = 50pF		10.0	14.5	1.0	16.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay Time (CLR-Q <sub>n</sub> )	3.3 ± 0.3	C <sub>L</sub> = 15pF		7.9	12.3	1.0	14.5	ns
			C <sub>L</sub> = 50pF		10.4	15.8	1.0	18.0	
		5.0 ± 0.5	C <sub>L</sub> = 15pF		5.4	8.1	1.0	9.5	
			C <sub>L</sub> = 50pF		6.9	10.1	1.0	11.5	
f <sub>MAX</sub>	Maximum Clock	3.3 ± 0.3	C <sub>L</sub> = 15pF	75	120		65	MHz	
			C <sub>L</sub> = 50pF	45	65		35		
		5.0 ± 0.5	C <sub>L</sub> = 15pF	125	170		105		
			C <sub>L</sub> = 50pF	85	115		75		
C <sub>IN</sub>	Input Capacitance		V <sub>CC</sub> = Open		4	10		10	pF
C <sub>PD</sub>	Power Dissipation Capacitance		(2)		23				pF

**Note:**

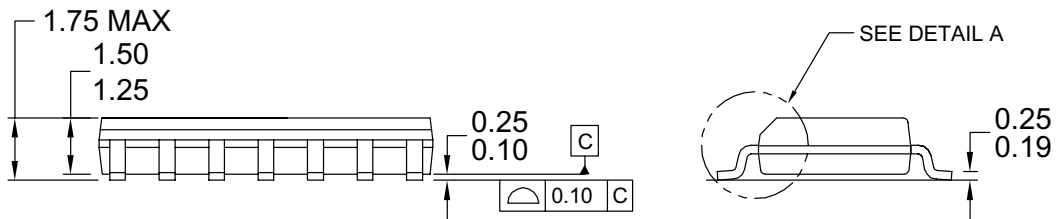
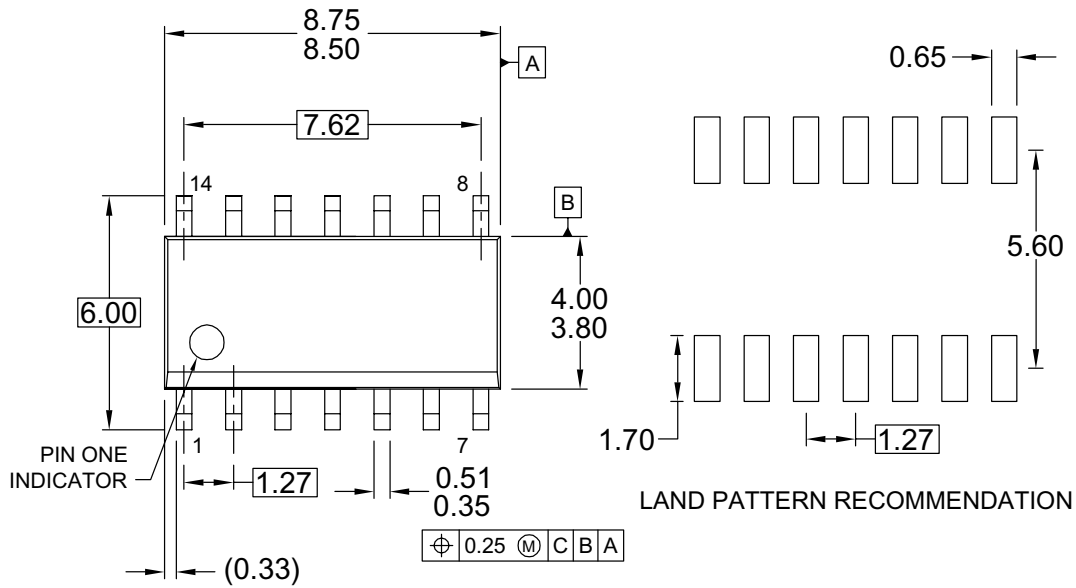
2. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC(Oper.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 2 \text{ (per Counter)}$$

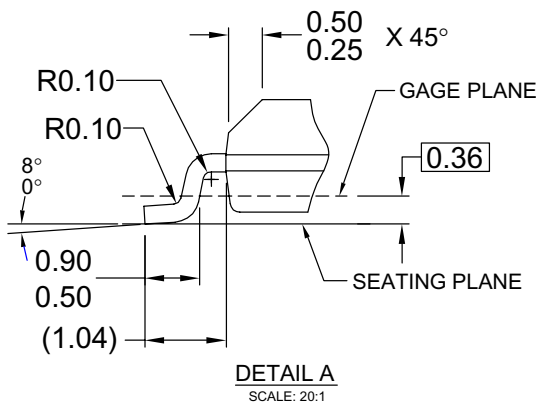
## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to +85°C		Units
			Typ.	Guaranteed Minimum	Guaranteed Minimum	Guaranteed Minimum	
t <sub>W(L)</sub> , t <sub>W(H)</sub>	Minimum Pulse Width (CP)	3.3 ± 0.3		5.0	5.0		ns
		5.0 ± 0.5		5.0	5.0		
t <sub>W(H)</sub>	Minimum Pulse Width (CLR)	3.3 ± 0.3		5.0	5.0		ns
		5.0 ± 0.5		5.0	5.0		
t <sub>REM</sub>	Minimum Removal Time	3.3 ± 0.3		5.0	5.0		ns
		5.0 ± 0.5		4.0	4.0		

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED



- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C,
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X145-14M
- E) DRAWING CONFORMS TO ASME Y14.5M-1994
- F) DRAWING FILE NAME: M14AREV13

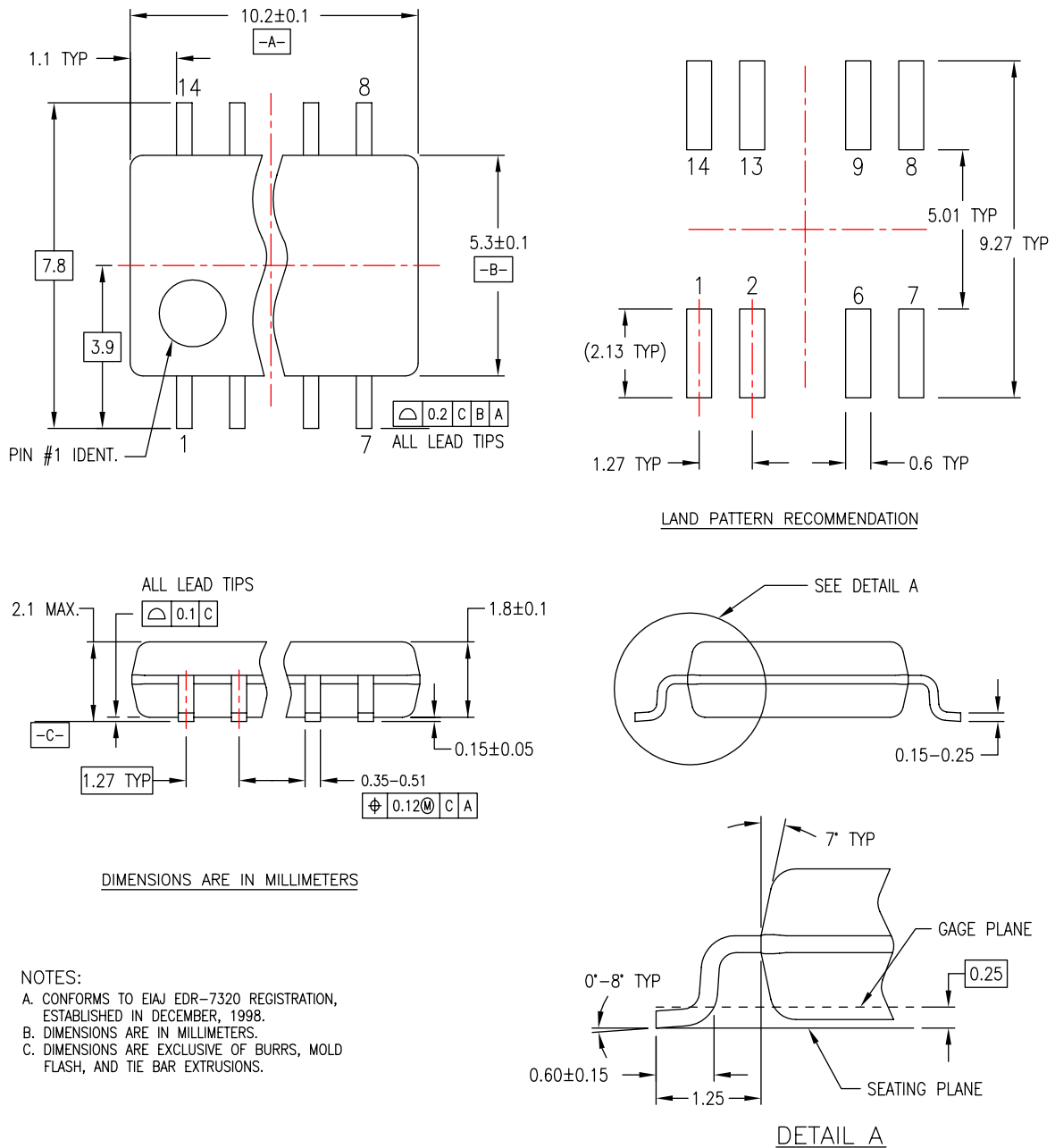
Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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Physical Dimensions (Continued)



M14DREVC

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

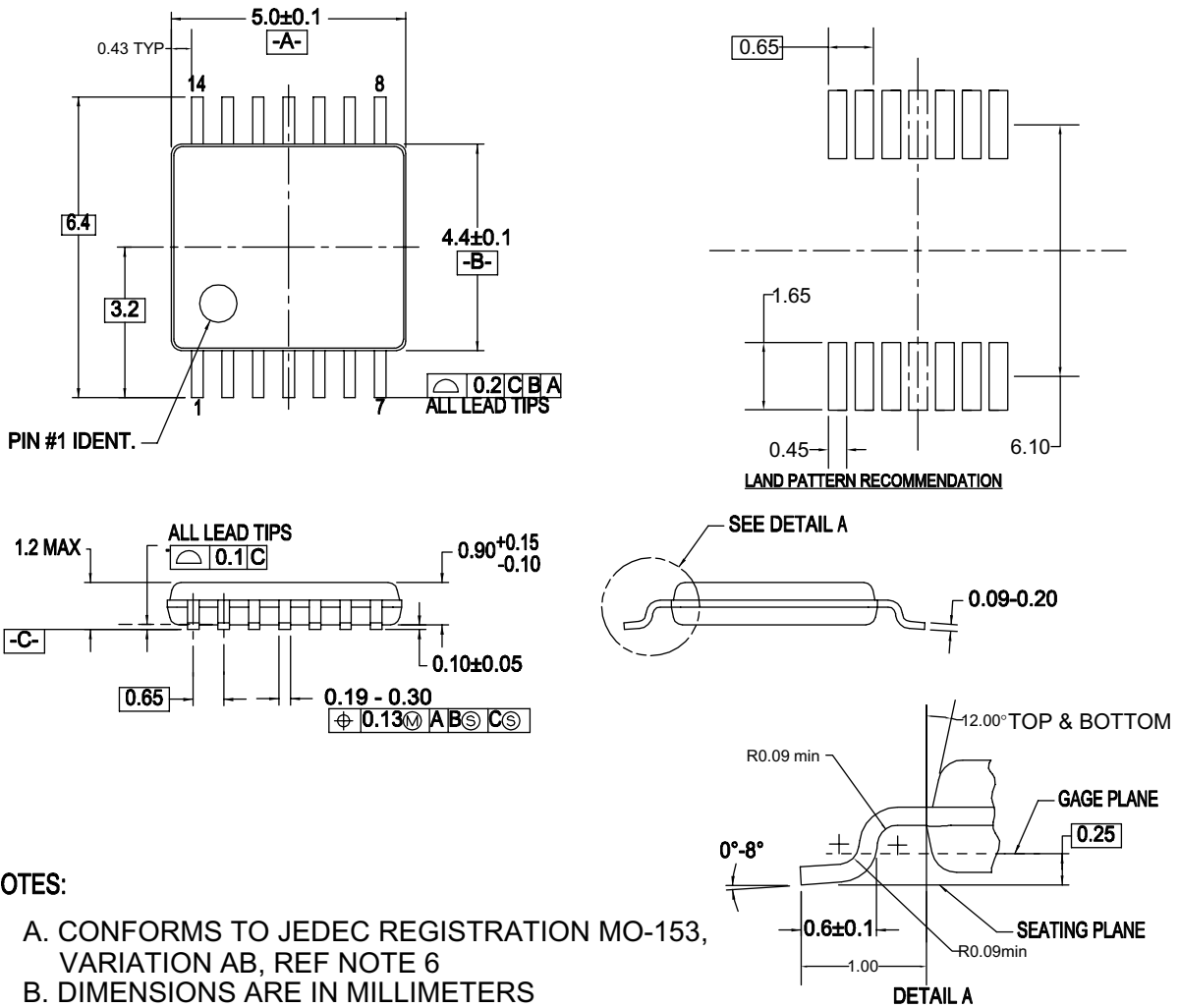
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Physical Dimensions (Continued)



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
- B. DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
- D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
- E. LANDPATTERN STANDARD: SOP65P640X110-14M
- F. DRAWING FILE NAME: MTC14REV6

Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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

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