

Ceramic Balance Filter

50Ω 4650 to 5150 MHz

BBFCV-492+



Generic photo used for illustration purposes only

CASE STYLE: JV1210C-4

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications

Available Tape and Reel at no extra cost

Reel Size	Devices/Reel
7"	20, 50, 100, 200, 500, 1000, 2000

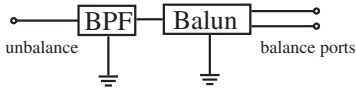
Features

- Small size (0.126"x0.098"x0.039")
- Temperature stable
- Hermetically sealed
- LTCC construction

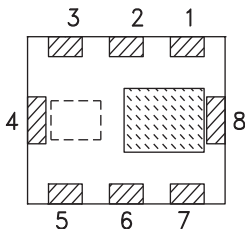
Applications

- 5G
- Cellular

Simplified Schematic



Top View



Pad Connections

Unbalanced Port	7
Balanced Port	3, 5
GND	2, 4, 8
GND or DC Feed	6
NC	1

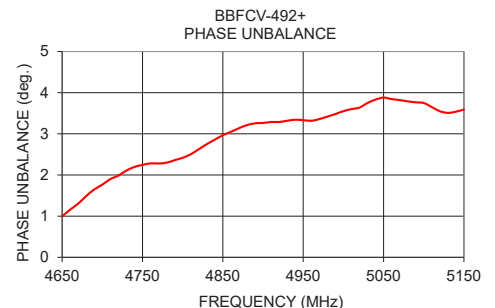
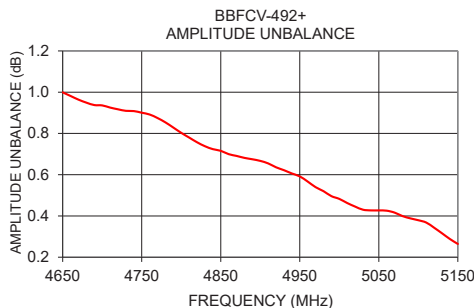
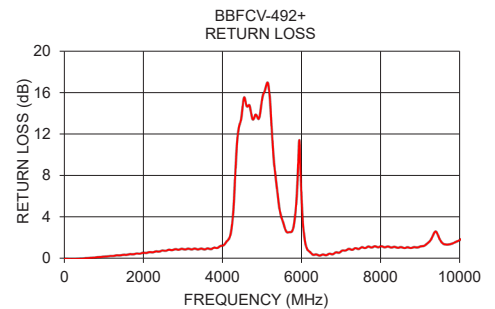
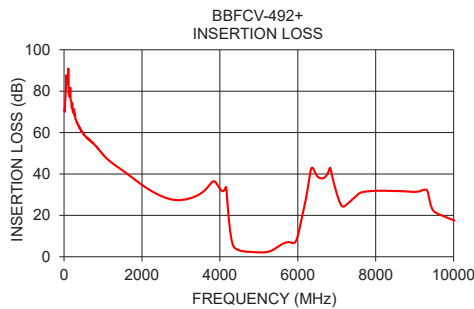
Electrical Specifications at 25°C

Parameter	Frequency (MHz)	Min.	Typ.	Max.	Unit
Impedance Ratio			2:1		
Insertion Loss	4650 - 5150	—	—	3.5	dB
Attenuation	50-1098	28	—	—	dB
	1098-4000	20	—	—	
	6696-8049	22	—	—	
	9645-12750	10	—	—	
Amplitude Unbalance	4650-5150	—	—	1.3	dB
Phase Unbalance	4650-5150	—	—	12	degree
Input VSWR	4650-5150	—	1.67	—	

Maximum Ratings

Operating Temperature	-55°C to +105°C
Storage Temperature ¹	-55°C to +105°C
RF Power Input ²	1W @25°C

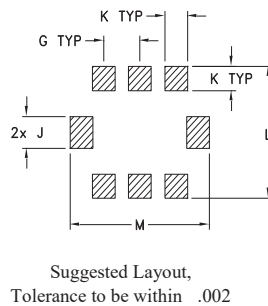
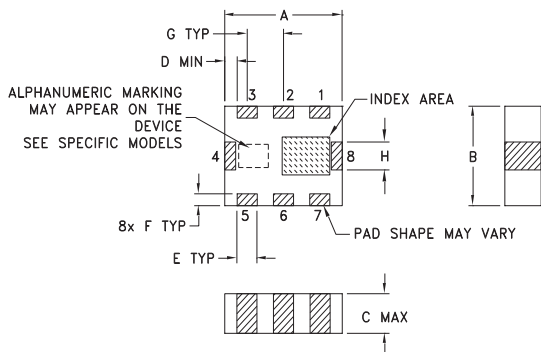
1. Refer to product storage temperature after installation
Suggestion for T&R unused product storage condition: +5 ~ +35 °C, Humidity 45~75%RH, 12 month Max
2. Derate linearly to 0.5W at 85°C



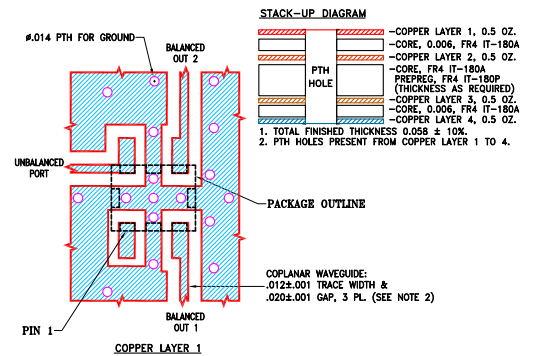
Typical Performance Data

Frequency (MHz)	Insertion Loss (dB)	Return Loss (dB)	Amplitude Unbalance (dB)	Phase Unbalance (Deg.)
10	71.41	0.06	1.38	100.60
50	81.78	0.04	2.23	151.82
100	83.48	0.04	8.13	134.82
500	59.00	0.08	9.62	168.96
1000	49.41	0.26	10.86	120.62
2000	34.69	0.62	1.97	57.65
3000	27.42	1.00	3.11	6.88
3500	30.50	1.00	1.03	40.22
4000	32.88	1.31	3.27	90.58
4650	2.52	14.66	1.00	1.33
5150	2.17	16.82	0.26	3.55
6000	10.14	5.42	0.91	0.65
7000	30.56	0.79	4.17	74.13
8000	31.83	1.25	1.36	63.10
9000	31.36	1.24	4.95	80.75
10000	17.71	1.88	3.06	167.42

Outline Drawing



Demo Board MCL P/N: TB-1053+
Suggested PCB Layout (PL-632)



- NOTES:
- PCB IS MULTILAYER PCB, SEE STACK-UP DIAGRAM.
 - TRACE WIDTH & GAP PARAMETERS ARE SHOWN FOR FR4 IT-180A WITH DIELECTRIC THICKNESS .006"±.0007"; COPPER: 1/2 OZ. FOR OTHER MATERIALS TRACE WIDTH AND GAP MAY NEED TO BE MODIFIED.
 - LAYERS 2,3,4 OF THE PCB ARE CONTINUOUS GROUND PLANE.

■ DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK

Outline Dimensions (inch/mm)

A	B	C	D	E	F	G
.126	.098	.039	.004	.022	.012	.039
3.2	2.5	1.0	0.1	0.56	0.3	1.0
H	J	K	L	M	wt	
.028	.031	.024	.130	0.15	grams	
0.7	0.8	0.6	3.30	3.81	0.030	

Additional Notes

- Performance and quality attributes and conditions not expressly stated in this specification document are intended to be excluded and do not form a part of this specification document.
- Electrical specifications and performance data contained in this specification document are based on Mini-Circuit's applicable established test performance criteria and measurement instructions.
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