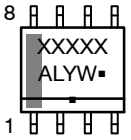
NCP4355

Secondary Side SMPS OFF Mode Controller for Low Standby Power

ON Semiconductor®

http://onsemi.com

SOIC−8
D SUFFIX
CASE 751



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 16 of this data sheet.

Description

The NCP4355 is a secondary side SMPS controller designed for use in applications which require extremely low no load power consumption. The device is capable of detecting “no load” conditions and entering the power supply into a low consumption OFF mode. During OFF mode, the primary side controller is turned off and energy is provided by the output capacitors thus eliminating the power consumption required to maintain regulation. During OFF mode, the output voltage relaxes and is allowed to decrease to an adjustable level. Once more energy is required, the NCP4355 automatically restarts the primary side controller by ONOFF current that flows through ONOFF optocoupler. The NCP4355 controls the primary controller with an “Active ON” signal, meaning that it only drives optocoupler current during ON mode to minimize consumption during OFF mode.

During normal power supply operation, the NCP4355 provides integrated voltage feedback regulation, replacing the need for a shunt regulator. The A and C versions include a current regulation loop in addition to voltage regulation.

The NCP4355 includes a LED driver pin (except C version) implemented with an open drain MOSFET driven by a 1 kHz square wave with a 12.5% duty cycle for indication purpose.

The NCP4355 is available in SOIC−8 package.

DEVICE OPTIONS

	NCP4355A	NCP4355B	NCP4355C
Adjustable Vmin	No	Yes	Yes
Current Regulation	Yes	No	Yes
LED driver	Yes	Yes	No

Features

- Operating Input Voltage Range: 3.5 V to 36.0 V
- Supply Current < 100 μA
- ±0.5% Reference Voltage Accuracy (T_J = 25°C)
- Constant Voltage and Constant Current (A and C versions) Control Loop
- Indication LED PWM Modulated Driver (except NCP4355C)
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Offline Adapters for Notebooks, Game Stations and Printers
- High Power AC–DC Converters for TVs, Set−Top Boxes, Monitors etc.

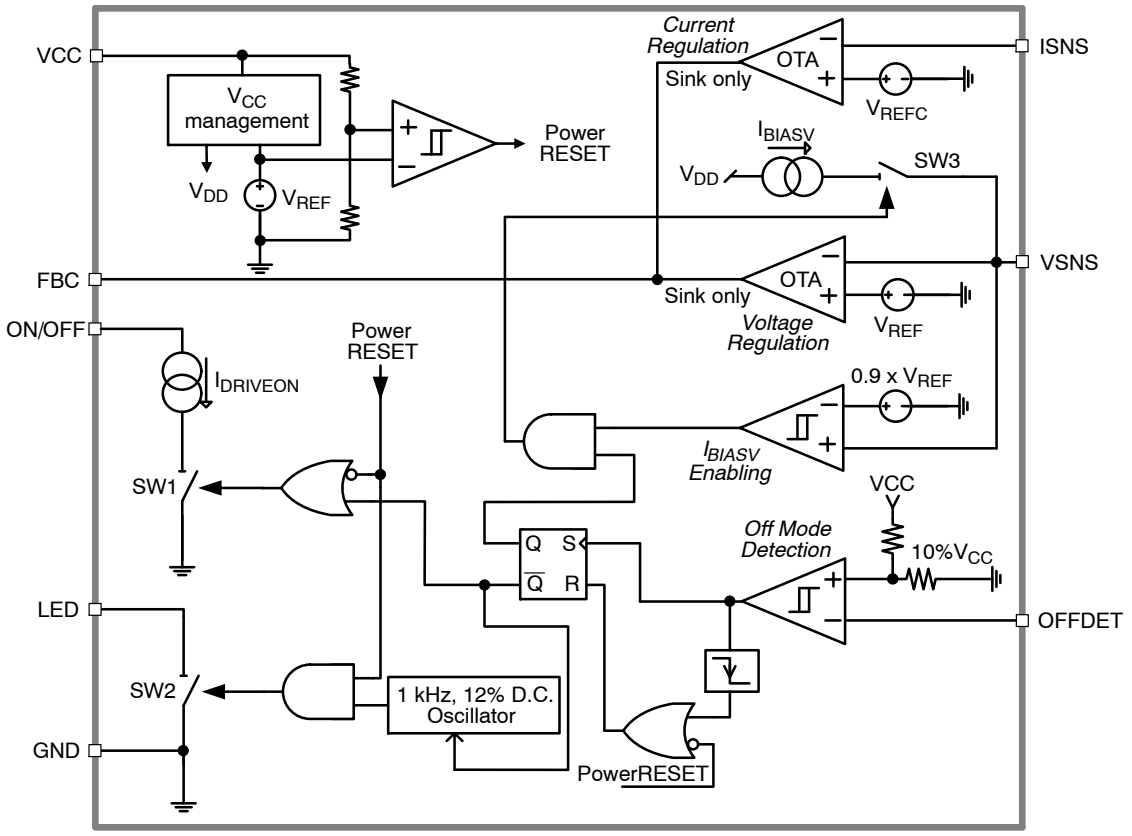


Figure 1. Simplified Block Diagram − NCP4355A

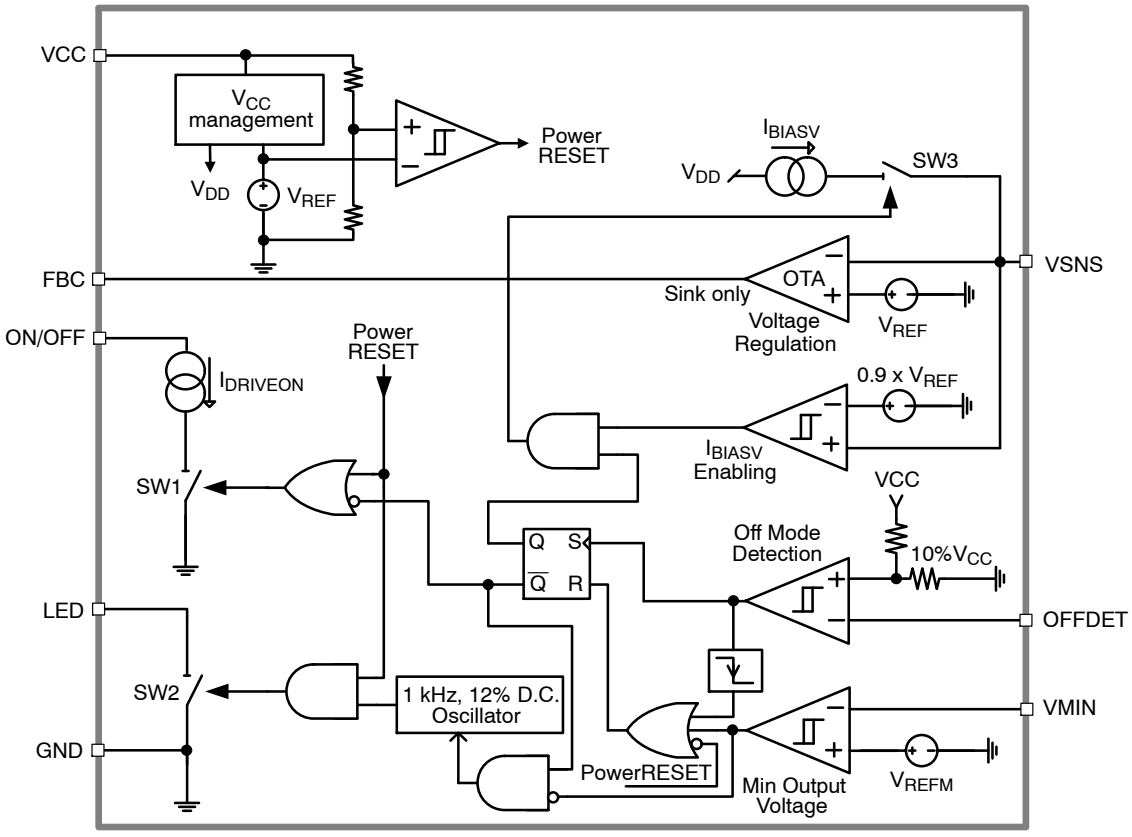


Figure 2. Simplified Block Diagram − NCP4355B

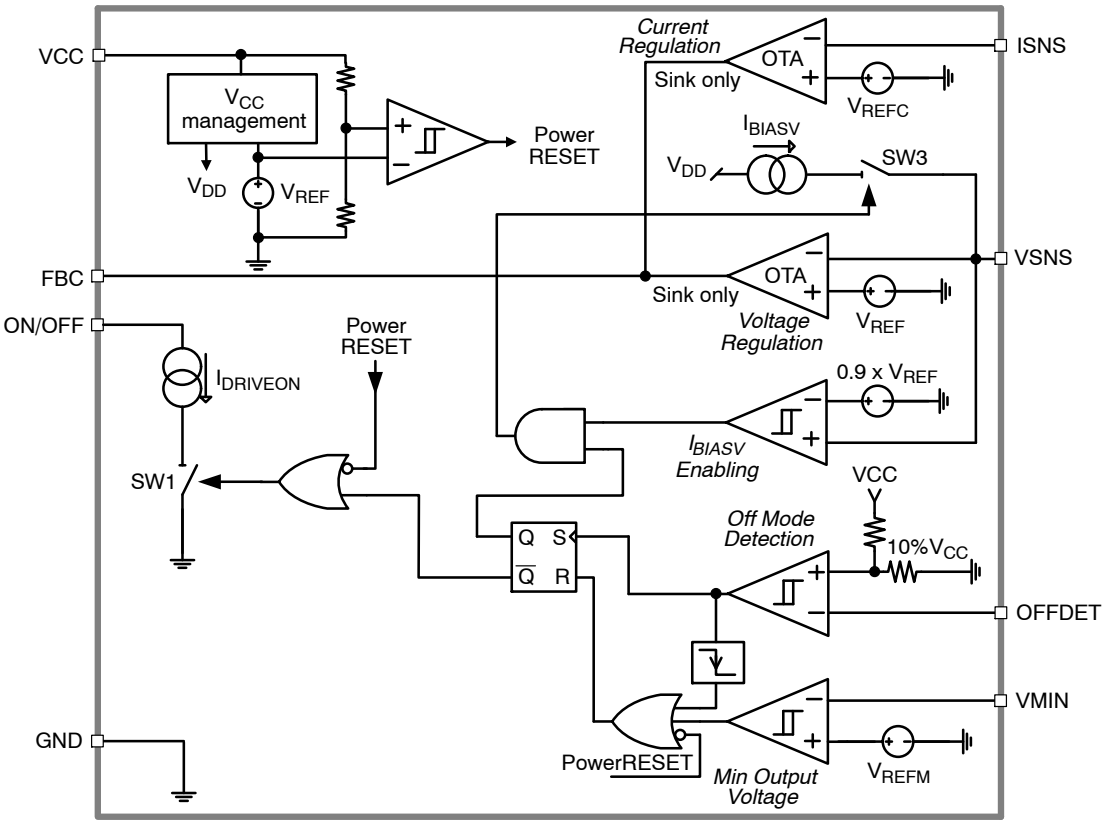


Figure 3. Simplified Block Diagram − NCP4355C

PIN FUNCTION DESCRIPTION

NCP4355A	NCP4355B	NCP4355C	Pin Name	Description
8	8	8	VCC	Supply voltage pin
7	7	7	GND	Ground
1	1	1	VSNS	Output voltage sensing pin, connected to output voltage divider
2	2	2	OFFDET	OFF mode detection input. Voltage divider provides adjustable off mode detection threshold
–	3	3	VMIN	Minimum output voltage adjustment
3	–	4	ISNS	Current sensing input for output current regulation, connect it to shunt resistor in ground branch.
4	4	–	LED	PWM LED driver output. Connected to LED cathode with current define by external serial resistance
6	6	6	FBC	Output of current sinking OTA amplifier or amplifiers driving feedback optocoupler's LED. Connect here compensation network (networks) as well.
5	5	5	ON/OFF	ON mode current sink. This output keeps primary control pin at low level in on mode.

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input Voltage		V_{CC}	−0.3 to 40.0	V
ON/OFF, FBC, LED Voltage		V_{ONOFF}, V_{FBC}, V_{LED}	−0.3 to V_{CC} + 0.3	V
VSNS, ISNS, OFFDET, VMIN Voltage		V_{SNS}, V_{ISNS}, V_{OFFDET}, V_{MIN}	−0.3 to 10.0	V
LED Current		I_{LED}	10	mA
Thermal Resistance − Junction−to−Air (Note 1)	NCP4355A/C NCP4355B	$R_{\theta JA}$	260 277	°C/W
Junction Temperature		T_J	−40 to 150	°C
Storage Temperature		T_{STG}	−60 to 150	°C
ESD Capability, Human Body Model (Note 2)		ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)		ESD_{MM}	250	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 50 mm^2, 1.0 oz. Copper spreader.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22−A114F
   ESD Machine Model tested per JESD22−A115C
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78D.

ELECTRICAL CHARACTERISTICS

$0°C \le T_J \le 125°C$; V_{CC} = 15 V; unless otherwise noted. Typical values are at T_J = +25°C.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum Operating Input Voltage		V_{CC}			36.0	V
VCC UVLO	V_{CC} rising	V_{CCUVLO}	3.75	4.00	4.25	V
	V_{CC} falling		3.22	3.50	3.78	
VCC UVLO Hysteresis		$V_{CCUVLOHYS}$	0.4	0.5		V
Quiescent Current In Regulation	NCP4355A	I_{CC}		125	155	μA
	NCP4355B			107	135	
	NCP4355C			115	155	
Quiescent Current In OFF mode	V_{SNS} < 1.12 V	I_{CCOFF}		90	110	μA
VOLTAGE CONTROL LOOP OTA						
Transconductance	Sink current only	gm_V		1		S
Reference Voltage	3.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 25°C	V_{REF}	1.244	1.250	1.256	V
	3.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 0 – 85°C		1.240	1.250	1.264	
	3.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 0 – 125°C		1.230	1.250	1.270	
Sink Current Capability	In regulation, V_{FBC} > 1.5 V	I_{SINKV}	2.5			mA
	In OFF mode, V_{FBC} > 1.5 V		1.2	1.5	2.0	mA
Inverting Input Bias Current	In regulation	I_{BIASV}	−100		100	nA
	In OFF mode, V_{SNS} > 1.12 V		−2.6	−2.3	−1.9	μA
Inverting Input Bias Current Threshold	In OFF mode	$V_{SNSBIASTH}$	1.07	1.12	1.17	V
CURRENT CONTROL LOOP OTA (except NCP4355B)						
Transconductance	Sink current only	gm_C		3		S
Reference Voltage		V_{REFC}	60.0	62.5	65.0	mV
Sink Current Capability	V_{FBC} > 1.5 V	I_{SINKC}	2.5			mA
Inverting Input Bias Current	I_{SNS} = V_{REFC}	I_{BIASC}	−100		100	nA
MINIMUM VOLTAGE COMPARATOR (except NCP4355A)						
Threshold Voltage		V_{REFM}	355	377	400	mV
Hysteresis	Output change from logic high to logic low	V_{MINH}		40		mV
OFF MODE DETECTION COMPARATOR						
Threshold Value	2.5 V ≤ V_{CC} ≤ 36.0 V	$V_{OFFDETTH}$		10% V_{CC}		V
	V_{CC} = 15 V		1.47	1.50	1.53	V
Hysteresis	Output change from logic high to logic low	$V_{OFFDETH}$		40		mV
LED DRIVER (except NCP4355C)						
Switching Frequency		f_{SWLED}		1		kHz
Duty Cycle		D_{LED}	10.0	12.5	15.0	%
Switch Resistance	I_{LED} = 5 mA	R_{SW2}		50		Ω
ON MODE CONTROL						
Sink Current	In ON mode, V_{ONOFF} > 0.6 V	$I_{DRIVEON}$	140	160	180	μA

TYPICAL CHARACTERISTICS

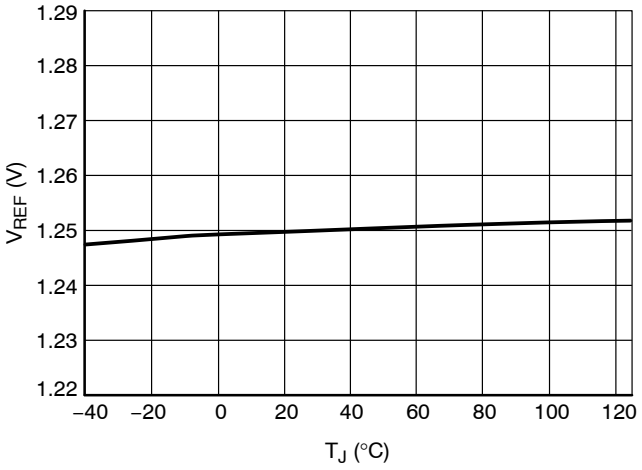


Figure 4. V_{REF} at V_{CC} = 15 V

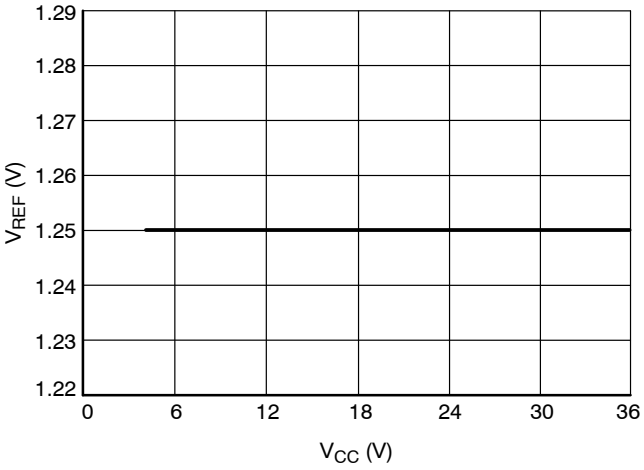


Figure 5. V_{REF} at T_J = 25°C

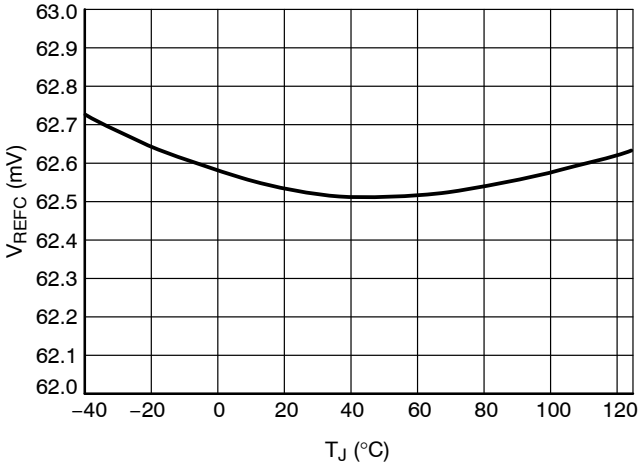


Figure 6. V_{REFC} at V_{CC} = 15 V

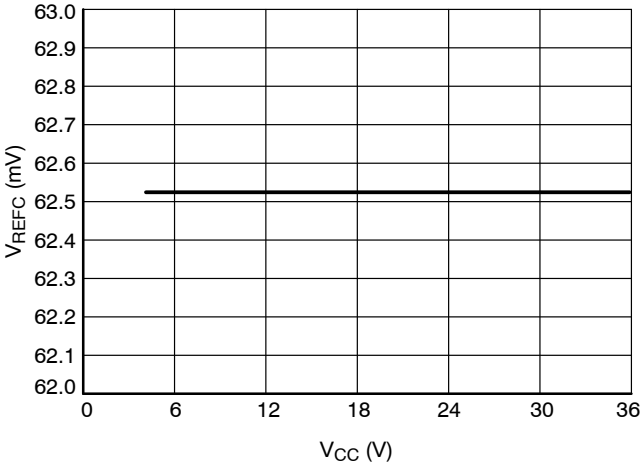


Figure 7. V_{REFC} at T_J = 25°C

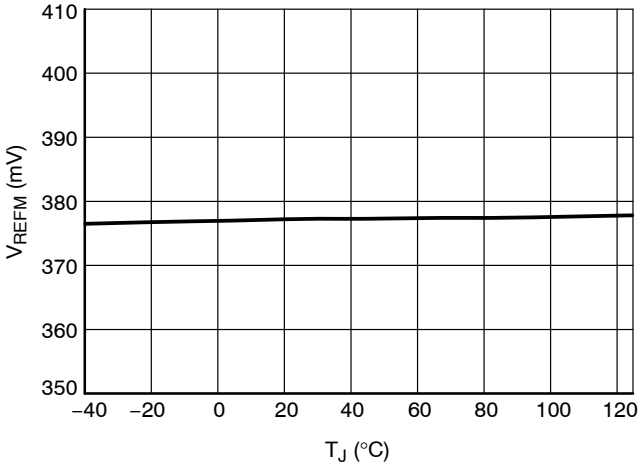


Figure 8. V_{REFM} at V_{CC} = 15 V

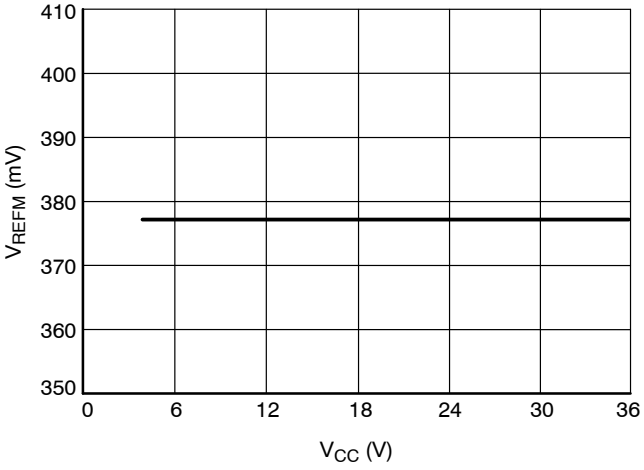


Figure 9. V_{REFM} at T_J = 25°C

TYPICAL CHARACTERISTICS

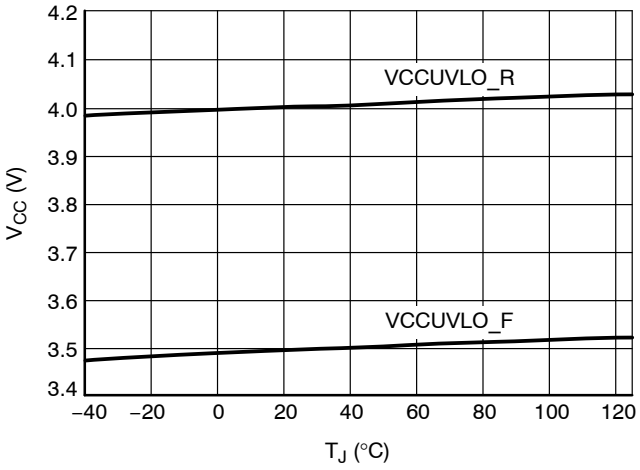


Figure 10. V_{CCUVLO}

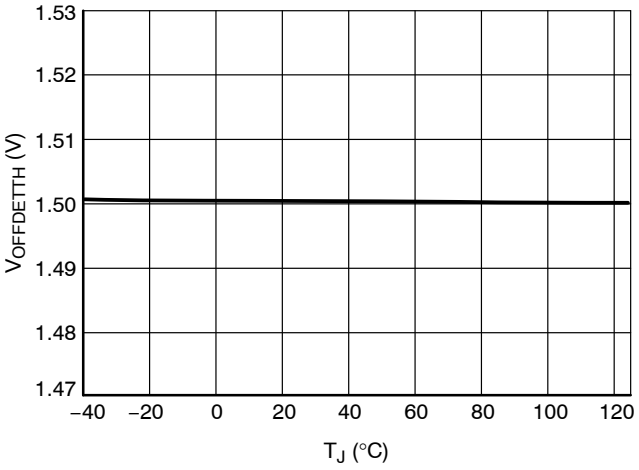


Figure 11. $V_{OFFDETTH}$ at V_{CC} = 15 V

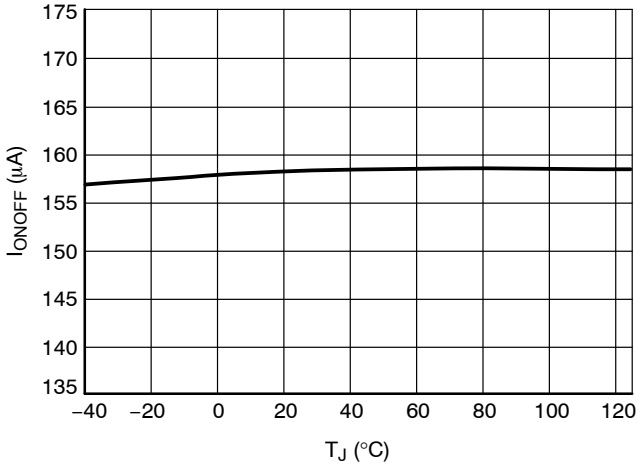


Figure 12. I_{ONOFF} at V_{CC} = 15 V

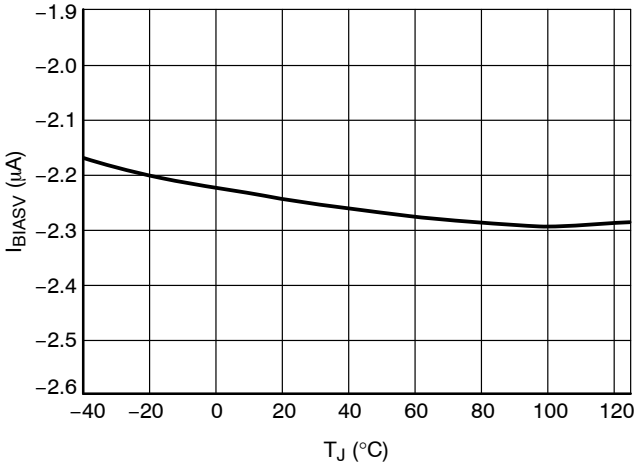


Figure 13. I_{BIASV} at V_{CC} = 15 V, $V_{SNS} > V_{SNSBIASTH}$

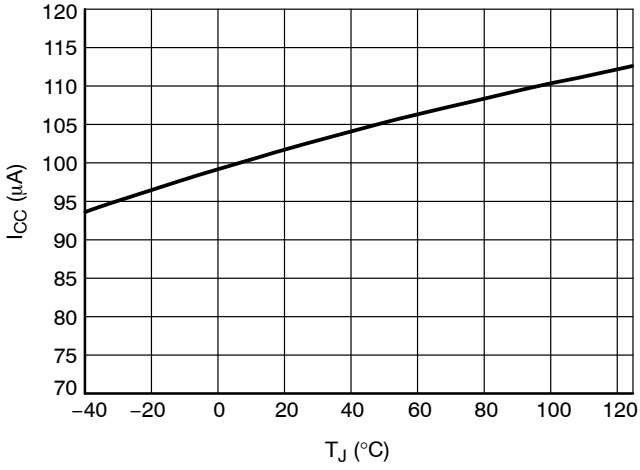


Figure 14. I_{CC} in Regulation at V_{CC} = 15 V for NCP4355B

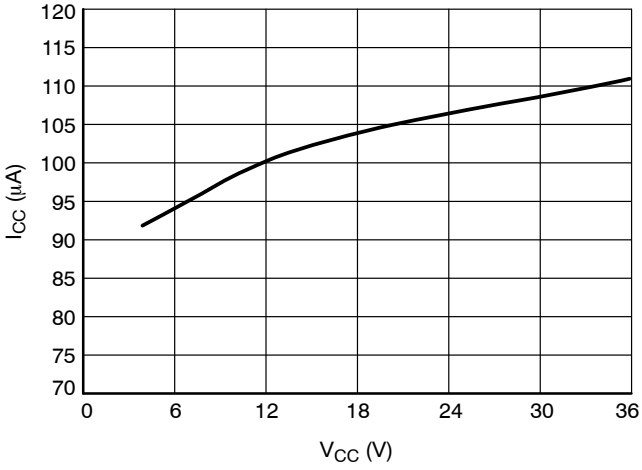


Figure 15. I_{CC} in Regulation at T_J = 25°C for NCP4355B

TYPICAL CHARACTERISTICS

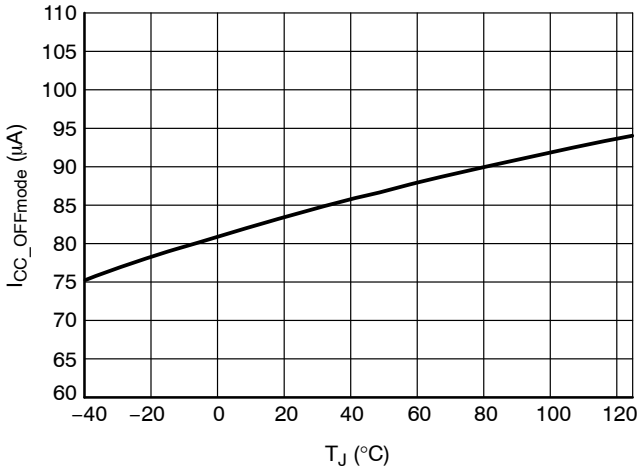


Figure 16. I_{CC} in OFF Mode at V_{CC} = 15 V, V_{SNS} < $V_{SNSBIASTH}$, for NCP4355B

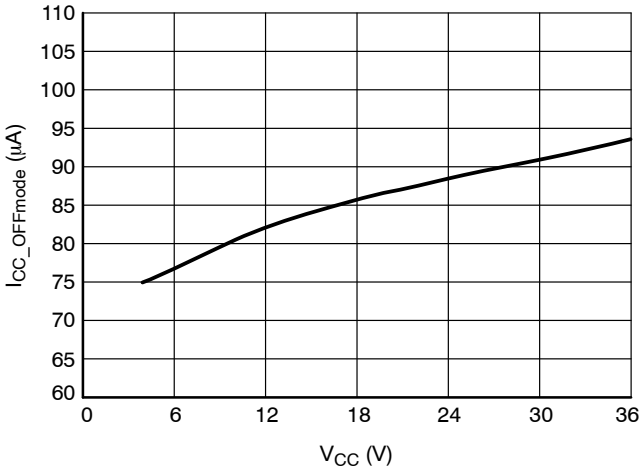


Figure 17. I_{CC} in OFF Mode at T_J = 25°C, V_{SNS} < $V_{SNSBIASTH}$, for NCP4355B

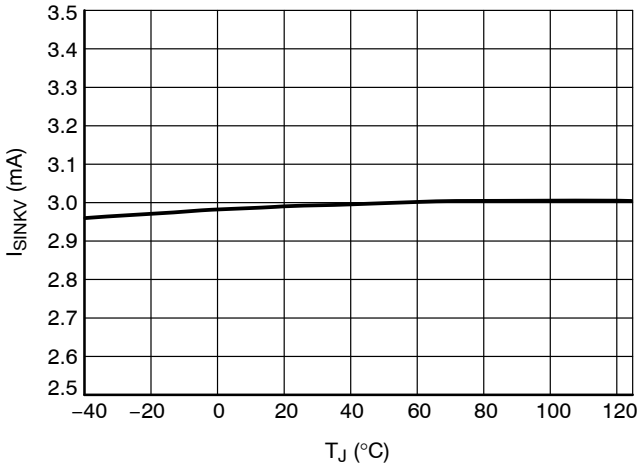


Figure 18. Voltage OTA Current Sink Capability in Regulation

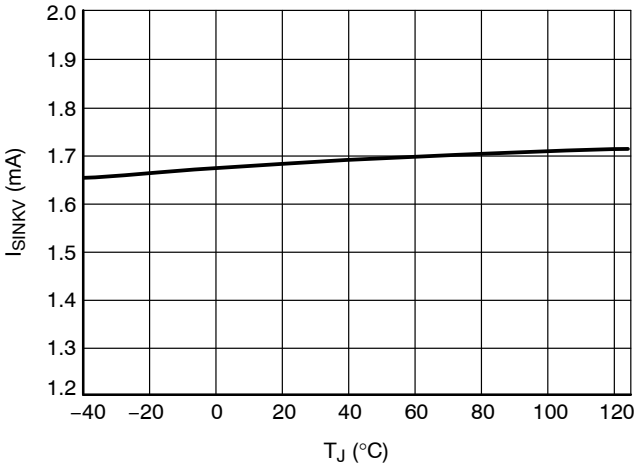


Figure 19. Voltage OTA Current Sink Capability in OFF Mode

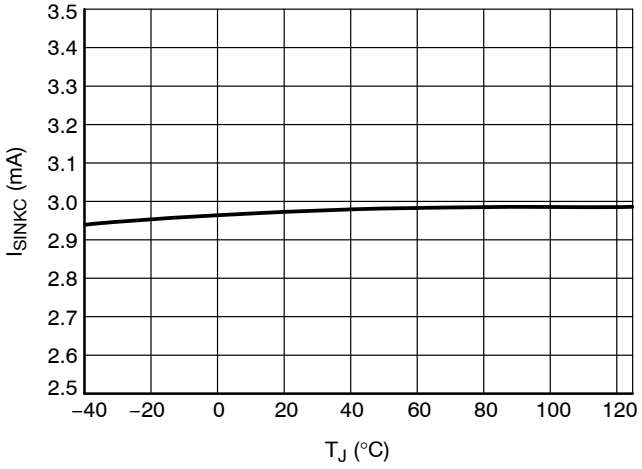


Figure 20. Current OTA Current Sink Capability

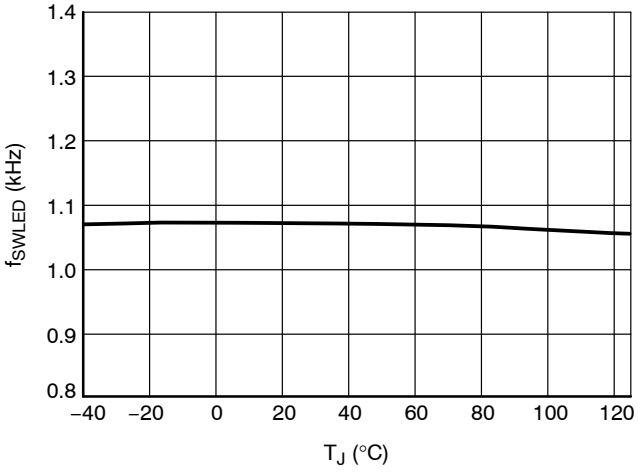


Figure 21. LED Switching Frequency at V_{CC} = 15 V

TYPICAL CHARACTERISTICS

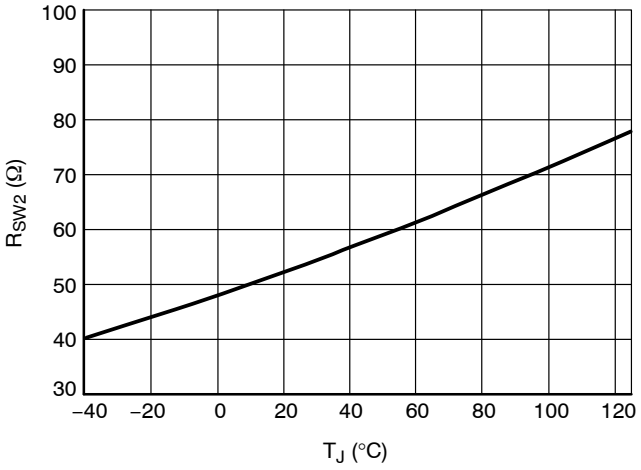


Figure 22. R_{SW2} at V_{CC} = 15 V

APPLICATION INFORMATION

Typical application circuits for NCP4355x are shown in Figure 24, Figure 25 and Figure 26. Each IC version contains different features. Please see Device options table or Block diagrams for detail information. NCP4355A does not have a VMIN pin for setting the minimum voltage level, therefore it needs a special circuit shown in Figure 24 in the dashed box. This is needed for correct detection of load connection in OFF mode. The same circuit can be used for other versions when high speed detection of load connection is needed.

Supply Voltage

The IC is supplied through VCC pin. Supply voltage should be taken from output voltage in range from 4.5 V up to 36 V. Power supply voltage should be separated from output voltage by a diode D3 and some energy should be stored in a VCC cap C6. Cap should be high enough to keep enough energy for ONOFF optocoupler and NCP4355x before primary controller is started. Time constant of the VCC cap C6 and the IC supply current should be smaller than time constant of power supply output filter and maximum output current in OFF mode. VCC pin should also be decoupled by 100 nF decoupling cap C5.

Voltage Regulation Path

The output voltage is detected on the VSNS pin by the R4, R5 and R6 voltage divider. This voltage is compared with the internal precise voltage reference. The voltage difference is amplified by gm_V of the transconductance amplifier. The amplifier output current is connected to the FBC pin. The compensation network is also connected to this pin to provide frequency compensation for the voltage regulation path. This FBC pin drives an optocoupler that provides regulation of primary side. The optocoupler is supplied via direct connection to VOUT line through resistor R1.

Regulation information is transferred through the optocoupler to the primary side controller where its FB pin is usually pulled down to reduce energy transferred to secondary output.

The VSNS voltage divider is shared with VMIN voltage divider. The shared voltage divider can be connected in two ways as shown in Figure 23. The divider type is selected based on the ratio between V_{MIN} and V_{OUT}. When the condition of Equation 1 is true, divider type 1 should be used.

$$V_{MIN} > \frac{V_{OUT} \times V_{REFM}}{V_{REF}} \quad \text{(eq. 1)}$$

Output voltage for divider type 1 can be computed by Equation 2

$$V_{OUT} = V_{REF}\frac{R4 + R5 + R6}{R5 + R6} \quad \text{(eq. 2)}$$

and for type 2 by Equation 3.

$$V_{OUT} = V_{REF}\frac{R4 + R5 + R6}{R6} \quad \text{(eq. 3)}$$

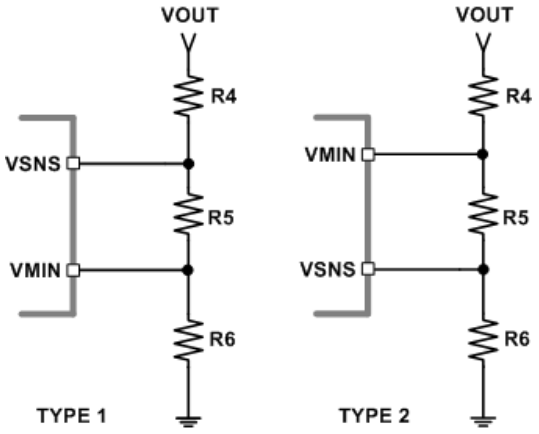


Figure 23. Shared Dividers Type

Current Regulation Path (A and C versions only)

The output current is sensed by the shunt resistor R11 in series with the load. Voltage drop on R11 is compared with internal precise voltage reference V_{REFC} at I_{SNS} transconductance amplifier input.

Voltage difference is amplified by gm_C to output current of amplifier, connected to FBC pin. Compensation network is connected between this pin and ISNS input to provide frequency compensation for current regulation path. Resistor R12 separates compensation network from sense resistor. Compensation network works into low impedance without this resistor that significantly decreases compensation network impact.

Current regulation point is set to current given by Equation 4.

$$I_{OUTLIM} = \frac{V_{REFC}}{R11} \quad \text{(eq. 4)}$$

OFF Mode Detection

OFF mode operation is advantageous for ultra low or zero output current condition. The very long off time and the ultra low power mode of the whole regulation system greatly reduces the overall consumption.

The output voltage is varying between nominal and minimal in OFF mode. When output voltage decreases below set (except NCP4355A) minimum level, primary controller is switch on until output capacitor C1 is charged again to the nominal voltage.

The OFF mode detection is based on comparison of output voltage and voltage loaded with fixed resistances (D2, C2, R7 and R8). Figure 27 shows detection waveforms. When output voltage is loaded with very low current, primary controller goes into skip mode (primary controller stops switching for some time). While output capacitor C1 is discharged very slowly (no load condition), a fixed load R7 and R8 discharges the capacitor C2 faster than load current discharges output voltage on C1.

Once OFFDET pin voltage is lower than $V_{OFFDETTH}$ (this threshold is derived from V_{CC} that is very close to V_{OUT}),

OFF mode is detected. In OFF mode SW1 is switched off and no I_{ONOFF} current is going through ON/OFF pin. The primary controller's REM pin voltage increases and primary IC goes in to off mode.

I_{BIASV} current flow from VSNS pin to feedback divider is also activated when OFF mode is detected. This current increases voltage at VSNS pin and due to it voltage OTA sinks reduced current through regulation optocoupler. OTA stops to sink current when VSNS voltage drops below V_{REF}. I_{BIASV} current disappears when VSNS voltage is lower than 90% of V_{REF}. This feature helps to avoid primary side switching when OFF mode is detected at secondary side and primary side is waiting for correct information at REM pin.

Minimum Output Voltage Detection (except NCP4355A)

Minimum output voltage level defines primary controller restart from OFF mode. It can be set by shared voltage divider with voltage regulation loop. When VMIN voltage drops below V_{REFM}, OFF mode is ended and primary controller restarts.

NCP4355A has no external adjustment and uses the internal minimum voltage level specified by minimum falling operation supply voltage and special load detection circuit for faster detection of load connection (T2, R16 and R17 at Figure 24). Principe of load connection detection is that when load is connected, output capacitor C1 is discharged faster than C6 capacitor by IC supply current. Voltage across D3 increases and when there is enough voltage to open T2 some current is injected into OFFDET divider. Voltage at OFFDET pin goes above 10% of V_{CC} and OFF mode ends. This circuit can also be used with B and C versions to dramatically speed up wakeup time from OFF mode. If this circuit is not used, it is necessary to wait for C6 discharge below VCC UVLO falling level before the primary controller is restarted.

LED Driver (except NCP4355C)

LED driver is active when VCC is higher than V_{CCMIN} and output voltage is in regulation (it is off during OFF mode). LED driver consists of an internal power switch controlled by PWM modulated logic signal and an external current limiting resistor R3. LED current can be computed by Equation 5

$$I_{LED} = \frac{V_{OUT} - V_{F\_LED}}{R3} \qquad \text{(eq. 5)}$$

PWM modulation is used to increase efficiency of LED.

Operation in OFF Mode Description

Operation waveforms in off mode and transition into OFF mode with primary controller are shown in Figure 28.

Figure shows waveforms from the first start (1) of the convertor. At first, primary controller charges VCC capacitor over the V_{CCON} level (2). When primary V_{CC} is over this level (3), primary controller starts to operate and V_{OUT} is slowly rising according to primary controller start up ramp to nominal voltage (4). When V_{OUT} is high enough, VCC capacitor is charged from auxiliary winding.

Primary FB pin voltage is above regulation range until V_{OUT} is at set level. Once V_{OUT} is at set level, the secondary controller starts to sink current from optocoupler LED's and primary FB voltage is stabilized in regulation region. With nominal output power (without skip mode) OFFDET pin voltage is higher than $V_{OFFDETTH}$ (typically 10% of V_{CC}).

After some time, the load current decreases to low level (5) and primary convertor uses skip mode (6) to keep regulation of output voltage at set level and save some energy. The skip mode consists of few switching cycles followed by missing ones to provide limited energy by light load. The number of missing cycles allows regulation for any output power.

While both C1 and C2 are discharged during the missing cycles, C2 discharge will be faster than C1 without output current, V_{OFFDET} drops below $V_{OFFDETTH}$ and OFF mode is detected (7). This situation is shown in Figure 27 in detail. When OFF mode is detected, current into ONOFF pin stops to flow (7) and voltage at primary REM pin increases over threshold level that forces primary controller into OFF mode. Internal pull−up current I_{BIASV} is switched on (7), VSNS pin voltage increases (thanks to I_{BIASV}) and voltage amplifier sinks reduced current at time (8), when VSNS is higher than V_{REF} (9), to keep primary FB voltage below switching level until REM pin voltage is high enough. I_{BIASV} current stops when VSNS voltage drops below 90% of V_{REF}.

Discharging of C1 continues (10) until output voltage drops below level set by voltage divider at VMIN pin (except NCP4355A where minimum V_{OUT} is defined only by VCC UVLO) (11). ONOFF current starts to flow, primary REM voltage decreases and primary VCC voltage is rising (12). Primary controller starts to operate, when VCC voltage is enough and FB voltage is at regulation area (13). Output capacitor C1 is recharged (14) to set voltage. If there is still light load condition primary controller goes to skip mode (15) again and after some time secondary controller detects OFF mode by very light or no load condition (16) and whole cycle is repeated.

Fast Restart From OFF Mode

The IC ends OFF mode when a load is connected to the output and V_{OUT} is discharged to V_{MIN} level. There exists another connection that allows transition to normal mode faster without waiting some time for V_{OUT} to discharge to V_{MIN} (it is necessary to use it with NCP4355A). This schematic is shown at Figure 24 in dashed box. The basic idea is that C6 is discharged by the IC faster than C1 by output load in OFF mode. When an output load is applied, capacitor C1 is discharged faster and this creates the voltage drop at D3. When there is enough voltage at D3, T2 is conducting and current is injected into the OFFDET divider through R16. OFFDET voltage higher than 10% of V_{CC} ends OFF mode and ON/OFF current starts to flow. Primary controller leaves OFF mode because voltage at REM pin increase above OFF mode detection threshold.

Normal operation waveforms for typical load detection connection and improved load detection waveforms are shown in Figure 29. Figure 30 shows waveforms for NCP4355A (without VMIN detection) in OFF mode and when load is connected during OFF mode. It can be seen that the application is waiting not for low V_{OUT}, but for low V_{CC} and then OFF mode is ended.

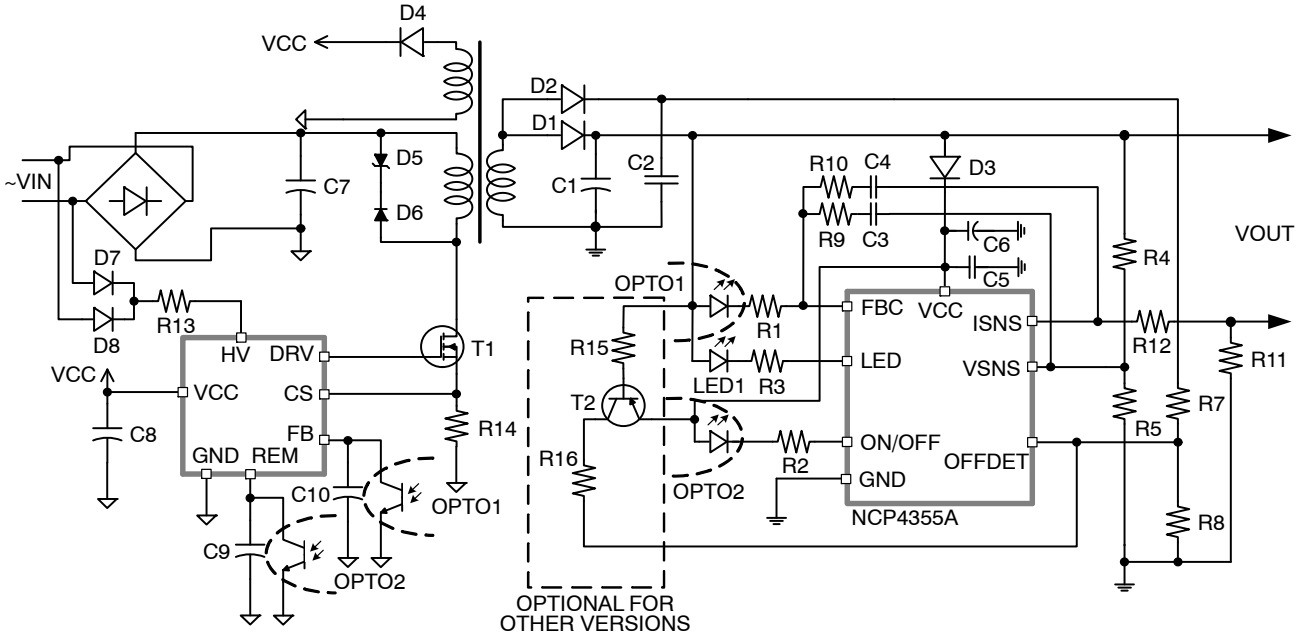


Figure 24. Typical Application Schematic for NCP4355A

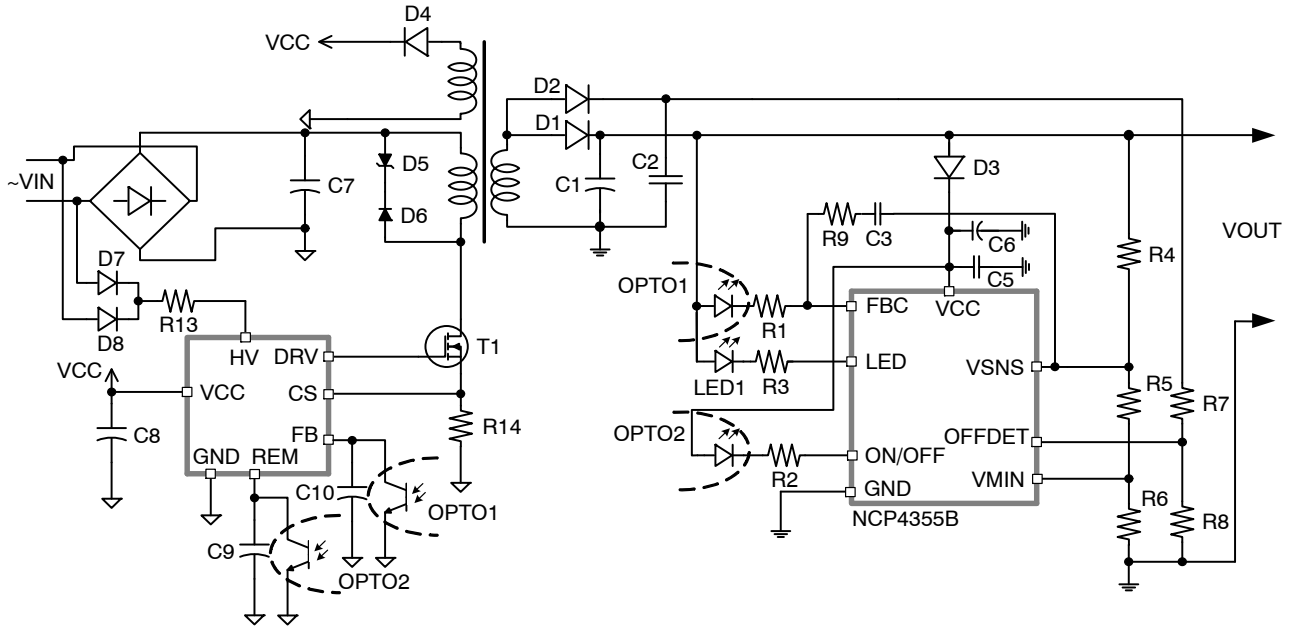


Figure 25. Typical Application Schematic for NCP4355B

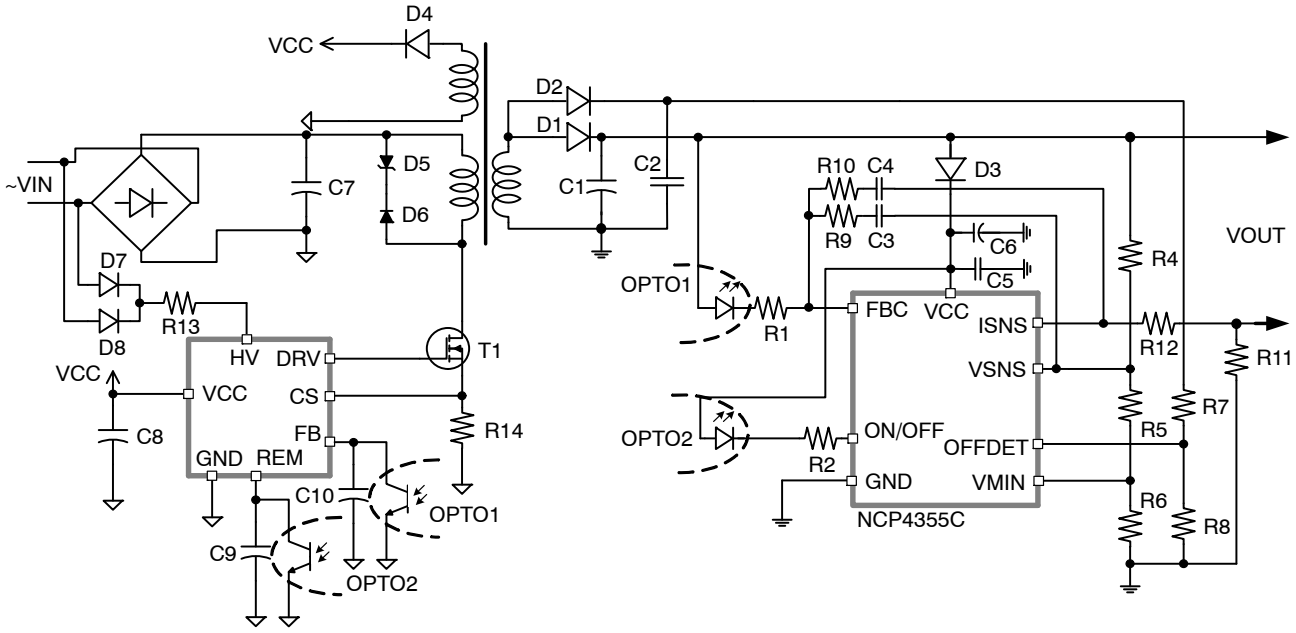


Figure 26. Typical Application Schematic for NCP4355C

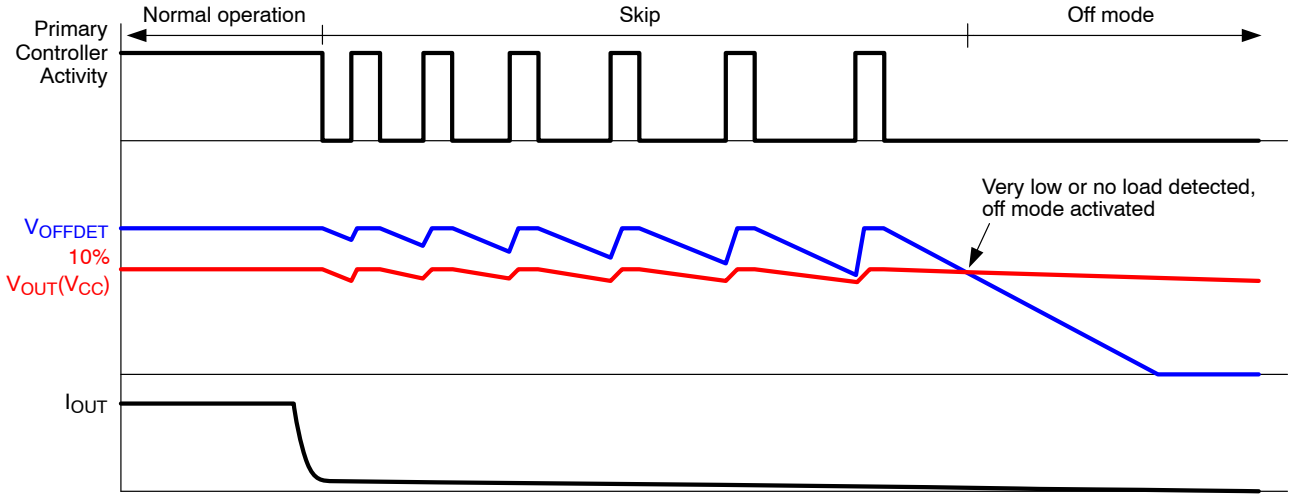


Figure 27. OFF Mode Detection

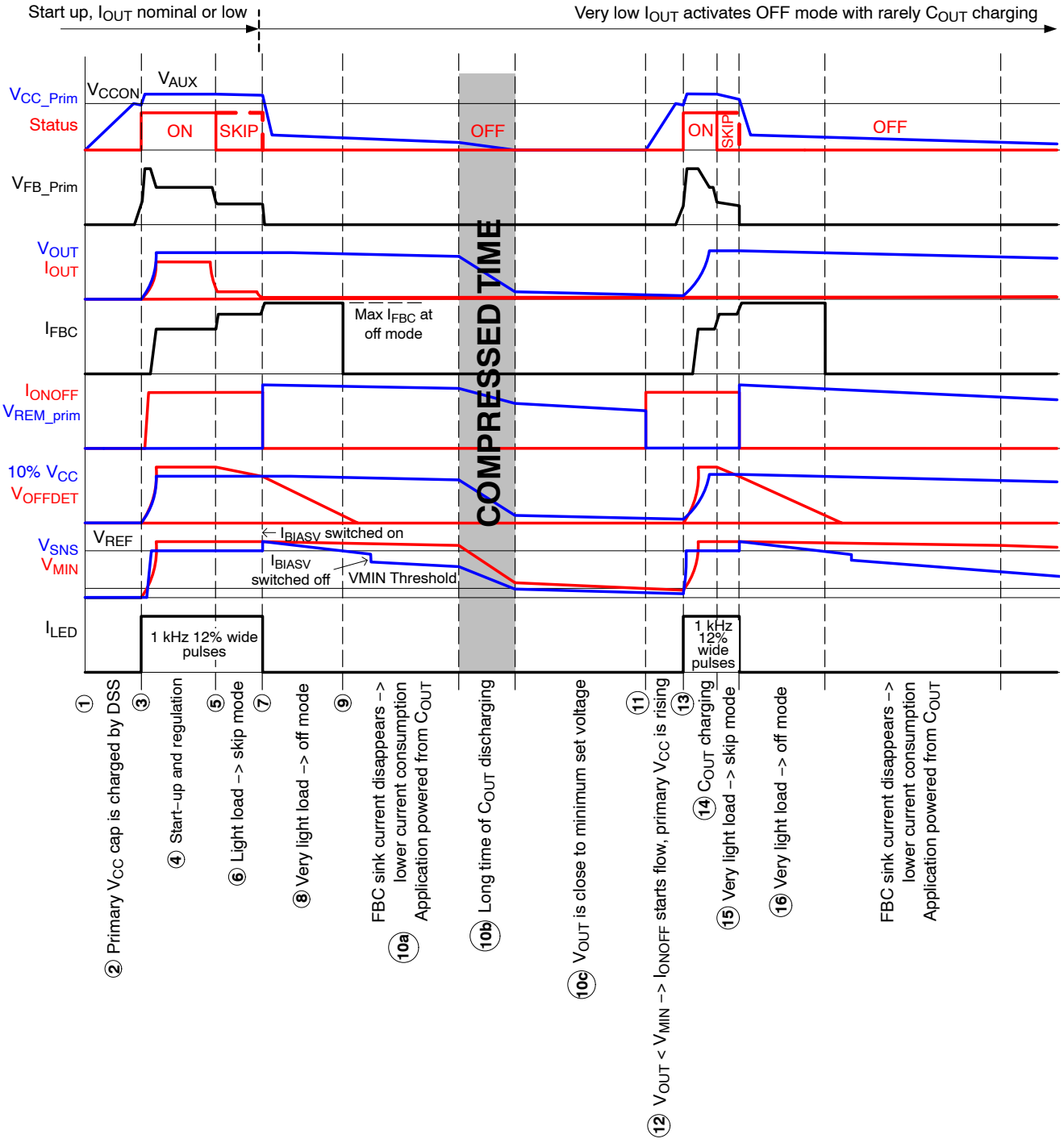


Figure 28. Typical Application States and Waveforms in OFF Mode with Active On Primary Controller

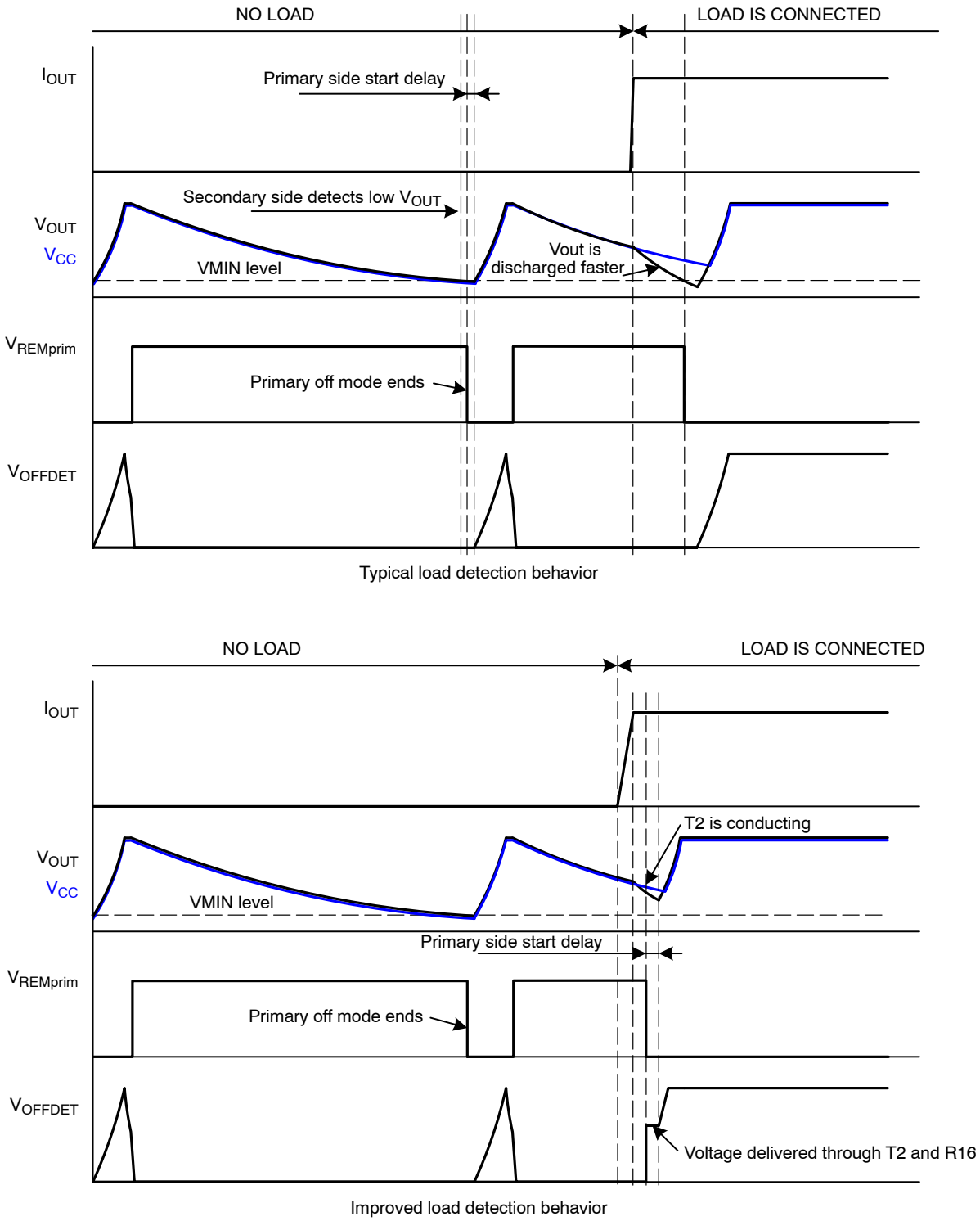


Figure 29. Typical and Improved Load Detection Comparison Waveforms

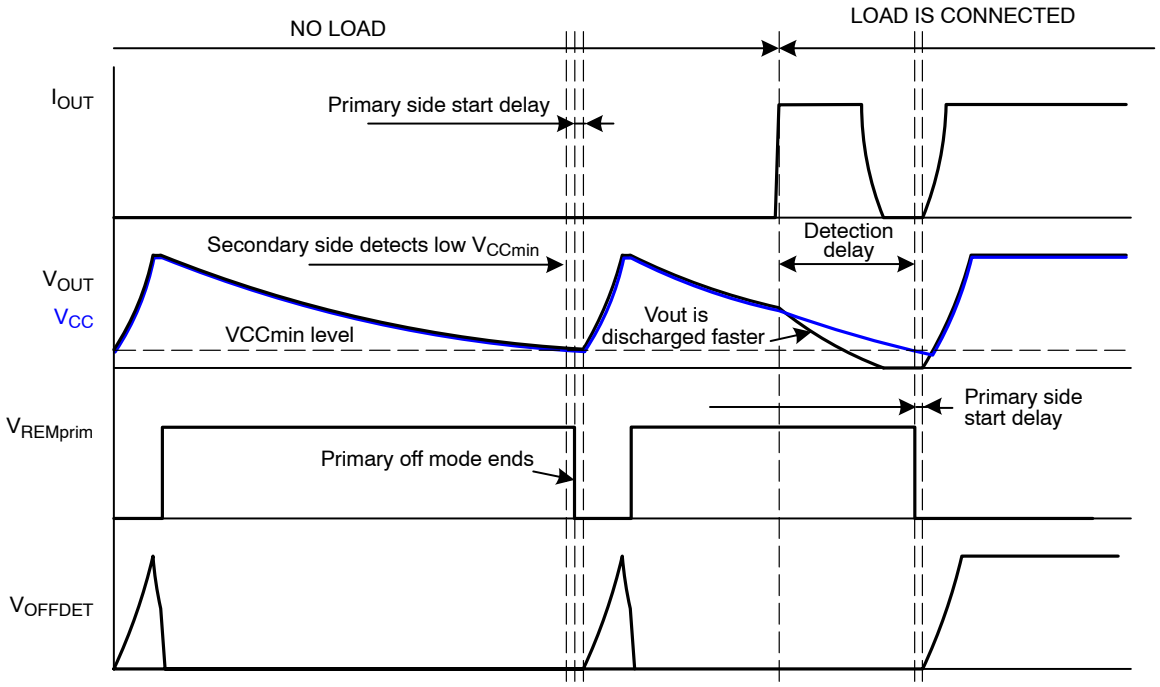


Figure 30. Typical Load Detection of NCP4355A Without External Detection Circuit Waveforms

ORDERING INFORMATION

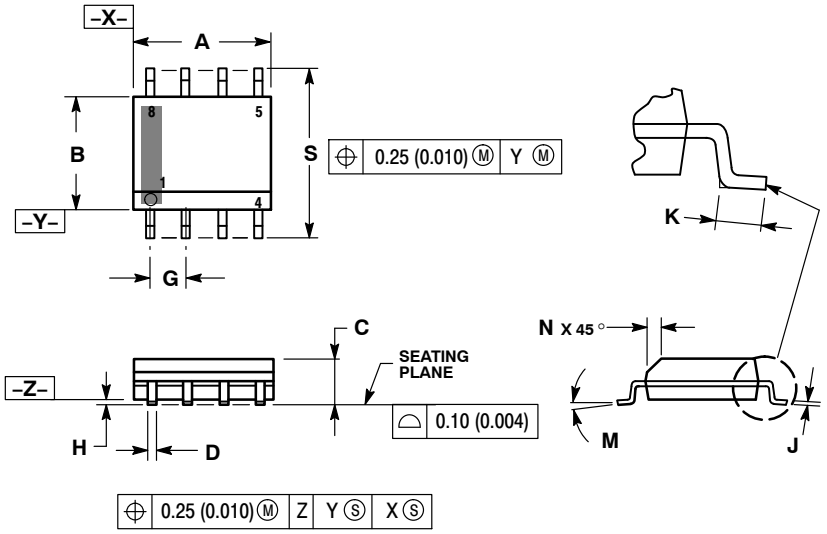
Device	Marking	Adjustable V_{MIN}	Current Regulation	LED Driver	Package	Shipping
NCP4355ADR2G	NCP4355A	No	Yes	Yes	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP4355BDR2G	NCP4355B	Yes	No	Yes	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP4355CDR2G	NCP4355C	Yes	Yes	No	SOIC−8 (Pb−Free)	2500 / Tape & Reel

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

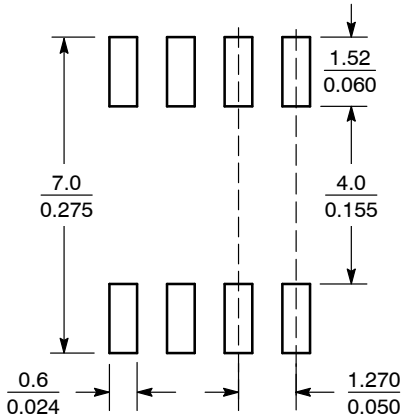
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

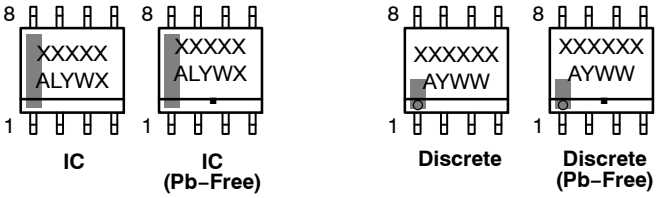
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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