



# PSMN004-60B

## N-channel TrenchMOS SiliconMAX standard level FET

Rev. 02 — 15 December 2009

Product data sheet

## 1. Product profile

### 1.1 General description

SiliconMAX standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

### 1.3 Applications

- High frequency computer motherboard DC-to-DC convertors
- OR-ing applications

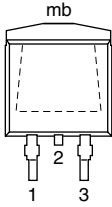
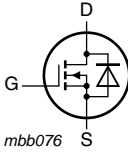
### 1.4 Quick reference data

Table 1. Quick reference

| Symbol                         | Parameter                        | Conditions   | Min | Typ | Max | Unit       |
|--------------------------------|----------------------------------|--|-----|-----|-----|------------|
| $V_{DS}$                       | drain-source voltage             | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$  | -   | -   | 60  | V          |
| $I_D$                          | drain current                    | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$<br>see <a href="#">Figure 1</a> and <a href="#">3</a>                       | -   | -   | 75  | A          |
| $P_{tot}$                      | total power dissipation          | $T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>  | -   | -   | 230 | W          |
| <b>Dynamic characteristics</b> |                                  |  |     |     |     |            |
| $Q_{GD}$                       | gate-drain charge                | $V_{GS} = 10\text{ V}; I_D = 75\text{ A};$<br>$V_{DS} = 48\text{ V}; T_j = 25\text{ °C};$<br>see <a href="#">Figure 11</a> | -   | 54  | -   | nC         |
| <b>Static characteristics</b>  |                                  |  |     |     |     |            |
| $R_{DSon}$                     | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A};$<br>$T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>    | -   | 3.1 | 3.6 | m $\Omega$ |

## 2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description                       | Simplified outline   | Graphic symbol  |
|-----|--------|-----------------------------------|--|---|
| 1   | G      | gate                              |  <p style="text-align: center;">SOT404 (D2PAK)</p> |  <p style="text-align: center;">mbb076</p> |
| 2   | D      | drain <a href="#">[1]</a>         |  |   |
| 3   | S      | source                            |  |   |
| mb  | D      | mounting base; connected to drain |  |   |

[1] It is not possible to make a connection to pin 2.

## 3. Ordering information

Table 3. Ordering information

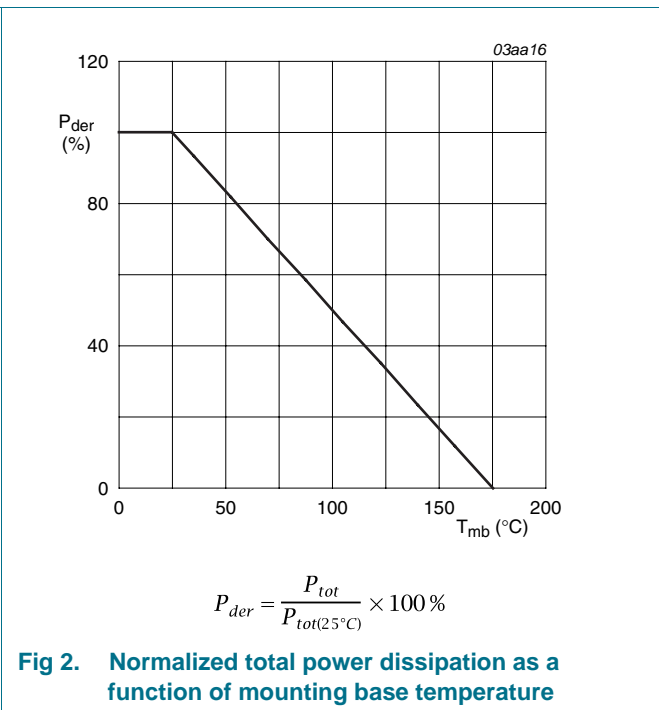
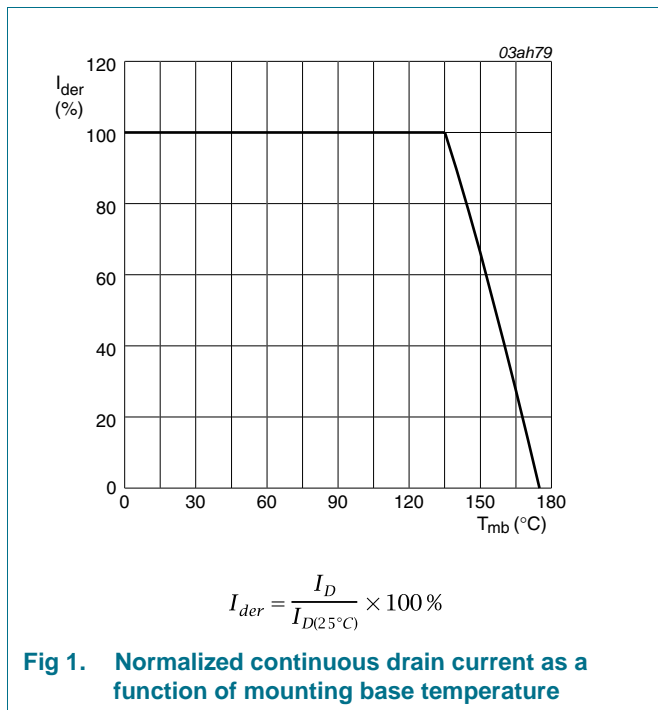
| Type number | Package |  | Version |
|-------------|---------|--|---------|
|             | Name    | Description  |         |
| PSMN004-60B | D2PAK   | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404  |

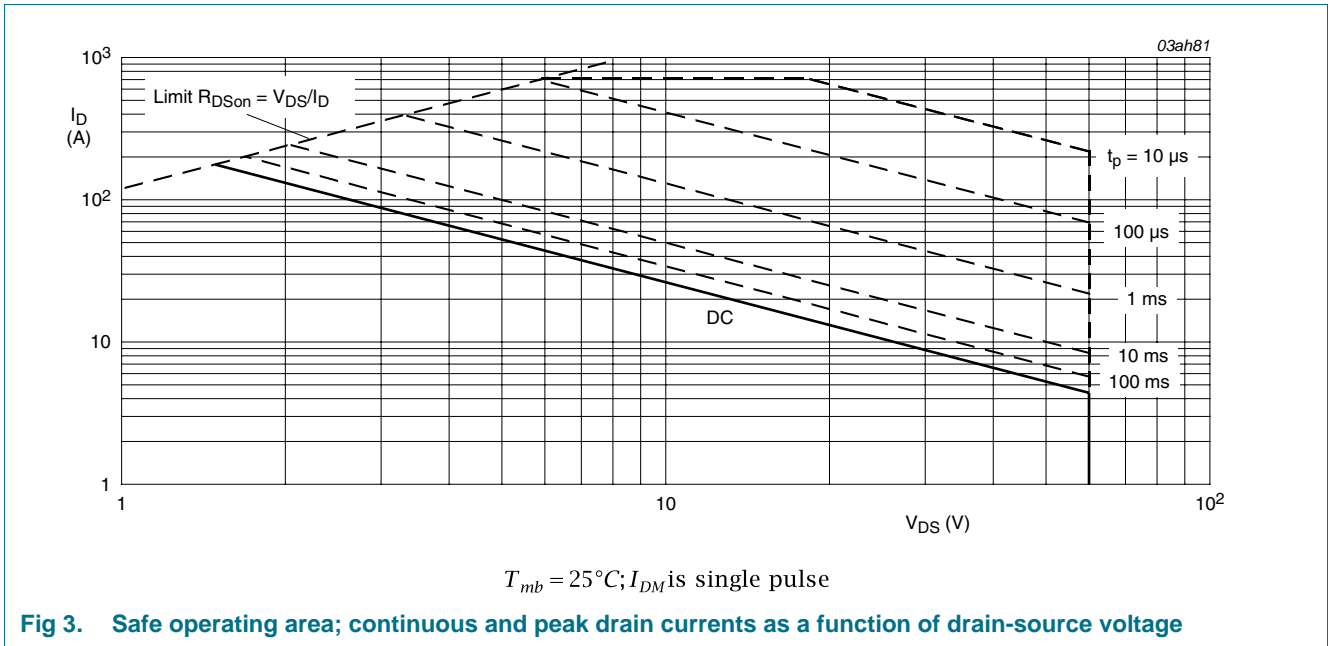
## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                      | Parameter                                     | Conditions  | Min | Max | Unit |
|-----------------------------|---|---|-----|-----|------|
| $V_{DS}$                    | drain-source voltage                          | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$   | -   | 60  | V    |
| $V_{DGR}$                   | drain-gate voltage                            | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$   | -   | 60  | V    |
| $V_{GS}$                    | gate-source voltage                           |   | -20 | 20  | V    |
| $I_D$                       | drain current                                 | $V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C};$ see <a href="#">Figure 1</a>  | -   | 75  | A    |
|                             |   | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ see <a href="#">Figure 1</a> and <a href="#">3</a>   | -   | 75  | A    |
| $I_{DM}$                    | peak drain current                            | $t_p \leq 10\text{ }\mu\text{s};$ pulsed; $T_{mb} = 25\text{ °C};$ see <a href="#">Figure 3</a>   | -   | 400 | A    |
| $P_{tot}$                   | total power dissipation                       | $T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>   | -   | 230 | W    |
| $T_{stg}$                   | storage temperature                           |   | -55 | 175 | °C   |
| $T_j$                       | junction temperature                          |   | -55 | 175 | °C   |
| $V_{GSM}$                   | peak gate-source voltage                      | pulsed; $t_p \leq 50\text{ }\mu\text{s}; \delta = 25\text{ %}; T_j \leq 150\text{ °C}$  | -30 | 30  | V    |
| <b>Source-drain diode</b>   |   |   |     |     |      |
| $I_S$                       | source current                                | $T_{mb} = 25\text{ °C}$   | -   | 75  | A    |
| $I_{SM}$                    | peak source current                           | $t_p \leq 10\text{ }\mu\text{s};$ pulsed; $T_{mb} = 25\text{ °C}$   | -   | 400 | A    |
| <b>Avalanche ruggedness</b> |   |   |     |     |      |
| $E_{DS(AL)S}$               | non-repetitive drain-source avalanche energy  | $V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 75\text{ A};$<br>$V_{sup} = 15\text{ V};$ unclamped; $t_p = 0.1\text{ ms}; R_{GS} = 50\text{ }\Omega$ | -   | 500 | mJ   |
| $I_{DS(AL)S}$               | non-repetitive drain-source avalanche current | $V_{GS} = 10\text{ V}; V_{sup} = 15\text{ V}; R_{GS} = 50\text{ }\Omega;$<br>$T_{j(\text{init})} = 25\text{ °C};$ unclamped   | -   | 75  | A    |

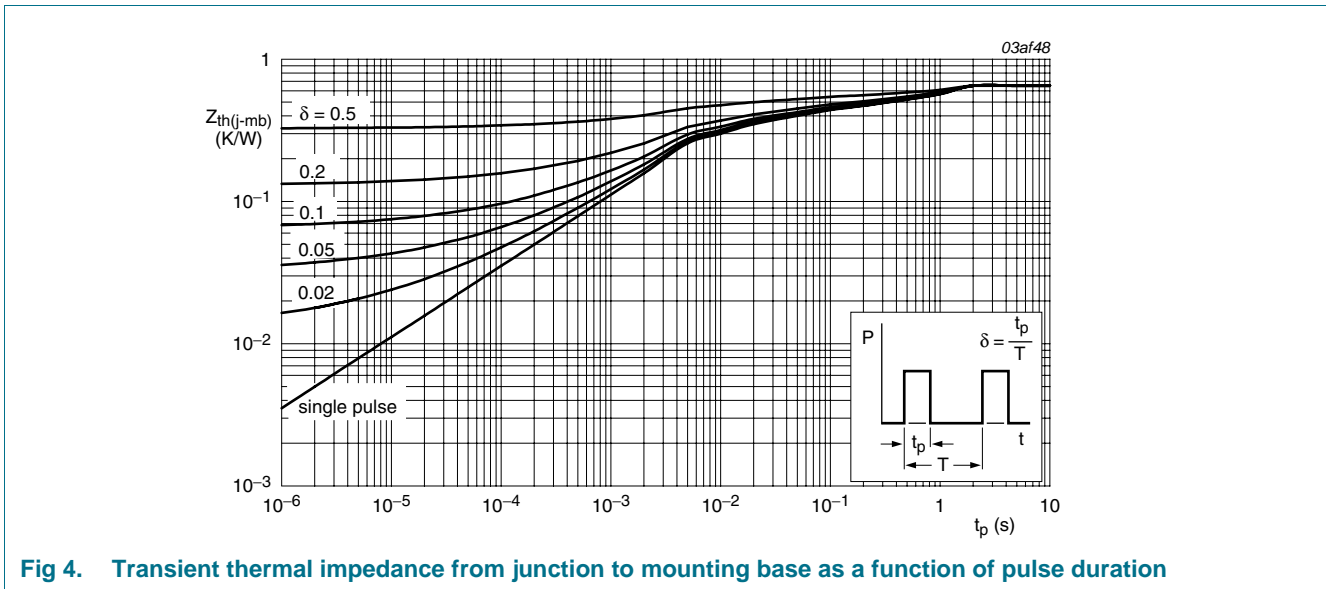




## 5. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol         | Parameter   | Conditions  | Min | Typ | Max  | Unit |
|----------------|---|---|-----|-----|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see <a href="#">Figure 4</a>                          | -   | -   | 0.65 | K/W  |
| $R_{th(j-a)}$  | thermal resistance from junction to ambient       | mounted on a printed circuit board; minimum footprint | -   | -   | 50   | K/W  |

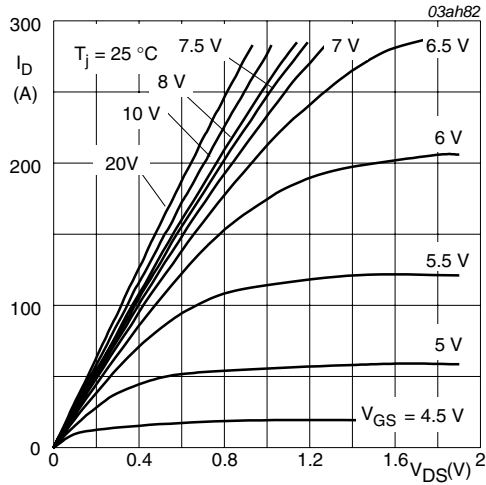


**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

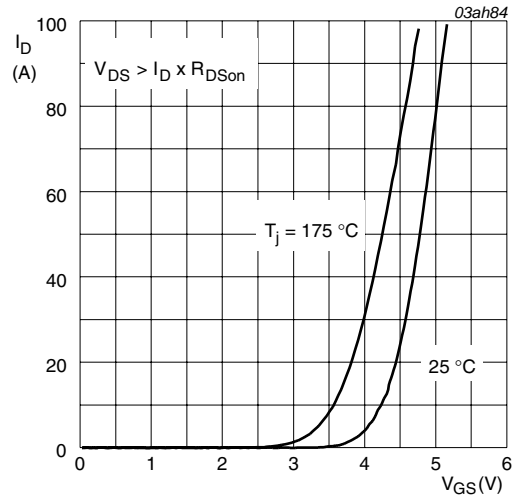
**Table 6. Characteristics**

| Symbol                         | Parameter                        | Conditions  | Min | Typ  | Max  | Unit          |
|--------------------------------|----------------------------------|---|-----|------|------|---------------|
| <b>Static characteristics</b>  |                                  |   |     |      |      |               |
| $V_{(BR)DSS}$                  | drain-source breakdown voltage   | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$   | 54  | -    | -    | V             |
|                                |                                  | $I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | 60  | -    | -    | V             |
| $V_{GS(th)}$                   | gate-source threshold voltage    | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 8</a>                                      | -   | -    | 4.4  | V             |
|                                |                                  | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 8</a>                                      | 1   | -    | -    | V             |
|                                |                                  | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 8</a>                                       | 2   | 3    | 4    | V             |
| $I_{DSS}$                      | drain leakage current            | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$   | -   | -    | 500  | $\mu\text{A}$ |
|                                |                                  | $V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -   | 0.02 | 1    | $\mu\text{A}$ |
| $I_{GSS}$                      | gate leakage current             | $V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$  | -   | 10   | 100  | nA            |
|                                |                                  | $V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$   | -   | 10   | 100  | nA            |
| $R_{DS(on)}$                   | drain-source on-state resistance | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>         | -   | 6.5  | 7.55 | m $\Omega$    |
|                                |                                  | $V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>          | -   | 3.1  | 3.6  | m $\Omega$    |
| <b>Dynamic characteristics</b> |                                  |   |     |      |      |               |
| $Q_{G(tot)}$                   | total gate charge                | $I_D = 75 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 11</a>         | -   | 168  | -    | nC            |
| $Q_{GS}$                       | gate-source charge               |   | -   | 36   | -    | nC            |
| $Q_{GD}$                       | gate-drain charge                |   | -   | 54   | -    | nC            |
| $C_{iss}$                      | input capacitance                | $V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 12</a>           | -   | 8300 | -    | pF            |
| $C_{oss}$                      | output capacitance               |   | -   | 1050 | -    | pF            |
| $C_{rss}$                      | reverse transfer capacitance     |   | -   | 550  | -    | pF            |
| $t_{d(on)}$                    | turn-on delay time               | $V_{DS} = 15 \text{ V}; R_L = 1.25 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$ | -   | 38   | -    | ns            |
| $t_r$                          | rise time                        |   | -   | 74   | -    | ns            |
| $t_{d(off)}$                   | turn-off delay time              |   | -   | 133  | -    | ns            |
| $t_f$                          | fall time                        |   | -   | 75   | -    | ns            |
| <b>Source-drain diode</b>      |                                  |   |     |      |      |               |
| $V_{SD}$                       | source-drain voltage             | $I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$ ; see <a href="#">Figure 13</a>                                 | -   | 0.8  | 1.2  | V             |



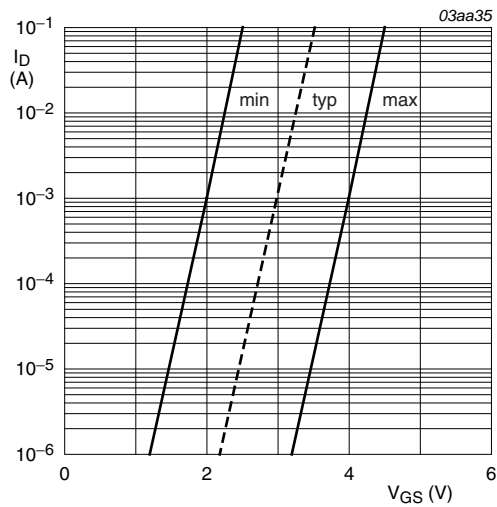
$T_j = 25^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



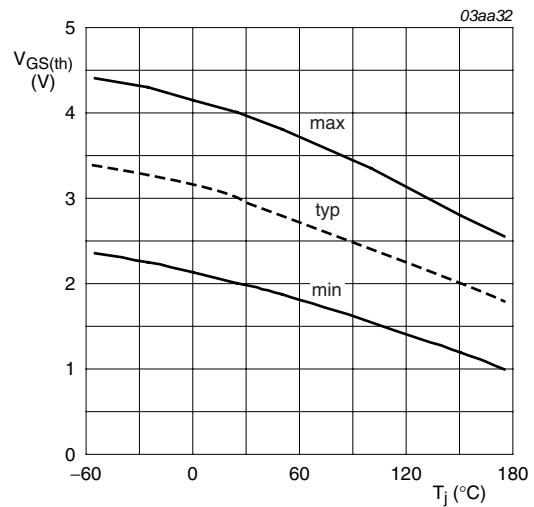
$T_j = 25^\circ\text{C}$  and  $175^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values



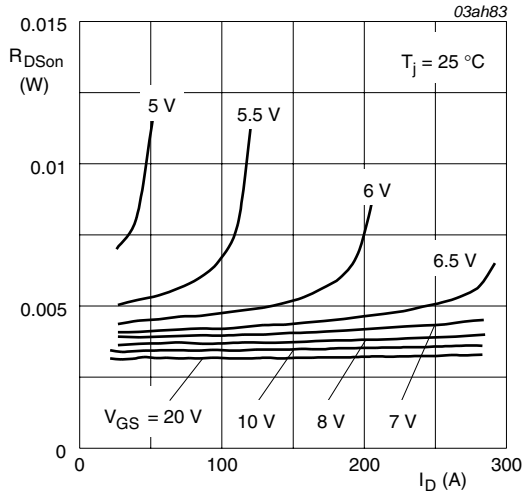
$T_j = 25^\circ\text{C}$ ;  $V_{DS} = 5\text{V}$

Fig 7. Sub-threshold drain current as a function of gate-source voltage



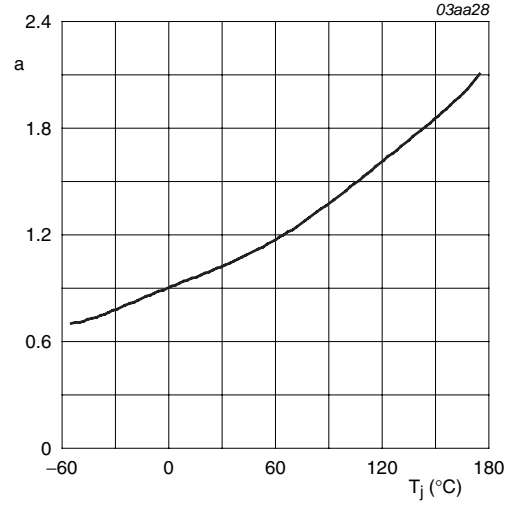
$I_D = 1\text{mA}$ ;  $V_{DS} = V_{GS}$

Fig 8. Gate-source threshold voltage as a function of junction temperature



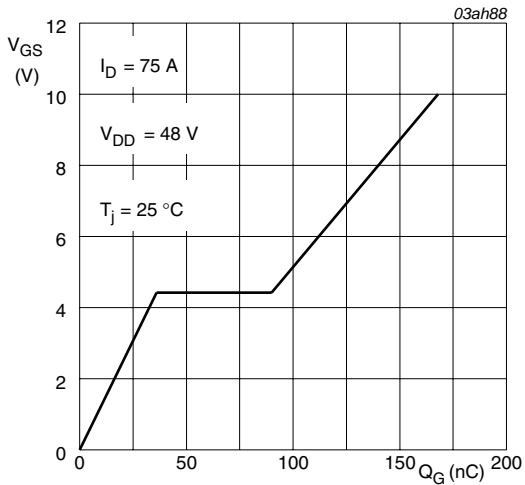
$T_j = 25^\circ\text{C}$

**Fig 9. Drain-source on-state resistance as a function of drain current; typical values**



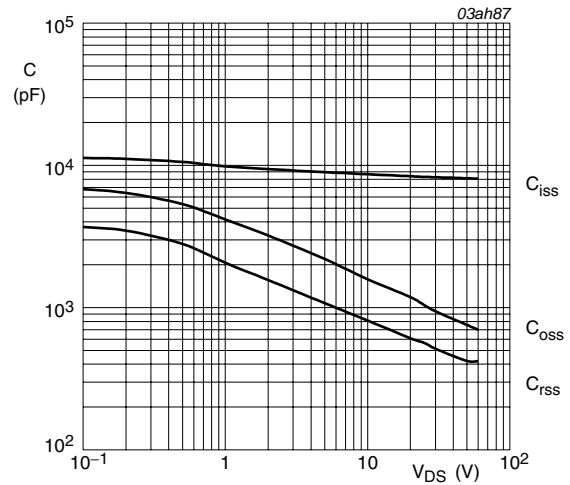
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

**Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature**



$I_D = 75\text{ A}; V_{DS} = 48\text{ V}$

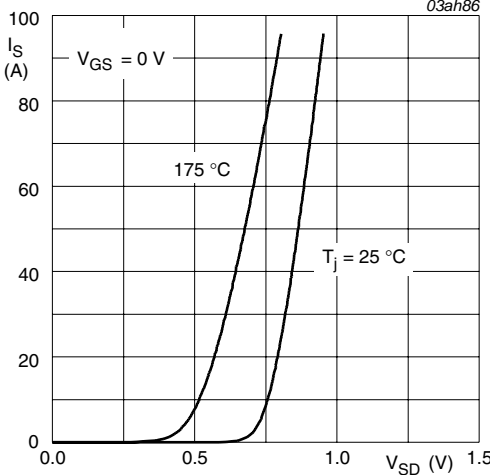
**Fig 11. Gate-source voltage as a function of gate charge; typical values**



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**





$T_j = 25^\circ C$  and  $175^\circ C; V_{GS} = 0V$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

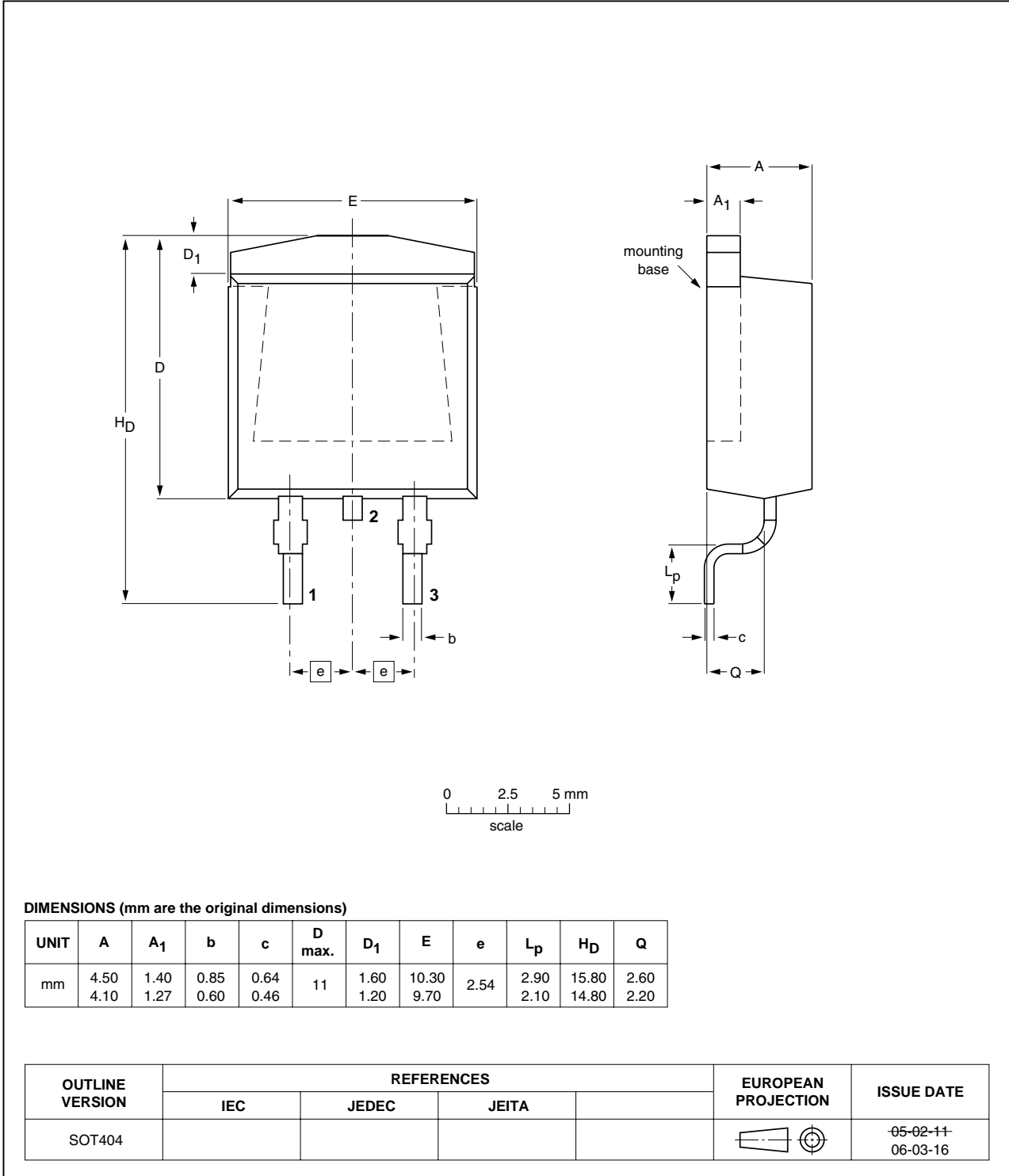


Fig 14. Package outline SOT404 (D2PAK)

## 8. Revision history

Table 7. Revision history

| Document ID                            | Release date | Data sheet status  | Change notice | Supersedes   |
|--|--------------|--------------------|---------------|--|
| PSMN004-60B_2                          | 20091215     | Product data sheet | -             | PSMN004_60P_60B-01   |
| Modifications:                         |              |                    |               |  |
|  |              |                    |               | <ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>• Legal texts have been adapted to the new company name where appropriate.</li><li>• Type number PSMN004-60B separated from data sheet PSMN004_60P_60B-01.</li></ul> |
| PSMN004_60P_60B-01<br>(9397 750 09156) | 20020426     | Product data       | -             | -  |

## 9. Legal information

### 9.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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