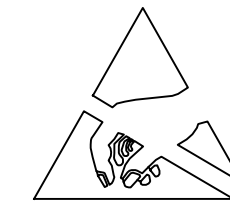


FLIR PCB Assembly Notes

The following assembly notes shall serve as the master and shall supersede all other notes contained in other files, ODB++ or Gerber, supplied by FLIR for the manufacture of this PCB
Unless otherwise specified.

Product material and assembly process to be RoHS 2 and REACH-181 compliant in accordance with the European Union Directive on the Restriction and use of Certain Hazardous Substances in Electrical and Electronic Equipment 2011/65/EU, as well as REACH restrictions consistent with Regulation (EC) 1907/2006, per the list of 181 SVHCs (Substances of Very High Concern).

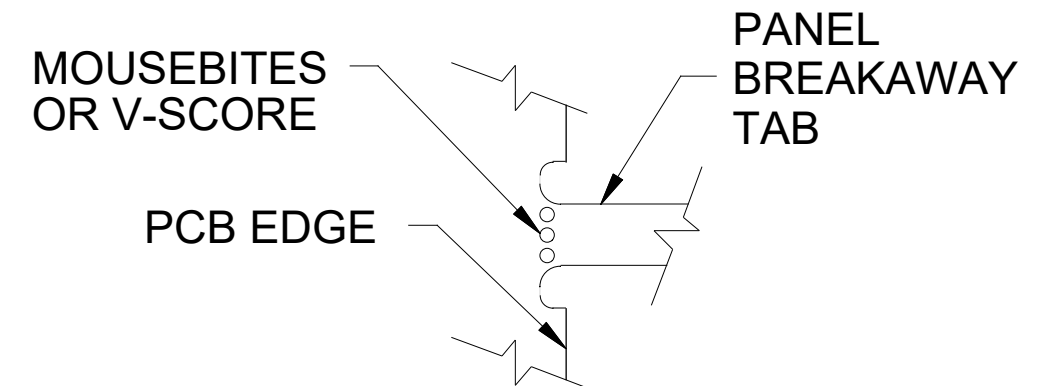
1. ALL IPC SPECIFICATIONS TO BE PER CLASS 2
2. PRIOR TO ASSEMBLY, ASSEMBLER TO VERIFY BARE BOARDS WERE BUILT PER IPC-6012 AND INSPECTED PER IPC-A-600
3. IF ASSEMBLER IS ALSO CONTRACTED TO PROVIDE FABRICATION, PRIOR TO FABRICATION CONFIRM THAT ALL COMPONENT FOOTPRINTS IN GERBER DATA CONFORM TO IPC-7351, OR OBTAIN WAIVER FROM FLIR FOR SPECIFIED COMPONENTS
4. PCBA TO BE MANUFACTURED TO IPC-610 WORKMANSHIP AND INSPECTION STANDARDS AND IN ACCORANCE WITH IPC-J-STD-001D. SOLDER JOINTS TO MEET APPLICABLE SOLERDABILITY TESTS PER IPC-J-STD-003
5. PCBA SOLDER ALLOY AND SOLDER PROCESSES TO BE FULLY ROHS COMPLIANT PER IPC-J-STD-006.
6. PCBA SOLDER PASTE TO BE ROHS COMPLIANT AND MEET IPC-HDBK-005 AND IPC-J-STD-005
7. PCBA SOLDER FLUXES TO BE ROHS COMPLIANT AND MEET IPC-J-STD-004
8. SOLDER REFLOW PROFILES TO BE DESIGNED IN CONSIDERATION OF ROHS COMPLIANCE AND TEMPERATURE LIMITS OF 370HR OR EQUIVALENT MATERIAL. UNLESS OTHERWISE INDICATED OR APPROPRIATE USE SOLDER PROFILE PER IPC/JEDEC J-STD-020C
9. PCBA IS STATIC SENSITIVE ASSEMBLY, STATIC ELIMINATING PROCESSES TO BE UTILIZED DURING ASSEMBLY AND HANDLING
10. PCBA DELIVERABLE TO BE FULLY ROHS COMPATIBLE AND TO BE MARKED TO INDICATE ROHS COMPLIANCE.
- 11 . REFER TO ACCOMPANYING BOM FOR PARTS NOT DESCRIBED IN THIS DOCUMENT OR PARTS INTENTIONALLY UNINSTALLED
- 12 . COMPONENT PINS 1 IDENTIFIED BY CIRCLE, BEVEL, TRIANGLE, OR RECESSED LINE
- 13 . TEST POINTS AND OTHER ELECTRICAL OR MECHANICAL CONTACT INTERFACES TO BE FREE OF FLUX, RESIDUE, AND CONTAMINATION
- 14 . UNLESS OTHERWISE DIRECTED, AFFIX LABEL IN AREA ADEQUATE FOR ACCESS AND LEGIBILITY. MARKINGS TO INCLUDE THE FOLLOWING:
 - A. FLIR PART NUMBER AND REVISION
 - B. MANUFACTURING LOT AND SERIAL NUMBER
 - C. DATE CODE
 - D. TEST-PASS INSPECTION
- 15 . TRIM COMPONENT LEADS WITHIN .062" OF PCB FROM SOLDER SIDE OF PCBA IF APPLICABLE.
16. FINISHED PCB PERIMETER TO BE FREE OF ALL BURRS, PITS, MOUSEBITES, AND V-SCORE RESIDUE. FINISHED PCB OUTLINE DIMENSIONS TOLERANCE .127 [.005]. FAILURE TO MEET THIS REQUIREMENT IS SUBJECT TO QA REJECTION.
17. FINISHED ASSEMBLY PCBs MUST BE INDIVIDUALLY BAGGED IN ANTI-STATIC BAGS OR STATIC DISSIPATIVE ESD SHIELDING BAGS



!CAUTION!
ELECTROSTATIC DISCHARGE SENSITIVE

PCB BREAKAWAY DETAIL

BREAKAWAY LOCATION TBD PER CM BEST FIT
 MOUSEBITE/V-SCORE LOCATED SUCH THAT NO BURRS ARE ON PCB OUTER PERIPHERY



REVISIONS			
REV	DESCRIPTION	DATE	ECN#
120	Signal table added and Pin numbering	11/21/2018	205022

The information contained herein does not contain technology as defined by EAR, 15 CFR772, is publicly available, and therefore not subject to EAR.

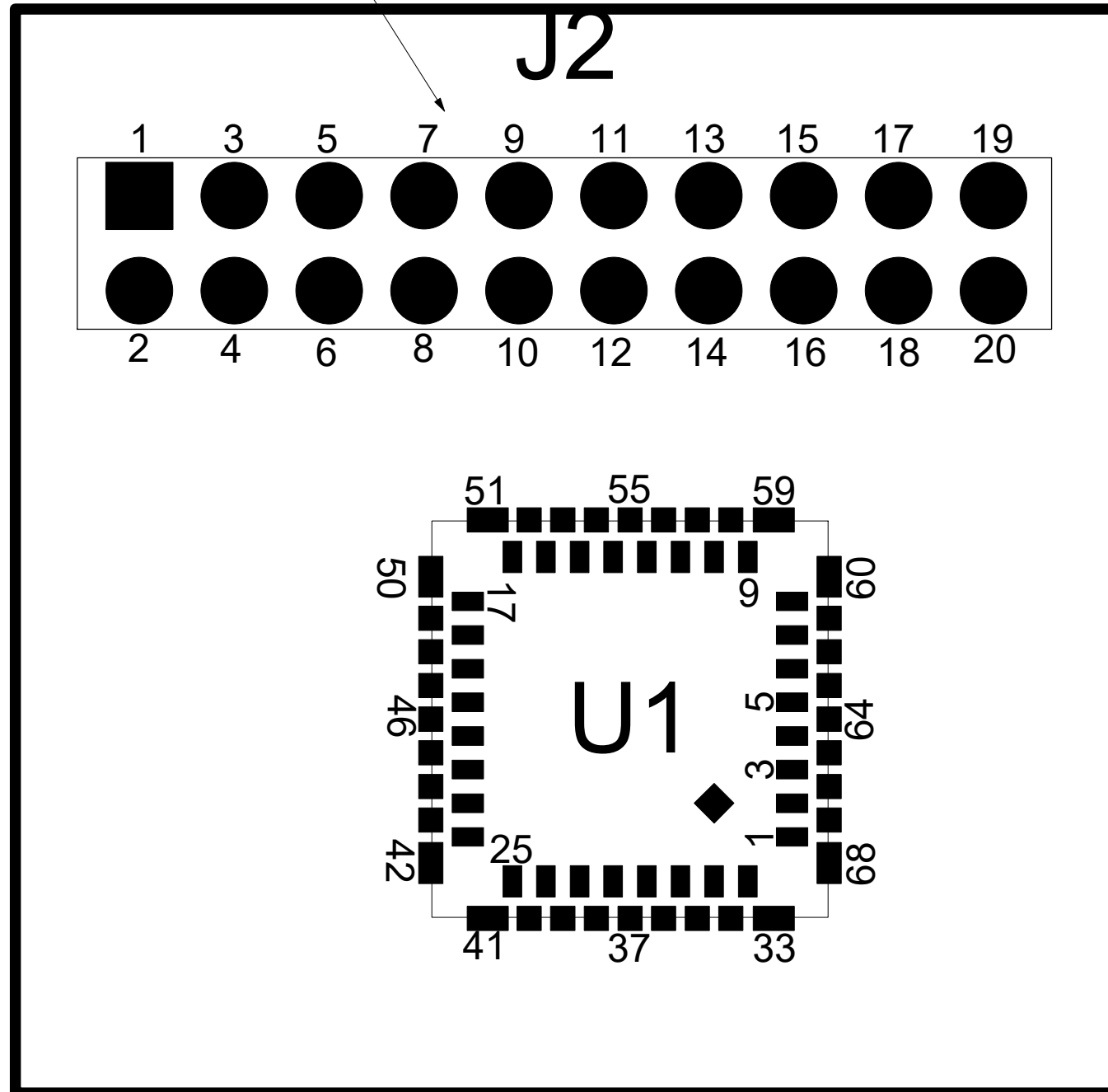
ASSEMBLY		FLIR Commercial Systems 6769 Hollister Ave, Goleta Ca, 93117 805-964-9797 www.flir.com			
DRAWN T.S. BUTTNER	DATE 10/9/2018	Lepton Breakout			
ENGINEER M.BROWN	DATE 10/9/2018				
CHECKED	DATE				
APPROVED	DATE	CAGE CODE	DWG NO 250-0577-05	REV 120	
ISSUED	DATE	SCALE N/A			SHEET 1 OF 3

"PROPRIETARY - FLIR Systems Inc."

Top-side View

J2 Installed on far side.

Please see sheet 4 of 4

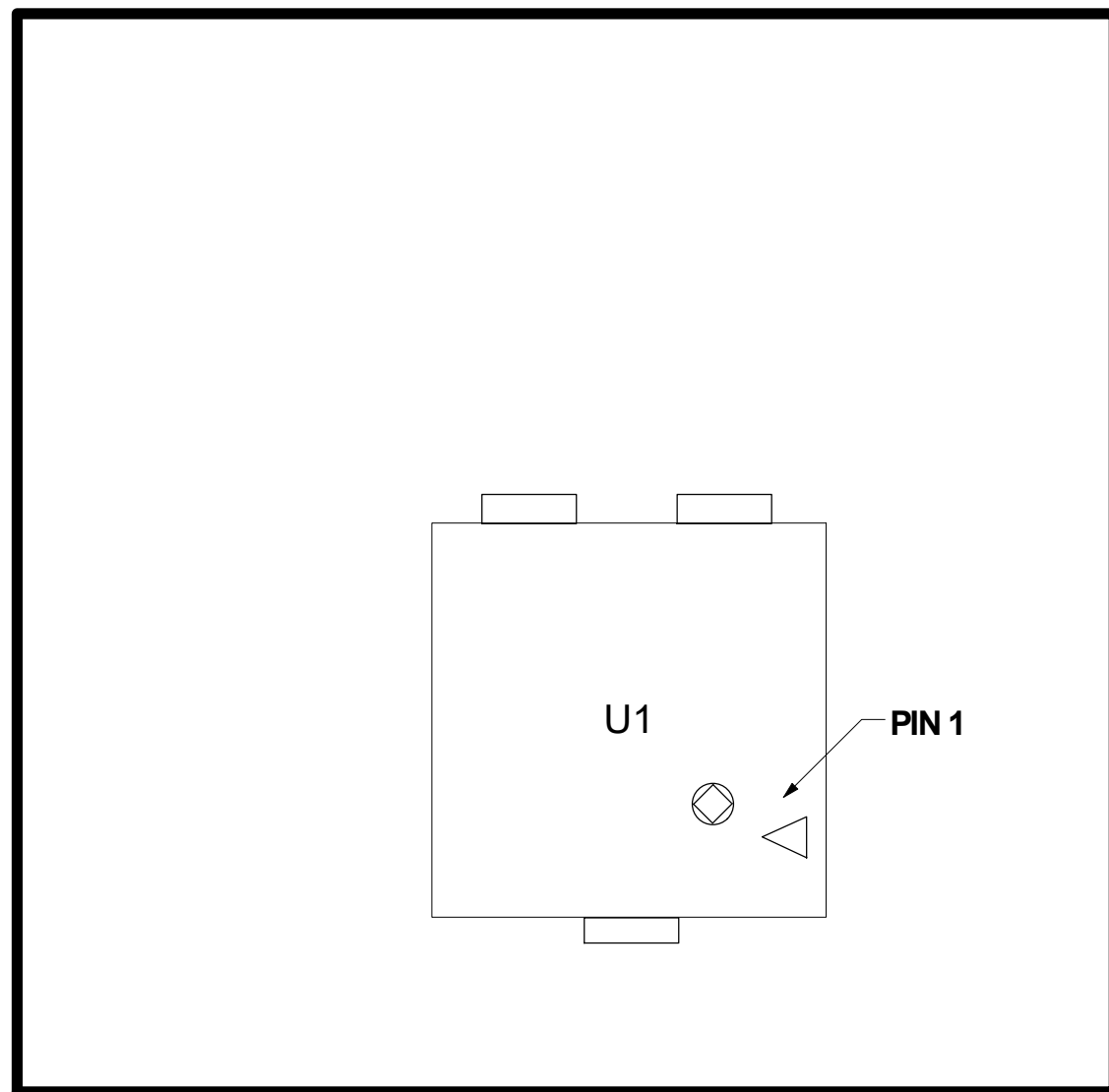


LEPTON BREAKOUT BOARD - SIGNAL IO TABLE	
Net Name	Net Pins
	J2.1 J2.19 U1.1 U1.6 U1.8 U1.9 U1.10 U1.15 U1.18 U1.20 U1.25 U1.27 U1.30 U1.33 U1.34 U1.35 U1.36 U1.37 U1.38 U1.39 U1.40 U1.41 U1.42 U1.43 U1.44 U1.45 U1.46 U1.47 U1.48 U1.49 U1.50 U1.51 U1.52 U1.53 U1.54 U1.55 U1.56 U1.57 U1.58 U1.59 U1.60 U1.61 U1.62 U1.63 U1.64 U1.65 U1.66 U1.67 U1.68 U2.2 U3.2 U4.5 U4.6 U4.7 U4.8 Y1.2
GND	
GPIO0	J2.11 U1.5
GPIO1	J2.14 U1.4
GPIO2	J2.13 U1.3
GPIO3	J2.15 U1.2
MASTER_CLK	J2.18 U1.26
PW_DWN_L	J2.20 U1.23
RESET_L	J2.17 U1.24
SCL	J2.8 U1.21
SDA	J2.5 U1.22
SPI_CLK	J2.7 U1.13
SPI_CS	J2.10 U1.14
SPI_MISO	J2.12 U1.12
SPI_MOSI	J2.9 U1.11
VCC12	J2.16 U1.7
VCC28	J2.4 U1.19
VCC28_IO	J2.6 U1.16
VPROG	J2.3 U1.17

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Top-side View

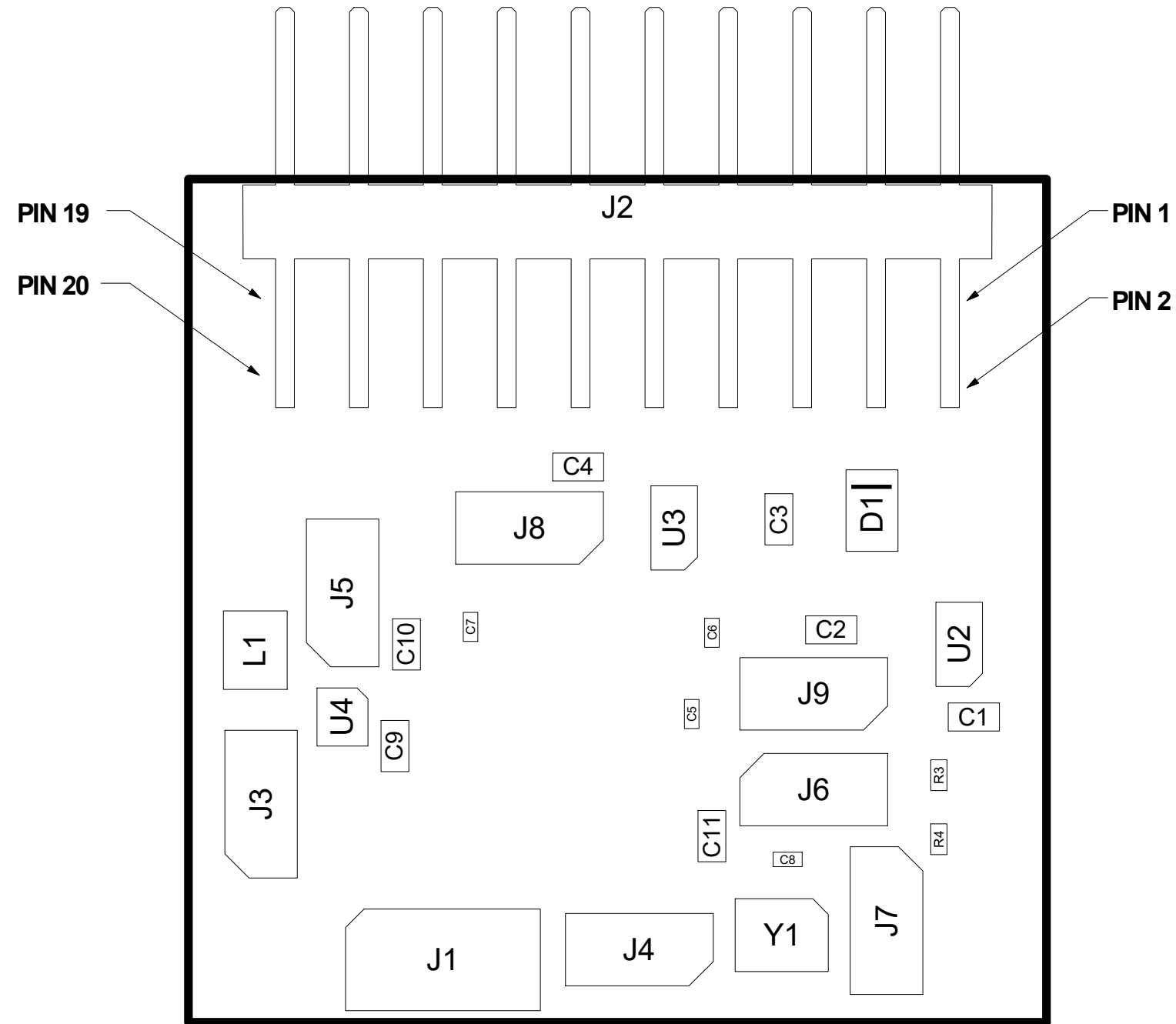


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	CAGE CODE	DWG NO	REV
		250-0577-25	120

Bottom-side View



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	CAGE CODE	DWG NO	REV
		250-0577-25	120