*Click **here** to ask an associate for production status of specific part numbers.*

DS28E50

DeepCover Secure SHA-3 Authenticator with ChipDNA PUF Protection

General Description

The DS28E50 secure authenticator combines FIPS 202-compliant secure hash algorithm (SHA-3) challenge and response authentication with Analog Devices' patented ChipDNA™ technology, a physically unclonable function (PUF) to provide a cost-effective solution with the ultimate protection against security attacks. The ChipDNA implementation utilizes the random variation of semiconductor device characteristics that naturally occur during wafer fabrication. The ChipDNA circuit generates a unique output value that is repeatable over time, temperature, and operating voltage. Attempts to probe or observe ChipDNA operation modifies the underlying circuit characteristics thus preventing discovery of the unique value used by the chip cryptographic functions. The DS28E50 utilizes the ChipDNA output as key content to cryptographically secure all device-stored data. With ChipDNA capability, the device provides a core set of cryptographic tools derived from integrated blocks including a SHA-3 engine, a FIPS/NIST-compliant true random number generator (TRNG), 2Kb of secured EEPROM, a decrement-only counter and a unique 64-bit ROM identification number (ROM ID). The unique ROM ID is used as a fundamental input parameter for cryptographic operations and serves as an electronic serial number within the application. The DS28E50 communicates over the single-contact 1-Wire® bus at both standard and overdrive speeds. The communication follows the 1-Wire protocol with the ROM ID acting as node address in the case of a multidevice 1-Wire network.

Applications

- Authentication of Medical Sensors and Tools
- Secure Management of Limited Use Consumables
- IoT Node Authentication
- Peripheral Authentication
- Reference Design License Management
- Printer Cartridge Identification and Authentication

Request DS28E50 Security User Guide

Benefits and Features

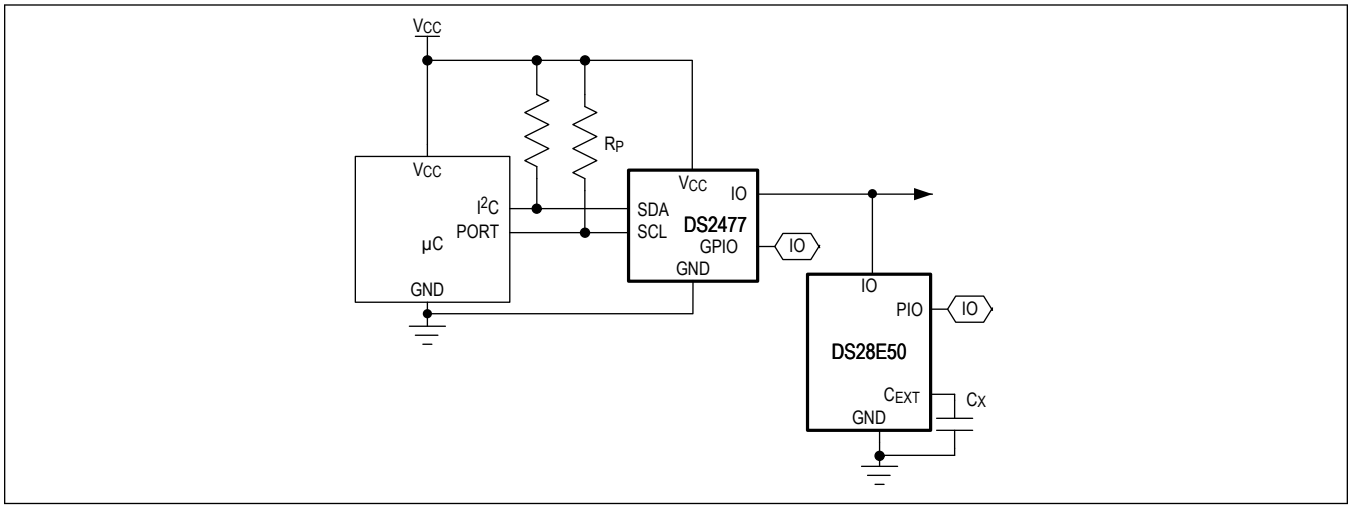
- Robust Countermeasures Protect Against Security Attacks
  - Patented Physically Unclonable Function Secures Device Data
  - Actively Monitored Die Shield Detects and Reacts to Intrusion Attempts
  - All Stored Data Cryptographically Protected from Discovery
- Efficient Secure Hash Algorithm Authenticates Peripherals
  - FIPS 202-Compliant SHA-3 Algorithm for Challenge/Response Authentication
  - FIPS 198-Compliant Keyed-Hash Message Authentication Code (HMAC)
  - TRNG with NIST SP 800-90B-Compliant Entropy Source
- Supplemental Features Enable Easy Integration into End Applications
  - 17-Bit One-Time Settable, Nonvolatile Decrement-Only Counter with Authenticated Read
  - One GPIO Pin with Optional Authentication Control
  - 2Kb of EEPROM for User Data, Key, and Control Registers
  - Unique and Unalterable Factory-Programmed 64-Bit Identification Number (ROM ID)
  - Single-Contact, 1-Wire Interface Communication with Host at 11.7kbps and 62.5kbps
  - Operating Range: 3.3V ±10%, -40°C to +85°C
  - 6-Pin TDFN-EP Package (3mm x 3mm) and 2-Pin SFN Package (3.5mm x 6.5mm)

ChipDNA is a trademark and 1-Wire is a registered trademark of Maxim Integrated Products, Inc.

Ordering Information appears at end of data sheet.

19-100367; Rev 2; 10/22

Typical Application Circuit



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Absolute Maximum Ratings

Voltage Range on Any Pin Relative to GND ..... -0.5V to +4.0V
Maximum Current into Any Pin..... -20mA to +20mA
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range .....-40°C to +125°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

6 TDFN-EP

Package Code	T633+2
Outline Number	21-0137
Land Pattern Number	90-0058
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	55°C/W
Junction to Case (θ_{JC})	9°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	42°C/W
Junction to Case (θ_{JC})	9°C/W

2 SFN

Package Code	T23A6MN+1
Outline Number	21-0575
Land Pattern Number	90-0431
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	N/A
Junction to Case (θ_{JC})	N/A

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IO PIN: GENERAL DATA						
1-Wire Pullup Voltage	V_{PUP}	System requirement	2.97	3.3	3.63	V
1-Wire Pullup Resistance	R_{PUP}	(*Note 1*)			1000	Ω
Input Capacitance	C_{IO}	(*Note 1*, *Note 2*)		0.1 + C_X		nF
Capacitor External	C_X	System requirement, IO pin at V_{PUP} (see *Note 23*)	399.5	470	540.5	nF
Input Load Current	I_L	IO pin at V_{PUP}		10	360	µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
High-to-Low Switching Threshold	V_{TL}	(*Note 3*, *Note 4*)		0.65 x V_{PUP}		V
Input Low Voltage	V_{IL}	(*Note 5*)			0.10 x V_{PUP}	V
Low-to-High Switching Threshold	V_{TH}	(*Note 3*, *Note 6*)		0.75 x V_{PUP}		V
Switching Hysteresis	V_{HY}	(*Note 3*, *Note 7*)		0.3		V
Output Low Voltage	V_{OL}	I_{OL} = 4mA (*Note 8*)			0.4	V
IO PIN: 1-Wire INTERFACE						
Recovery Time (*Note 9*)	t_{REC}	Standard speed, R_{PUP} = 1000Ω	25			µs
		Overdrive speed, R_{PUP} = 1000Ω, T_A = -40°C to +55°C	5			
		Overdrive speed, R_{PUP} = 1000Ω T_A = -40°C to +85°C	10			
		Directly prior to reset pulse: R_{PUP} = 1000Ω	100			
Rising-Edge Hold-off (*Note 10*)	t_{REH}	Applies to standard speed only		1		µs
Time Slot Duration (*Note 11*)	t_{SLOT}	Standard speed	85			µs
		Overdrive speed	16			
IO PIN: 1-Wire RESET, PRESENCE-DETECT CYCLE						
Reset Low Time	t_{RSTL}	System requirement, standard speed	480		640	µs
		System requirement, overdrive speed	48		80	
Reset High Time (*Note 21*)	t_{RSTH}	Standard speed	480			µs
		Overdrive speed	48			
Presence-Detect Sample Time (*Note 12*)	t_{MSP}	Standard speed	65		75	µs
		Overdrive speed	7		10	
IO PIN: 1-Wire WRITE						
Write-Zero Low Time (*Note 13*)	t_{W0L}	Standard speed	60		120	µs
		Overdrive speed	6		15.5	
	t_{W1L}	Standard speed	0.25		15	
		Overdrive speed	0.25		2	
IO PIN: 1-Wire READ						
Read Low Time (*Note 14*)	t_{RL}	Standard speed	0.25		15 - δ	µs
		Overdrive speed	0.25		2 - δ	
Read Sample Time (*Note 14*)	t_{MSR}	Standard speed	t_{RL} + δ		15	µs
		Overdrive speed	t_{RL}+ δ		2	
PIO PIN						
Output Low	$PIOV_{OL}$	$PIOI_{OL}$ = 4mA (*Note 8*)			0.4	V

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Low	$PIOV_{IL}$		-0.3		0.20 x V_{PUP}	V
Input High	$PIOV_{IH}$		0.7 x V_{PUP}		V_{PUP} + 0.3	V
Leakage Current	$PIOI_L$		-1		+2	µA
STRONG PULLUP OPERATION						
Strong Pullup Current	I_{SPU}	(*Note 15*)			10	mA
Strong Pullup Voltage	V_{SPU}	(*Note 15*)	2.8			V
Read Memory	t_{RM}				50	ms
Write Memory	t_{WM}				100	ms
Write Memory - Secret	t_{WM_SEC}	(*Note 22*)			N/A	ms
Blockwise Write Memory	t_{WM_BL}	Page data changes limited to one of four 8-byte blocks (refer to the *DS28E50 Security User Guide*)			60	ms
Write State	t_{WS}				60	ms
Read State	t_{RS}				N/A	ms
TRNG Generation	t_{RNG}				25	ms
TRNG On-Demand Check	t_{ODC}				40	ms
Computation Time	t_{CMP}				5	ms
EEPROM						
Write/Erase Cycles (Endurance)	N_{CY}	(*Note 16*, *Note 17*)	100k			
Data Retention	t_{DR}	T_A = +85°C (*Note 18*, *Note 19*, *Note 20*)	10			years

Note 1: System requirement. Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times.

Note 2: Value represents the typical parasite capacitance when V_{PUP} is first applied. Once the parasite capacitance is charged, it does not affect normal communication. Typically, during normal communication, the parasite capacitance is effectively ~100pF.

Note 3: V_{TL}, V_{TH}, and V_{HY} are a function of the internal supply voltage, which is a function of V_{PUP}, R_{PUP}, 1-Wire timing, and capacitive loading on IO. Lower V_{PUP}, higher R_{PUP}, shorter t_{REC}, and heavier capacitive loading all lead to lower values of V_{TL}, V_{TH}, and V_{HY}.

Note 4: Voltage below which, during a falling edge on IO, a logic zero is detected.

Note 5: The voltage on IO must be less than or equal to V_{ILMAX} at all times the controller is driving IO to a logic-zero level.

Note 6: Voltage above which, during a rising edge on IO, a logic one is detected.

Note 7: After V_{TH} is crossed during a rising edge on IO, the voltage on IO must drop by at least V_{HY} to be detected as logic zero.

Note 8: The I-V characteristic is linear for voltages less than 1V.

Note 9: System requirement. Applies to a single device attached to a 1-Wire line.

Note 10: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.

Note 11: Defines maximum possible bit rate. Equal to $1/(t_{W0LMIN} + t_{RECMIN})$.

Note 12: System requirement. Interval after t_{RSTL} during which a bus controller can read a logic zero on IO if there is a DS28E50 present. The power-up presence detect pulse can be outside this interval, but completes within 2ms after power-up.

Note 13: System requirement. ε in Figure 4 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to V_{TH}. The actual maximum duration for the controller to pull the line low is $t_{W1LMAX} + t_F - ε$ and $t_{W0LMAX} + t_F - ε$, respectively.

Note 14: System requirement. δ in Figure 4 represents the time required for the pullup circuitry to pull the voltage on IO up from V_{IL} to the input-high threshold of the bus controller. The actual maximum duration for the controller to pull the line low is t_{RLMAX} + t_F.

Note 15: Current drawn from IO during a SPU operation interval. The pullup circuit on IO during the SPU operation interval should be such that the voltage at IO is greater than or equal to V_{SPUMIN}. A low-impedance bypass of R_{PUP} activated during the SPU operation is the recommended way to meet this requirement.

Note 16: Write-cycle endurance is tested in compliance with JESD47G

Note 17: Not 100% production tested; guaranteed by reliability monitor sampling.

Note 18: Data retention is tested in compliance with JESD47G.

Note 19: Guaranteed by 100% production test at elevated temperature for a shorter time; equivalence of this production test to the data sheet limit at operating temperature range is established by reliability testing.

Note 20: EEPROM writes can become nonfunctional after the data-retention time is exceeded. Long-term storage at elevated temperatures is not recommended.

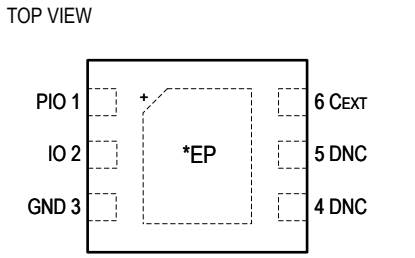
Note 21: An additional reset or communication sequence cannot begin until the reset high time has expired.

Note 22: Guaranteed by design and/or characterization only. Not production tested.

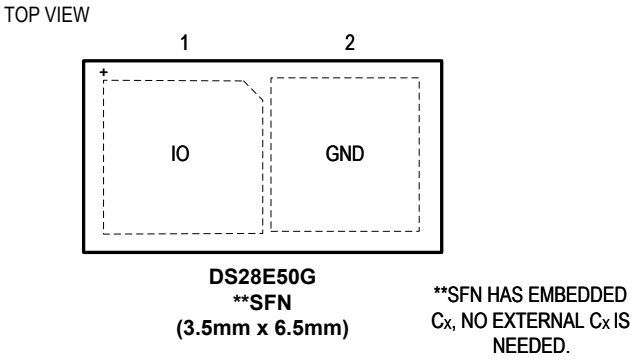
Note 23: SFN packages include an embedded capacitor C_X, therefore only the TDFN package requires an external capacitor C_X. (See the *Functional Diagrams*.)

Pin Configuration

TDFN-EP



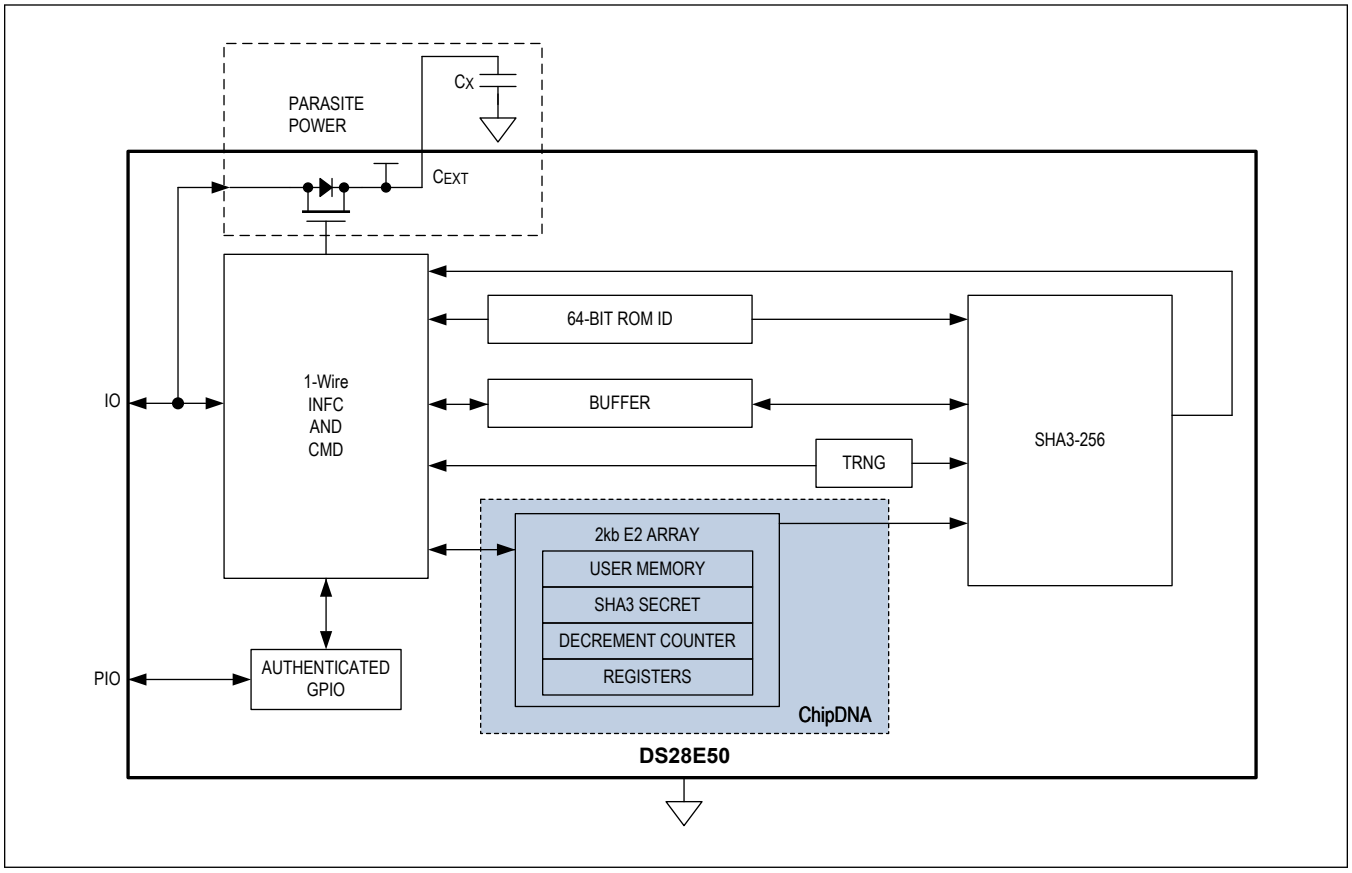
SFN



Pin Description

PIN		NAME	FUNCTION
TDFN-EP	SFN		
1	—	PIO	General-Purpose IO
2	1	IO	1-Wire IO
3	2	GND	Ground
4, 5	—	DNC	Do Not Connect
6	—	C_{EXT}	Input for External Capacitor (TDFN only, see *Note 23*)
—	—	EP	Exposed Pad (TDFN Only). Solder evenly to the board's ground plane for proper operation. Refer to *Application Note 3273: Exposed Pads: A Brief Introduction* for additional information.

Functional Diagram



Detailed Description

The DS28E50 integrates the Analog Devices ChipDNA capability to protect all device stored data from invasive discovery. In addition to the PUF and SHA-3 engines for signatures, the device integrates a FIPS/NIST compliant TRNG, 2Kb EEPROM for user memory, SHA-3 secret storage, and control registers. One user page can optionally be designated as a decrement-only counter. The PIO pin can be independently operated under command control and includes configurability supporting authenticated and nonauthenticated operation. The device operates from a 1-Wire interface with a parasitic supply by way of an external capacitor.

Design Resource Overview

Operation of the DS28E50 involves use of device EEPROM and execution of device function commands. The following section provides an overview including the decrement counter. Refer to the *DS28E50 Security User Guide* for details.

Memory

A 2Kb secured EEPROM array provides SHA-3 secret storage, along with a decrement counter, and/or general-purpose, user-programmable memory. Depending on the memory space, there are either default or user-programmable options to set protection modes.

General-Purpose I/O (GPIO)

The open-drain PIO pin can be read and controlled in an authenticated or nonauthenticated manner. Authenticated operation includes measures to prevent replay attacks. Upon power-up, the default state for the PIO pin is in high impedance.

Function Commands

After a 1-Wire reset/presence cycle and ROM function command sequence is successful, a command start can be accepted and then followed by a device function command. In general, these commands follow Figure 1. Within this diagram, the data transfer is verified when writing and reading by a 16-bit CRC (CRC-16). The CRC-16 is computed as described in *Application Note 27: Understanding and Using Cyclic Redundancy Checks with Maxim 1-Wire and iButton Products*.

Decrement Counter

The optional 17-bit decrement counter can be written one time on a dual-purpose page of memory. A dedicated device function command is used to decrement the count value by one with each call. Once the count value reaches a value of 0, no additional decrements are possible.

1-Wire Bus System

The 1-Wire bus is a system that has a single bus controller and one or more peripherals. In all instances, the DS28E50 is a peripheral device. The bus controller is typically a microcontroller or a coprocessor like the DS2477 . The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus controller.

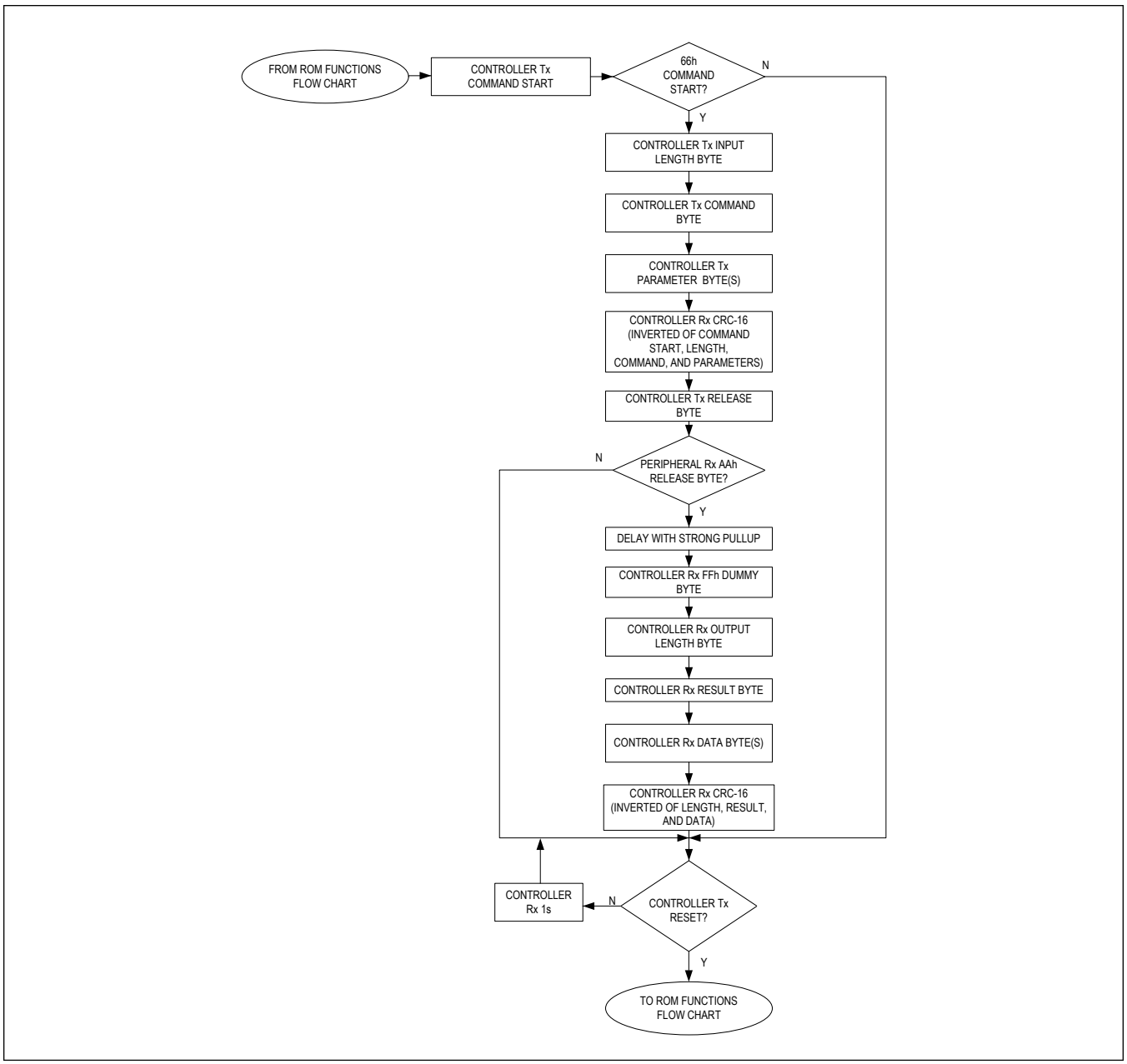


Figure 1. Device Function Flow Chart

Hardware Configuration

The 1-Wire bus has only a single line by definition; it is important that each device on the bus can drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open-drain or three-state outputs. The 1-Wire port of the DS28E50 is open drain with an internal circuit equivalent. A multidrop bus consists of a 1-Wire bus with multiple peripherals attached. The DS28E50 supports both a standard and overdrive communication speed of 11.7kbps (max) and 62.5kbps (max), respectively. The value of the pullup resistor primarily depends on the network size and load conditions. The DS28E50 requires a pullup resistor of 1kΩ (max) at any speed. The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus must be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 15.5µs (overdrive speed) or more than 120µs

(standard speed), one or more devices on the bus could be reset.

Transaction Sequence

The protocol for accessing the DS28E50 through the 1-Wire port is as follows:

- Initialization
- ROM Function command
- Device Function command
- Transaction/data

Initialization

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus controller followed by presence pulse(s) transmitted by the peripheral(s). The presence pulse lets the bus controller know that the DS28E50 is on the bus and is ready to operate. For more details, see the *1-Wire Signaling and Timing* section.

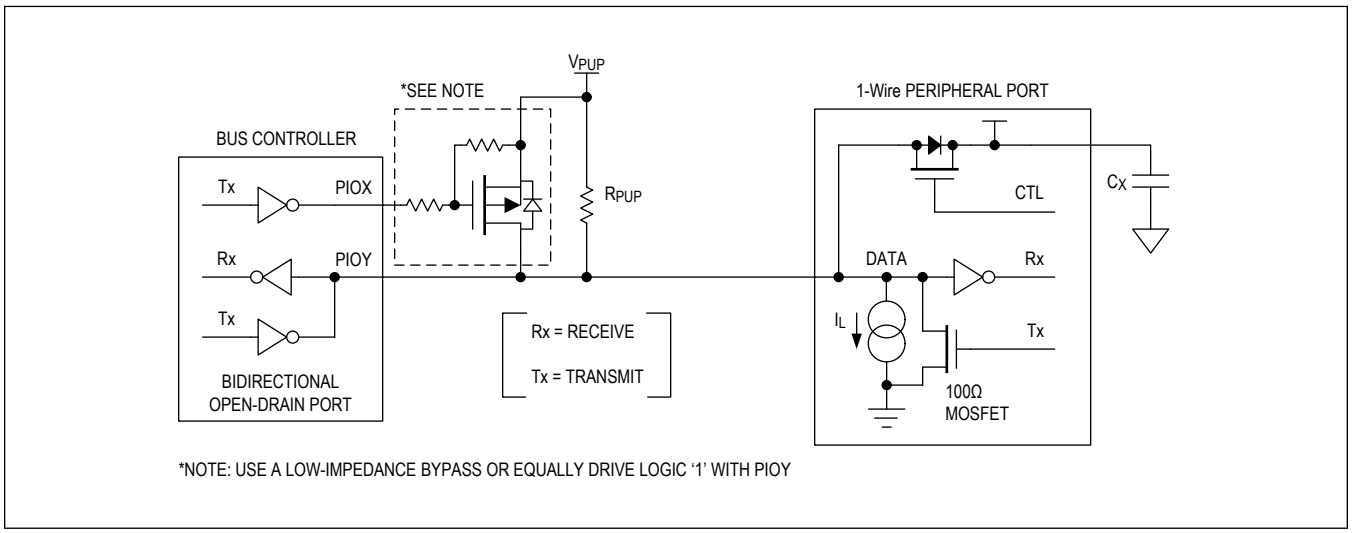


Figure 2. Hardware Configuration

1-Wire Signaling and Timing

The DS28E50 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus controller initiates all falling edges. The DS28E50 can communicate at two speeds: standard and overdrive. If not explicitly set into the overdrive mode, the DS28E50 communicates at standard speed. While in overdrive mode, the fast timing applies to all waveforms. To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 3 as ε, and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS28E50 when determining a logical level, not triggering any events. Figure 3 shows the initialization sequence required to begin any communication with the DS28E50. A reset pulse followed by a presence pulse indicates that the DS28E50 is ready to receive data, given the correct ROM and device function command. If the bus controller uses slew-rate control on the falling edge, it must pull down the line for t_{RSTL} + t_F to compensate for the edge. A t_{RSTL} duration of 480µs or longer exits the overdrive mode, returning the device to standard speed. If the DS28E50 is in overdrive mode and t_{RSTL} is no longer than 80µs, the device remains in overdrive mode. If the device is in overdrive mode and t_{RSTL} is between 80µs and 480µs, the device resets, but the communication speed is undetermined. After the bus controller has released the line, it goes into receive mode. Now, the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in the case of a special driver chip, through the active circuitry. Now, the 1-Wire bus is pulled to V_{PUP} through the pullup resistor. When

the threshold V_{TH} is crossed, the DS28E50 waits and then transmits a presence pulse by pulling the line low. To detect a presence pulse, the controller must test the logical state of the 1-Wire line at t_{MSP}.

Immediately after t_{RSTH} has expired, the DS28E50 is ready for data communication. In a mixed population network, t_{RSTH} should be extended to a minimum 480µs at standard speed and a 48µs at overdrive speed to accommodate other 1-Wire devices.

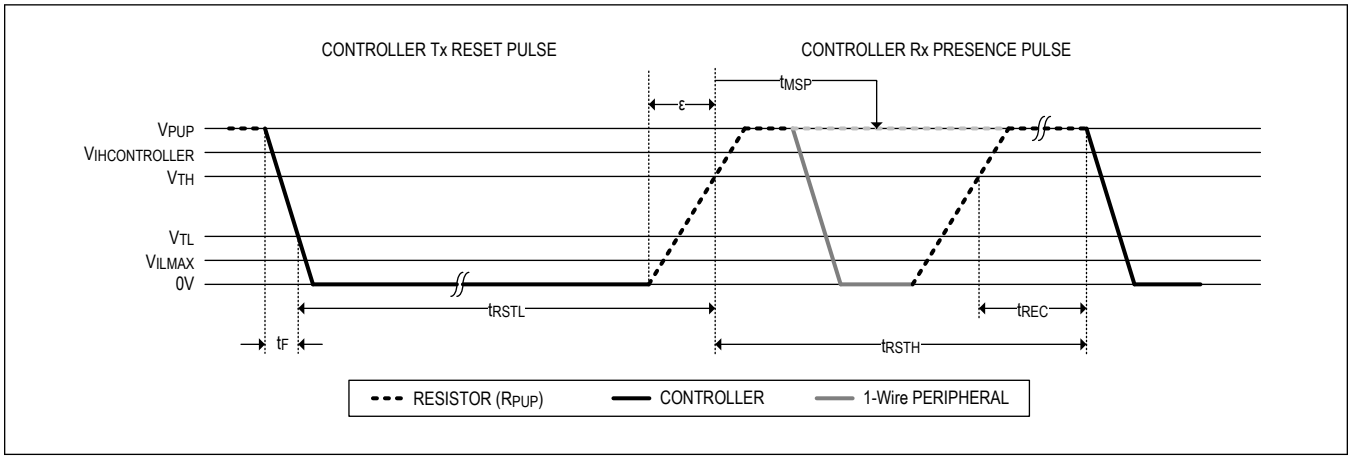


Figure 3. Initialization Procedure: Reset and Presence Pulse

Read/Write Time Slots

Data communication with the DS28E50 takes place in time slots that carry a single bit each. Write time slots transport data from bus controller to peripheral. Read time slots transfer data from peripheral to controller. Figure 4 illustrates the definitions of the write and read time slots. All communication begins with the controller pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS28E50 starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

Controller to Peripheral

For a write-one time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a write-zero time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. For the most reliable communication, the voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS28E50 needs a recovery time t_{REC} before it is ready for the next time slot.

Peripheral to Controller

A read-data time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS28E50 starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS28E50 does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over. The sum of t_{RL} + δ (rise time) on one side and the internal timing generator of the DS28E50 on the other side define the controller sampling window (t_{MSRMIN} to t_{MSRMAX}), in which the controller must perform a read from the data line. For the most reliable communication, t_{RL} should be as short as permissible, and the controller should read close to, but no later than t_{MSRMAX}. After reading from the data line, the controller must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS28E50 to get ready for the next time slot. Note that t_{REC} specified herein applies only to a single DS28E50 attached to a 1-Wire line. For multidevice configurations, t_{REC} must be extended to accommodate the additional 1-Wire device input capacitance. Alternatively, an interface that performs active pullup during the 1-Wire recovery time such as the special 1-Wire line drivers can be used.

1-Wire ROM Commands

Once the bus controller has detected a presence, it can issue one of the seven ROM function commands that the DS28E50 supports. All ROM function commands are 8 bits long. For operational details, see Figure 5 and Figure 6. A descriptive list of these ROM function commands follows in the subsequent sections and the commands are summarized in Table 1.

Table 1. 1-Wire ROM Commands Summary

ROM FUNCTION COMMAND	CODE	DESCRIPTION
Search ROM	F0h	Search for a device
Read ROM	33h	Read ROM from device (single drop)
Match ROM	55h	Select a device by ROM number
Skip ROM	CCh	Select only device on 1-Wire
Resume	A5h	Selected device with RC bit set
Overdrive Skip ROM	3Ch	Put all devices in overdrive
Overdrive Match ROM	69h	Put the device with the ROM in overdrive

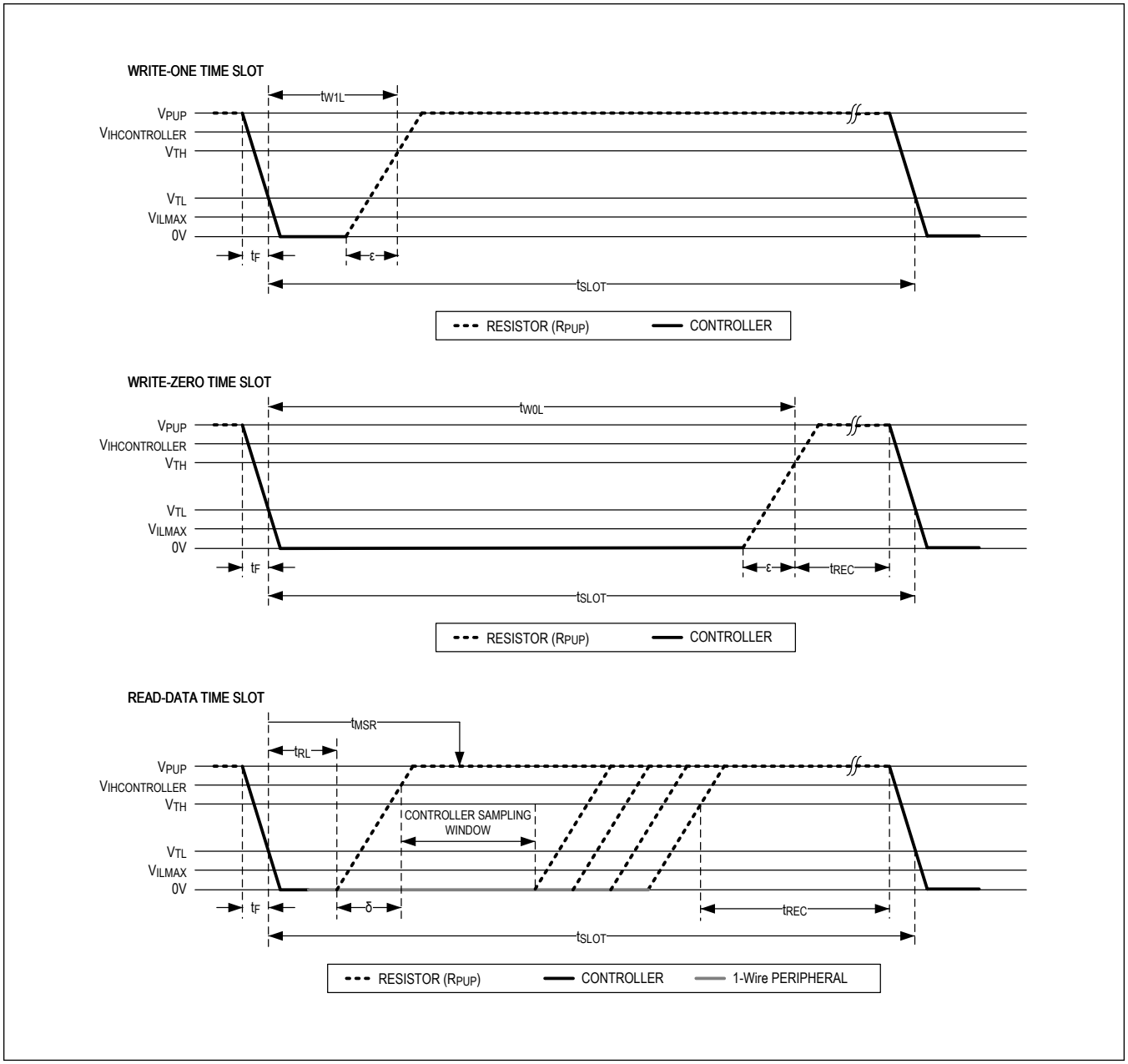


Figure 4. Read/Write Timing Diagrams

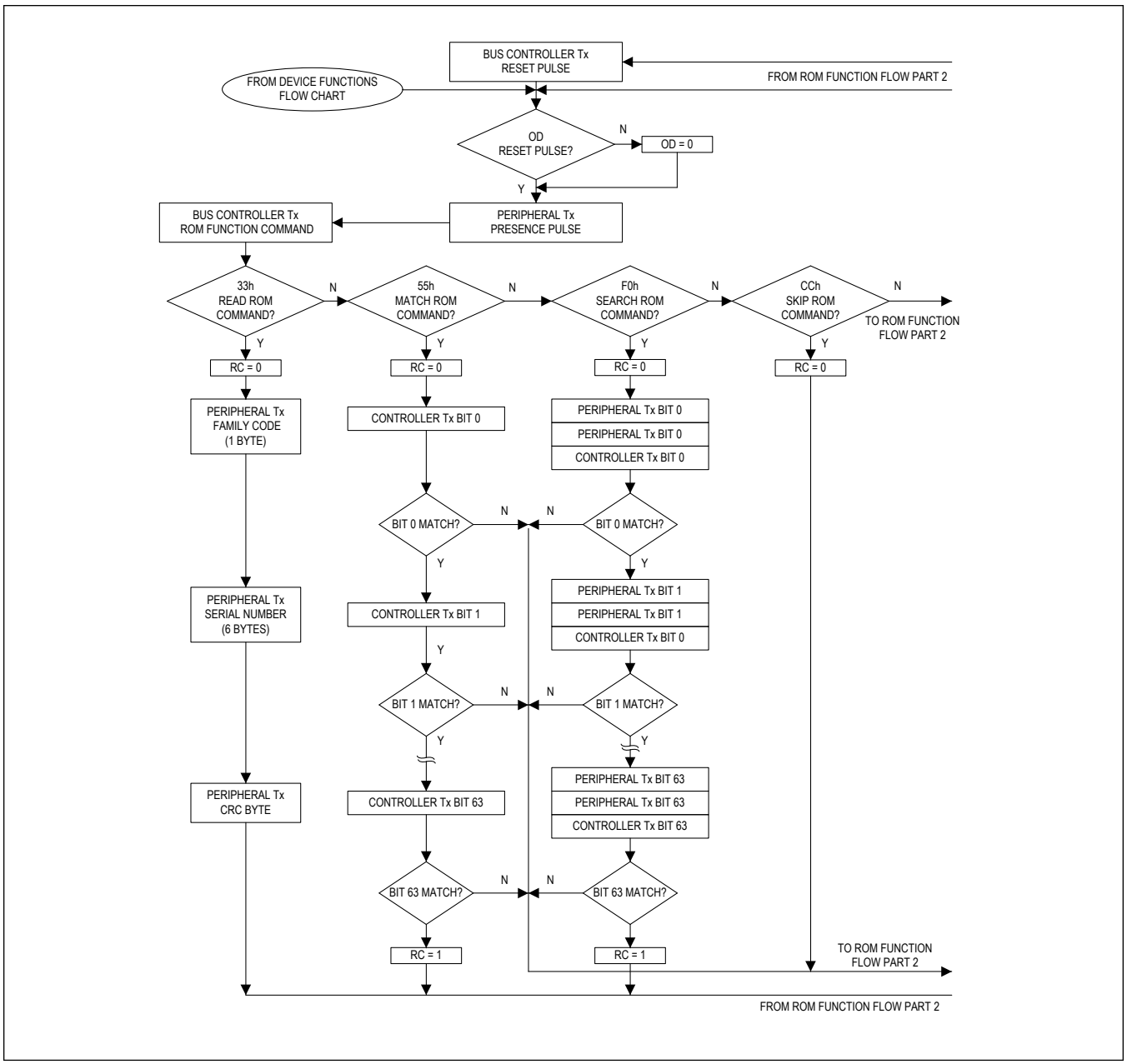


Figure 5. ROM Function Flow, Part 1

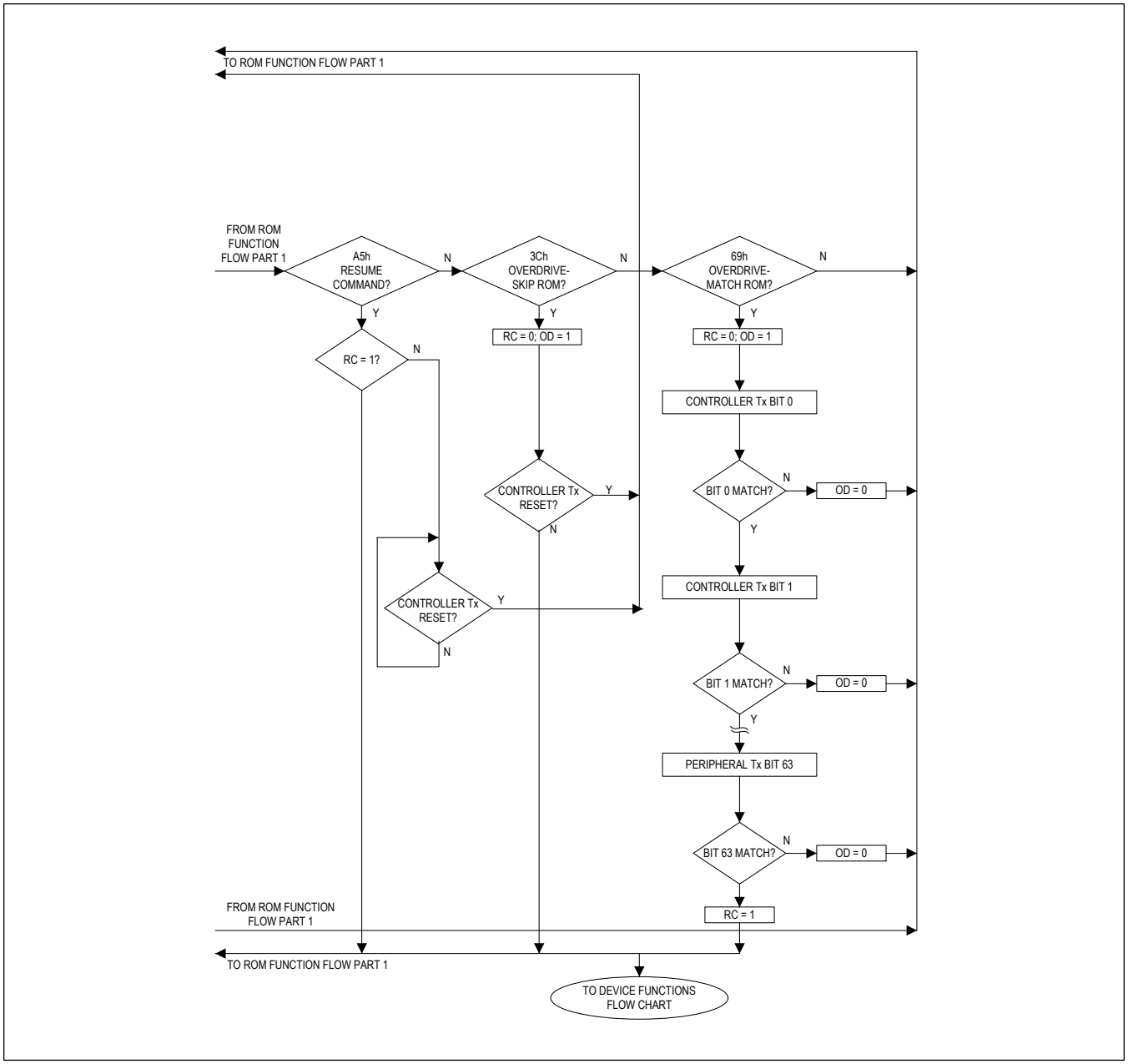


Figure 6. ROM Function Flow, Part 2

Search ROM[F0h]

When a system is initially brought up, the bus controller might not know the number of devices on the 1-Wire bus or their ROM ID numbers. By taking advantage of the wired-AND property of the bus, the controller can use a process of elimination to identify the ID of all peripheral devices. For each bit in the ID number, starting with the least significant bit, the bus controller issues a triplet of time slots. On the first slot, each peripheral device participating in the search outputs the true value of its ID number bit. On the second slot, each peripheral device participating in the search outputs the complemented value of its ID number bit. On the third slot, the controller writes the true value of the bit to be selected. All peripheral devices that do not match the bit written by the controller stop participating in the search. If both of the read bits are zero, the controller knows that peripheral devices exist with both states of the bit. By choosing which state

to write, the bus controller branches in the search tree. After one complete pass, the bus controller knows the ROM ID number of a single device. Additional passes identify the ID numbers of the remaining devices. Refer to *Application Note 187: 1-Wire Search Algorithm* for a detailed discussion, including an example.

Read ROM[33h]

The Read ROM command allows the bus controller to read the DS28E50's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single peripheral on the bus. If more than one peripheral is present on the bus, a data collision occurs when all peripherals try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number result in a mismatch of the CRC.

Match ROM[55h]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus controller to address a specific DS28E50 on a multidrop bus. Only the DS28E50 that exactly matches the 64-bit ROM sequence responds to the subsequent device function command. All other peripherals wait for a reset pulse. This command can be used with a single device or multiple devices on the bus.

Skip ROM [CCh]

This command can save time in a single-drop bus system by allowing the bus controller to access the device functions without providing the 64-bit ROM ID. If more than one peripheral is present on the bus and, for example, a read command is issued following the Skip ROM command, data collision occurs on the bus as multiple peripherals transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Resume [A5h]

To maximize the data throughput in a multidrop environment, the Resume command is available. This command checks the status of the RC bit and, if it is set, directly transfers control to the device function commands, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive-Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume command. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume command.

Overdrive-Skip ROM [3Ch]

On a single-drop bus this command can save time by allowing the bus controller to access the device functions without providing the 64-bit ROM ID. Unlike the normal Skip ROM command, the Overdrive-Skip ROM command sets the DS28E50 into the overdrive mode (OD = 1). All communication following this command must occur at overdrive speed until a reset pulse of minimum 480µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus, this command sets all overdrive-supporting devices into overdrive mode. To subsequently address a specific overdrive-supporting device, a reset pulse at overdrive speed must be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one peripheral supporting overdrive is present on the bus and the Overdrive-Skip ROM command is followed by a read command, data collision occurs on the bus as multiple peripherals transmit simultaneously (open-drain pulldowns produce a wired-AND result).

Overdrive-Match ROM [69h]

The Overdrive-Match ROM command followed by a 64-bit ROM sequence transmitted at overdrive speed allows the bus controller to address a specific DS28E50 on a multidrop bus and to simultaneously set it in overdrive mode. Only the DS28E50 that exactly matches the 64-bit ROM sequence responds to the subsequent device function command. peripherals already in overdrive mode from a previous Overdrive-Skip ROM or successful Overdrive-Match ROM command remain in overdrive mode. All overdrive-capable peripherals return to standard speed at the next reset pulse of minimum 480µs duration. The Overdrive-Match ROM command can be used with a single device or multiple devices on the bus.

Improved Network Behavior (Switch-Point Hysteresis)

In a 1-Wire environment, line termination is possible only during transients controlled by the bus controller (1-Wire driver). 1-Wire networks, therefore, are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a peripheral device to lose synchronization with the controller and, consequently, result in a Search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS28E50 uses a 1-Wire front end that is less sensitive to noise.

The DS28E50's 1-Wire front-end has the following features:

- There is additional lowpass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at overdrive speed.
- There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH}, but does not go below V_{TH} - V_{HY}, it is not recognized (Figure 7, Case A). The hysteresis is effective at any 1-Wire speed.
- There is a time window specified by the rising edge hold-off time t_{REH} during which glitches are ignored, even if they extend below the V_{TH} - V_{HY} threshold (Figure 7, Case B, $t_{GL} < t_{REH}$). Deep voltage drops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the tREH window cannot be filtered out and are taken as the beginning of a new time slot (Figure 7, Case C, $t_{GL} \geq t_{REH}$).

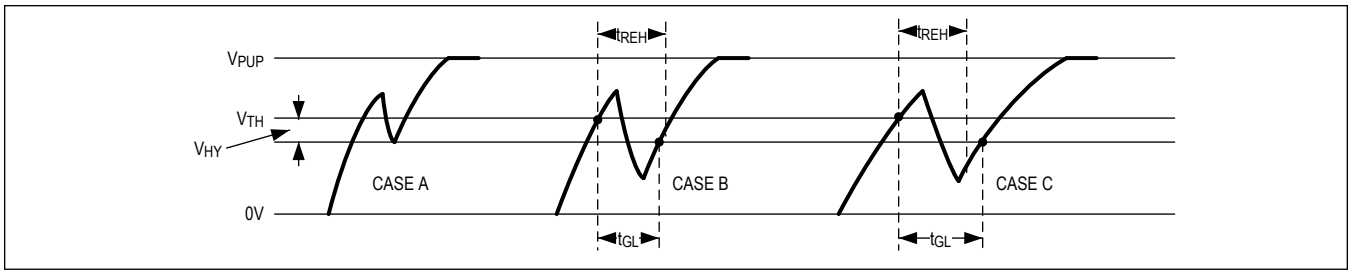


Figure 7. Noise Suppression Scheme

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS28E50Q+T	-40°C to +85°C	6 TDFN-*EP (2.5k pcs)
DS28E50G+T	-40°C to +85°C	2 SFN (2.5k pcs)

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/18	Initial release	—
1	9/18	Added Blockwise Write Memory parameter to Electrical Characteristics table	5
2	10/22	Added SFN package	1, 6, 9, 10, 22