FAIRCHILD™

Is Now Part of

ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD™

January 2015

FSA2380 — Low R$_{ON}$ (0.75 Ω) 3:1 Negative Swing Audio Source Switch

Features

- 10 µA Maximum I$_{CCT}$ Current Over An Expanded Control Voltage Range (V$_{IN}$=2.6 V, V$_{CC}$=4.3 V)
- C$_{ON}$ Capacitance 70 pF Typical
- 0.75 Ω Typical On Resistance (R$_{ON}$)
- 1Bn, 2Bn Ports Support Negative Swing Audio to -2 V
- -3 db Bandwidth: > 120 MHz
- Low Power Consumption (1 µA maximum)
- Power-Off Feature for 1 A/2 A Pin (I$_{IN}$ < 2 µA)
- Packaged in Pb-Free 14-Pin TSSOP and DQFN

Applications

- Cell Phone, PDA, Digital Camera, and Notebook
- LCD Monitor, TV, and Set-Top Box

Description

The FSA2380 is a Double-Pole, Triple Throw (DP3T) multiplexer that routes three dual-channel sources of data or audio under the control of a single pair of select pins. The FSA2380 has special circuitry on the 1A/2A pins to allow a power-off feature. With the V$_{CC}$ supply removed and voltage on the 1A/2A pins, there is minimal leakage current into the 1A/2A data pins. The FSA2380 also features very low quiescent current and a power-off feature to extend battery life. The low quiescent current feature allows mobile handset applications direct interface with the baseband processor general-purpose I/Os. Typical applications involve switching in portables and consumer applications, such as cell phones, digital cameras, and notebooks with hubs or controllers.

.

Ordering Information

| Part Number	Top Mark	Packing Description
FSA2380BQX	2380	14-Terminal Depopulated very thin Quad Flat-pack No leads (DQFN) 2.5 x 3.0 mm, JEDEC MO-241
FSA2380MTCX	FSA2380	14-Lead Thin Shrink Small Outline Package (TSSOP) 4.4 mm wide, JEDEC MO-153

.

Analog Symbol
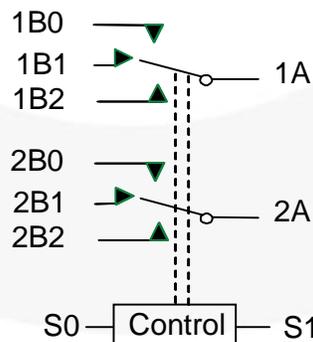
Figure 1.   FSA2380 Analog Symbol

Pin Assignments
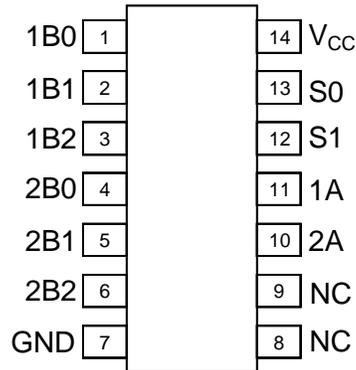
Figure 2.   TSSOP-14 (Top Through View)
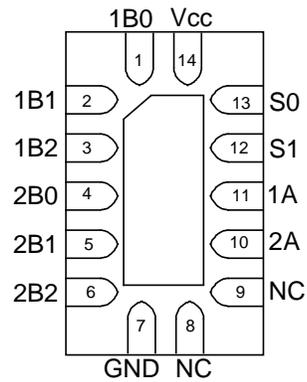
Figure 3.   DQFN-14 (Top Through View)

Pin Descriptions

Name	Description
S0, S1	Switch Control Selects
1A, 2A	A Data Bus (Common)
1Bn, 2Bn	Multiplexed Source inputs

Truth Table

S1	S0	Function
LOW Logic Level	LOW Logic Level	Disconnected (Hi-Z)
LOW Logic Level	HIGH Logic Level	1B0 = 1A; 2B0 = 2A
HIGH Logic Level	LOW Logic Level	1B1 = 1A; 2B1 = 2A
HIGH Logic Level	HIGH Logic Level	1B2 = 1A; 2B2 = 2A

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V$_{CC}$	Supply Voltage		-0.5	6.0	V
V$_{SW}$	Switch I/O Voltage[1]	1Bn, 2Bn Pins	V$_{CC}$-5.5	V$_{CC}$+0.3	V
		1A, 2A Pins	V$_{CC}$-5.5	V$_{CC}$+0.3	V
V$_{CNTRL}$	Control Input Voltage[1] S0, S1 Pins		-0.5	6.0	V
I$_{IK}$	Input Clamp Diode Current		-50		mA
I$_{SW}$	Switch I/O Current (Continuous)			350	mA
I$_{SWPEAK}$	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)			500	mA
P$_D$	Power Dissipation at 85°C	DQFN-14		2.5	µW
		TSSOP-14		2.5	µW
T$_{STG}$	Storage Temperature Range		-65	+150	°C
T$_J$	Maximum Junction Temperature			+150	°C
T$_L$	Lead Temperature (Soldering, 10 seconds)			+260	°C
ESD	Human Body Model (JEDEC: JESD22-A114)	All Pins		5500	
		I/O to GND		8000	kV
		VCC to GND		8000	
	Charged Device Model (JEDEC-JESD22-C101)			2000	kV

Note:
1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V$_{CC}$	Supply Voltage		2.7	5.0	V
V$_{CNTRL}$	Control Input Voltage (V$_{S0:S1}$)		0	V$_{CC}$	V
V$_{SW}$	Switch I/O Voltage		V$_{CC}$ -5.5	V$_{CC}$	
T$_A$	Operating Temperature		-40	+85	°C
θ$_{JA}$	Thermal Resistance (free air)	DQFN-14		145	°C/W
		TSSOP-14			

DC Electrical Characteristics

All typical values are at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V$_{CC}$ (V)	T$_A$ = - 40°C to +85°C			Unit
				Min.	Typ.	Max.	
	Analog Signal Range			V$_{CC}$ - 5.5		V$_{CC}$	V
V$_{IK}$	Clamp Diode Voltage					1.2	V
V$_{IH}$	Control Input Voltage HIGH		2.7 to 3.6	1.2			V
			3.6 to 4.3	1.5			
V$_{IL}$	Control Input Voltage LOW		2.7 to 3.6			0.5	
			3.6 to 4.3			0.7	
I$_{IN}$	Control Input Leakage	V$_{IN}$ = 0 to V$_{CC}$	4.3			±1	µA
I$_{OFF}$	Power Off Leakage Current (Common Port Only 1A, 2A)	Common Port (1A, 2A) V$_{SW}$ = 0 to 4.3 V V$_{CC}$ = 0 V	0V			±10	µA
I$_{NO(0FF)}$	Off-Leakage Current of Port (1Bn, 2Bn)	1Bn, 2Bn or 1A, 2A = 0.3 V, V$_{CC}$ -0.5 V, or Floating	4.3	-50	10	50	nA
I$_{NC(ON)}$	On-Leakage Current of Port 1Bn, 2Bn	1Bn, 2Bn or 1A, 2 A = 0.3 V, V$_{CC}$ -0.5 V, or Floating	4.3	-50	10	50	nA
R$_{ON}$	Switch On Resistance[2]	1Bn or 2Bn = 0 V, 0.7 V, 2.0 V, 2.7 V; I$_{ON}$ = -100 mA See Figure 7, Figure 8	2.70		0.75	2.00	Ω
ΔR$_{ON}$	Delta On Resistance[3]	1Bn or 2Bn = 0.7 V, V$_{CC}$, I$_{ON}$ = -100 mA	2.70		0.50		Ω
R$_{FLAT(ON)}$	On Resistance Flatness[4]	1Bn or 2Bn = 0V, 0.7 V, 2.0 V, 2.7 V; I$_{ON}$ = -100 mA See Figure 7, Figure 8	2.7 to 4.3		0.23	0.40	Ω
I$_{CC}$	Quiescent Supply Current	V$_{SW}$ = 0 or V$_{CC}$-0.3 I$_{OUT}$ = 0	4.3		22	500	nA
I$_{CCT}$	Increate in Quiescent Supply Current per Control Voltage and V$_{CC}$	V$_{CNTRL}$ = 2.6 V	4.3		2.0	10.0	µA
		V$_{CNTRL}$ = 1.8 V			6.5	15.0	

Notes:

2. R$_{ON}$ measured by the voltage drop between 1Bn (2Bn) and 1A (2A) pins at identical current through the switch. R$_{ON}$ is determined by the lower of the voltage on the two pins.
3. Guaranteed by characterization, not production tested.
4. Flatness is defined as the difference between the maximum and minimum values of on resistance over the specified range of conditions.

AC Electrical Characteristics

All typical value are for V_{CC} = 3.3 V at 25ºC unless otherwise specified.

Symbol	Parameter	Conditions	V$_{CC}$ (V)	T$_A$ = - 40°C to +85°C			Unit
				Min.	Typ.	Max.	
t$_{ON}$	Turn-On Time S[0:1] to Output	V$_{Bn}$ = 1.5 V, R$_L$ = 50Ω, C$_L$ = 35 pF Figure 10, Figure 12	2.7 to 4.3		30	60	ns
t$_{OFF}$	Turn-Off Time S[0:1] to Output	V$_{Bn}$ = 1.5 V, R$_L$ = 50Ω, C$_L$ = 35 pF Figure 10, Figure 12	2.7 to 4.3		22	45	ns
t$_{PD}$	Propagation Delay[5]	R$_L$ = 50 Ω, C$_L$ = 5 pF Figure 13	3.3		0.25		ns
t$_{BBM}$	Break-Before-Make[5]	R$_L$ = 50 Ω, C$_L$ = 5 pF V$_{IN1}$ = V$_{IN2}$ = V$_{IN3}$ = 1.5 V Figure 11	2.7 to 4.3	1	6		ns
Q	Charge Injection	R$_{GEN}$ = 0 Ω, C$_L$ = 100 pF, R$_L$ = OPEN Figure 14	2.7 to 4.3		9		pC
O$_{IRR}$	Off-Isolation	f = 100 kHz, R$_L$ = 50 Ω Figure 4, Figure 16	2.7 to 4.3		-68		dB
Xtalk	Non-Adjacent Channel Crosstalk	f = 100 kHz, R$_L$ = 50 Ω Figure 5, Figure 17	2.7 to 4.3		-60		dB
THD	Total Harmonic Distortion	f = 20 Hz to 20 kHz, R$_L$ = 600 Ω,V$_{SW}$ = 0.5V$_{pp}$, Figure 20	2.7 to 4.3		0.01		%
BW	-3 db Bandwidth	R$_L$ = 50 Ω, C$_L$ = 0, 5 pF Figure 6, Figure 15	2.7 to 4.3		120		MHz

Note:
5. Guaranteed by characterization, not production tested.

Capacitance

| Symbol	Parameter	Conditions	T$_A$ = - 40°C to +85°C	Unit
			Typical	
C$_{IN}$	Control Pin Input Capacitance	V$_{CC}$ = 0 V	2.75	pF
C$_{ON}$	A/B On Capacitance	V$_{CC}$ = 3.3 V; S[0:1] = 01, 10, 11; f = 1 MHz Figure 19	70	pF
C$_{OFFA}$	Port 1A, 2A Off Capacitance	V$_{CC}$ = 3.3 V, S[0:1] = 00 Figure 18	42	pF
C$_{OFFB}$	Port 1Bn, 2Bn Off Capacitance	V$_{CC}$ = 3.3 V, S[0:1] = 00 Figure 18	20	pF

Typical Characteristics
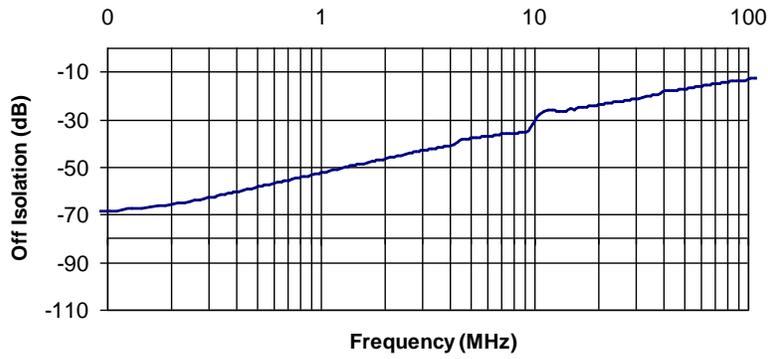
Figure 4.   Off Isolation V$_{CC}$ = 3.3 V,C$_L$ = 0 pF
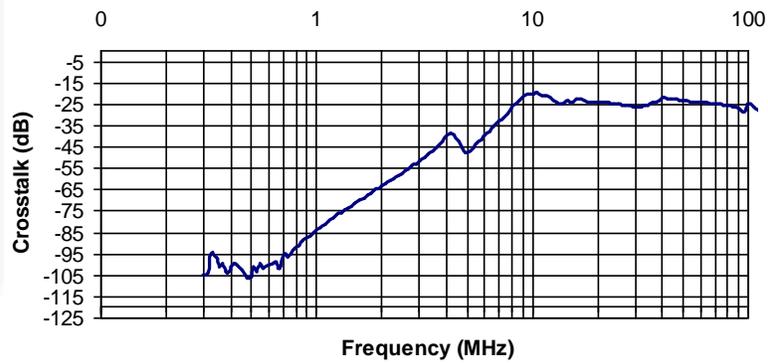
Figure 5.   Non-Adjacent Crosstalk V$_{CC}$ = 3.3 V,C$_L$ = 0 pF
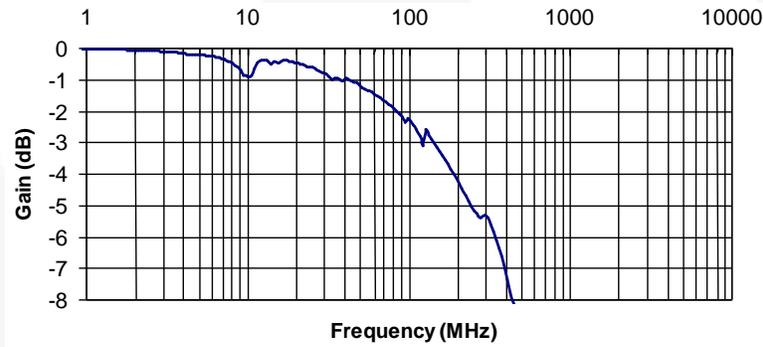
Figure 6.   Bandwidth V$_{CC}$ = 3.3 V,C$_L$ = 0 pF

R$_{ON}$
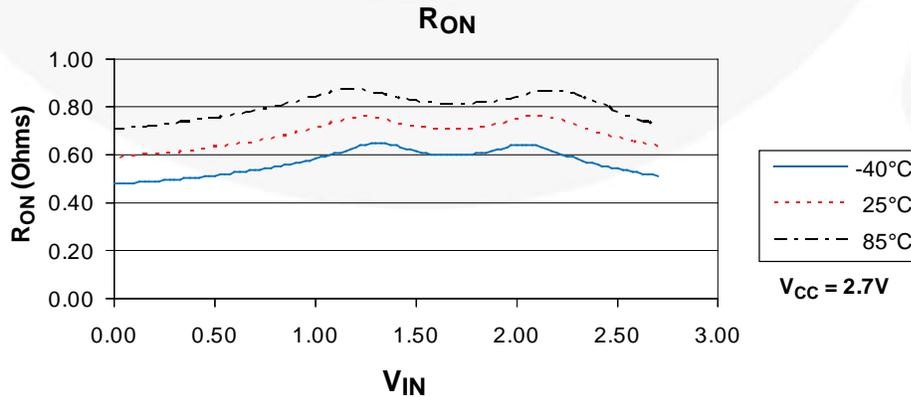
Figure 7.   Switch On Resistance, R$_{ON}$ V$_{CC}$ = 2.7 V

Test Diagrams
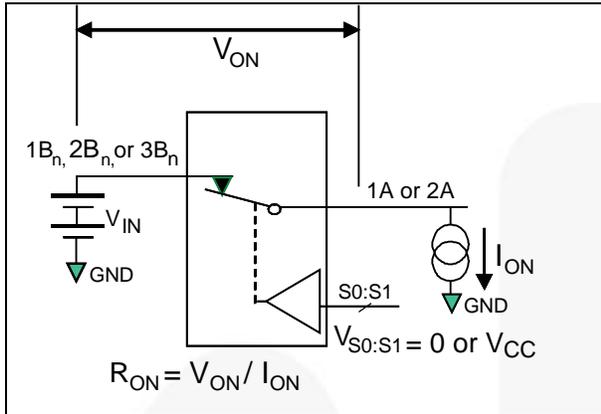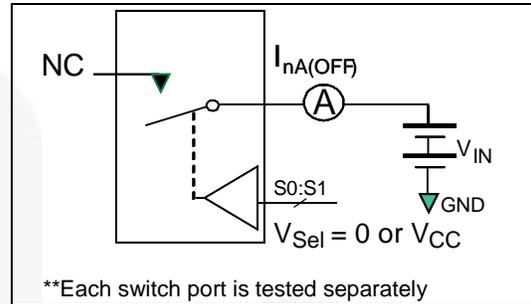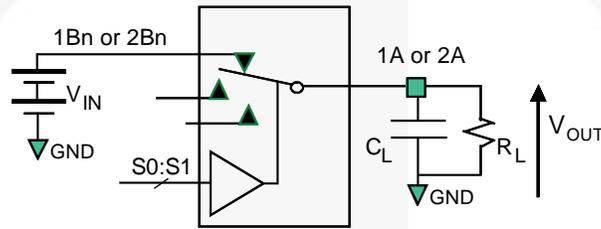
V_{ON}

1B$_n$, 2B$_n$, or 3B$_n$

V_{IN}

GND

1A or 2A

I_{ON}

GND

S0:S1

$V_{S0:S1} = 0$ or V_{CC}

$R_{ON} = V_{ON} / I_{ON}$

Figure 8.   On Resistance

NC

$I_{nA(OFF)}$

A

V_{IN}

GND

S0:S1

$V_{Sel} = 0$ or V_{CC}

**Each switch port is tested separately

Figure 9.   Off Leakage

1Bn or 2Bn

V_{IN}

GND

S0:S1

1A or 2A

C_L

R_L

V_{OUT}

GND

R_L and C_L are functions of the application
environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance

Figure 10.   AC Test Circuit Load
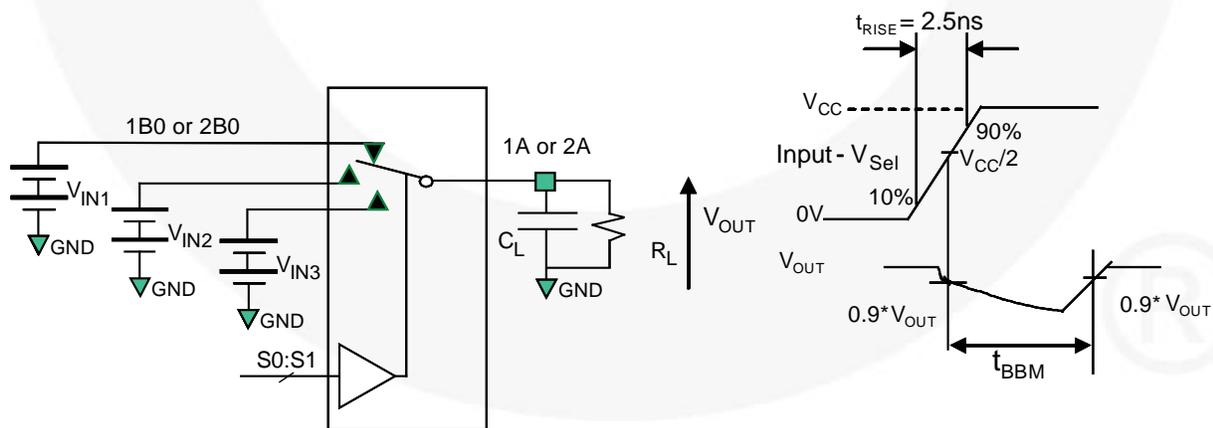
1B0 or 2B0

V_{IN1}

GND

V_{IN2}

GND

V_{IN3}

GND

S0:S1

1A or 2A

C_L

R_L

V_{OUT}

$t_{RISE} = 2.5ns$

V_{CC}

90%

Input - V_{Sel}

$V_{CC}/2$

0V

10%

V_{OUT}

$0.9*V_{OUT}$

$0.9* V_{OUT}$

t_{BBM}

R_L and C_L are functions of the application
environment (see AC Tables for specific values)
C_L includes test fixture and stray capacitance

Figure 11.   Break-Before-Make Timing

Test Diagrams (Continued)
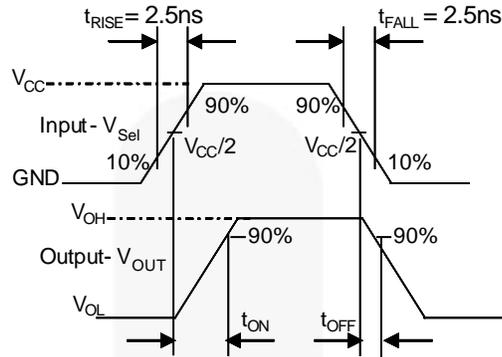
Figure 12.   Turn-On / Turn-Off Waveforms
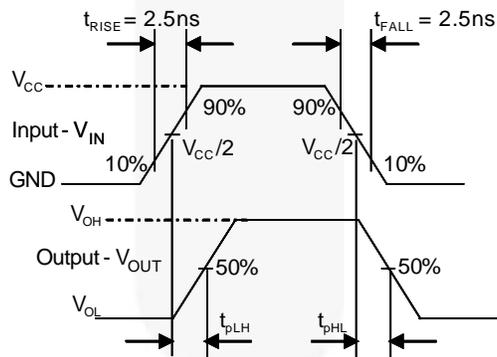
Figure 13.   Switch Propagation Delay Waveforms

$$Q = \Delta V_{OUT} \cdot C_L$$
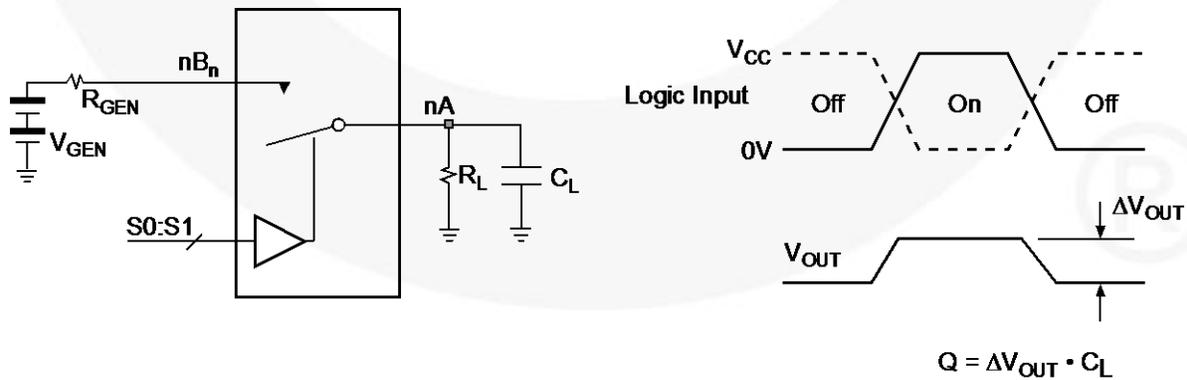
Figure 14.   Charge Injection Test

Test Diagrams (Continued)

R$_S$ and R$_T$ are functions of the application
environment (see AC Tables for specific values)

Figure 15.   Bandwidth

R$_S$ and R$_T$ are functions of the application
environment (see AC Tables for specific values

Off -Isolation = 20 Log (V$_{OUT}$ / V$_{IN}$)
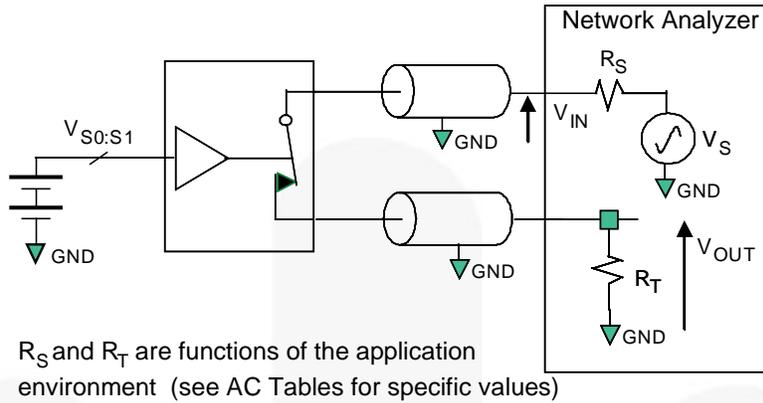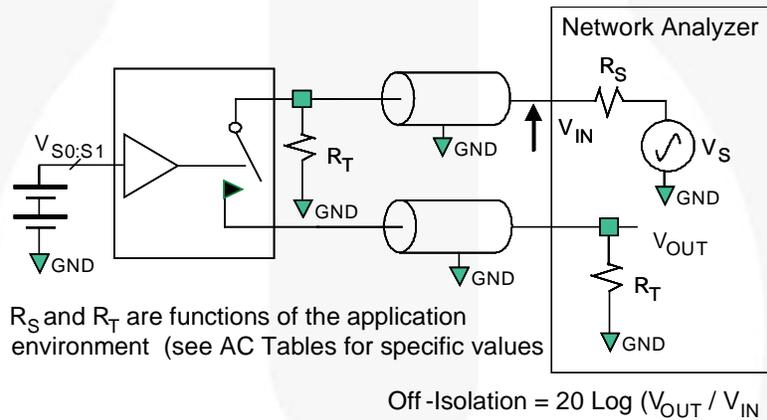
Figure 16.   Channel Off Isolation

CROSSTALK = 20 Log (V$_{OUT}$/ V$_{IN}$)
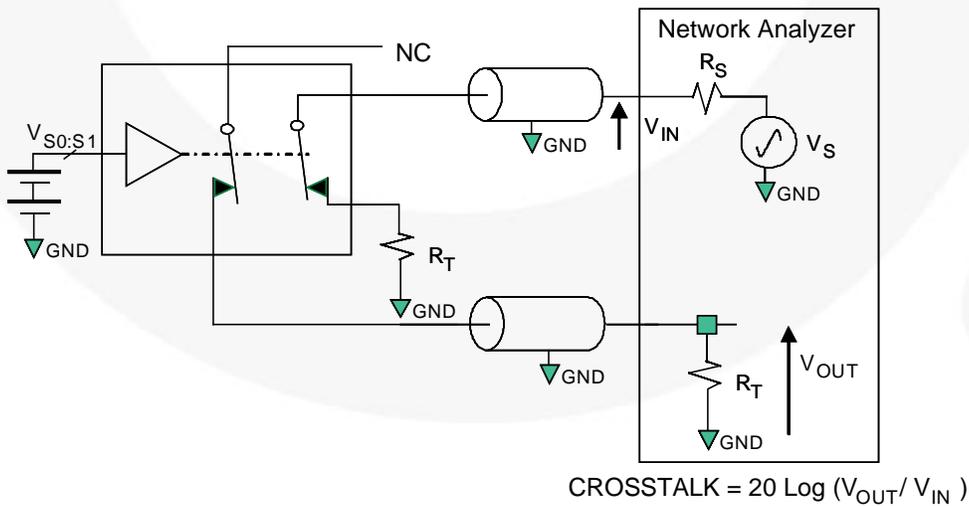
Figure 17.   Non-Adjacent Channel-to-Channel Crosstalk

Test Diagrams (Continued)
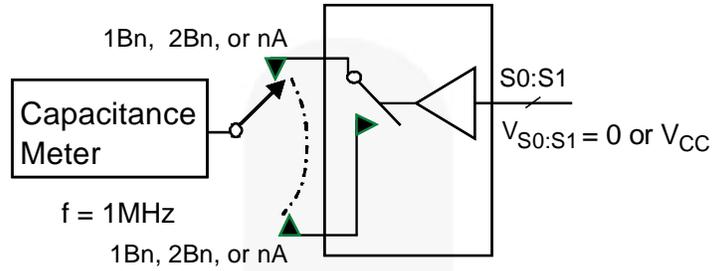
Figure 18.   Channel Off Capacitance
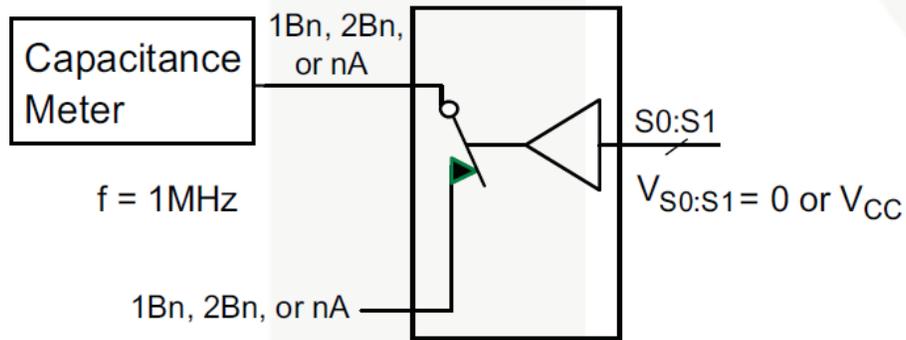
Figure 19.   Channel On Capacitance
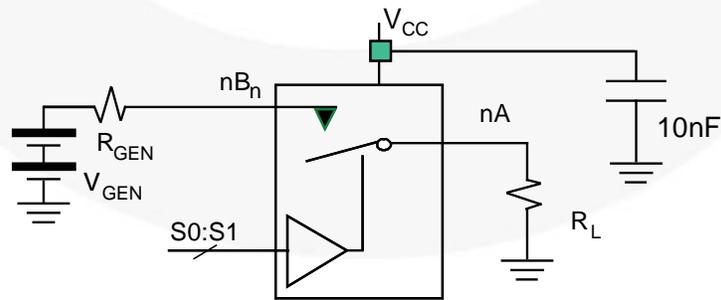
Figure 20.   Total Harmonic Distortion

TOP VIEW

2X □ 0.05 C

3.00   ◄ B

A

2.50

□ 0.05 C
2X

PIN #1 QUADRANT

TOP VIEW

SIDE VIEW

0.80±0.05

// 0.10 C

0.20±0.05

□ 0.08 C

0.025±0.025
SEATING
PLANE

SIDE VIEW

C

BOTTOM VIEW

3.00±0.05

1.65±0.05

0.370±0.05
(14X)

PIN #1 IDENT

2   6

1

0.50

14

7

1.15±0.05

8

2.50±0.05

13   9

0.25±0.05
(14X)

0.50

2.00

BOTTOM VIEW

⌖ 0.10 Ⓜ C A B
0.05 Ⓜ C

RECOMMENDED LAND PATTERN

4.00 MAX

2.20 MAX

1.40 MAX

13   9

1.00
MAX

14

0.50 TYP

8

1.70
MAX

1

7

3.50
MAX

(0.90)

2   6

0.50 TYP   0.24 TYP
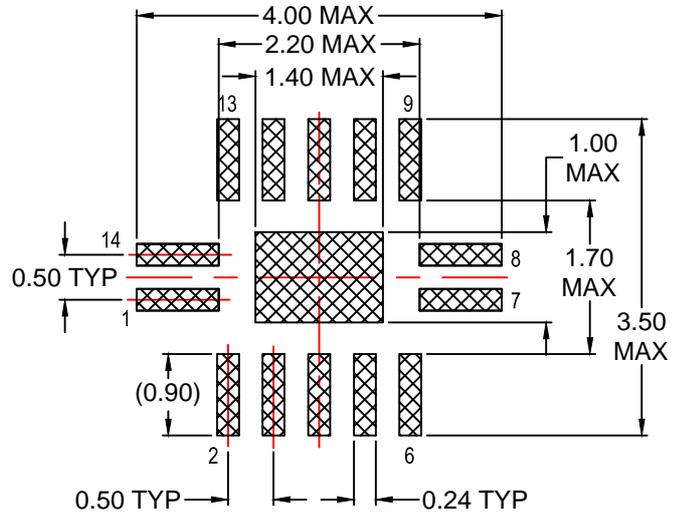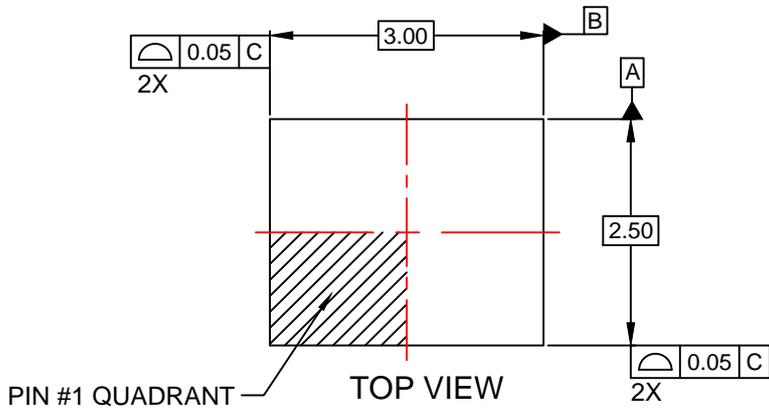
RECOMMENDED LAND PATTERN
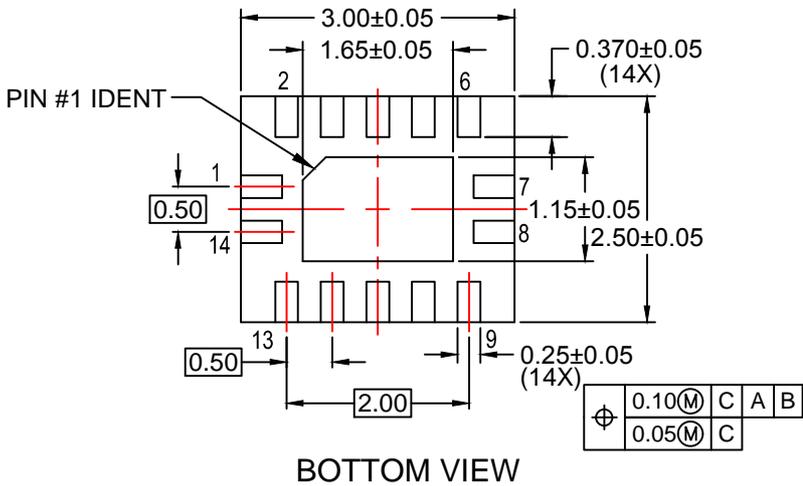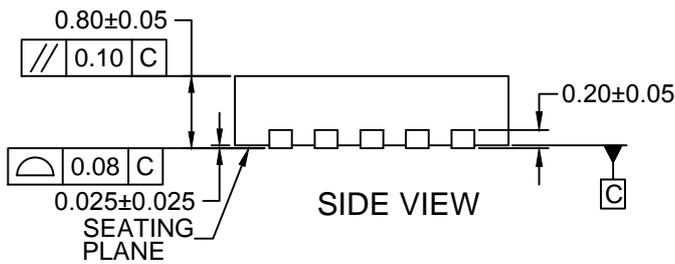
NOTES:

A. CONFORMS TO JEDEC REGISTRATION
   MO-241, VARIATION AA

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER
   ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS
   EXISTING INDUSTRY LAND PATTERN.

E. DRAWING FILENAME: MKT-MLP14Arev2.

FAIRCHILD.

PUBLICATION ORDERING INFORMATION

© Semiconductor Components Industries, LLC

www.onsemi.com