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Ultra-Low Power, Single-Channel Integrated Biopotential (R-to-R Detection) AFE

MAX30004

General Description

The MAX30004 is a complete, biopotential, analog front-end solution for wearable applications. It offers high performance for clinical and fitness applications, with ultra-low power for long battery life. The MAX30004 is a single biopotential channel providing heart rate detection.

The biopotential channel has ESD protection, EMI filtering, internal lead biasing, DC leads-off detection, ultra-low power leads-on detection during standby mode. Soft power-up sequencing ensures no large transients are injected into the electrodes. The biopotential channel also has high input impedance, low noise, high CMRR, programmable gain, various low-pass and high-pass filter options, and a high resolution analog-to-digital converter. The biopotential channel is DC coupled, can handle large electrode voltage offsets, and has a fast recovery mode to quickly recover from overdrive conditions, such as defibrillation and electrosurgery.

The MAX30004 is available in a 30-bump wafer-level package (WLP), operating over the 0°C to +70°C commercial temperature range.

Applications

- Single Lead Wireless Patches for At-Home/ In-Hospital Monitoring
- Chest Band Heart Rate Monitors for Fitness Applications

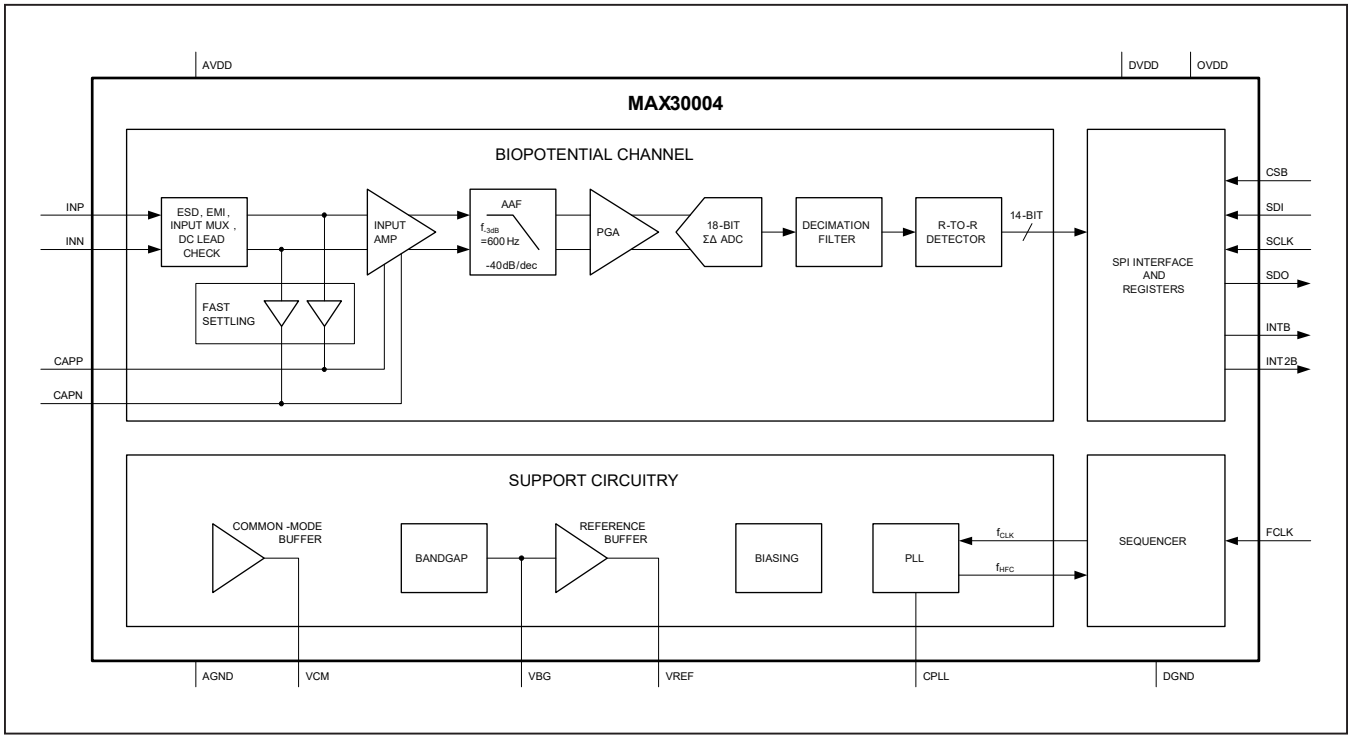
***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Heart Rate Detection with Interrupt Feature Eliminates the Need to Extract and Process the ECG Data on the Microcontroller
  - Robust R-R Detection in High Motion Environment at Extremely Low Power
- Clinical-Grade Biopotential AFE with High-Resolution Data Converter
  - 15.5 Bits Effective Resolution with 5µV_{P-P} Noise
- Better Dry Starts Due to Much Improved Real World CMRR and High Input Impedance
  - Fully Differential Input Structure with CMRR > 100dB
- Offers Better Common-Mode to Differential Mode Conversion Due to High Input Impedance
  - High Input Impedance > 500MΩ for Extremely Low Common-to-Differential Mode Conversion
- Minimum Signal Attenuation at the Input During Dry Start Due to High Electrode Impedance
- High DC Offset Range of ±650mV (1.8V, typ) Allows to Be Used with Wide Variety of Electrodes
- High AC Dynamic Range of 65mV_{P-P} Will Help the AFE Not Saturate in the Presence of Motion/Direct Electrode Hits
- Longer Battery Life Compared to Competing Solutions
  - 85µW at 1.1V Supply Voltage
- Leads-On Interrupt Feature Keeps the µC in Deep Sleep Mode with RTC Off Until Valid Lead Condition is Detected
  - Lead-On Detect Current: 0.7µA (typ)
- Configurable Interrupts Allows the µC Wake-Up Only on Every Heart Beat Reducing the Overall System Power
- High-Speed SPI Interface
- Shutdown Current of 0.5µA (typ)

19-8732; Rev 1; 1/23

Functional Diagram



Absolute Maximum Ratings

AV_{DD} to AGND .....-0.3V to +2.0V
DV_{DD} to DGND .....-0.3V to +2.0V
AV_{DD} to DV_{DD}.....-0.3V to +0.3V
OV_{DD} to DGND .....-0.3V to +3.6V
AGND to DGND .....-0.3V to +0.3V
CSB, SCLK, SDI, FCLK to DGND .....-0.3V to +3.6V
SDO, INTB, INT2B to
DGND .....-0.3V to the lower of (3.6V and OV_{DD} + 0.3V)
All other pins to
AGND .....-0.3V to the lower of (2.0V and AV_{DD} + 0.3V)
Maximum Current into Any Pin.....±50mA

Continuous Power Dissipation (T_A = +70°C)
30-Bump WLP (derate 24.3mW/°C
above +70°C) 1945.5mW
Operating Temperature Range.....0°C to +70°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (Soldering, 10sec).....+300°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....44°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIOPOTENTIAL CHANNEL						
AC Differential Input Range		V_{AVDD} = +1.1V, THD < 0.3%	-15		+15	mV_{p-p}
		V_{AVDD} = +1.8V, THD < 0.3%		±32.5		
DC Differential Input Range		V_{AVDD} = +1.1V, shift from nominal gain < 2%	-300		+300	mV
		V_{AVDD} = +1.8V		±650		
Common Mode Input Range		V_{AVDD} = +1.1V, from V_{MID}, shift from nominal gain < 2%	-150		+150	mV
		V_{AVDD} = +1.8V, from V_{MID}, shift from nominal gain < 2%		±550		
Common Mode Rejection Ratio	CMRR	0Ω source impedance, f = 64Hz (Note 3)	105	115		dB
		With impedance mismatch (Note 4)		77		
Input Referred Noise		BW = 0.05 - 150Hz, G_{CH} = 20x		0.82		μV_{RMS}
				5.4		μV_{p-p}
		BW = 0.05 - 40Hz, G_{CH} = 20x (Note 3)		0.53	1.0	μV_{RMS}
				3.5	6.6	μV_{p-p}
Input Leakage Current		T_A = +25°C	-1	0.1	+1	nA
Input Impedance (INA)		Common-mode, DC		45		GΩ
		Differential, DC		1500		MΩ

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Total Harmonic Distortion	THD	V_{AVDD} = +1.80V, V_{IN} = 65mV_{p-p}, F_{IN} = 64Hz, G_{CH} = 20x, electrode offset = ±300mV			0.025		%
		V_{AVDD} = +1.1V, V_{IN} = 30mV_{p-p}, F_{IN} = 64Hz, G_{CH} = 20x, electrode offset = ±300mV				0.3	
Gain Setting	G_{CH}	Programmable, see GAIN[1:0]			20 to 160		V/V
Gain Error		V_{AVDD} = +1.8V, G_{CH} = 20x, INP = INN = VMID		-2.5		+2.5	%
		V_{AVDD} = +1.1V, G_{CH} = 20x, INP = INN = VMID		-4.5		+4.5	%
Offset Error		(Note 5)			0.1		% of FSR
ADC Resolution					18		Bits
ADC Sample Rate		Programmable, see RATE[1:0]			125 to 512		SPS
CAPP to CAPN Impedance	R_{HPF}	FHP = 1/(2Π x R_{HPF} x C_{HPF}), C_{HPF} = capacitance between CAPP and CAPN		320	450	600	kΩ
Analog High-Pass Filter Slew Current		Fast recovery enabled (1.8V)			160		µA
		Fast recovery enabled (1.1V)			55		
		Fast recovery disabled			0.09		
Fast Settling Recovery Time		C_{HPF} = 10µF			500		ms
Digital Low Pass Filter		Linear phase FIR filter, ECG_RATE = 00, 01	DLPF[0:1] = 01		40		Hz
			DLPF[0:1] = 10		100		
			DLPF[0:1] = 11		150		
Digital High Pass Filter		Phase-corrected 1st-order IIR filter. DHPF = 1			0.5		Hz
Power Supply Rejection	PSRR	Lead bias disabled, DC			107		dB
		Lead bias disabled, f = 64Hz			110		
INPUT MUX							
DC Lead Off Check		Pullup/ pulldown	DCLOFF_IMAG[2:0] = 001		5		nA
			DCLOFF_IMAG[2:0] = 010		10		
			DCLOFF_IMAG[2:0] = 011		20		
			DCLOFF_IMAG[2:0] = 100		50		
			DCLOFF_IMAG[2:0] = 101		100		

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Lead Off Comparator Low Threshold		DCLOFF_VTH[1:0] = 11 (Note 6)			V_{MID} - 0.50		V
		DCLOFF_VTH[1:0] = 10 (Note 7)			V_{MID} - 0.45		
		DCLOFF_VTH[1:0] = 01 (Note 8)			V_{MID} - 0.40		
		DCLOFF_VTH[1:0] = 00			V_{MID} - 0.30		
DC Lead Off Comparator High Threshold		DCLOFF_VTH[1:0] = 11 (Note 6)			V_{MID} + 0.50		V
		DCLOFF_VTH[1:0] = 10 (Note 7)			V_{MID} + 0.45		
		DCLOFF_VTH[1:0] = 01 (Note 8)			V_{MID} + 0.40		
		DCLOFF_VTH[1:0] = 00			V_{MID} + 0.30		
Lead Bias Impedance		Lead bias enabled	RBIASV[1:0] = 00		50		MΩ
			RBIASV[1:0] = 01		100		
			RBIASV[1:0] = 10		200		
Lead Bias Voltage	V_{MID}	Lead bias enabled			V_{AVDD}/ 2.15		V
INTERNAL REFERENCE/COMMON-MODE							
V_{BG} Output Voltage	V_{BG}				0.650		V
V_{BG} Output Impedance					100		kΩ
External V_{BG} Compensation Capacitor	C_{VBG}			1			µF
V_{REF} Output Voltage	V_{REF}	T_A = +25°C		0.995	1.000	1.005	V
V_{REF} Temperature Coefficient	TC_{REF}	T_A = 0°C to +70°C			10		ppm/°C
V_{REF} Buffer Line Regulation					330		µV/V
V_{REF} Buffer Load Regulation		I_{LOAD} = 0 to 100µA			25		µV/µA
External V_{REF} Compensation Capacitor	C_{REF}			1	10		µF
V_{CM} Output Voltage	V_{CM}				0.650		V
External V_{CM} Compensation Capacitor	C_{CM}			1	10		µF
DIGITAL INPUTS (SDI, SCLK, CSB, FCLK)							
Input-Voltage High	V_{IH}			0.7 × V_{OVDD}			V
Input-Voltage Low	V_{IL}					0.3 × V_{OVDD}	V
Input Hysteresis	V_{HYS}				0.05 × V_{OVDD}		V

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Capacitance	C_{IN}				10		pF
Input Current	I_{IN}			-1		+1	µA
DIGITAL OUTPUTS (SDO, INTB, INT2B)							
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA		V_{OVDD} – 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 1mA				0.4	V
Three-State Leakage Current				-1		+1	µA
Three-State Output Capacitance					15		pF
POWER SUPPLY							
Analog Supply Voltage	V_{AVDD}	Connect V_{AVDD} to V_{DVDD}		1.1		2.0	V
Digital Supply Voltage	V_{DVDD}	Connect V_{DVDD} to V_{AVDD}		1.1		2.0	V
Interface Supply Voltage	V_{OVDD}	Power for I/O drivers only		1.65		3.6	V
Supply Current	I_{AVDD} + I_{DVDD}	R-R Operation	V_{AVDD} = V_{DVDD} = +1.1V		76		µA
			V_{AVDD} = V_{DVDD} = +1.8V		100		
			V_{AVDD} = V_{DVDD} = +2.0V		110	122	
		ULP Lead On Detect	T_A = +70°C		0.98		
			T_A = +25°C		0.73	2.5	
Interface Supply Current	I_{OVDD}	V_{OVDD} = +1.65V, ADC at 512sps (Note 9)			0.2		µA
		V_{OVDD} = +3.6V, ADC at 512sps (Note 9)			0.6	1.6	
Shutdown Current	I_{SAVDD} + I_{SDVDD}	V_{AVDD} = V_{DVDD} = 2.0V	T_A = +70°C		0.79		µA
			T_A = +25°C		0.51	2.5	
	I_{SOVDD}	V_{OVDD} = +3.6V, V_{AVDD} = V_{DVDD} = +2.0V				1.1	

Timing Characteristics

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS						
SCLK Frequency	f_{SCLK}		0		12	MHz
SCLK Period	t_{CP}		83			ns
SCLK Pulse Width High	t_{CH}		15			ns
SCLK Pulse Width Low	t_{CL}		15			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	To 1st SCLK rising edge (RE)	15			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive RE preceding 1st RE	0			ns
CSB Rise to SCLK Rise Hold Time	t_{CSH1}	Applies to 32nd RE, executed write	10			ns
CSB Rise to SCLK Rise	t_{CSA}	Applies to 32nd RE, aborted write sequence	15			ns
SCLK Rise to CSB Fall	t_{CSF}	Applies to 32nd RE	100			ns
CSB Pulse-Width High	t_{CSPW}		20			ns
SDI-to-SCLK Rise Setup Time	t_{DS}		8			ns
SDI to SCLK Rise Hold Time	t_{DH}		8			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 20pf			40	ns
		C_{LOAD} = 20pf, V_{AVDD} = V_{DVDD} ≥ 1.8V, V_{OVDD} ≥ 2.5V			20	ns
SCLK Fall to SDO Hold	t_{DOH}	C_{LOAD} = 20pf	2			ns
CSB Fall to SDO Fall	t_{DOE}	Enable time, C_{LOAD} = 20pf			30	ns

Timing Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable time			35	ns
FCLK Frequency	f_{FCLK}	External reference clock	32.768			kHz
FCLK Period	t_{FP}			30.52		µs
FCLK Pulse-Width High	t_{FH}	50% duty cycle assumed		15.26		µs
FCLK Pulse-Width Low	t_{FL}	50% duty cycle assumed		15.26		µs

Note 2: Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 3: Guaranteed by design and characterization. Not tested in production.
Note 4: One electrode drive with <10Ω source impedance, the other driven with 51kΩ in parallel with a 47nF per IEC60601-2-47.
Note 5: Inputs connected to 51kΩ in parallel with a 47nF to V_{CM}.
Note 6: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.65V.
Note 7: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.55V.
Note 8: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.45V.
Note 9: f_{SCLK} = 4MHz, burst mode, EFIT = 8, C_{SDO} = C_{INTB} = 50pF.

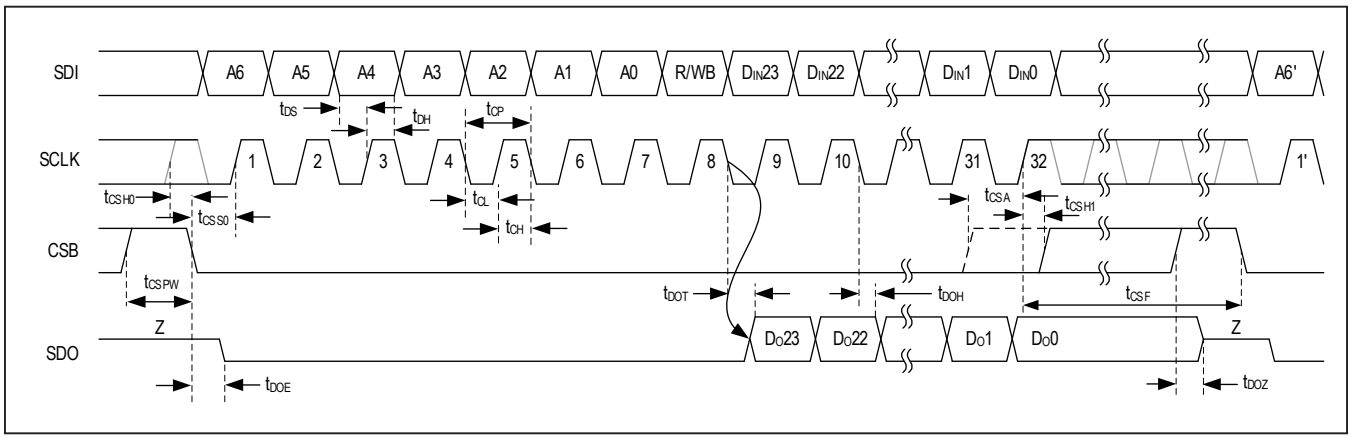


Figure 1a. SPI Timing Diagram

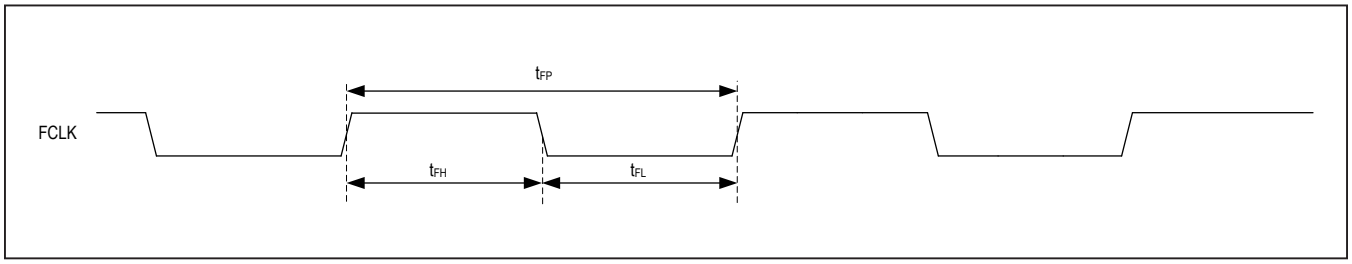
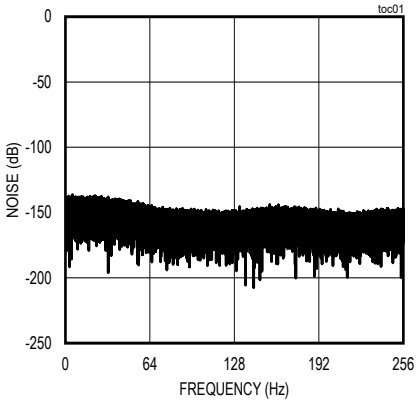


Figure 1b. FCLK Timing Diagram

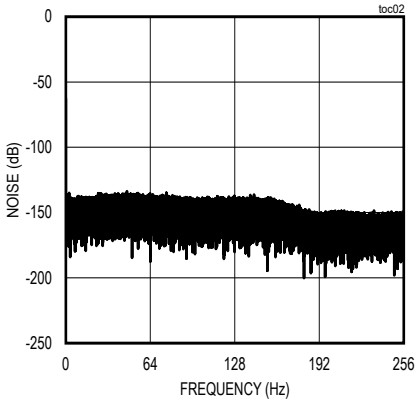
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

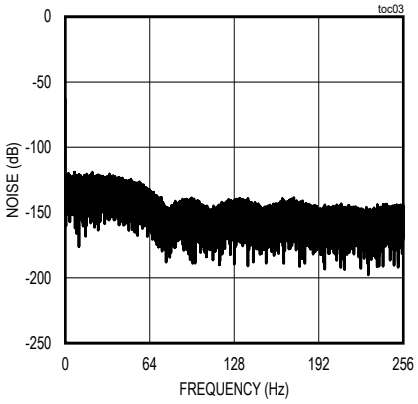
CHANNEL NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 20, LPF = 40Hz



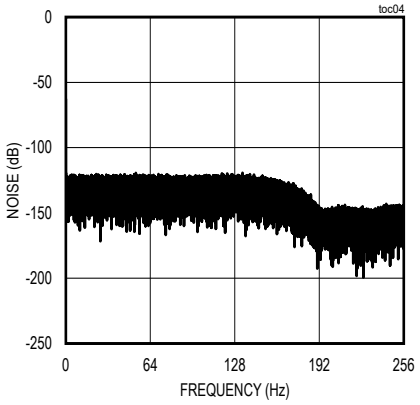
CHANNEL NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 20, LPF = 150Hz



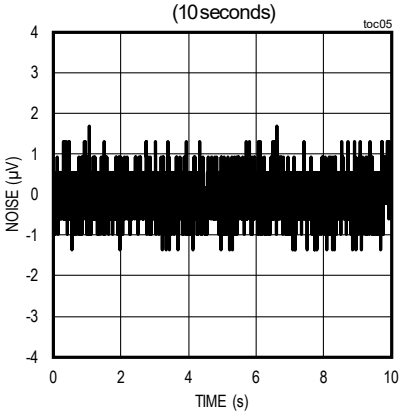
CHANNEL NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 160, LPF = 40Hz



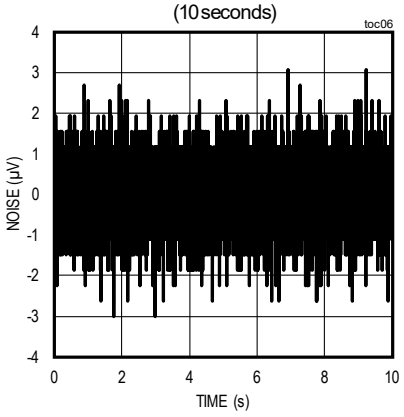
CHANNEL NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 160, LPF = 150Hz



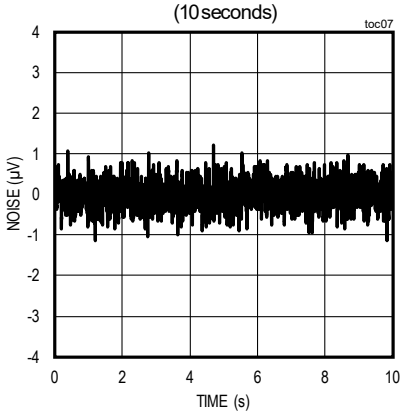
CHANNEL INPUT-REFERRED NOISE vs. TIME
GAIN = 20, LPF = 40Hz
(10 seconds)



CHANNEL INPUT-REFERRED NOISE vs. TIME
GAIN = 20, LPF = 150Hz
(10 seconds)



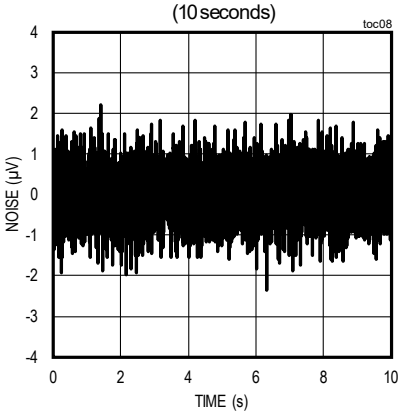
CHANNEL INPUT-REFERRED NOISE vs. TIME
GAIN = 160, LPF = 40Hz
(10 seconds)



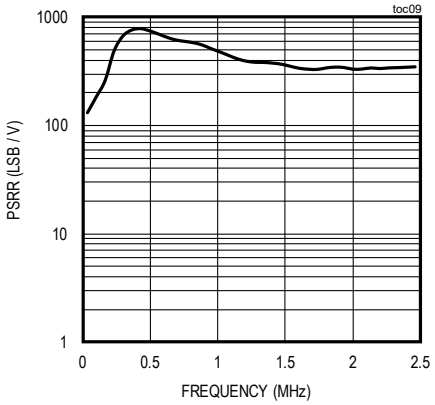
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

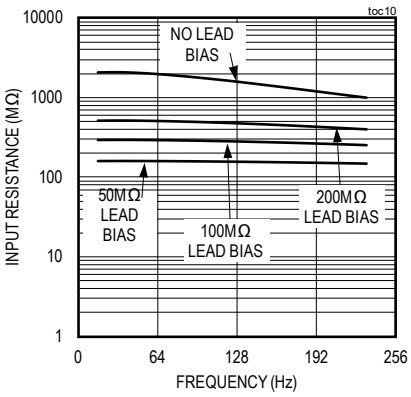
CHANNEL INPUT-REFERRED NOISE vs. TIME
GAIN = 160, LPF = 150Hz
(10 seconds)



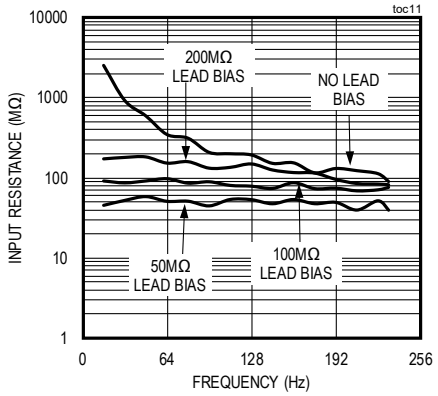
CHANNEL PSRR vs. FREQUENCY



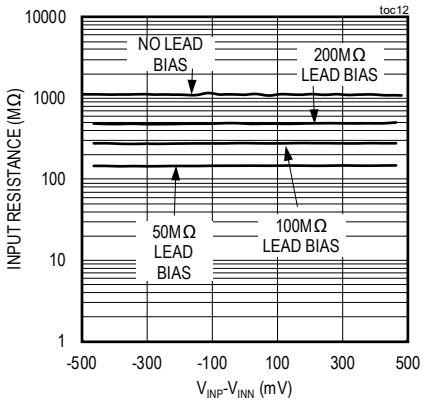
DIFFERENTIAL INPUT RESISTANCE vs. FREQUENCY



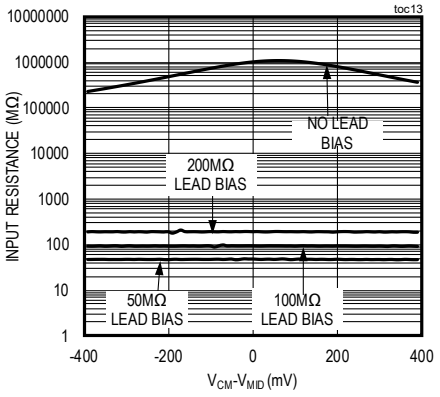
COMMON-MODE INPUT RESISTANCE vs. FREQUENCY



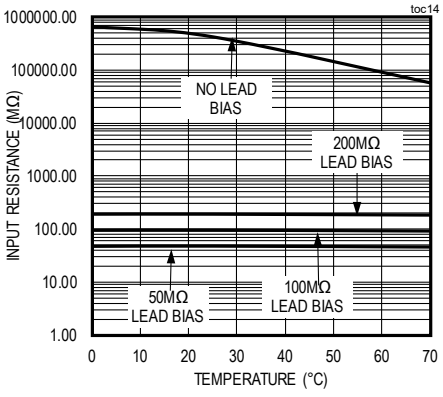
DIFFERENTIAL INPUT RESISTANCE vs. VOLTAGE



COMMON-MODE INPUT RESISTANCE vs. VOLTAGE



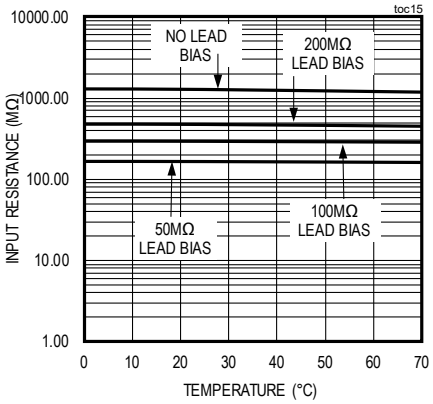
COMMON-MODE INPUT RESISTANCE vs. TEMPERATURE



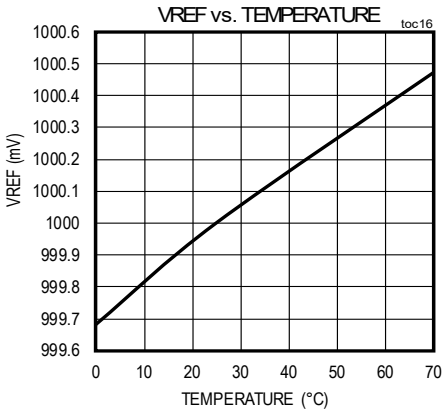
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

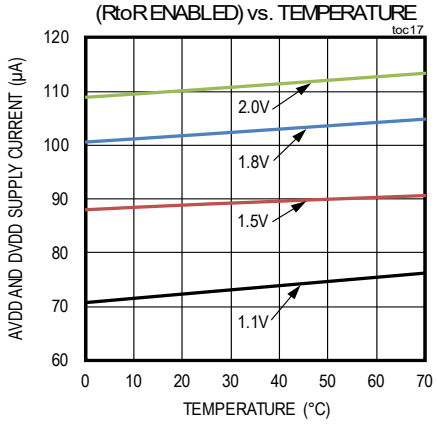
DIFFERENTIAL INPUT RESISTANCE vs. TEMPERATURE



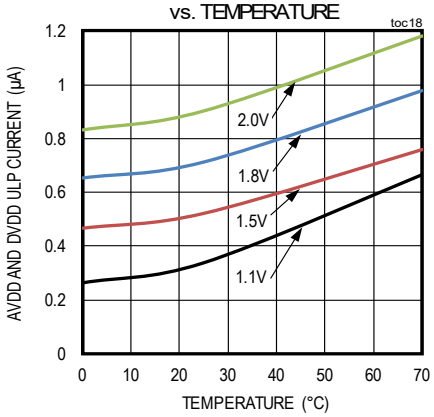
VREF vs. TEMPERATURE



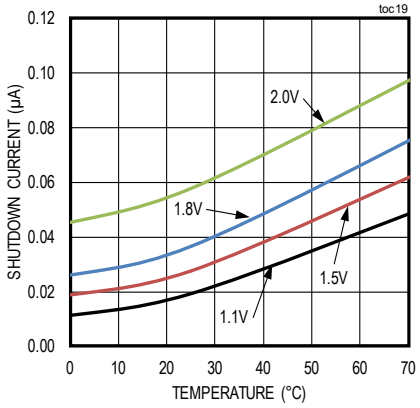
AVDD AND DVDD SUPPLY CURRENT (RtoR ENABLED) vs. TEMPERATURE



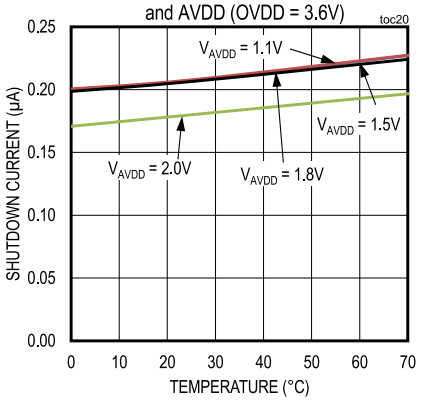
AVDD AND DVDD ULP CURRENT vs. TEMPERATURE



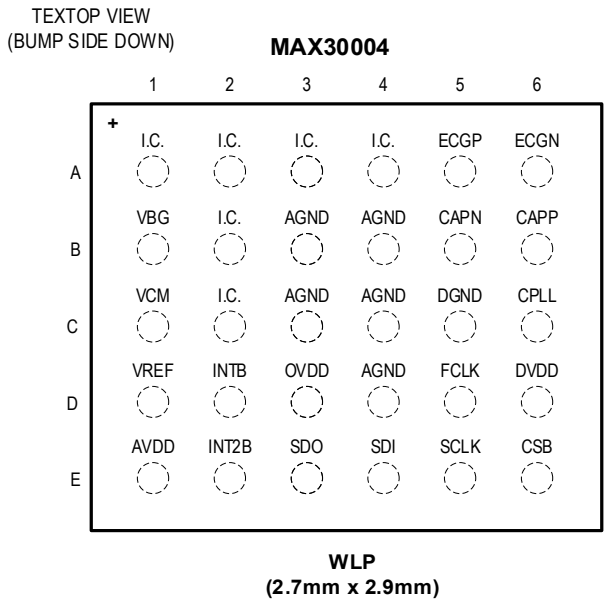
AVDD SHUTDOWN CURRENT



OVDD SHUTDOWN CURRENT vs. TEMPERATURE and AVDD (OVDD = 3.6V)



Pin Configuration



WLP
(2.7mm x 2.9mm)

Pin Description

BUMP WLP	NAME	FUNCTION
A1, A2, A3, A4, B2, C2	I.C.	Internally Connected. Connect to AGND.
B3, B4, C3, C4, D4	AGND	Analog Power and Reference Ground. Connect into the printed circuit board ground plane.
A5	INP	Positive Input
A6	INN	Negative Input
B6	CAPP	Analog High-Pass Filter Input. Connect a 1µF X7R capacitor (CHPF) between CAPP and CAPN to form a 0.5Hz high-pass response in the channel.
B5	CAPN	Analog High-Pass Filter Input. Connect a 1µF X7R capacitor (CHPF) between CAPP and CAPN to form a 0.5Hz high-pass response in the channel.
C6	CPLL	PLL Loop Filter Input. Connect 1nf C0G ceramic capacitor between CPLL and AGND.

Pin Description (continued)

BUMP WLP	NAME	FUNCTION
C5	DGND	Digital Ground for Both Digital Core and I/O Pad Drivers. Recommended to connect to AGND plane.
D6	DVDD	Digital Core Supply Voltage. Connect to AVDD
D5	FCLK	External 32.768kHz Clock that Controls the Sampling of the Internal Sigma-Delta Converters and Decimator.
E6	CSB	Active-Low Chip-Select Input. Enables the serial interface.
E5	SCLK	Serial Clock Input. Clocks data in and out of the serial interface when CSB is low.
E4	SDI	Serial Data Input. SDI is sampled into the device on the rising edge of SCLK when CSB is low.
E3	SDO	Serial Data Output. SDO will change state on the falling edge of SCLK when CSB is low. SDO is three-stated when CSB is high.
D3	OVDD	Logic Interface Supply Voltage
E2	INT2B	Interrupt 2 Output. INT2B is an active-low status output. It can be used to interrupt an external device.
D2	INTB	Interrupt Output. INTB is an active low status output. It can be used to interrupt an external device.
E1	AVDD	Analog Core Supply Voltage. Connect to DVDD.
D1	VREF	ADC Reference Buffer Output. Connect a 10µF X7R ceramic capacitor between VREF and AGND.
C1	VCM	Common Mode Buffer Output. Connect a 10µF X5R ceramic capacitor between VCM and AGND.
B1	VBG	Bandgap Noise Filter Output. Connect a 1.0µF X7R ceramic capacitor between VBG and AGND.

Detailed Description

ESD Protection

INP, INN		IEC61000-4-2 Contact Discharge (Note 10)	±8	kV
		IEC61000-4-2 Air-Gap Discharge (Note 10)	±15	
		HMM (Human Metal Model)	±8	
All Other Pins		JEDEC JESD22-A114 HBM Transient Pulse	±2.5	kV

Note 10: ESD test performed with 1kΩ series resistor designed to withstand 8kV surge voltage.

Biopotential Channel

Figure 2 illustrates the biopotential channel block diagram, excluding the ADC. The channel comprises an input MUX, a fast-recovering instrumentation amplifier, an anti-alias filter, and a programmable gain amplifier. The MUX includes several features such as ESD protection, EMI filtering, lead biasing, leads off checking, and ultra-low power leads-on checking. The output of this analog channel drives an 18-bit Sigma-Delta ADC.

Input MUX

The input MUX shown in Figure 3 contains integrated ESD and EMI protection, DC leads off detect current sources, lead-on detect, series isolation switches, and lead biasing.

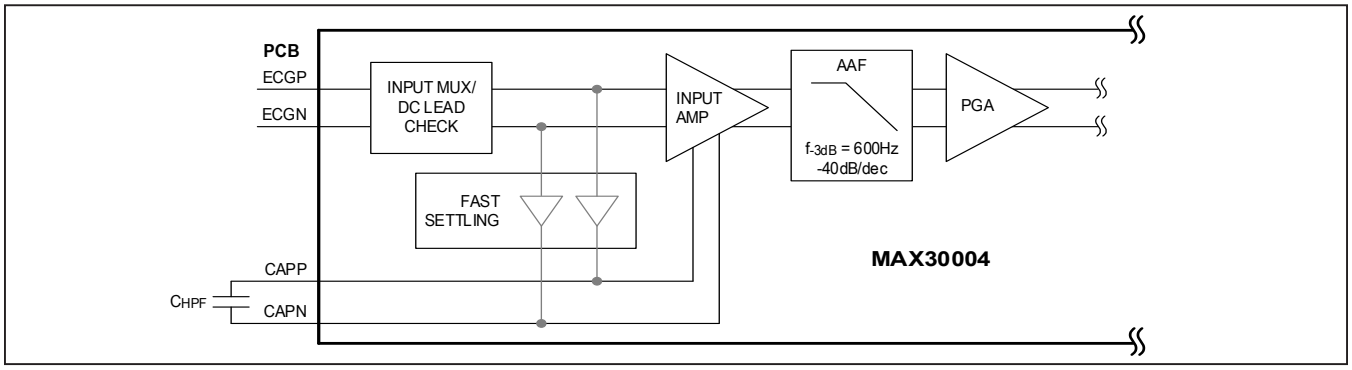


Figure 2. Channel Input Amplifier and PGA Excluding the ADC

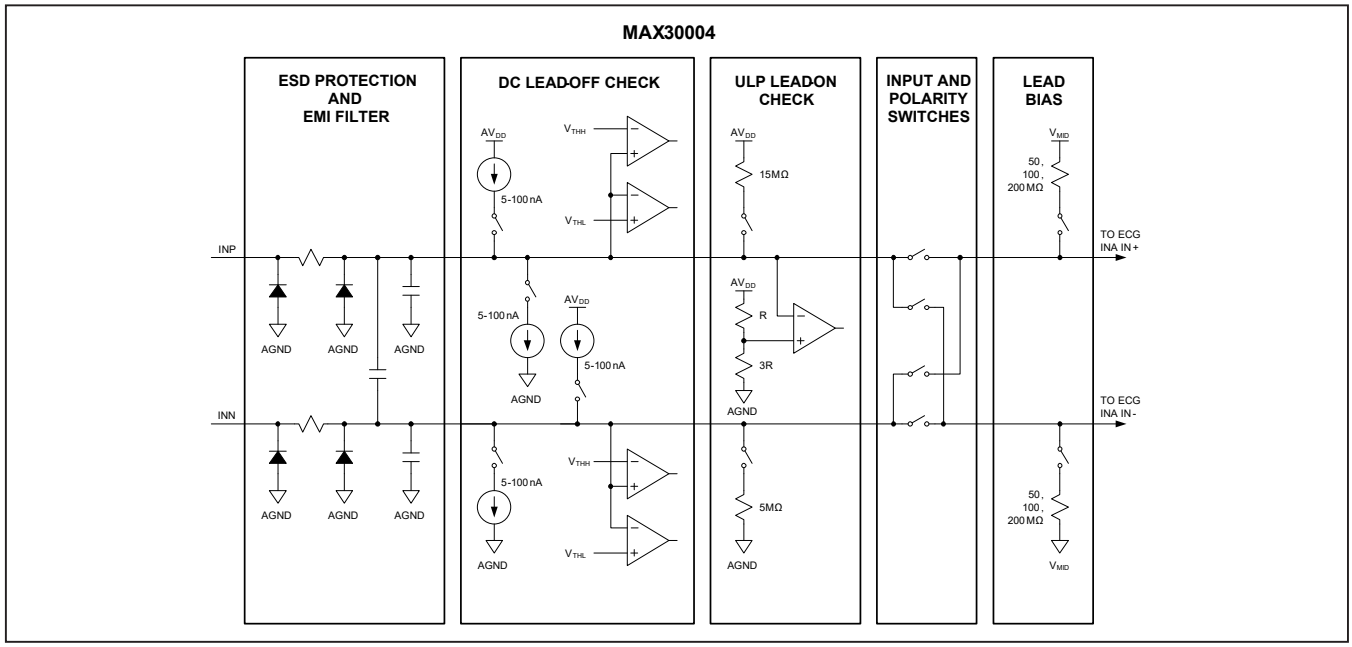


Figure 3. Input MUX

EMI Filtering and ESD Protection

EMI filtering of the INP and INN inputs consists of a single pole, low pass, differential, and common mode filter with the pole located at approximately 32MHz. The INP and INN inputs also have input clamps that protect the inputs from ESD events.

- ±8kV using the Contact Discharge method specified in IEC61000-4-2 ESD
- ±15kV using the Air Gap Discharge method specified in IEC61000-4-2 ESD
- ±8kV HBM
- For IEC61000-4-2 ESD protection, use 1kΩ series resistors on INP and INN that are rated to withstand 8kV surge voltages.

DC Leads-Off Detection and ULP Leads-On Detection

The input MUX leads-off detect circuitry consists of programmable sink/source DC current sources that allow for DC leads-off detection while the channel is powered up in normal operation and an ultra-low-power (ULP) leads-on detect while the channel is powered down.

The MAX30004 accomplishes DC leads-off detection by applying a DC current to pull the input voltage up to above V_{MID} + V_{TH} or down to below V_{MID} - V_{TH}. The current sources have user selectable values of 0nA, 5nA, 10nA, 20nA, 50nA, and 100nA that allow coverage of dry and wet electrode impedance ranges. Supported thresholds are V_{MID} ± 0.30V (recommended), V_{MID} ± 0.40V, V_{MID} ± 0.45V, and V_{MID} ± 0.50V. A threshold of 400mV, 450mV, and 500mV should only be used when V_{AVDD} ≥ 1.45V, 1.55V, and 1.65V, respectively. A dynamic comparator protects against false flags generated by the input amplifier and input chopping. The comparator checks for a minimum continuous violation (or threshold exceeded) of 115ms to 140ms depending on the setting of FMSTR[1:0] before asserting any one of the LDOFF_* interrupt flags (Figure 4). See registers CNFG_GEN (0x10) and CNFG_MUX 0x14) for configuration settings and see Table 1 for recommended values given electrode type and supply voltage. The 0nA setting can also be used with the V_{MID} ± 300mV threshold to monitor the input compliance of the INA when DC leads-off detection is not needed.

The ULP lead on detect operates by pulling INN low with a pulldown resistance larger than 5mΩ and pulling INP high with a pullup resistance larger than 15mΩ. A low-power comparator determines if INP is pulled below a predefined threshold that occurs when both electrodes make contact with the body. When the impedance between INP and INN is less than 40MΩ, an interrupt LONINT is asserted, alerting the µC to a leads-on condition.

Lead Bias

The MAX30004 limits the INP and INN DC input common mode range to V_{MID} ±150mV at V_{AVDD} = 1.1V or V_{MID} ±550mV (typ) at V_{AVDD} = 1.8V. This range can be maintained either through external/internal lead-biasing.

Internal DC lead-biasing consists of 50MΩ, 100MΩ, or 200MΩ selectable resistors to V_{MID} that drive the electrodes within the input common mode requirements of the channel and can drive the connected body to the proper common mode voltage level. See register CNFG_GEN (0x10) to select a configuration. The common-mode voltage, V_{CM}, can optionally be used as a body bias to drive the body to the common-mode voltage by connecting V_{CM} to a separate electrode on the body through a 200kΩ or higher resistor to limit current into the body, according to IEC 60601-1:2005, 8.7.3. If this is utilized, the internal lead bias resistors to V_{MID} can be disabled.

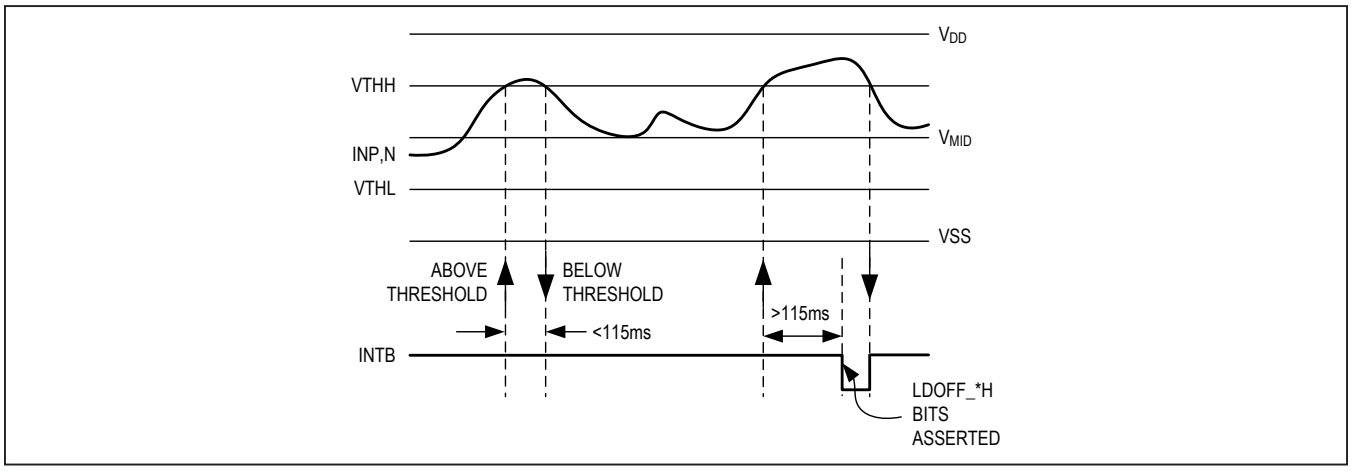


Figure 4. Lead-Off Detect Behavior

Table 1. Recommended Lead Bias (Rb), Current Source Values, and Thresholds for Electrode Impedances

I_{DC} V_{TH}	ELECTRODE IMPEDANCE							
	<100kΩ	**100kΩ - 200kΩ**	**200kΩ - 400kΩ**	**400kΩ - 1MΩ**	**1MΩ - 2MΩ**	**2MΩ - 4 MΩ**	**4MΩ - 10MΩ**	**10MΩ - 20MΩ**
I_{DC} = 10nA	All settings of R_b V_{TH} = V_{MID} ± 300mV, ±400mV							
I_{DC} = 20nA	All settings of R_b All settings of V_{TH}							All settings of R_b V_{TH} = V_{MID} ±400mV, ±450mV, ±500mV
I_{DC} = 50nA	All settings of R_b All settings of V_{TH}						All settings of R_b V_{TH} = V_{MID} ±450mV, ±500mV	
I_{DC} = 100nA	All settings of R_b All settings of V_T					All settings of Rb V_{TH} = V_{MID} ±400mV, ±450mV, ±500mV		

Isolation Switches

The series switches in the MAX30004 isolate INP and INN pins (subject) from the internal signal path. the series switches are disabled by default. They must be enabled to record R-to-R data.

Gain Settings and Input Range

The device's biopotential channel contains an input instrumentation amplifier that provides low-noise, fixed 20V/V gain amplification of the differential signal, rejects differential DC voltage due to electrode polarization, rejects common-mode interference primarily due to AC mains interference, and provides high input impedance to guarantee high CMRR even in the presence of severe electrode impedance mismatch (see Figure 2). The differential DC rejection corner frequency is set by an external capacitor (C_{HPF}) placed between pins CAPP and CAPN, refer to Table 2 for appropriate value selection. There are three recommended options for the cutoff frequency: 5Hz, 0.5Hz, and 0.05Hz. Setting the cutoff frequency to 5Hz provides the most motion artifact rejection, making it best suited for heart rate monitoring. 0.5Hz and 0.05Hz can be used for applications requiring moderate and no motion artifact rejection respectively. The high-pass corner frequency is calculated by the following equation:

$$1/(2\pi \times R_{HPF} \times C_{HPF})$$

RHPF is specified in the *Electrical Characteristics* table.

Following the instrumentation amplifier is a 2-pole active anti-aliasing filter with a 600Hz -3dB frequency that provides 57dB of attenuation at half the modulator sampling rate (approximately 16kHz) and a PGA with programmable gains of 1, 2, 4, and 8V/V for an overall gain of 20, 40, 80, and 160V/V. The instrumentation amplifier and PGA are chopped to minimize offset and 1/f noise. Gain settings are configured through the CNFG_CH (0x15) register. The useable common-mode range is V_{MID} ±150mV at V_{AVDD} = 1.1V or V_{MID} ±550mV (typ) at V_{AVDD} = 1.8V. Internal lead biasing can be used to meet this requirement. The useable DC differential range is ±300mV at V_{AVDD} = 1.1V or ±650mV (typ) at V_{AVDD} = 1.8V to allow for electrode polarization voltages on each electrode. The input AC differential range is ±32.5mV or ±65mV_{P-P}.

Table 2. Analog HPF Corner Frequency Selection

C_{HPF}	HPF CORNER FREQUENCY
0.1µ	≤ 5Hz
1.0µ	≤ 0.5Hz
10µ	≤ 0.05Hz

Fast Recovery Mode

The input instrumentation amplifier has the ability to rapidly recover from an excessive overdrive event such as a defibrillation pulse, high-voltage external pacing, and electro-surgery interference. There are two modes of recovery that can be used: automatic or manual recovery. The mode is programmed by the FAST[1:0] bits in the MNGR_DYN (0x05) register.

Automatic mode engages once the saturation counter exceeds approximately 125ms (t_{SAT}). The counter is activated the first time the ADC output exceeds the symmetrical threshold defined by the FAST_TH[5:0] bits in the MNGR_DYN (0x05) register and accumulates the time that the ADC output exceeds either the positive or negative threshold. If the saturation counter exceeds 125ms, it triggers the fast settling mode (if enabled) and resets. The saturation counter can also be reset prior to triggering the fast settling mode if the ADC output falls below the threshold continuously for 125ms (t_{BLW}). This feature is designed to avoid false triggers due to the QRS complex. Once triggered, fast settling mode will be engaged for 500ms, see Figure 5.

In manual mode, a user algorithm running on the host microcontroller or an external stimulus input will generate the trigger to enter fast recovery mode. The host microcontroller then enables the manual fast recovery mode in the MNGR_DYN (0x05) register. The manual fast recovery mode can be of a much shorter duration than the automatic mode and allows for more rapid recovery. One such example is recovery from external high-voltage pacing signals in a few milliseconds to allow the observation of a subsequent p-wave.

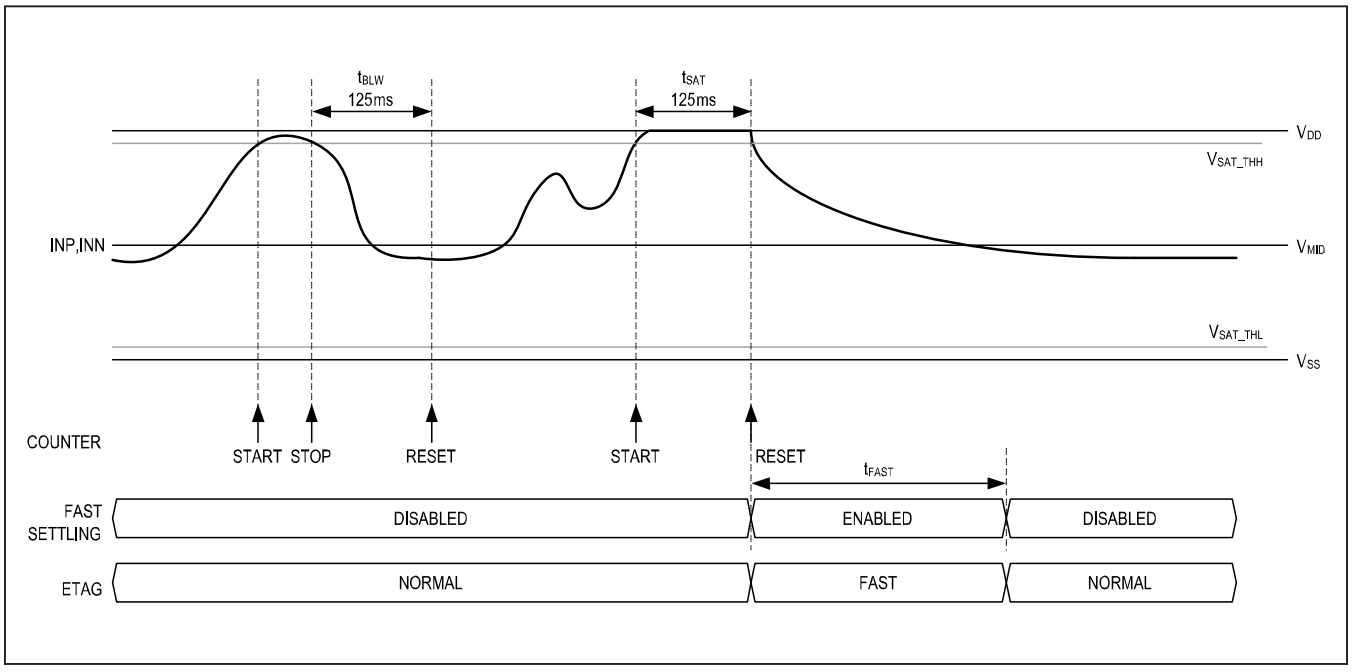


Figure 5. Automatic Fast Settling Behavior

R-to-R Detection

The MAX30004 contains built-in hardware to detect R-to-R intervals using an adaptation of the Pan-Tompkins QRS detection algorithm[1]. The timing resolution of the R-R interval is approximately 8ms and depends on the setting of FMSTR [1:0] in CNFG_GEN (0x10) register. See Table 19 for the timing resolution of each setting.

When an R event is identified, the RRINT status bit is asserted and the RTOR_REG (0x25) register is updated with the count seen since the last R event. Figure 6 illustrates the R-R interval on a QRS complex. Refer to registers CNFG_RTOR1 (0x1D) and CNFG_RTOR2 (0x1E) for configuration details.

The latency of the R-to-R value written to the RTOR Interval Memory Register is the sum of the R-to-R decimation delay and the R-to-R detection delay blocks. The R-to-R decimation factor is fixed at 256 and the decimation delay (t_{R2R_DEC}) is always 3,370 FMSTR clocks, as shown in Table 3.

The detection circuit consists of several digital filters and signal processing delays. These depend on the WNDW[3:0] bits in the CNFG_RTOR (0x1D) register. The detection delay (t_{R2R_DET}) is described by the following equation:

t_{R2R_DET} = 5,376 + 256 x WNDW in FMSTR clocks where WNDW is an integer from 0 to 15 and the total latency (t_{R2R_DEL}) is the sum of the two delays and summarized in the equation below:

$t_{R2R\_DEL} = t_{R2R\_DEC} + t_{R2R\_DET}$ = 3,370 + 5,376 + 256 x WNDW in FMSTR clocks where WNDW is an integer from 0 to 15.

Reference and Common Mode Buffer

The MAX30004 features internally generated reference voltages. The bandgap output (V_{BG}) pin requires an external 1.0µF capacitor to AGND and the reference output (V_{REF}) pin requires a 10µF external capacitor to AGND for compensation and noise filtering.

A common-mode buffer is provided to buffer 650mV which is used to drive common mode voltages for internal blocks. Use a 10µF external capacitor between V_{CM} to AGND to provide compensation and noise filtering.

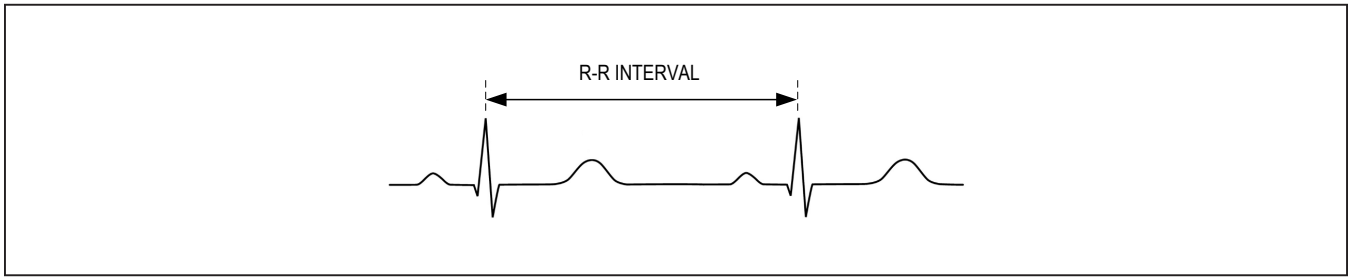


Figure 6. R-to-R Interval Illustration

Table 3. R-to-R Decimation Delay in ms and FMSTR CLK vs. Register Settings, FCLK = 32.768Hz

FMSTR [1:0]	FMSTR FREQ IN FCLKs	FMSTR FREQ (Hz)	DECIMATION	RTOR TIME RESOLUTION (ms)	DELAY IN R-TO-R DECIMATION	
					IN FMSTR CLKs	IN ms
00	FCLK	32,768	256	7.8125	3370	102.844
01	FCLK x 625/640	32,000	256	8.0	3370	105.313
10	FCLK x 625/640	32,000	256	8.0	3370	105.313
11	FCLK x 640/656	31,968.78	256	8.0078	3370	105.415

[1] *J. Pan and W.J. Tompkins, "A Real-Time QRS Detection Algorithm," IEEE Trans. Biomed. Eng., vol. 32, pp. 230-236*

Sample Synchronization Pulse

The MAX30004 offers a sample synchronization pulse that allows the direct observation of the channel sample instant for either synchronization between multiple devices or as a monitoring feature during debug. When enabled (EN_SAMP in either register EN_INT or EN_INT2), the MAX30004 generates an interrupt either every sample instant, or every second, fourth, or 16th sample instant, based on the setting of SAMP_IT[1:0] in register MNGR_INT. The sample instants are defined by the channel ADC, and are not R-to-R samples. Therefore, the interval between individual sample instants is dependent on the channel data rate as defined by FMSTR[1:0] and RATE[1:0]. The clear behavior of the sample synchronization pulse is affected by the CLR_SAMP bit in register MNGR_INT. When this feature is used, it is recommended to use a dedicated interrupt output for just the sample synchronization pulse.

SPI Interface Description

32-Bit Read/Write Sequences

The MAX30004 interface is SPI/QSPI/Micro-wire/DSP compatible. The operation of the SPI interface is shown in Figure 1. Data is strobed into the MAX30004 on SCLK rising edges. The device is programmed and accessed by a 32 cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a one byte command word (comprised of a seven bit address and a Read/$\overline{\text{Write}}$ mode indicator (i.e., A[6:0] + R/$\overline{\text{W}}$) followed by a three-byte data word. The MAX30004 is compatible with the CPOL = 0/CPHA = 0 and CPOL = 1/CPHA = 1 modes of operation.

Write mode operations will be executed on the 32nd SCLK rising edge using the first four bytes of data available. In write mode, any data supplied after the 32nd SCLK rising edge will be ignored. Subsequent writes require CSB to de-assert high and then assert low for the next write command. In order to abort a command sequence, the rise of CSB must precede the updating (32nd) rising-edge of SCLK, meeting the t_{CSA} requirement.

Read mode operations will access the requested data on the 8th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the µC to sample the data MSB on the 9th SCLK rising edge. Configuration and status data are all available via normal mode read back sequences. If more than 32 SCLK rising edges are provided in a normal read sequence then the excess edges will be ignored and the device will read back zeros.

If accessing the STATUS register, all interrupt updates will be made in response to the 30th SCLK rising edge, allowing for internal synchronization operations to occur.

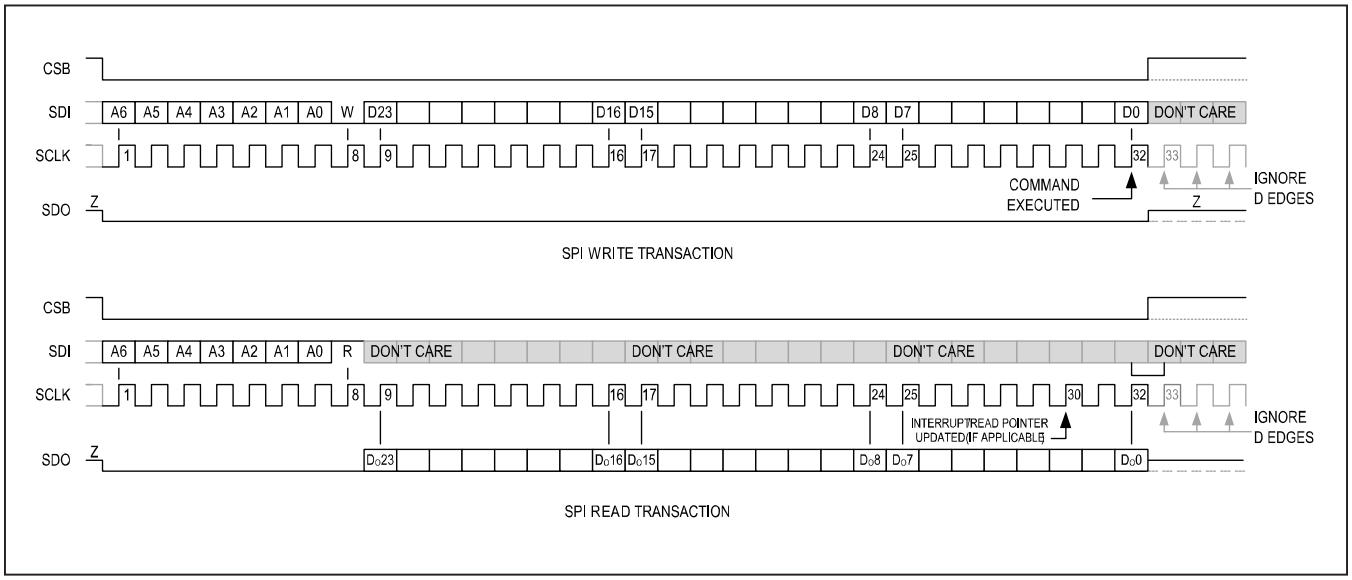


Figure 7. SPI Normal Mode Transaction Diagrams

User Command and Register Map

REG [6:0]	NAME	R/W MODE	DATA INDEX (D_{INDEX})							
			23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x00	NO-OP	R/W	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x
0x01	STATUS	R	x	x	FSTINT	DCLOFFINT	x	x	x	x
			x	x	x	x	LONINT	RRINT	SAMP	PLLINT
			0	0	x	x	LOFF_PH	LOFF_PL	LOFF_NH	LOFF_NL
0x02 0x03	EN_INT EN_INT2	R/W	x	x	EN_FSTINT	EN_DCLOFFINT	x	x	x	x
			x	x	x	x	EN_LONINT	EN_RRINT	EN_SAMP	EN_PLLINT
			x	x	x	x	x	x	INTB_TYPE[1:0]	
0x04	MNGR_INT	R/W	x	x	x	x	x	x	x	x
			x	x	x	x	x	x	x	x
			x	CLR_FAST	CLR_RRINT[1:0]		x	CLR_SAMP	SAMP_IT[3:0]	
0x05	MNGR_DYN	R/W	FAST[1:0]		FAST_TH[5:0]					
			x	x	x	x	x	x	x	x
			x	x	x	x	x	x	x	x
0x08	SW_RST	W	Data Required for Execution = 0x000000							
0x09	RESTART	W	Data Required for Execution = 0x000000							
0x0A	RTOR_RST	W	Data Required for Execution = 0x000000							
0x0F	INFO	R	0	1	0	1	REV_ID[3:0]			
			x	x	0	0	x	x	x	x
			x	x	x	x	x	x	x	x
0x10	CNFG_GEN	R/W	EN_ULP_LON[1:0]		FMSTR[1:0]		EN_CH	x	x	x
			x	x	EN_DCLOFF[1:0]		IPOL	IMAG[2:0]		
			VTH[1:0]		EN_RBIAS[1:0]		RBIASV[1:0]		RBIASP	RBIASN

User Command and Register Map (continued)

REG [6:0]	NAME	R/W MODE	DATA INDEX (D_{INDEX})							
			23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x14	CNFG_ MUX	R/W	POL	x	OPENP	OPENN	x	x	x	x
			x	x	x	x	x	x	x	x
			x	x	x	x	x	x	x	x
0x15	CNFG_	R/W	RATE[1:0]		x	x	x	x	GAIN[1:0]	
			x	DHPF	DLPF[1:0]		x	x	x	x
			x	x	x	x	x	x	x	x
0x1D	CNFG_ RTOR1	R/W	WNDW[3:0]				RGAIN[3:0]			
			EN_RTOR	x	PAVG[1:0]		PTSF[3:0]			
			x	x	x	x	x	x	x	x
0x1E	CNFG_ RTOR2	R/W	x	x	HOFF[5:0]					
			x	x	RAVG[1:0]		x	RHSF[2:0]		
			x	x	x	x	x	x	x	x
0x25	RTOR	R	R-to-R Interval Register Read Back				See *RTOR DATA* description for details			
0x7F	NO-OP	R/W	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x

Register Descriptions

NO_OP (0x00 and 0x7F) Registers

No Operation (NO_OP) registers are read-write registers that have no internal effect on the device. If these registers are read back, DOUT remains zero for the entire SPI transaction. Any attempt to write to these registers is ignored without impact to internal operation.

STATUS (0x01) Register

STATUS is a read-only register that provides a comprehensive overview of the current status of the device. The first two bytes indicate the state of all interrupt terms (regardless of whether interrupts are enabled in registers EN_INT (0x02) or EN_INT2 (0x03)). All interrupt terms are active high. The last byte includes detailed status information for conditions associated with the interrupt terms.

Table 4. STATUS (0x01) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x01	STATUS	R	x	x	FSTINT	DCLOFF INT	x	x	x	x
			x	x	x	x	LONINT	RRINT	SAMP	PLLINT
			x	x	x	x	LDOFF_ PH	LDOFF_ PL	LDOFF_ NH	LDOFF_ NL

Table 5. Status (0x01) Register Meaning

INDEX	NAME	MEANING
D[21]	FSTINT	Fast Recovery Mode. Issued when the Fast Recovery Mode is engaged (either manually or automatically). Status and Interrupt Clear behavior is defined by CLR_FAST, see MNGR_INT for details.
D[20]	DCLOFFINT	DC Lead-Off Detection Interrupt. Indicates that the MAX30004 has determined it is in leads off condition (as selected in CNFG_GEN) for more than 115ms. Remains active as long as the leads-off condition persists, then held until cleared by STATUS read back (32nd SCLK).

Table 5. Status (0x01) Register Meaning (continued)

INDEX	NAME	MEANING
D[11]	LONINT	Ultra-Low Power (ULP) Leads-On Detection Interrupt. Indicates that the MAX30004 has determined it is in a leads-on condition (as selected in CNFG_GEN). LONINT is asserted whenever EN_ULP_LON[1:0] in register CNFG_GEN is set to either 0b01 or 0b10 to indicate that the ULP leads on detection mode has been enabled. The STATUS register has to be read back once after ULP leads-on detection mode has been activated to clear LONINT and enable leads-on detection. LONINT remains active while the leads-on condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[10]	RRINT	R-to-R Detector R Event Interrupt. Issued when the R-to-R detector has identified a new R event. Clear behavior is defined by CLR_RRINT[1:0]; see MNGR_INT for details.
D[9]	SAMP	Sample Synchronization Pulse. Issued on the ADC base-rate sampling instant, for use in assisting µC monitoring and synchronizing other peripheral operations and data, generally recommended for use as a dedicated interrupt. Frequency is selected by SAMP_IT[1:0], see MNGR_INT for details. Clear behavior is defined by CLR_SAMP, see MNGR_INT for details.
D[8]	PLLINT	PLL Unlocked Interrupt. Indicates that the PLL has not yet achieved or has lost its phase lock. PLLINT will only be asserted when the PLL is powered up and active (Channel enabled). Remains asserted while the PLL unlocked condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[3]	LDOFF_PH	DC Lead Off Detection Detailed Status. Indicates that the MAX30004 has determined (as selected by CNFG_GEN): INP is above the high threshold (V_{THH}), INP is below the low threshold (V_{THL}), INN is above the high threshold (V_{THH}), INN is below the low threshold (V_{THL}), respectively. Remains active as long as the leads-off detection is active and the leads-off condition persists, then held until cleared by STATUS read back (32nd SCLK). LDOFF_PH to LDOFF_NL are detailed status bits that are asserted at the same time as DCLOFFINT.
D[2]	LDOFF_PL	
D[1]	LDOFF_NH	
D[0]	LDOFF_NL	

EN_INT (0x02) and EN_INT2 (0x03) Registers

EN_INT and EN_INT2 are read/write registers that govern the operation of the INTB output and INT2B output, respectively. The first two bytes indicate which interrupt input terms are included in the interrupt output OR term (ex. a one in an EN_INT register indicates that the corresponding input term is included in the INTB interrupt output OR term). See the STATUS register for detailed descriptions of the interrupt terms. The power-on reset state of all EN_INT terms is 0 (ignored by INT).

EN_INT and EN_INT2 can also be used to mask persistent interrupt conditions in order to perform other interrupt-driven operations until the persistent conditions are resolved.

INTB_TYPE[1:0] allows the user to select between a CMOS or an open-drain NMOS mode INTB output. If using open-drain mode, an option for an internal 125kΩ pullup resistor is also offered.

All INTB and INT2B types are active-low (INTB low indicates the device requires servicing by the µC); however, the open-drain mode allows the INTB line to be shared with other devices in a wired-or configuration.

In general, it is suggested that INT2B be used to support specialized/dedicated interrupts of use in specific applications, such as the self-clearing versions of SAMP or RRINT.

Table 6. EN_INT (0x02) and EN_INT2 (0x03) Register Maps

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x02 0x03	EN_INT EN_INT2	R/W	x	x	EN_ FSTINT	EN_DCL OFFINT	x	x	x	x
			x	x	x	x	EN_ LONINT	EN_ RRINT	EN_ SAMP	EN_ PLLINT
			x	x	x	x	x	x	INTB_TYPE[1:0]	

Table 7. EN_INT (0x02 and 0x03) Register Meaning

INDEX	NAME	DEFAULT	FUNCTION
D[23:20] D[11:8]	EN_FSTINT EN_DCLOFFINT EN_LONINT EN_RRINT EN_SAMP EN_PLLINT	0x0000	Interrupt Enables for interrupt terms in STATUS[23:8] 0 = Individual interrupt term is not included in the interrupt OR term 1 = Individual interrupt term is included in the interrupt OR term
D[1:0]	INTB_TYPE[1:0]	11	INTB Port Type (EN_INT Selections) 00 = Disabled (high impedance) 01 = CMOS Driver 10 = Open-Drain NMOS Driver 11 = Open-Drain NMOS Driver with Internal 125kΩ Pullup Resistance
		11	INT2B Port Type (EN_INT2 Selections) 00 = Disabled (high impedance) 01 = CMOS Driver 10 = Open-Drain nMOS Driver 11 = Open-Drain nMOS Driver with Internal 125kΩ Pullup Resistance

MNGR_INT (0x04)

MNGR_INT is a read/write register that manages the operation of the configurable interrupt bits. Finally, this register contains the configuration bits supporting the sample synchronization pulse (SAMP) and RTOR heart rate detection interrupt (RRINT).

Table 8. MNGR_INT (0x04) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x04	MNGR_INT	R/W	x	x	x	x	x	x	x	x
			x	x	x	x	x	x	x	x
			x	CLR_FAST	CLR_RRINT[1:0]		x	CLR_SAMP	SAMP_IT[1:0]	

Table 9. MNGR_INT (0x04) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[6]	CLR_FAST	0	FAST MODE Interrupt Clear Behavior: 0 = FSTINT remains active until the FAST mode is disengaged (manually or automatically), then held until cleared by STATUS read back (32nd SCLK). 1 = FSTINT remains active until cleared by STATUS read back (32nd SCLK), even if the MAX30004 remains in FAST recovery mode. Once cleared, FSTINT will not be re-asserted until FAST mode is exited and re-entered, either manually or automatically.
D[5:4]	CLR_RRINT[1:0]	00	RTOR R Detect Interrupt (RRINT) Clear Behavior: 00 = Clear RRINT on STATUS Register Read Back 01 = Clear RRINT on RTOR Register Read Back 10 = Self-Clear RRINT after one data rate cycle, approximately 2ms to 8ms 11 = Reserved. Do not use.
D[2]	CLR_SAMP	1	Sample Synchronization Pulse (SAMP) Clear Behavior: 0 = Clear SAMP on STATUS Register Read Back (recommended for debug/evaluation only). 1 = Self-clear SAMP after approximately one-fourth of one data rate cycle.
D[1:0]	SAMP_IT[1:0]	00	Sample Synchronization Pulse (SAMP) Frequency 00 = issued every sample instant 01 = issued every 2nd sample instant 10 = issued every 4th sample instant 11 = issued every 16th sample instant

MNGR_DYN (0x05)

MNGR_DYN is a read/write register that manages the settings of any general/dynamic modes within the device. The Fast Recovery modes and thresholds are managed here. Unlike many CNFG registers, changes to dynamic modes do not require a RESTART operation.

SW_RST (0x08)

SW_RST (Software Reset) is a write-only register/command that resets the MAX30004 to its original default conditions at the end of the SPI SW_RST transaction (i.e. the 32nd SCLK rising edge). Execution occurs only if DIN[23:0] = 0x000000. The effect of a SW_RST is identical to power-cycling the device.

Table 10. MNGR_DYN (0x05) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x05	MNGR_DYN	R/W	FAST[1:0]		FAST_TH[5:0]					
			x	x	x	x	x	x	x	x
			x	x	x	x	x	x	x	x

Table 11. MNGR_DYN (0x05) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[23:22]	FAST[1:0]	00	Fast Recovery Mode Selection (High-Pass Filter Bypass): 00 = Normal Mode (Fast Recovery Mode Disabled) 01 = Manual Fast Recovery Mode Enable (remains active until disabled) 10 = Automatic Fast Recovery Mode Enable (Fast Recovery automatically activated when/while outputs are saturated, using FAST_TH). 11 = Reserved. Do not use.
D[21:16]	FAST_TH[5:0]	0x3F	Automatic Fast Recovery Threshold: If FAST[1:0] = 10 and the output of a measurement exceeds the symmetric thresholds defined by 2048*FAST_TH for more than 125ms, the Fast Recovery mode will be automatically engaged and remain active for 500ms. For example, the default value (FAST_TH = 0x3F) corresponds to an output upper threshold of 0x1F800, and an output lower threshold of 0x20800.

Table 12. SW_RST (0x08) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x08	SW_RST	W	D[23:16] = 0x00							
			D[15:8] = 0x00							
			D[7:0] = 0x00							

RESTART (0x09)

RESTART (Restart) is a write-only register/command that begins new RTOR operations and recording, beginning on the internal MSTR clock edge following the end of the SPI RESTART transaction (i.e., the 32nd SCLK rising edge). Execution occurs only if DIN[23:0] = 0x000000. In addition to restarting the operations of any active R-to-R circuitry, RESTART also resets and clears the DSP filters (to midscale), allowing the user to effectively set the “Time Zero” for the RTOR data. No configuration settings are impacted. For best results, users should wait until the PLL has achieved lock before restarting if the CNFG_GEN settings have been altered.

Once the device is initially powered up, it needs to be fully configured prior to launching recording operations. Likewise, anytime a change to CNFG_GEN or CNFG_CH registers are made discontinuities in the RTOR record may occur. The RESTART command provides a means to restart operations cleanly following any such disturbances.

RTOR_RST (0x0A)

RTOR_RST is a write-only register/command that begins a new data recording by resetting the memories and resuming the record with the next available data. Execution occurs only if DIN[23:0] = 0x000000. Unlike the RESTART command, the operations of any active data and R-to-R circuitry are not impacted by RTOR_RST, so, therefore, no settling/recovery transients apply.

Table 13. RESTART (0x09) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x09	RESTART	W	D[23:16] = 0x00							
			D[15:8] = 0x00							
			D[7:0] = 0x00							

Table 14. RTOR_RST (0x0A) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x0A	RTOR_RST	W	D[23:16] = 0x00							
			D[15:8] = 0x00							
			D[7:0] = 0x00							

INFO (0x0F)

INFO is a read-only register that provides information about the MAX30004. The first nibble contains an alternating bit pattern to aide in interface verification. The second nibble contains the revision ID. The third nibble includes part ID information. The final 3 nibbles contain a serial number for Maxim internal use—note that individual units are not given unique serial numbers, and these bits should not be used as serial numbers for end products, though they may be useful during initial development efforts.

Note: Due to internal initialization procedures, this command will not read-back valid data if it is the first command executed following either a power-cycle event, or a SW_RST event.

CNFG_GEN (0x10)

CNFG_GEN is a read/write register which governs general settings, most significantly the master clock rate for all internal timing operations. Anytime a change to CNFG_GEN is made, there may be discontinuities in the data record may occur. The RESTART command can be used to restore internal synchronization resulting from configuration changes. Note when EN_CH is logic-low, the device is in one of two ultra-low power modes (determined by EN_ULP_LON).

Table 19 shows the data rates that can be realized with various setting of FMSTR, along with RATE configuration bits available in the CNFG_CH register.

Table 15. INFO (0x0F) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x0F	INFO	R	0	1	0	1	REV_ID[3:0]			
			x	X	0	0	x	x	x	x
			x	x	x	x	x	x	x	x

Table 16. INFO (0x0F) Register Meaning

INDEX	NAME	MEANING
D[19:16]	REV_ID[3:0]	Revision ID

Table 17. CNFG_GEN (0x10) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x10	CNFG_GEN	R/W	EN_ULP_LON[1:0]		FMSTR[1:0]		EN_RTOR	x	x	x
			x	x	EN_DCLOFF[1:0]		IPOL	IMAG[2:0]		
			VTH[1:0]		EN_RBIAS[1:0]		RBIASV[1:0]		RBIASP	RBIASN

Table 18. CNFG_GEN (0x10) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[23:22]	EN_ULP_LON [1:0]	00	Ultra-Low Power Lead-On Detection Enable 00 = ULP Lead-On Detection disabled 01 = ULP Lead-On Detection enabled 10 = Reserved. Do not use. 11 = Reserved. Do not use. ULP mode is only active when the RTOR channel is powered down/disabled.
D[21:20]	FMSTR[1:0]	00	Master Clock Frequency. Selects the Master Clock Frequency (FMSTR), and Timing Resolution (T_{RES}). These are generated from FCLK, which is always 32.768Khz. 00 = F_{MSTR} = 32768Hz, T_{RES} = 15.26µs (512Hz data progressions) 01 = F_{MSTR} = 32000Hz, T_{RES} = 15.63µs (500Hz data progressions) 10 = F_{MSTR} = 32000Hz, T_{RES} = 15.63µs (200Hz data progressions) 11 = F_{MSTR} = 31968.78Hz, T_{RES} = 15.64µs (199.8049Hz data progressions)
D[19]	EN_CH	0	Channel Enable 0 = Channel disabled 1 = Channel enabled Note: The channel must be enabled to allow R-to-R operation.
D[13:12]	EN_DCLOFF	00	DC Lead-Off Detection Enable 00 = DC Lead-Off Detection disabled 01 = DCLOFF Detection applied to the INP/INN pins 10 = Reserved. Do not use. 11 = Reserved. Do not use. DC Method, requires active selected channel, enables DCLOFF interrupt and status bit behavior. Uses current sources and comparator thresholds set below.
D[11]	DCLOFF_ IPOL	0	DC Lead-Off Current Polarity (if current sources are enabled/connected) 0 = INP - Pullup INN – Pulldown 1 = INP - Pulldown INN – Pullup
D[10:8]	DCLOFF_ IMAG[2:0]	000	DC Lead-Off Current Magnitude Selection 000 = 0nA (Disable and Disconnect Current Sources) 001 = 5nA 010 = 10nA 011 = 20nA 100 = 50nA 101 = 100nA 110 = Reserved. Do not use. 111 = Reserved. Do not use.
D[7:6]	DCLOFF_ VTH[1:0]	00	DC Lead-Off Voltage Threshold Selection 00 = V_{MID} ± 300mV 01 = V_{MID} ± 400mV 10 = V_{MID} ± 450mV 11 = V_{MID} ± 500mV
D[5:4]	EN_RBIAS[1:0]	00	Enable and Select Resistive Lead Bias Mode 00 = Resistive Bias disabled 01 = Resistive Bias enabled if EN_CH is also enabled 10 = Reserved. Do not use. 11 = Reserved. Do not use. If EN_CH is not asserted at the same time as prior to EN_RBIAS[1:0] being set to 01, then EN_RBIAS[1:0] will remain set to 00.

Table 18. CNFG_GEN (0x10) Register Functionality (continued)

INDEX	NAME	DEFAULT	FUNCTION
D[3:2]	RBIASV[1:0]	01	Resistive Bias Mode Value Selection 00 = R_{BIAS} = 50MΩ 01 = R_{BIAS} = 100MΩ 10 = R_{BIAS} = 200MΩ 11 = Reserved. Do not use.
D[1]	RBIASP	0	Enables Resistive Bias on Positive Input 0 = INP is not resistively connected to V_{MID} 1 = INP is connected to V_{MID} through a resistor (selected by RBIASV).
D[0]	RBIASN	0	Enables Resistive Bias on Negative Input 0 = INN is not resistively connected to V_{MID} 1 = INN is connected to V_{MID} through a resistor (selected by RBIASV).

Table 19. Master Frequency Summary Table

FMSTR [1:0]	MASTER FREQUENCY (f_{MSTR}) (Hz)	DATA RATES & RELATED TIMING (RATE SELECTIONS)		CALIBRATION TIMING RESOLUTION (CAL_RES) (µs)
		CHANNEL	RTOR	
		DATA RATE (sps)	TIMING RESOLUTION (RTOR_RES) (ms)	
00	32768	00 = 512 01 = 256 10 = 128	7.8125	30.52
01	32000	00 = 500 01 = 250 10 = 125	8.000	31.25
10	32000	10 = 200	8.000	31.25
11	31968.78	10 =199.8049	8.008	31.28

CNFG_MUX (0x14)

CNFG_MUX is a read/write register which configures the operation, settings, and functionality of the Input Multiplexer.

CNFG_CH (0x15)

CNFG_CH is a read/write register that configures the operation, settings, and functionality of the Biopotential channel. Anytime a change to CNFG_CH is made, there may be discontinuities in the data record.

Table 20. CNFG_EMUX (0x14) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x14	CNFG_ MUX	R/W	POL	x	OPENP	OPENN	x	x	x	x
			x	x	x	x	x	x	x	x
			x	x	x	x	x	x	x	x

Table 21. CNFG_MUX (0x14) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[23]	POL	0	Input Polarity Selection 0 = Non-Inverted 1 = Inverted
D[21]	OPENP	1	Open the INP Input Switch (most often used for testing and calibration studies) 0 = INP is internally connected to the AFE Channel 1 = INP is internally isolated from the AFE Channel
D[20]	OPENN	1	Open the INN Input Switch (most often used for testing and calibration studies) 0 = INN is internally connected to the AFE Channel 1 = INN is internally isolated from the AFE Channel

Table 22. CNFG_CH (0x15) Register Map

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x15	CNFG_ CH	R/W	RATE[1:0]		x	x	x	x	GAIN[1:0]	
			x	DHPF	DLPF[1:0]		x	x	x	x
			x	x	x	x	x	x	x	x

Table 23. CNFG_CH (0x15) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[23:22]	RATE[1:0]	10	Sample Data Rate (also dependent on F_{MSTR} selection, see CNFG_GEN Table 24):
			FMSTR = 00: f_{MSTR} = 32768Hz, t_{RES} = 15.26µs (512Hz data progressions) 00 = 512sps 01 = 256sps 10 = 128sps 11 = Reserved. Do not use.
			FMSTR = 01: f_{MSTR} = 32000Hz, t_{RES} = 15.63µs (500Hz data progressions) 00 = 500sps 01 = 250sps 10 = 125sps 11 = Reserved. Do not use.
			FMSTR = 10: f_{MSTR} = 32000Hz, t_{RES} = 15.63µs (200Hz data progressions) 00 = Reserved. Do not use. 01 = Reserved. Do not use. 10 = 200sps 11 = Reserved. Do not use.
			FMSTR = 11: f_{MSTR} = 31968Hz, t_{RES} = 15.64µs (199.8Hz data progressions) 00 = Reserved. Do not use. 01 = Reserved. Do not use. 10 = 199.8sps 11 = Reserved. Do not use.
D[17:16]	GAIN[1:0]	00	Gain Setting 00 = 20V/V 01 = 40V/V 10 = 80V/V 11 = 160V/V

Table 23. CNFG_CH (0x15) Register Functionality (continued)

INDEX	NAME	DEFAULT	FUNCTION
D[14]	DHPF	1	Digital High-Pass Filter Cutoff Frequency 0 = Bypass (DC) 1 = 0.50Hz
D[13:12]	DLPF[1:0]	01	Digital Low-Pass Filter Cutoff Frequency 00 = Bypass (Decimation only, no FIR filter applied) 01 = approximately 40Hz (Except for 125 and 128sps settings, see Table 24.) 10 = approximately 100Hz (Available for 512, 256, 500, and 250sps data Rate selections only) 11 = approximately 150Hz (Available for 512 and 500sps data rate selections only) **Note:** See Table 24. If an unsupported DLPF setting is specified, the 40Hz setting (DLPF[1:0] = 01) will be used internally; the CNFG_CH register will continue to hold the value as written, but return the effective internal value when read back.

Table 24. Supported RATE and DLPF Options

CNFG_GEN FMSTR[1:0]	RATE[1:0] SAMPLE RATE (sps)	DLPF[1:0]/DIGITAL LPF CUTOFF			
		00	01 (Hz)	10 (Hz)	11 (Hz)
00 = 32768Hz	00 = 512	Bypass	40.96	102.4	153.6
	01 = 256	Bypass	40.96	102.4	**40.96**
	10 = 128	Bypass	28.35	**28.35**	**28.35**
01 = 32000Hz	00 = 500	Bypass	40.00	100.0	150.0
	01 = 250	Bypass	40.00	100.0	**40.00**
	10 = 125	Bypass	27.68	**27.68**	**27.68**
10 = 32000Hz	10 = 200	Bypass	40.00	**40.00**	**40.00**
11 = 31968Hz	10 = 199.8	Bypass	39.96	**39.96**	**39.96**

Note: *Combinations shown in grey are unsupported and will be internally mapped to the default settings shown.*

CNFG_RTOR1 and CNFG_RTOR2 (0x1D & 0x1E)

CNFG_RTOR is a two-part read/write register that configures the operation, settings, and function of the RTOR heart rate detection block. The first register contains algorithmic voltage gain and threshold parameters, the second contains algorithmic timing parameters.

RTOR Interval Memory Register (1 Word x 24 Bits)

The RTOR Interval (RTOR) memory register is a single read-only register consisting of 14 bits of timing interval information, left justified (and 8 unused bits, set to zero).

The RTOR register stores the time interval between the last two R events, as identified by the RTOR detection circuitry, which operates on the channel output data. Each LSB in the RTOR register is approximately equal to 8ms (CNFG_GEN for exact figures). The resulting 14-bit storage interval can thus be approximately 130 seconds in length, again depending on device settings.

Each time the RTOR detector identifies a new R event, the RTOR register is updated, and the RRINT interrupt term is asserted (see *STATUS (0x01) Register* for details).

Users wishing to log heart rate based on RTOR register data should set CLR_RRINT equals 01 in the MNGR_INT register. This will clear the RRINT interrupt term after the RTOR register has been read back, preparing the device for identification of the next RTOR interval.

Users wishing to log heart rate based on the time elapsed between RRINT assertions using the µC to keep track of the time base (and ignoring the RTOR register data) have two choices for interrupt management. If CLR_RRINT equals 00 in the MNGR_INT register, the RRINT interrupt term will clear after each STATUS register read back, preparing the device for identification of the next RTOR interval. If CLR_RRINT equals 10 in the MNGR_INT register, the RRINT interrupt term will self-clear after each one full data cycle has passed, preparing the device for identification of the next RTOR interval (this mode is recommended only if using the INT2B as a dedicated heart rate indicator).

If the RTOR detector reaches an overflow state after several minutes without detection of an R event, the counter will simply roll over, and the lack of the RRINT activity on the dedicated INT2B line will inform the µC that no RTOR activity was detected.

Table 25. CNFG_RTOR and CNFG_RTOR2 (0x1D and 0x1E) Register Maps

REG	NAME	R/W	23 / 15 / 7	22 / 14 / 6	21 / 13 / 5	20 / 12 / 4	19 / 11 / 3	18 / 10 / 2	17 / 9 / 1	16 / 8 / 0
0x1D	CNFG_ RTOR1	R/W	WNDW[3:0]				GAIN[3:0]			
			EN_ RTOR	x	PAVG[1:0]		PTSF[3:0]			
			x	x	x	x	x	x	x	x
0x1E	CNFG_ RTOR2	R/W	x	x	HOFF[5:0]					
			x	x	RAVG[1:0]		x	RHSF[2:0]		
			x	x	x	x	x	x	x	x

Table 26. CNFG_RTOR and CNFG_RTOR2 (0x1D and 0x1E) Register Functionality

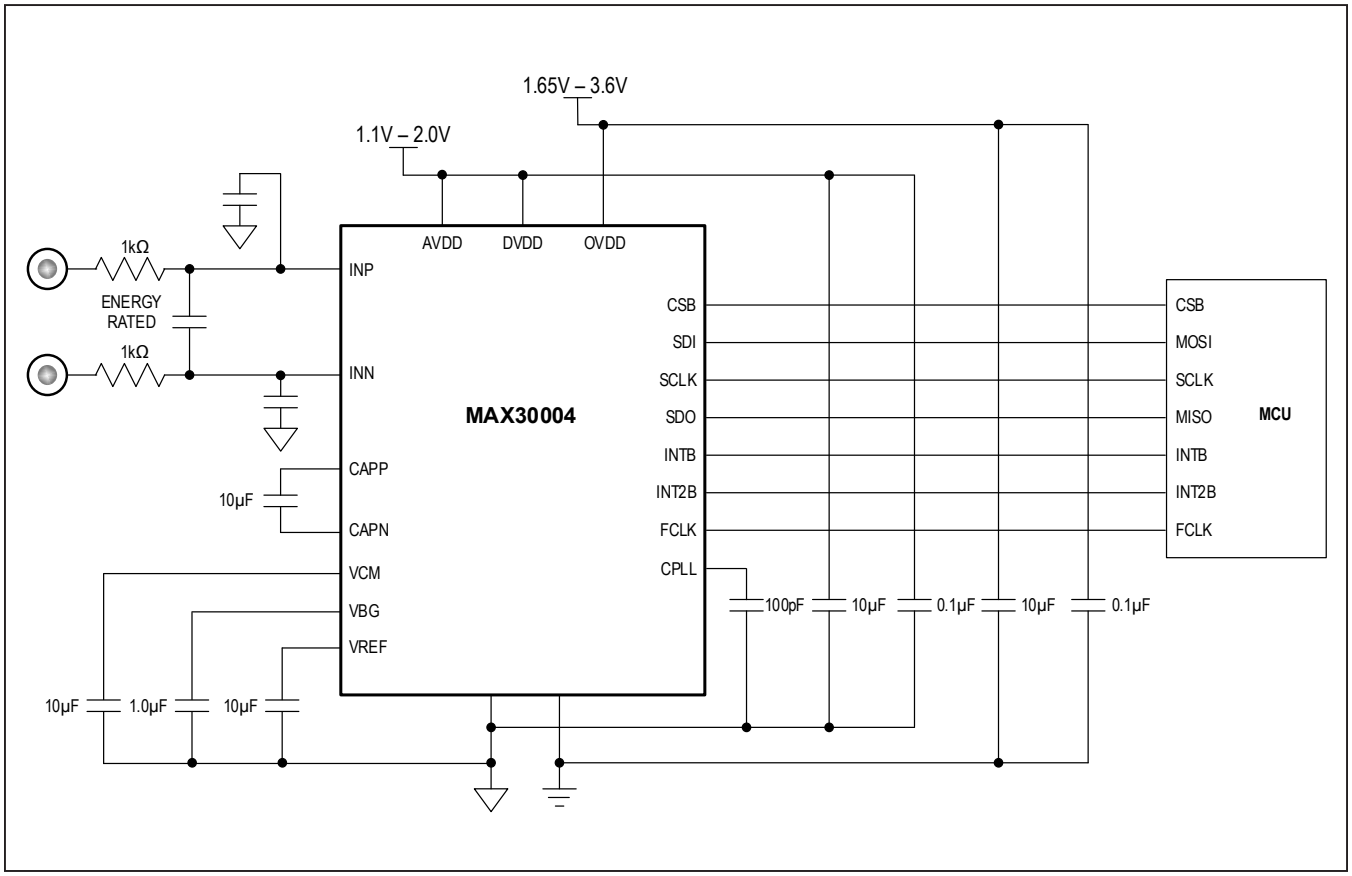
INDEX	NAME	DEFAULT	FUNCTION
			CNFG_RTOR1 (0x1D)
D[23:20]	WNDW[3:0]	0011	This is the width of the averaging window, which adjusts the algorithm sensitivity to the width of the QRS complex. R-to-R Window Averaging (Window Width = RTOR_WNDW[3:0]*8ms) 0000 = 6 0001 = 8 0010 = 10 0011 = 12 (default = 96ms) 0100 = 14 0101 = 16 0110 = 18 0111 = 20 1000 = 22 1001 = 24 1010 = 26 1011 = 28 1100 = Reserved. Do not use. 1101 = Reserved. Do not use. 1110 = Reserved. Do not use. 1111 = Reserved. Do not use.
D[19:16]	GAIN[3:0]	1111	R-to-R Gain (where Gain = 2^GAIN[3:0], plus an auto-scale option). This is used to maximize the dynamic range of the algorithm. 0000 = 1 1000 = 256 0001 = 2 1001 = 512 0010 = 4 1010 = 1024 0011 = 8 1011 = 2048 0100 = 16 1100 = 4096 0101 = 32 1101 = 8192 0110 = 64 1110 = 16384 0111 = 128 1111 = Auto-Scale (default) In Auto-Scale mode, the initial gain is set to 64.
D[15]	EN_RTOR	0	RTOR Detection Enable 0 = RTOR Detection disabled 1 = RTOR Detection enabled if EN_CH is also enabled.

Table 26. CNFG_RTOR and CNFG_RTOR2 (0x1D and 0x1E) Register Functionality (continued)

INDEX	NAME	DEFAULT	FUNCTION
D[13:12]	PAVG[1:0]	10	R-to-R Peak Averaging Weight Factor This is the weighting factor for the current RTOR peak observation vs. past peak observations when determining peak thresholds. Lower numbers weight current peaks more heavily. 00 = 2 01 = 4 10 = 8 (default) 11 = 16 Peak_Average(n) = [Peak(n) + (RTOR_PAVG-1) x Peak_Average(n-1)]/RTOR_PAVG.
D[11:8]	PTSF[3:0]	0011	R-to-R Peak Threshold Scaling Factor This is the fraction of the Peak Average value used in the Threshold computation. Values of 1/16 to 16/16 are selected directly by (RTOR_PTSF[3:0]+1)/16, default is 4/16.
CNFG_ RTOR2 (0x1E)D [21:16]	HOFF[5:0]	10_0000	R-to-R Minimum Hold Off This sets the absolute minimum interval used for the static portion of the Hold Off criteria. Values of 0 to 63 are supported, default is 32 $t_{HOLD\_OFF\_MIN}$ = HOFF[5:0] * t_{RTOR}, where t_{RTOR} is ~8ms, as determined by FMSTR[1:0] in the CNFG_GEN register. (representing approximately ¼ second). The R-to-R Hold Off qualification interval is t_{Hold_Off} = MAX($t_{Hold\_Off\_Min}$, $t_{Hold\_Off\_Dyn}$) (see below).
D[13:12]	RAVG[1:0]	10	R-to-R Interval Averaging Weight Factor This is the weighting factor for the current RtoR interval observation vs. the past interval observations when determining dynamic holdoff criteria. Lower numbers weight current intervals more heavily. 00 = 2 01 = 4 10 = 8 (default) 11 = 16 Interval_Average(n) = [Interval(n) + (RAVG-1) x Interval_Average(n-1)]/RAVG.
D[10:8]	RHSF[2:0]	100	R-to-R Interval Hold Off Scaling Factor This is the fraction of the RtoR average interval used for the dynamic portion of the holdoff criteria (t_{HOLD_OFFDYN}). Values of 0/8 to 7/8 are selected directly by RTOR_RHSF[3:0]/8, default is 4/8. If 000 (0/8) is selected, then no dynamic factor is used and the holdoff criteria is determined by HOFF[5:0] only (see above).

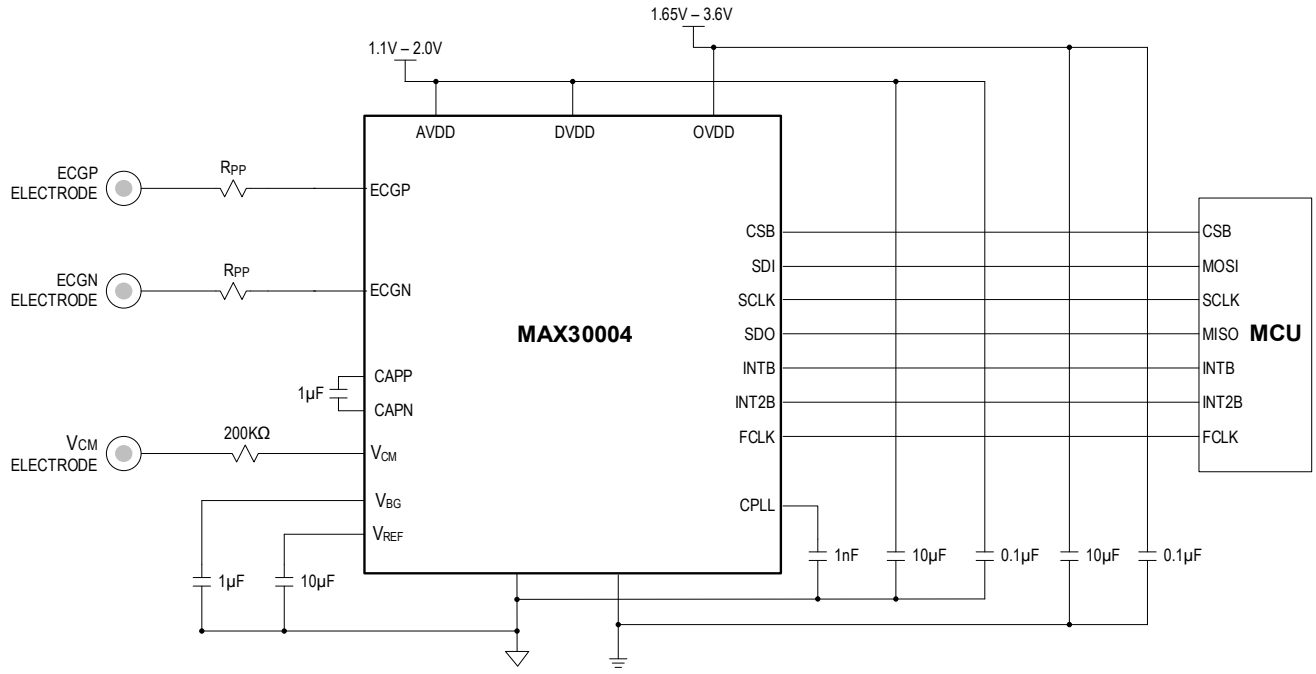
Typical Application Circuit

MAX30004



Typical Application Circuit (continued)

Three-Dry-Electrode, Wrist-Worn ECG Monitor Typical Application Circuit



NOTES:

- R_{PP} ARE PATIENT PROTECTION RESISTORS. THESE MUST BE CHOSEN TO SATISFY IEC 60601-1 PATIENT SAFETY REQUIREMENTS FOR THE PARTICULAR APPLICATION.
- V_{CM} REQUIRES A 200KΩ RESISTOR. THIS IS REQUIRED TO LIMIT CURRENT FROM THE V_{CM} AND ALSO ACTS AS A PATIENT PROTECTION RESISTOR.
- IN A DRY ELECTRODE APPLICATION, THE ECG INPUT IMPEDANCE SHOULD REMAIN HIGH, MEANING THE MAX30004 LEAD BIAS RESISTORS SHOULD NOT BE ENABLED. V_{CM} IS USED TO SET THE BODY BIAS VOLTAGE.

Application Diagrams

Two Electrode Heart Rate Fitness

See Figure 8 for an example of a fitness monitoring configuration.

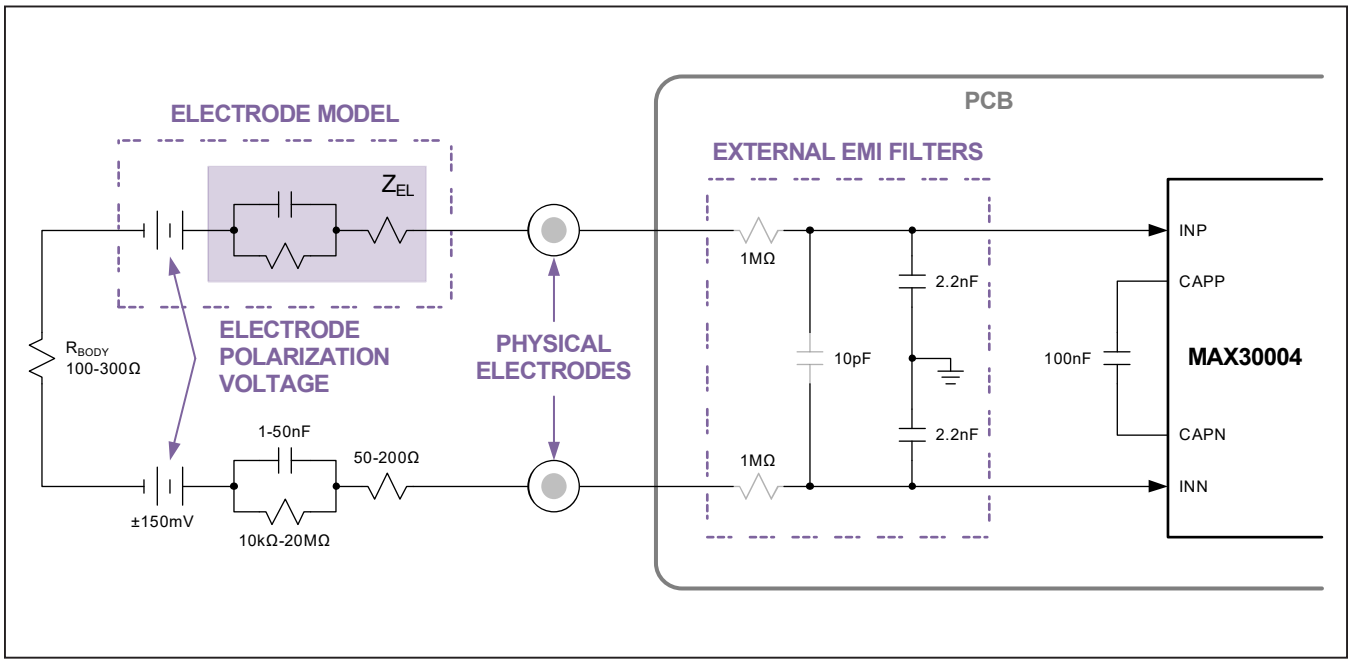


Figure 8. Two Electrode Heart Rate Monitoring for Fitness

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX30004CWV+	0°C to +70°C	30 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
30 WLP	W302L2+1	**21-100074**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/16	Initial release	—
1	1/23	Updated General Description, Benefits and Features, Absolute Maximum Ratings, Package Thermal Characteristics, Electrical Characteristics table, Timing Characteristics table, Figure 1a, TOC20, Pin Configuration, Pin Description table, Detailed Description, EMI Filtering and ESD Protection, DC Leads-Off Detection and ULP Leads-On Detection, Lead Bias, Gain Settings and Input Range, Table 7, Table 12, Table 13, Table 14, Table 15, Table 23, Table 24, and added Typical Application Circuit, updated Ordering Information table, and Package Information table	1, 3-8, 11-16, 24, 26-28, 33, 37, 38