MICROCHIP TC4423M/TC4424M/TC4425M

3A Dual High-Speed Power MOSFET Drivers

Features

- High Peak Output Current: 3A
- Wide Input Supply Voltage Operating Range:
  - 4.5V to 18V
- High Capacitive Load Drive Capability:
  - 1800 pF in 25 ns
- Short Delay Times: <40 ns (typ)
- Matched Rise/Fall Times
- Low Supply Current:
  - With Logic '1' Input – 3.5 mA (Max)
  - With Logic '0' Input – 350 µA (Max)
- Low Output Impedance: 3.5Ω (typ)
- Latch-Up Protected: Will Withstand 1.5A Reverse Current
- Logic Input: Will Withstand Negative Swing Up To 5V
- ESD Protected: 4 kV
- Pin-compatible with the TC4426M/TC4427M/ TC4428M and TC4426AM/TC4427AM/ TC4428AM devices
- Wide Operating Temperature Range:
  - -55°C to +125°C
- See TC4423/TC4424/TC4425 Data Sheet (DS21421) for additional temperature range and packaging offerings

Applications

- Switch-mode Power Supplies
- Pulse Transformer Drive
- Line Drivers

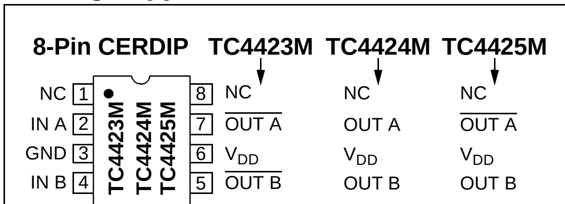
General Description

The TC4423M/TC4424M/TC4425M devices are a family of 3A, dual output buffers/MOSFET drivers. Pin-compatible with both the TC4426M/TC4427M/ TC4428M and TC4426AM/4427AM/4428AM families (dual 1.5A drivers), the TC4423M/TC4424M/TC4425M family has an increased latch-up current rating of 1.5A, making them even more robust for operation in harsh electrical environments.

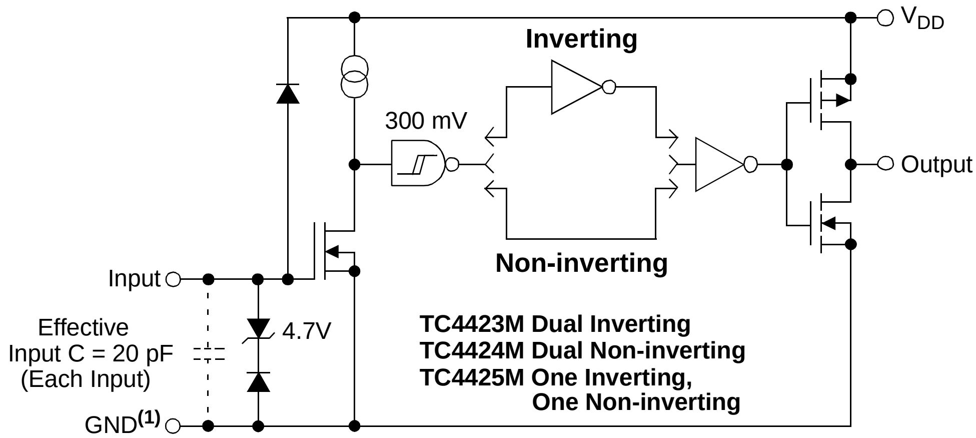
As MOSFET drivers, the TC4423M/TC4424M/ TC4425M can easily charge 1800 pF gate capacitance in under 35 nsec, while providing low enough impedances in both the on and off states to ensure the MOSFET's intended state will not be affected, even by large transients.

The TC4423M/TC4424M/TC4425M inputs may be driven directly from either TTL or CMOS (2.4V to 18V). In addition, 300 mV of hysteresis is built-in to provide noise immunity and to allow the device to be driven from slowly rising or falling waveforms.

Package Types



Functional Block Diagram



Note 1: Unused inputs should be grounded.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ....+22V
Input Voltage, IN A or IN B..........(V_{DD} + 0.3V) to (GND – 5V)

† **Notice:** Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, T_A = +25°C, with 4.5V $\le V_{DD} \le$ 18V.

Parameters	Sym	Min	Typ	Max	Units	Conditions
Input						
Logic ‘1’, High Input Voltage	V_{IH}	2.4	—	—	V	
Logic ‘0’, Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-1	—	1	µA	0V $\le V_{IN} \le V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance, High	R_{OH}	—	2.8	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	3.5	5	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	3	—	A	
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	>1.5	—	A	Duty cycle $\le$ 2%, t $\le$ 300 µsec.
Switching Time (Note 1)						
Rise Time	t_R	—	23	35	ns	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Fall Time	t_F	—	25	35	ns	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Delay Time	t_{D1}	—	33	75	ns	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Delay Time	t_{D2}	—	38	75	ns	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Power Supply						
Power Supply Current	I_S	— —	1.5 0.15	2.5 0.25	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.

DC CHARACTERISTICS (OVER OPERATING TEMPERATURE RANGE)

Electrical Specifications: Unless otherwise indicated, operating temperature range with 4.5V $\leq V_{DD} \leq$ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Input						
Logic ‘1’, High Input Voltage	V_{IH}	2.4	—	—	V	
Logic ‘0’, Low Input Voltage	V_{IL}	—	—	0.8	V	
Input Current	I_{IN}	-10	—	+10	µA	$0V \leq V_{IN} \leq V_{DD}$
Output						
High Output Voltage	V_{OH}	V_{DD} – 0.025	—	—	V	
Low Output Voltage	V_{OL}	—	—	0.025	V	
Output Resistance, High	R_{OH}	—	3.7	8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Output Resistance, Low	R_{OL}	—	4.3	8	Ω	I_{OUT} = 10 mA, V_{DD} = 18V
Peak Output Current	I_{PK}	—	3.0	—	A	
Latch-Up Protection Withstand Reverse Current	I_{REV}	—	>1.5	—	A	Duty cycle $\leq$ 2%, t $\leq$ 300 µsec
Switching Time (Note 1)						
Rise Time	t_R	—	28	60	ns	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Fall Time	t_F	—	32	60	ns	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Delay Time	t_{D1}	—	32	100	ns	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Delay Time	t_{D2}	—	38	100	ns	**Figure 4-1**, **Figure 4-2**, C_L = 1800 pF
Power Supply						
Power Supply Current	I_S	— —	2.0 0.2	3.5 0.3	mA	V_{IN} = 3V (Both inputs) V_{IN} = 0V (Both inputs)

Note 1: Switching times ensured by design.

TEMPERATURE CHARACTERISTICS

Electrical Specifications: Unless otherwise noted, all parameters apply with 4.5V $\leq V_{DD} \leq$ 18V.						
Parameters	**Sym**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
Temperature Ranges						
Specified Temperature Range (M)	T_A	-55	—	+125	ºC	
Maximum Junction Temperature	T_J	—	—	+150	ºC	
Storage Temperature Range	T_A	-65	—	+150	ºC	
Package Thermal Resistances						
Thermal Resistance, 8L-CERDIP	θ_{JA}	—	150	—	ºC/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

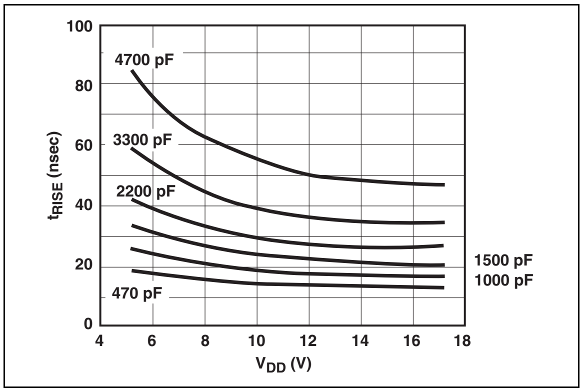


FIGURE 2-1: Rise Time vs. Supply Voltage.

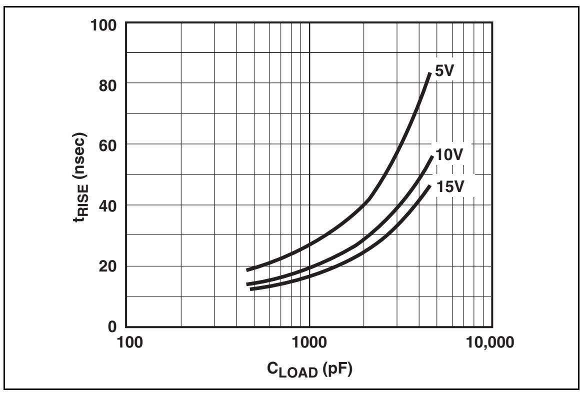


FIGURE 2-2: Rise Time vs. Capacitive Load.

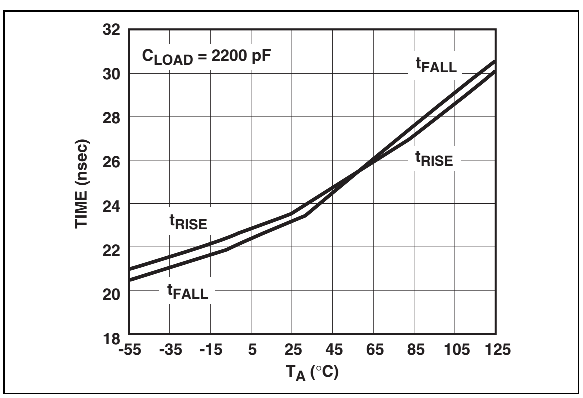


FIGURE 2-3: Rise and Fall Times vs. Temperature.

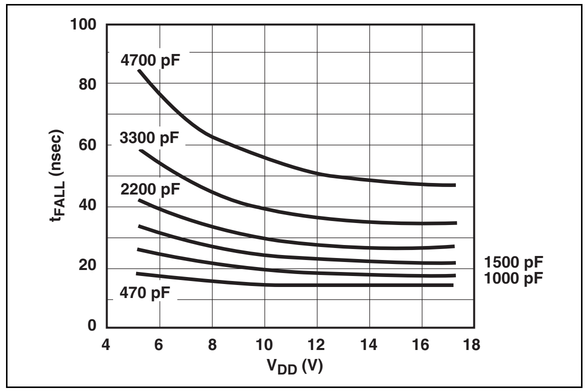


FIGURE 2-4: Fall Time vs. Supply Voltage.

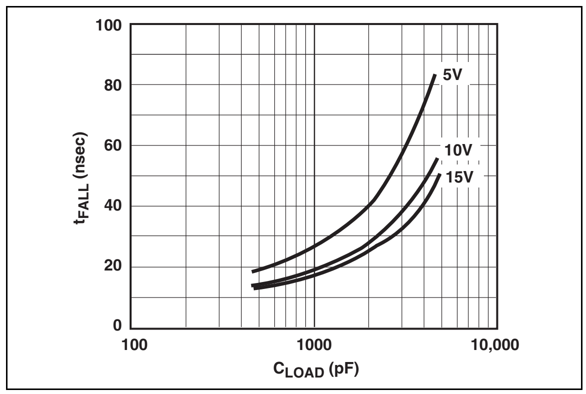


FIGURE 2-5: Fall Time vs. Capacitive Load.

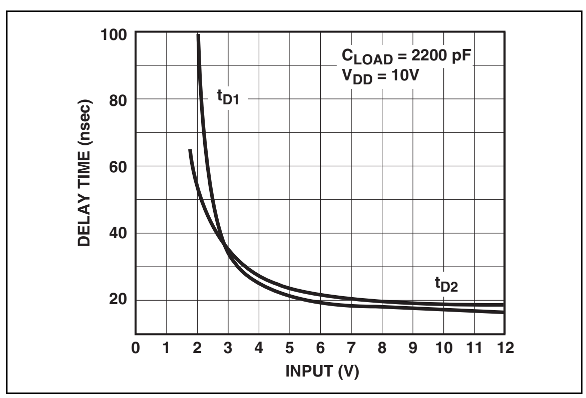


FIGURE 2-6: Propagation Delay vs. Input Amplitude.

Typical Performance Curves (Continued)

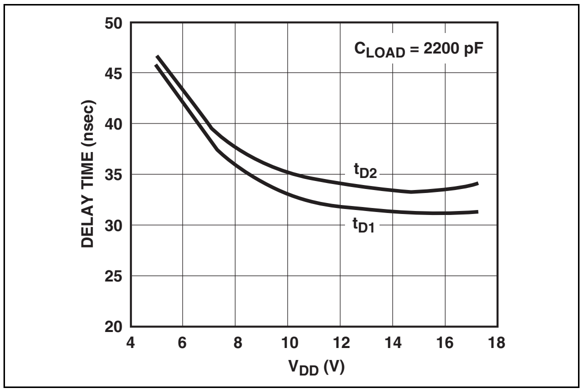


FIGURE 2-7: *Propagation Delay Time vs. Supply Voltage.*

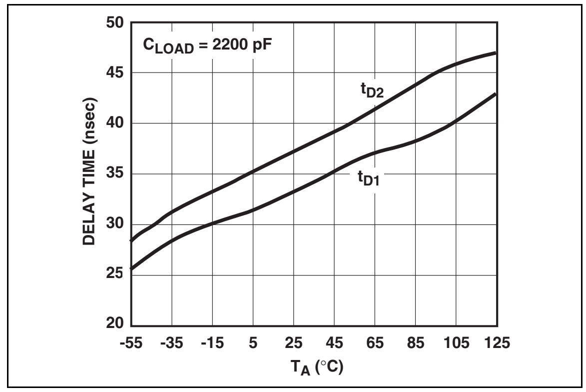


FIGURE 2-10: *Propagation Delay Time vs. Temperature.*

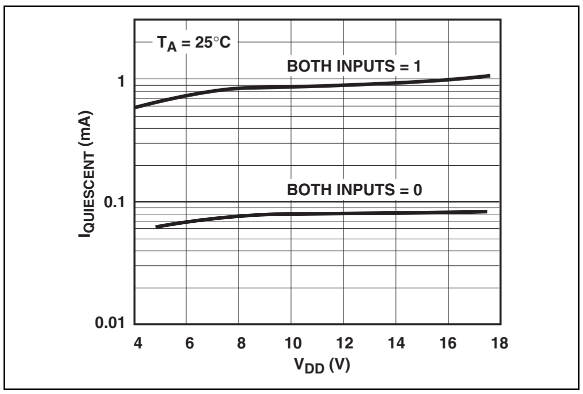


FIGURE 2-8: *Quiescent Current vs. Supply Voltage.*

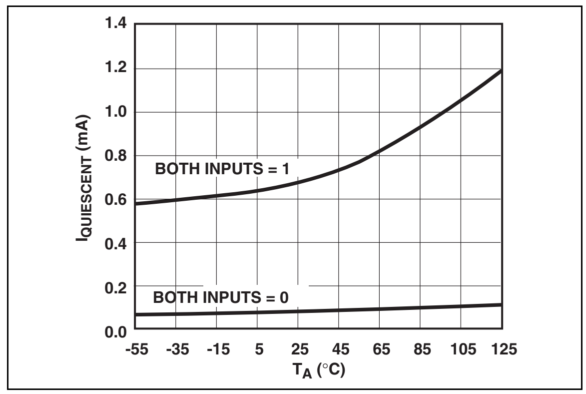


FIGURE 2-11: *Quiescent Current vs. Temperature.*

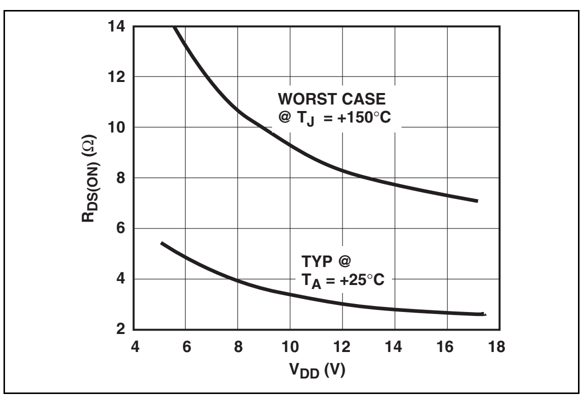


FIGURE 2-9: *Output Resistance (Output High) vs. Supply Voltage.*

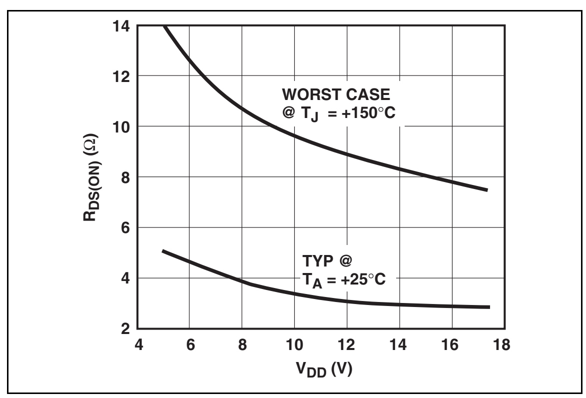


FIGURE 2-12: *Output Resistance (Output Low) vs. Supply Voltage.*

Typical Performance Curves (Continued)

Note: Load on single output only

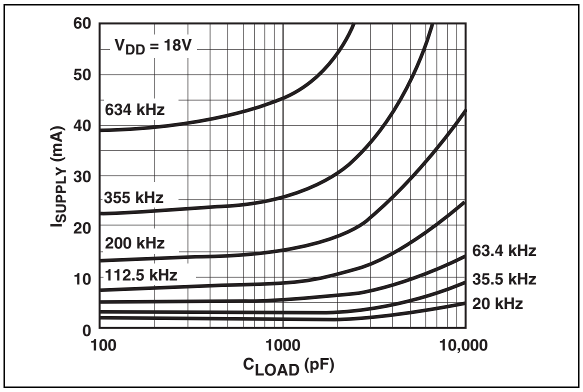


FIGURE 2-13: *Supply Current vs. Capacitive Load.*

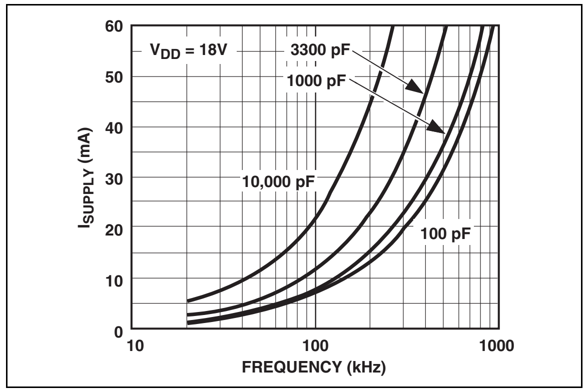


FIGURE 2-16: *Supply Current vs. Frequency.*

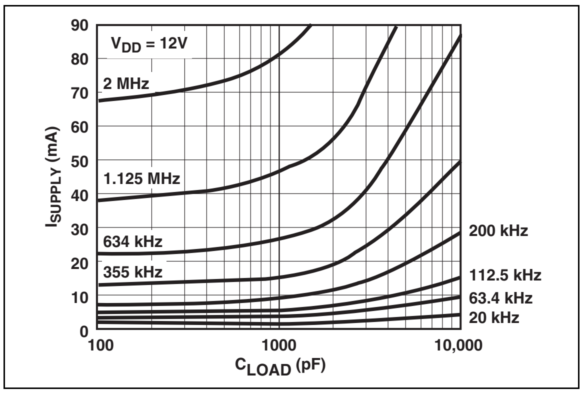


FIGURE 2-14: *Supply Current vs. Capacitive Load.*

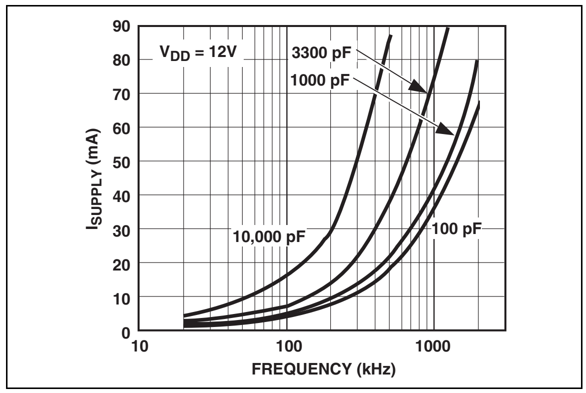


FIGURE 2-17: *Supply Current vs. Frequency.*

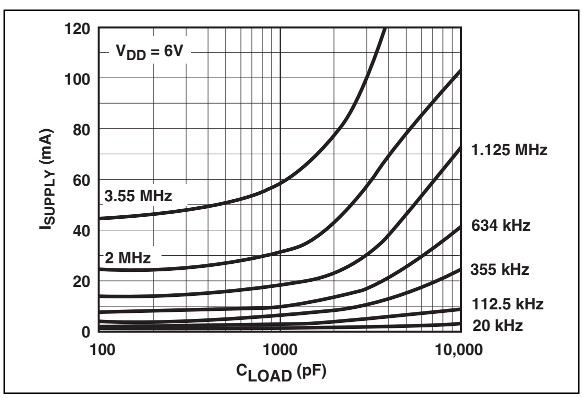


FIGURE 2-15: *Supply Current vs. Capacitive Load.*

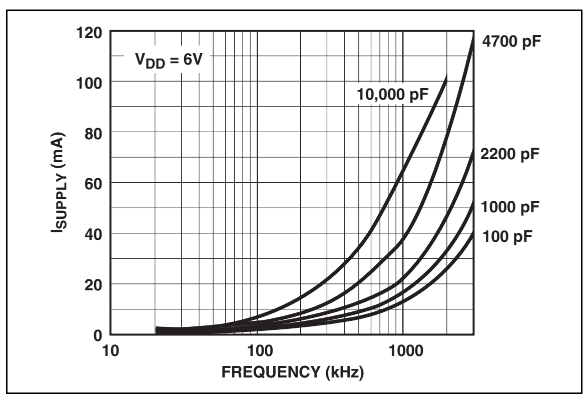
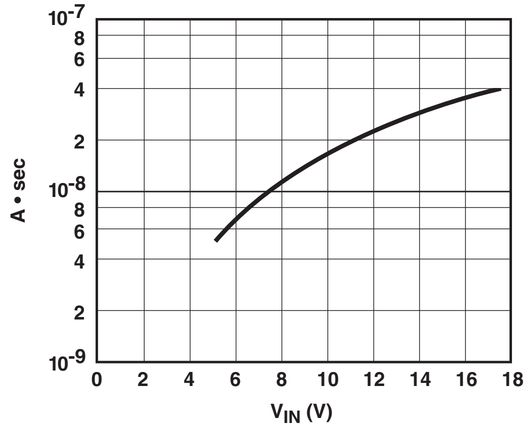


FIGURE 2-18: *Supply Current vs. Frequency.*

Typical Performance Curves (Continued)



Note: The values on this graph represent the loss seen by both drivers in a package during one complete cycle. For a single driver, divide the stated values by 2. For a single transition of a single driver, divide the stated value by 4.

FIGURE 2-19: *TC4423M Crossover Energy.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

8-Pin CERDIP	Symbol	Description
1	NC	No connection
2	IN A	Input A
3	GND	Ground
4	IN B	Input B
5	OUT B	Output B
6	V_{DD}	Supply input
7	OUT A	Output A
8	NC	No connection

3.1 Input A (IN A)

IN A is a TTL/CMOS-compatible input that controls OUT A. This input has 300 mV of hysteresis between the high and low input levels that allows it to be driven from slow rising and falling signals, as well as providing noise immunity.

3.2 Input B (IN B)

IN B is a TTL/CMOS-compatible input that controls OUT B. This input has 300 mV of hysteresis between the high and low input levels that allows it to be driven from slow rising and falling signals, as well as providing noise immunity.

3.3 Output B (OUT B)

OUT B is a CMOS push-pull output that is capable of sourcing and sinking 3A peaks of current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. This output also has a reverse current latch-up rating of 1.5A.

3.4 Output A (OUT A)

OUT A is a CMOS, push-pull output that is capable of sourcing and sinking 3A peaks of current (V_{DD} = 18V). The low output impedance ensures the gate of the external MOSFET will stay in the intended state even during large transients. This output also has a reverse current latch-up rating of 1.5A.

3.5 Supply Input (V_{DD})

V_{DD} is the bias supply input for the MOSFET driver and has a voltage range of 4.5V to 18V. This input must be decoupled to ground with a local ceramic capacitor. This bypass capacitor provides a localized low-impedance path for the peak currents that are to be provided to the load.

3.6 Ground (GND)

GND is the device return pin. The ground pin(s) should have a low-impedance connection to the bias supply source return. High peak currents will flow out the ground pin(s) when the capacitive load is being discharged.

4.0 APPLICATIONS INFORMATION

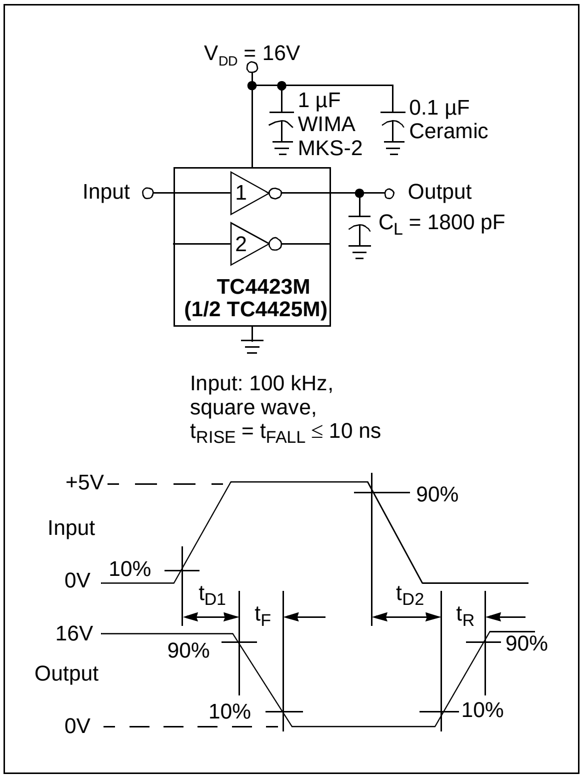


FIGURE 4-1: *Inverting Driver Switching Time.*

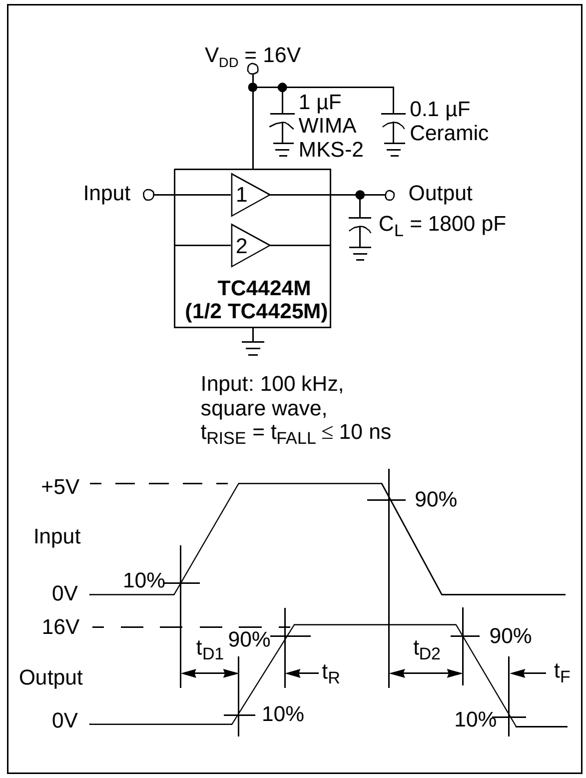
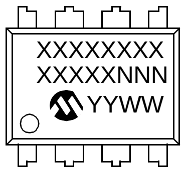


FIGURE 4-2: *Non-inverting Driver Switching Time.*

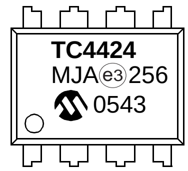
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

8-Lead CERDIP (300 mil)



Example:

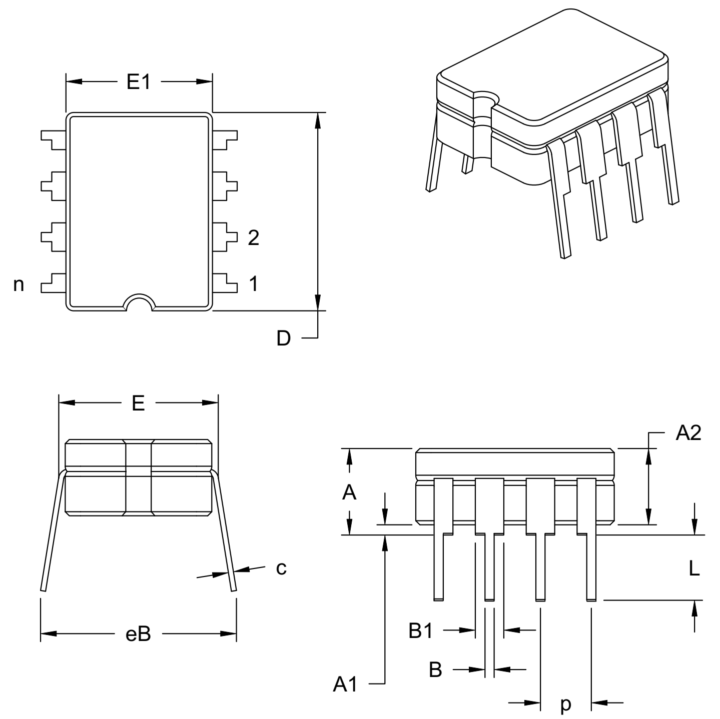


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	e3	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

8-Lead Ceramic Dual In-line – 300 mil (CERDIP)

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.180	.200	4.06	4.57	5.08
Standoff §	A1	.020	.030	.040	0.51	0.77	1.02
Shoulder to Shoulder Width	E	.290	.305	.320	7.37	7.75	8.13
Ceramic Pkg. Width	E1	.230	.265	.300	5.84	6.73	7.62
Overall Length	D	.370	.385	.400	9.40	9.78	10.16
Tip to Seating Plane	L	.125	.163	.200	3.18	4.13	5.08
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.055	.065	1.14	1.40	1.65
Lower Lead Width	B	.016	.018	.020	0.41	0.46	0.51
Overall Row Spacing	eB	.320	.360	.400	8.13	9.15	10.16

*Controlling Parameter

JEDEC Equivalent: MS-030

Drawing No. C04-010

APPENDIX A: REVISION HISTORY

Revision B (January 2013)

Added a note to each package outline drawing.

Revision A (March 2005)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX
Device and Temperature Range	Package

Device:	TC4423M: 3A Dual MOSFET Driver, Inverting, -55°C to +125°C TC4424M: 3A Dual MOSFET Driver, Non-Inverting, -55°C to +125°C TC4425M: 3A Dual MOSFET Driver, Complementary, -55°C to +125°C
Package:	JA = Ceramic DIP, (300 mil body), 8-lead

Examples:

a) TC4423MJA: 3A Dual MOSFET Driver, Inverting, -55°C to +125°C 8LD CERDIP package.

a) TC4424MJA: 3A Dual MOSFET Driver, Non-Inverting, -55°C to +125°C 8LD CERDIP package.

a) TC4425MJA: 3A Dual MOSFET Driver, Complementary, -55°C to +125°C 8LD CERDIP package.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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ISBN: 9781620769188

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