
ML9271

48-Bit Grid/Anode VFD Driver

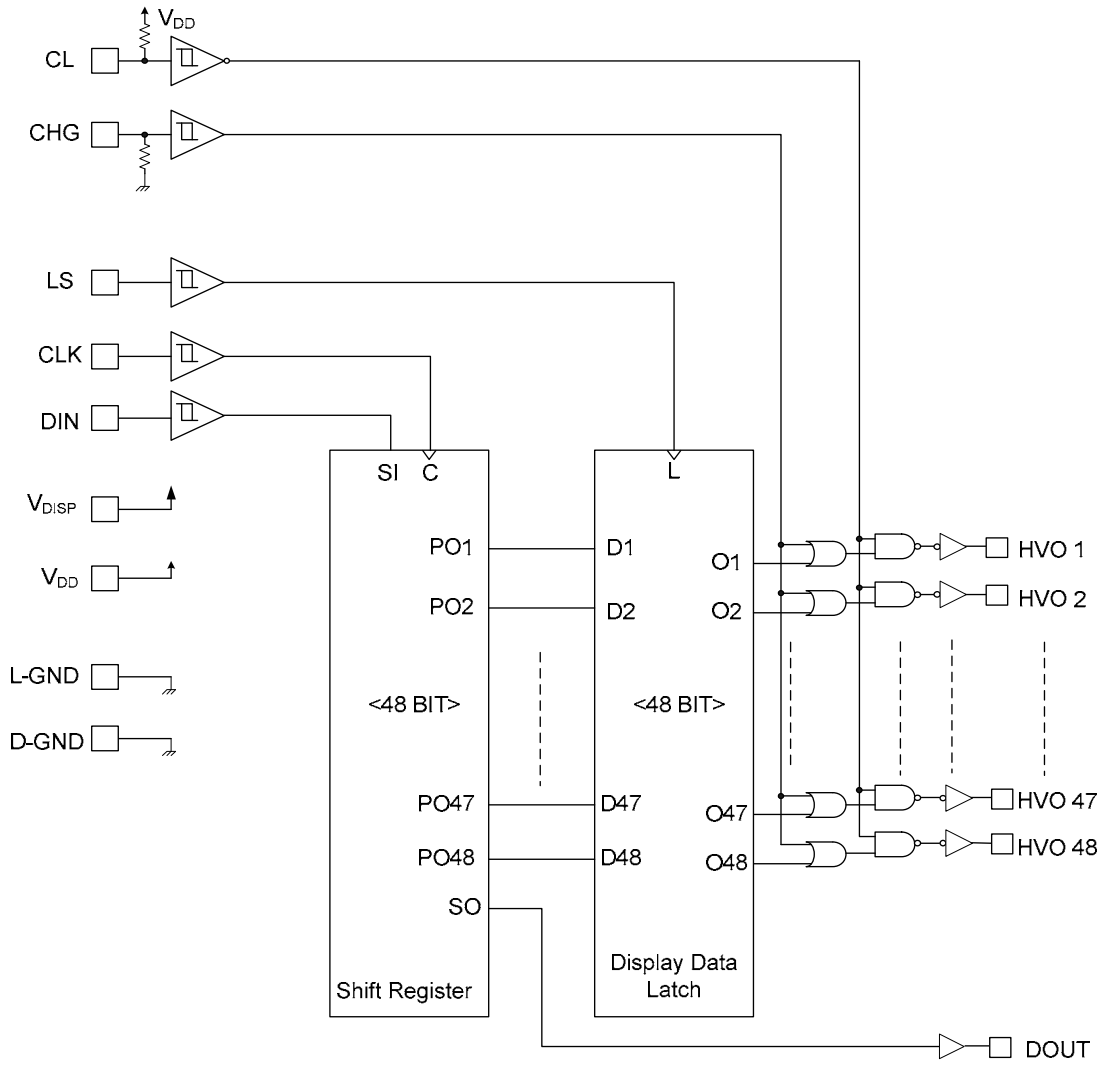
GENERAL DESCRIPTION

The ML9271 is a monolithic IC designed for directly driving the anodes of the vacuum fluorescent display tube. The circuit contains a 48-bit shift register circuit, 48-bit latch circuit, and 48 output circuits on a single chip. Display data is serially stored in the shift register at the rising edge of CLOCK pulse. Setting the CL pin high allows all the driver outputs to be driven low, which makes it possible to set the display clear. Setting the CHG pin high with the CL pin set low allows all the driver outputs to be driven high for testing.

FEATURES

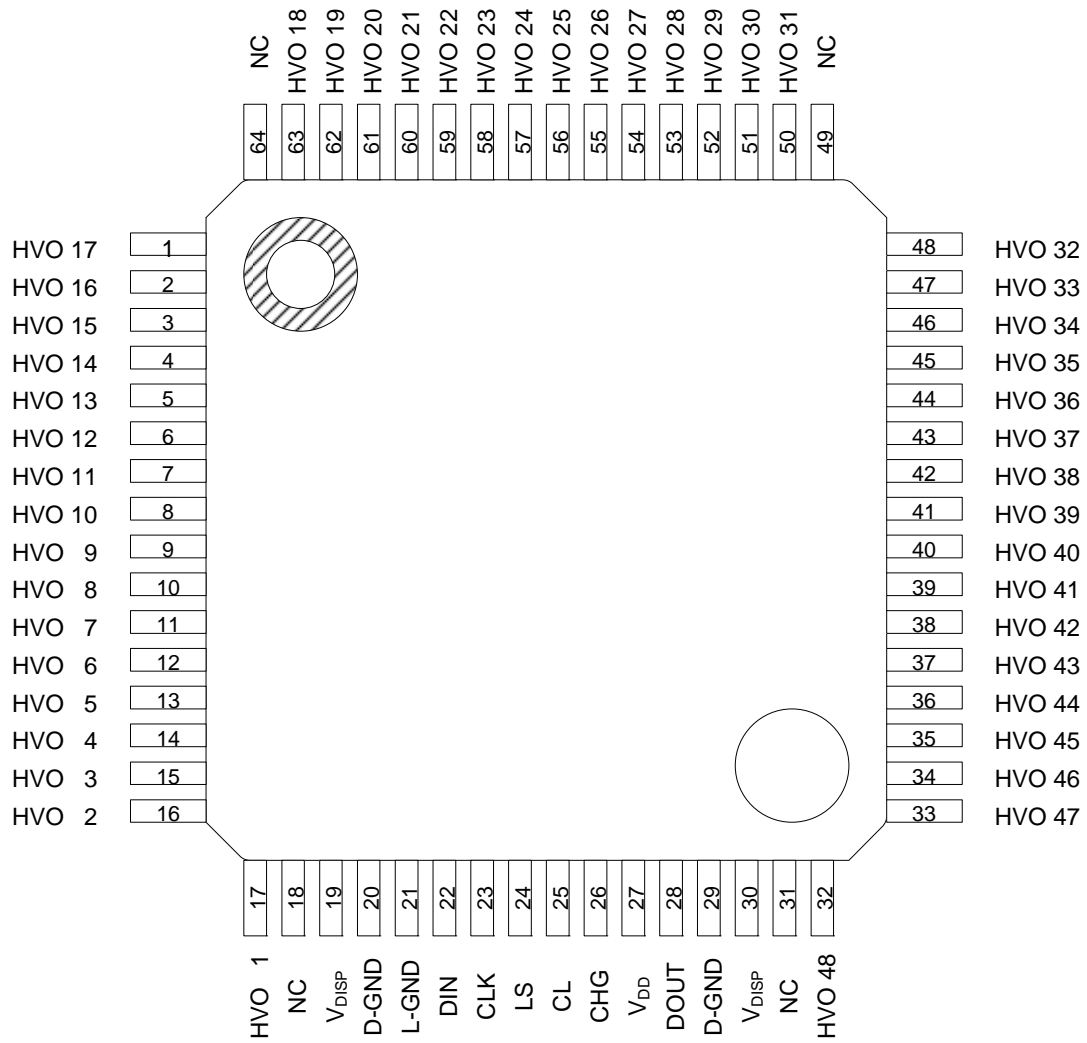
- Logic power supply (V_{DD}) : 3.3V±10% or 5.0 V±10%
- VFD tube drive power supply (V_{DISP}) : 8 to 18 V
- Operating temperature range : -40 to +105°C
- VFD driver outputs can be connected directly to the VFD tube. No pull-down resistor is required.
- VFD driver output current (HVO1 to HVO48) : -6.0 mA
- Clock frequency : 5.0MHz
- Package : 64-pin plastic QFP (QFP64-P-1414-0.80-BK)
: Al-Pad Chip

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)

64-Pin Plastic QFP



NC: No-Connection pin

PIN DESCRIPTION

Pin	Symbol	Type	Function	Description
1 to 17, 32 to 48, 50 to 63	HVO1 to HVO48	O	Driver Outputs	Driver output pins, which correspond to individual bits of the shift register.
19,30	V _{DISP}	—	Driver Power Supply	Power supply pins for driver circuit. Both pin 19 and pin 30 should be connected externally.
27	V _{DD}	—	Logic Power Supply	Power supply pin for logic.
20,29	D-GND	—	Driver GND	GND pins for the driver circuits. Both pin 20 and pin 29 should be connected externally.
21	L-GND	—	Logic GND	GND pin for the logic circuit.
22	DIN	I	Data Input	Input pin without pull-up or pull-down resistor. The input pin to the shift register. Inputs to display data are synchronized with the clock signal. (positive logic)
23	CLK	I	Clock Input	Input pin without pull-up or pull-down resistor. Data of the shift register is shifted from one stage to the next on each rising edge of the clock pulses.
24	LS	I	Latch Strobe Input	Input pin without pull-up or pull-down resistor. When LS is high, the latch is shunted and the shift register outputs become latched. The latch holds the outputs from the shift register just before LS goes from low to high.
25	CL	I	Clear Input	Clear input pin with a pull-up resistor. This pin is normally low. On this condition, driver output changes to high or low according to the latch output level. When CL is high, all driver output pins are fixed to low.
26	CHG	I	Test Input	Test input pin with a pull-down resistor. This pin is normally low. When CL is high, all driver output pins are fixed to low irrespective of CHG. When CL is low and CHG is low, the driver outputs change to high or low according to the latch output level. When CHG is high and CL is low, all driver outputs are high for testing.
28	DOUT	O	Data Output	Serial output pin from the shift register.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Logic Supply Voltage *1	V _{DD}	—	−0.3 to 6.5	V
Driver Supply Voltage *1, *2	V _{DISP}	—	−0.3 to 25	V
Input Voltage *1	V _{IN}	Applicable to all input pins	−0.3 to V _{DD} +0.3	V
Data Output Voltage *1	V _{O1}	Applicable to the data output pins	−0.3 to V _{DD} +0.3	V
Driver Output Voltage *1	V _{O2}	Applicable to the driver output pins	−0.3 to V _{DISP} +0.3	V
Storage Temperature	T _{STG}	—	−55 to 150	°C
Power Dissipation	P _D	T _a < 105°C 64-pin plastic QFP	339	mW
Thermal Resistance *3	R _{j-a}	—	59	°C/W
Output Current	I _{O1}	HVO1 to HVO48	−18.0 to 2.0	mA
	I _{O2}	DOUT	−2.0 to 2.0	

*1 Maximum supply voltage with respect to L-GND and D-GND

*2 Catastrophic breakdown may occur if the applied voltage exceeds the rating value.

*3 Thermal resistance of the package (between junction and atmosphere)

The junction temperature (T_j) given by the following formula should not exceed 150°C.

$$T_j = P \times R_{j-a} + T_a \quad (P \text{ is the maximum power dissipation})$$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply Voltage	V_{DD}	When the logic supply voltage is 3.3 V (typ.)	3.0	3.3	3.6	V
		When the logic supply voltage is 5.0 V (typ.)	4.5	5.0	5.5	V
Driver Supply Voltage	V_{DISP}	Applicable to the driver supply voltage pin	8	—	18	V
CLK Frequency	f_{CLK}	See the Timing Diagram	—	—	5.0	MHZ
Operating Temperature	T_a	64-pin plastic QFP	-40	—	105	°C
	T_j	Al-Pad Chip	-40	—	115	

ELECTRICAL CHARACTERISTICS**DC Characteristics**(V_{DD} = 5.0 V±10% or V_{DD} = 3.3 V±10%, V_{DISP} = 8 to 18 V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	
High Level Input Voltage	V _{IH}	All inputs	V _{DD} = 5.0V±10%	0.7 V _{DD}	—	—	V	
			V _{DD} = 3.3V±10%	0.8 V _{DD}	—	—	V	
Low Level Input Voltage	V _{IL}	All inputs	V _{DD} = 5.0V±10%	—	—	0.3 V _{DD}	V	
			V _{DD} = 3.3V±10%	—	—	0.2 V _{DD}	V	
High Level Input Current	I _{IH1}	V _I = V _{DD}	CHG pin	V _{DD} = 5.0V	100	—	600	μA
				V _{DD} = 3.3V	50	—	300	μA
	I _{IH2}		Other input pins	-1	—	1	μA	
Low Level Input Current	I _{IL1}	V _I = 0 V	CL pin	V _{DD} = 5.0V	-600	—	-100	μA
				V _{DD} = 3.3V	-300	—	-50	μA
	I _{IL2}		Other input pins	-1	—	1	μA	
High Level Driver Output Voltage	V _{OH1}	HVO1 to HVO48	I _{OH1} = -6.0mA V _{DISP} = 9.5v	V _{DISP} -1.0	—	—	V	
	V _{OH2}	DOUT	I _{OH2} = -0.1mA	V _{DD} -1.0	—	—	V	
Low Level Driver Output Voltage	V _{OL1}	HVO1 to HVO48	I _{OL1} = 0.2mA	—	—	1.0	V	
	V _{OL2}	DOUT	I _{OL2} = 0.1mA	—	—	1.0	V	
Supply Current (1) (Dynamic Mode)	I _{DD}	V _{DD}	V _{DD} = 5.0V±10% Input Data = "1" "0" "1" ...	—	—	2.5	mA	
			V _{DD} = 3.3V ±10% Input Data = "1" "0" "1" ...	—	—	2.0	mA	
	I _{DISP}	V _{DISP}	Input Data = "1" "0" "1" ...	—	—	0.5	mA	
Supply Current (2) (Static Mode)	I _{DDS}	V _{DD}	No Operation, Typ.: Ta = 25°C Max.: Ta = 85°C	—	1.0	10.0	μA	
	I _{DISPS}	V _{DISP}		—	1.0	20.0	μA	
Voltage Difference Between GND Pins	V _{GND}	Voltage difference between D-GND and L-GND *1		-0.1	0	0.1	V	

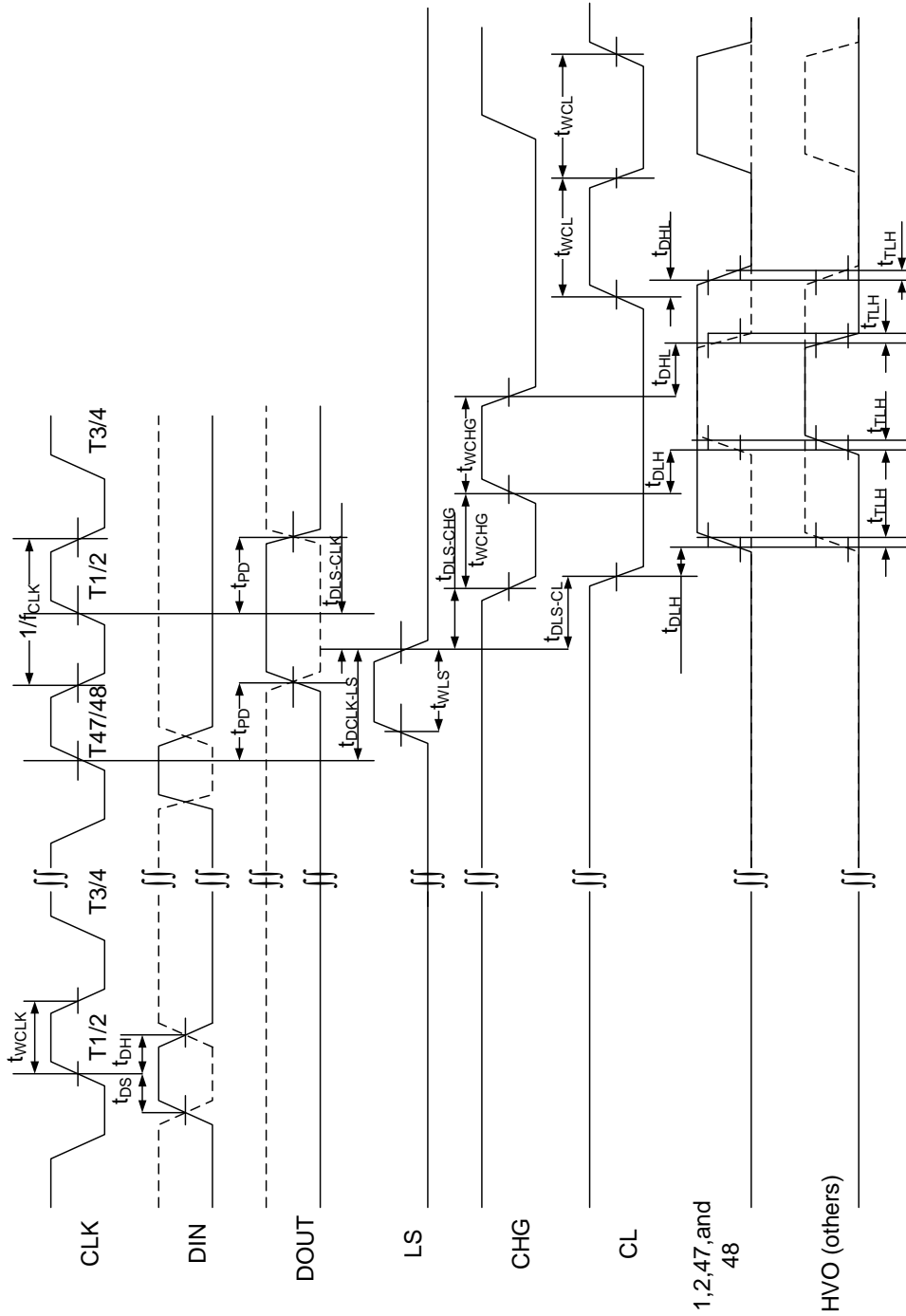
*1 The D-GND and L-GND pins are not connected internally. Therefore, set the voltage between D-GND and L-GND at the same voltage level by connecting these pins externally.

AC Characteristics(V_{DD} = 5.0 V \pm 10% or V_{DD} = 3.3 V \pm 10%, V_{DISP} = 8 to 18 V, Ta = -40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLK Pulse Width	t _{WCLK}	—	100	—	—	ns
Data Setup Time	t _{DS}	—	50	—	—	ns
Data Hold Time	t _{DH}	—	50	—	—	ns
LS Pulse Width	t _{WLS}	—	50	—	—	ns
CHG Pulse Width	t _{WCHG}	—	5	—	—	μs
CL Pulse Width	t _{WCL}	—	5	—	—	μs
CLK-LS Delay Time	t _{DCLK-LS}	—	50	—	—	ns
LS-CLK Delay Time	t _{DLS-CLK}	—	50	—	—	ns
LS-CHG Delay Time	t _{DLS-CHG}	—	0	—	—	ns
LS-CL Delay Time	t _{DLS-CL}	—	0	—	—	ns
CLK-DOUT Delay time	t _{PD}	C _{II} = 30 pF	—	25	50	ns
All Output Delay Time	t _{DLH}	C _{ld} = 100 pF t _R = 20 to 80% t _F = 80 to 20%	—	1.0	2.0	μs
	t _{DHL}		—	1.0	2.0	μs
All Output Slew Rate	t _{TLH}	C _{ld} = 100 pF t _R = 20 to 80% t _F = 80 to 20%	—	0.5	1.0	μs
	t _{THL}		—	0.5	1.0	μs

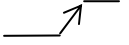

TIMING DIAGRAMS

Symbol	$V_{DD} = 3.3\text{ V} \pm 10\%$	$V_{DD} = 5.0\text{ V} \pm 10\%$
V_{IH} / V_{IL}	$0.8 V_{DD} / 0.2 V_{DD}$	$0.7 V_{DD} / 0.3 V_{DD}$
V_{OH} / V_{OL}	$0.8 V_{DISP} / 0.2 V_{DISP}$	$0.8 V_{DISP} / 0.2 V_{DISP}$
	$0.8 V_{DD} / 0.2 V_{DD}$	$0.8 V_{DD} / 0.2 V_{DD}$



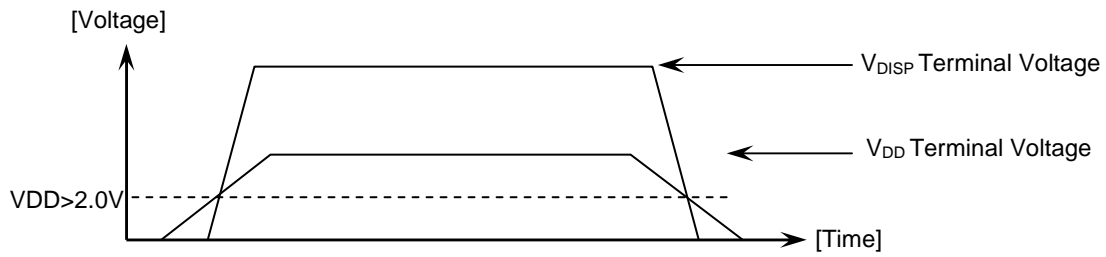
FUNCTIONAL DESCRIPTION

Funtion Table

CLOCK	DIN	PO1	PO2	PO3	PO4PO46	PO47	PO48	DOUT
	H	H	PO1k	PO2k	PO3kPO45k	PO46k	PO47k	PO47k
	L	L	PO1k	PO2k	PO3kPO45k	PO46k	PO47k	PO47k

CL	CHG	LS	POn	HVOn
H	X	X	X	L
L	H	X	X	H
L	L	H	H	H
L	L	H	L	L
L	L	L	X	NC

L: Low Level, H: High Level, X: Don't Care, NC: No Change

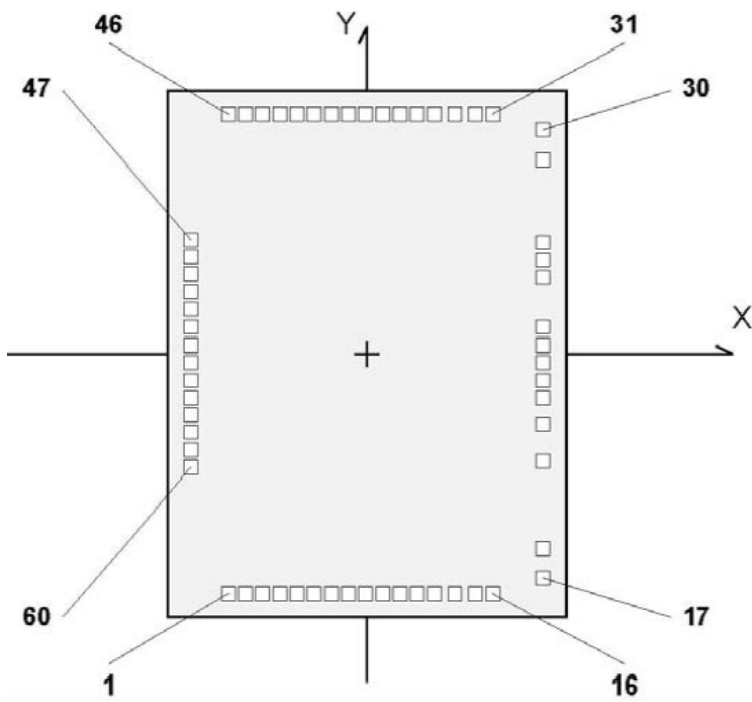
POWER-ON/OFF TIMING

To prevent IC from malfunctioning, V_{DISP} should be applied after V_{DD} is applied.
When the power is turned off, V_{DD} should be applied after V_{DISP} is applied.

PAD CONFIGURATION

Pad Layout

Chip Size: 2.32×3.00mm
 Chip Thickness: 350±30 μm
 Pad size Metal 90μm×90μm PV Pad hole 80μm×80μm

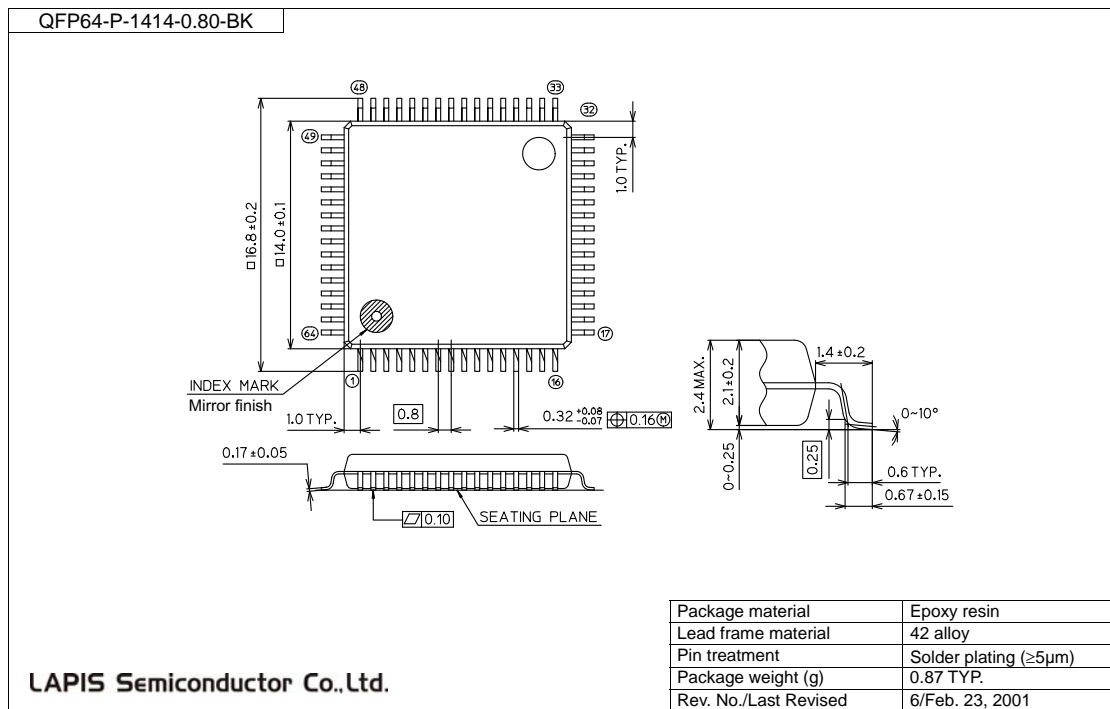


Pad Coordinates

Pad	Symbol	X (μm)	Y (μm)	Pad	Symbol	X (μm)	Y (μm)
1	HVO17	-808	-1365	31	HVO47	732	1365
2	HVO16	-708	-1365	32	HVO46	632	1365
3	HVO15	-608	-1365	33	HVO45	512	1365
4	HVO14	-508	-1365	34	HVO44	392	1365
5	HVO13	-408	-1365	35	HVO43	292	1365
6	HVO12	-308	-1365	36	HVO42	192	1365
7	HVO11	-208	-1365	37	HVO41	92	1365
8	HVO10	-108	-1365	38	HVO40	-8	1365
9	HVO9	-8	-1365	39	HVO39	-108	1365
10	HVO8	92	-1365	40	HVO38	-208	1365
11	HVO7	192	-1365	41	HVO37	-308	1365
12	HVO6	292	-1365	42	HVO36	-408	1365
13	HVO5	392	-1365	43	HVO35	-508	1365
14	HVO4	512	-1365	44	HVO34	-608	1365
15	HVO3	632	-1365	45	HVO33	-708	1365
16	HVO2	732	-1365	46	HVO32	-808	1365
17	HVO1	1025	-1274	47	HVO31	-1025	650
18	VDISP	1025	-1106	48	HVO30	-1025	550
19	D-GND	1025	-612	49	HVO29	-1025	450
20	L-GND	1025	-403	50	HVO28	-1025	350
21	DIN	1025	-250	51	HVO27	-1025	250
22	CLK	1025	-150	52	HVO26	-1025	150
23	LS	1025	-50	53	HVO25	-1025	50
24	CL	1025	50	54	HVO24	-1025	-50
25	CHG	1025	150	55	HVO23	-1025	-150
26	VDD	1025	433	56	HVO22	-1025	-250
27	DOUT	1025	533	57	HVO21	-1025	-350
28	D-GND	1025	633	58	HVO20	-1025	-450
29	VDISP	1025	1106	59	HVO19	-1025	-550
30	HVO48	1025	1274	60	HVO18	-1025	-650

PACKAGE DIMENSIONS

(Unit: mm)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact ROHM's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL9271-01	Dec. 21, 2005	–	–	Preliminary edition 1
FEDL9271-01	Mar. 1, 2007	–	–	Final edition 1

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