LTM9013
300MHz Wideband/DPD Receiver

DESCRIPTION

Demonstration circuit DC1931 is a 300MHz wideband/digital pre-distortion (DPD) receiver subsystem featuring the LTM®9013. The DC1931 card is designed to plug into the DC1371 data acquisition demo board. It is configured with an IF highpass filter, designed to provide a corner frequency of approximately 1MHz. Other corner frequencies may be realized by changing a small number of element values on the DC1931; see the LTM9013 data sheet for details. The digital output can easily be analyzed with Linear Technology's PScope™ data processing software, which is available for no charge at http://www.linear.com.

Design files for this circuit board are available at http://www.linear.com/demo

QUICK START PROCEDURE

Validating the performance of the LTM9013 is simple with DC1931, and requires only two input sources, a clock source, a computer, and a lab power supply. The DC1931 demonstration circuit board should have the jumper settings as default positions (as per Table 1) which configures the ADC in serial programming mode. In the default configurations, JP1-JP4 should be left in the default locations. This will pull the SPI lines high through weak pull-up resistors so that the SPI commands can be sent from the PC. When JP1 is set to PAR, then jumpers JP2-JP4 can be configured manually. Refer to Figure 1 for proper board evaluation equipment setup and follow the procedure below:

1. Connect the power supply as shown in Figure 1. There are onboard low noise voltage regulators that provide the three supply voltages for the LTM9013. The entire board and all components share a common ground. The power supply should still be a low noise lab power supply capable of supplying at least 1A.

2. Provide an encode clock to the ADC via SMA connector J3. Use a low phase-noise clock source such as a filtered RF signal generator or a high quality clock oscillator.

Note: Similar to having a noisy input, a high jitter (phase noise) encode clock will degrade the signal-to-noise ratio (SNR) of the system.

3. Apply an RF input signal via SMA connector J1. For best results, use a low distortion, low noise signal generator with sufficient filtering to avoid degrading the performance of the receiver.

4. Apply an LO input signal via SMA connector J2. Note that the difference in frequency between this signal and the RF signal will be the baseband frequency resulting at the I and Q channels and ADC inputs.

Table 1: DC1931 Connectors and Jumpers

REFERENCE	FUNCTION
J1 (RF)	Board RF Signal Input. Impedance-Matched to 50Ω for Use with Lab Signal Generators.
J2 (LO)	Board LO Signal Input. Impedance-Matched to 50Ω for Use with Lab Signal Generators.
J3 (CLK)	Board Clock Input. Impedance-Matched to 50Ω. Drive with a Low Phase Noise Clock Oscillator or Filtered Sine Wave Signal Source.
J4 (digital data)	DC1371 Interface Connector.
JP1(I/0)	Selects Serial or Parallel Configuration Setting. Default is SER. (Refer to Data Sheet for Function of JP2-JP4 in Serial Mode.)
JP2 (CLK Stabilizer)	Enables Clock Duty Cycle Stabilizer. Default is Disable.
JP3 (ADC Sleep)	Sets ADC Sleep mode. Default is RUN.
JP4 (LVDS Current)	Selects LVDS Output Current. Default is 3.5mA
JP5 (Amp Run)	Enables IF Amplifier. Default is EN.
JP6 (I/Q Enable)	Enables I/Q Demodulator. Default is EN.
JP7 (IP2 Adjust)	Enables IP2 Adjust. Default is Disable.
JP8 (Write Enable)	Enables/Disables Writing to the EEPROM. Default is EN.

QUICK START PROCEDURE

5. Observe the ADC output with demo circuit DC1371, a USB cable, a Windows computer, and Linear Technology's PScope data processing software.
6. Note the IF gain of the LTM9013 may be adjusted using R25 (I channel), and R31 (Q channel).
7. The 2nd order linearity of the LTM9013 may be adjusted over a limited range by first setting JP7 to the EN position, and then using R15 (I channel) and R7 (Q channel).

Using PScope Software

PScope, downloadable from Linear Technology's website http://www.linear.com/software, processes data from the DC1371 data acquisition board and displays FFT and signal analysis information on the computer screen.

The onboard EEPROM U5 should enable automatic board detection and auto-configuration of the software, but if the user wishes to change the settings, they can easily do so. From the Configure menu in the toolbar, uncheck "Autodetect Device". The default settings for DC1931 are shown in Figure 2.

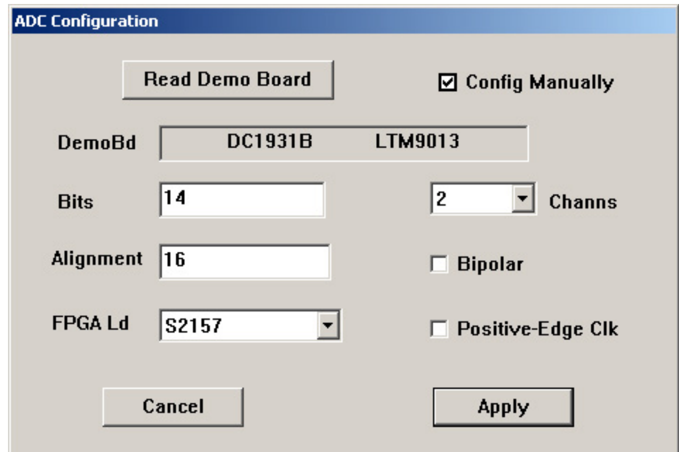


Figure 2. Entering the Correct Device Information for Your ADC. Select the Correct Parameters for the DC1931. Under Normal Conditions, PScope Should Automatically Recognize the Board and Adjust the Software Settings Accordingly

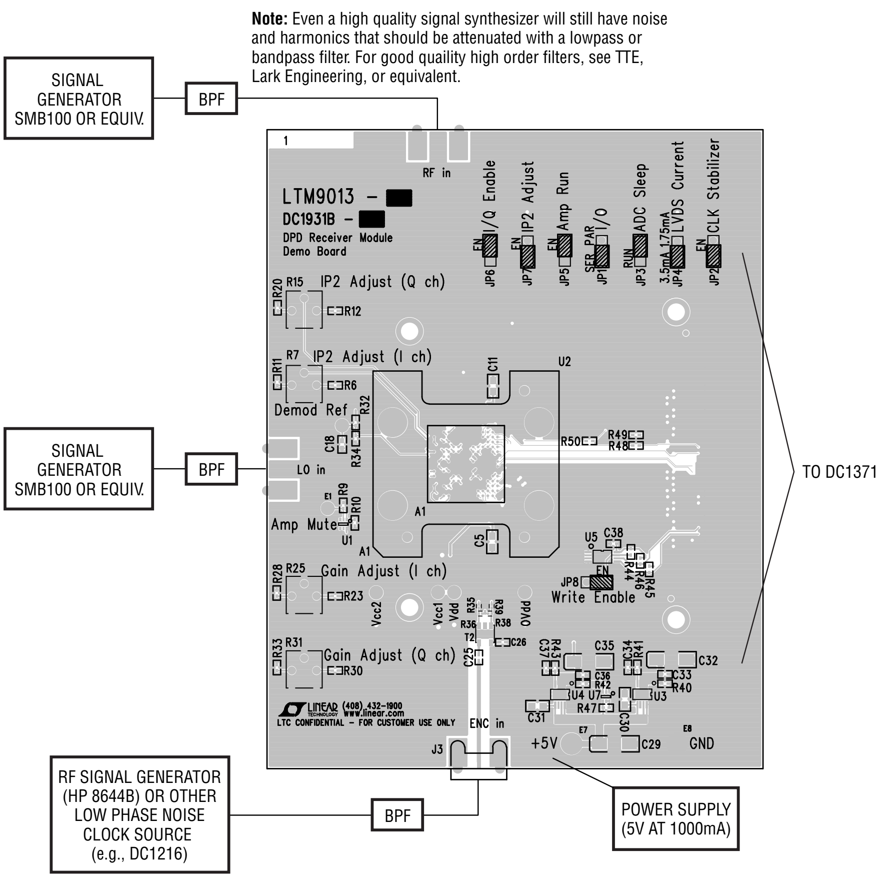
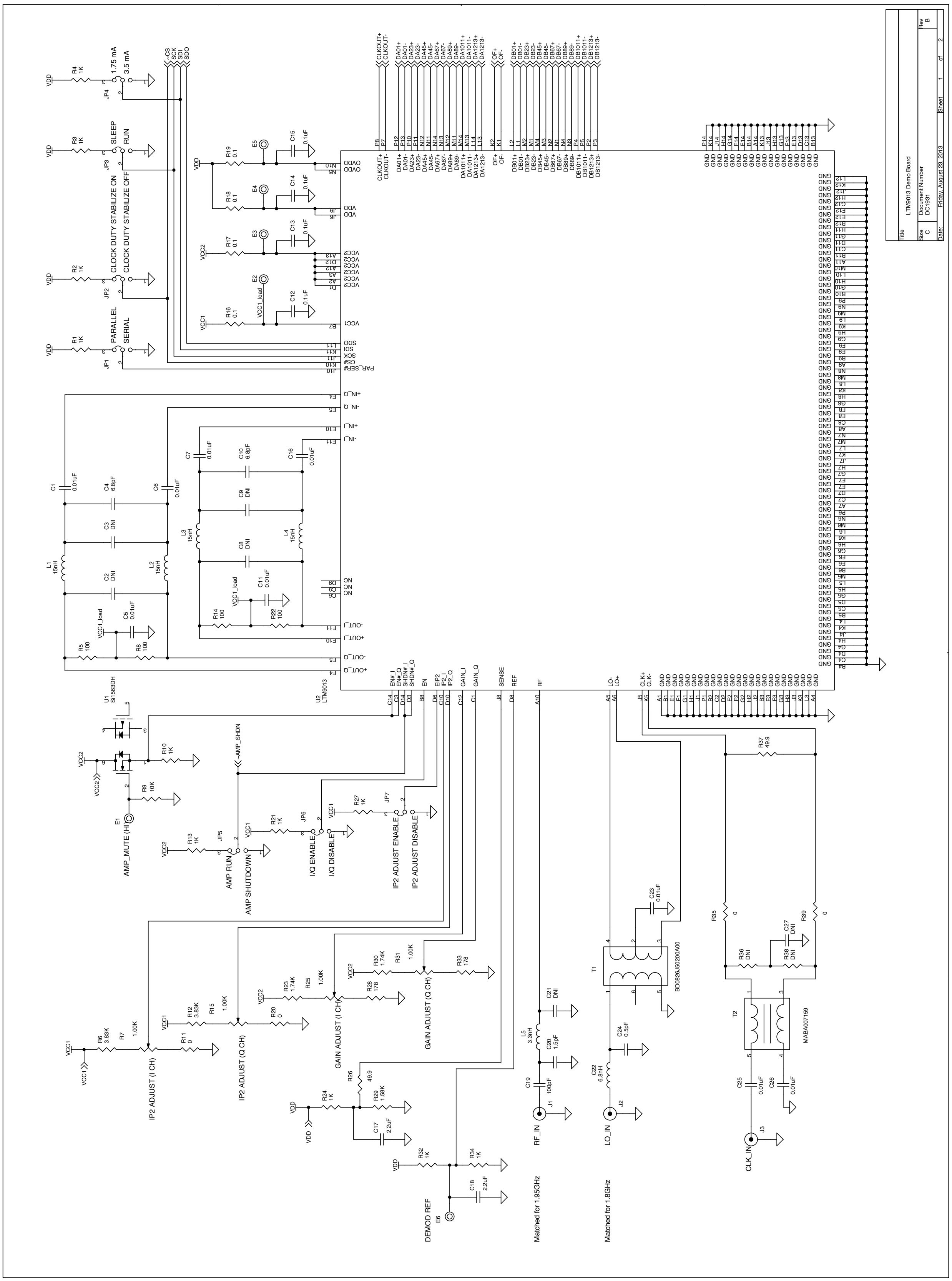


Figure 1. Proper Measurement Equipment Setup

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	9	C12-C15, C33, C34, C36-C38	CAP, X5R, 0.1µF, 10V, 10%, 0402	AVX, 0402ZD104KAT2A
2	3	C29, C32, C35	CAP, TANT, 47µF, 10V, 10%, C 6032	VISHAY/293D476X9010C2TE3
3	1	C19	CAP, C0G, 100pF, 25V, 1%, 0402	AVX, 04023A101FAT
4	0	C21, C27, R36, R38	CAP, DNI, 0402	
5	0	C2, C3, C8, C9	CAP, DNI, 0805	
6	2	C17, C18	CAP, X7R, 2.2µF, 6.3V, 10%, 0603	AVX, 06036C225KAT2A
7	2	C31, C30	CAP, X5R, 4.7µF, 10V, 20%, 0805	AVX, 0805ZD475MAT2A
8	7	C1, C6, C7, C16, C23, C25, C26	CAP, X7R, 0.01µF, 16V, 10%, 0402	AVX, 0402YC103KAT2A
9	2	C5, C11	CAP, X7R, 0.01µF, 16V, 10%, 0805	AVX, 0805YC103KAT2A
10	1	C20	CAP, C0G, 1.5pF, 25V, 1%, 0402	AVX, 04023A1R5FAT
11	2	C4, C10	CAP, C0G, 6.8pF, 25V, 1%, 0402	AVX, 04023A6R8FAT
12	1	C24	CAP, C0G, 0.5pF, 25V, 1%, 0402	AVX, 04023A0R5FAT
13	1	J4	CONN., SNGL-END ARRAY MALE 160POS	SAMTEC, ASP-134606-01
14	8	JP1-JP8	HEADER, 3X1, 2mm	SULLIN, NRPN031PAEN-RC
15	8	JP1-JP8	SHUNT	SAMTEC, 2SN-BK-G
16	3	J1, J2, J3	CONN, SMA, 50Ω EDGE-LAUNCH	E.F.JOHNSON, 142-0701-851
17	4	R11, R20, R35, R39	RES, 0Ω JUMPER, 0402	VISHAY, CRCW04020000Z0ED
18	1	C22	IND, 6.8nH, 5%, 0402	TOKO, LL1005-FHL6N8J
19	1	L5	IND, 3.3nH, 5%, 0402	TOKO, LL1005-FHL3N3J
20	4	L1, L2, L3, L4	IND, 15nH, 5%, 0402	TOKO, LL1005-FHL15NJ
21	2	R6, R12	RES, 3.83k, 1%, 1/16, 0402	VISHAY, CRCW04023K83FKED
22	1	R29	RES, 1.58k, 1%, 1/16, 0402	VISHAY, CRCW04021K58FKED
23	4	R5, R8, R14, R22	RES, 100Ω, 1%, 1/16, 0603	VISHAY, CRCW0603100RFKED
24	4	R16, R17, R18, R19	RES, 0.1Ω, 1%, 1/10, 0603	VISHAY, WSL0603R1000FEA
25	1	R43	RES, 182k, 1%, 1/10, 0603	VISHAY, CRCW0603182KFKEA
26	2	R33, R28	RES, 178Ω, 1%, 1/16, 0402	VISHAY, CRCW0402178RFKED
27	2	R26, R37	RES, 49.9Ω, 1%, 1/20, 0201	VISHAY, CRCW020149R9FKED
28	4	R9, R44, R45, R46	RES, 10k, 1%, 1/16, 0402	VISHAY, CRCW040210K0FKED
29	4	R7, R15, R25, R31	POT., TRIMMER, 1kΩ 1/4” SQ CERM SL ST	BOURNS, 3362P-1-102TLF
30	2	R23, R30	RES, 1.74k, 1%, 1/16, 0402	VISHAY, CRCW04021K74FKED
31	2	R42, R40	RES, 3.00k, 1%, 1/16, 0402	VISHAY, CRCW04023K00FKED
32	12	R1, R2, R3, R4, R10, R13, R21, R24, R27, R32, R34, R47	RES, 1k, 5%, 1/16, 0402	VISHAY, CRCW04021K00JNED
33	1	R41	RES, 330K OHM, 1%, 1/10, 0603	VISHAY, CRCW0603330KFKEA
34	1	T2	TRANSFORMER, RF, SMT, 1:1 BALUN	MA COM, MABA-007159-000000
35	1	T1	TRANSFORMER, RF, SMT, 4:1 BALUN	ANAREN, BD0826J50200A00
36	6	E1, E2, E3, E4, E5, E6	TURRET, 0.063	MILL-MAX, 2308-02-00-80-00-00-07-0
37	2	E7, E8	TURRET, 0.094	MILL-MAX, 2501-02-00-80-00-00-07-1
38	2	U7, U1	IC, CMOS FET, SI1563DH	VISHAY SILICONIX, SI1563DH
39	2	U4, U3	IC, VREG,ADJ,1.1A,DD8	LINEAR TECH, LT3080EDD#PBF
40	1	U5	IC EEPROM 32KBIT 400KHZ 8TSSOP	MICROCHIP, 24LC32A-I/ST
41	1	U2	MODULE, LTM9013IY	LINEAR TECH, LTM9013IY
42	1		FAB, PCB, DC1931B	DEMO CIRCUIT DC1931B
43	1		STENCIL SET, DC1931B	STENCIL DC1931B

SCHEMATIC DIAGRAM



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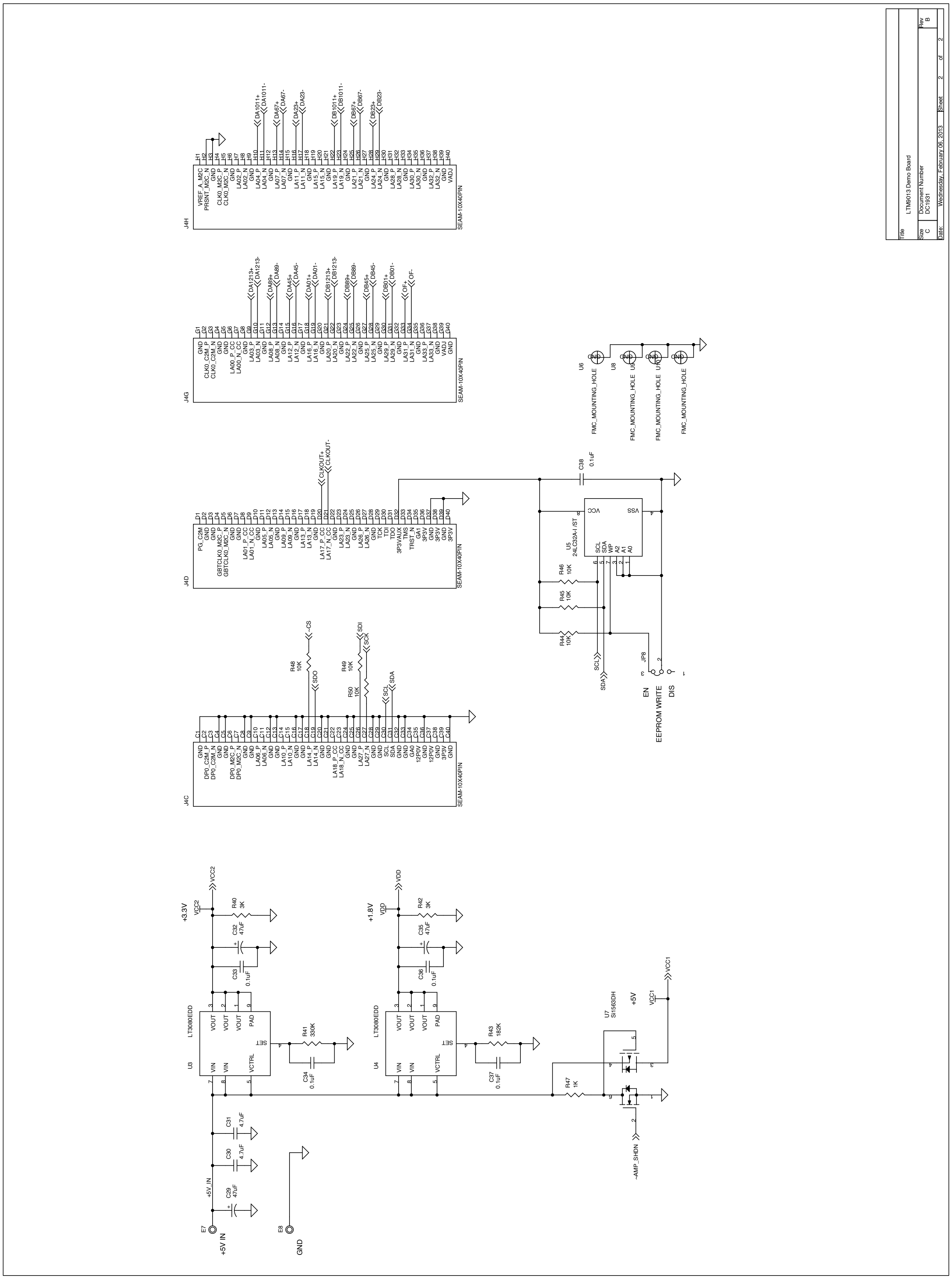

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