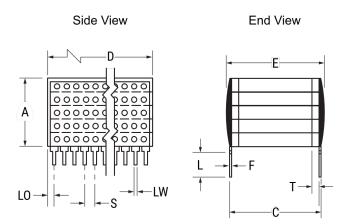




KPS LDD Comm SMPS, Ceramic, 75 uF, 10%, 50 VDC, BX, N/A



Click here for the 3D model.

Dimensions	
D	25.715mm +/-1.585mm
L	6.35mm MIN
Т	1.397mm MAX
S	2.54mm TYP
F	0.254mm +/-0.051mm
Α	16.51mm MAX
С	11.43mm +/-0.635mm
Е	12.7mm NOM
G	1.4mm +/-0.25mm
LO	1.586mm MAX
LW	0.508mm +/-0.051mm

Packaging Specifications	
Packaging	Waffle, Box
Packaging Quantity	28

General Information		
Series	KPS LDD Comm SMPS	
Style	Leaded Stacked Chip	
Description	Low ESR, High Current Stacked Ceramic Chips	
Features	Low ESR, High Current, High Performance	
RoHS	No	
Prop 65	▲ WARNING: Cancer and reproductive harm - http://www.p65warnings.ca.gov.	
SCIP Number	4221181d-d71c-4d0a-af45-5eab760732b2	
Termination	60/40 Solder Coated	
Lead	Wire Leads	
Failure Rate	N/A	
Testing and Reliability	Commercial	
AEC-Q200	No	
Notes	Note: Number of chips in stack depends on design. Number of Chips in this stack = 5. Note: Lead alignment within pin rows shall be within ±.0.13 mm.	

Specifications	
Capacitance	75 uF
Capacitance Tolerance	10%
Voltage DC	50 VDC
Dielectric Withstanding Voltage	125 VDC
Temperature Range	-55/+125°C
Temperature Coefficient	BX
Dissipation Factor	2.5% 1 kHz 25C
Aging Rate	1% Loss/Decade Hour
Insulation Resistance	1.3 GOhms

Statements of suitability for certain applications are based on our knowledge of typical operating conditions for such applications, but are not intended to constitute - and we specifically disclaim - any warranty concerning suitability for a specific customer application or use. This Information is intended for use only by customers who have the requisite experience and capability to determine the correct products for their application. Any technical advice inferred from this Information or otherwise provided by us with reference to the use of our products is given gratis, and we assume no obligation or liability for the advice given or results obtained.