

IV1Q12160T4 – 1200V 160mΩ SiC MOSFET

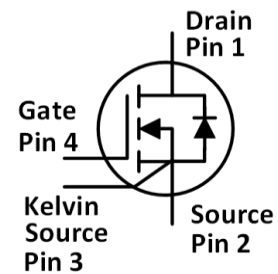
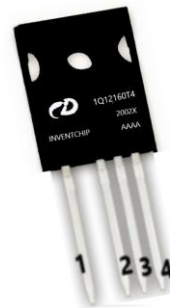
Features:

- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- High operating junction temperature capability
- Very fast and robust intrinsic body diode
- Kelvin gate input easing driver circuit design

Applications:

- Solar inverters
- UPS
- Motor drivers
- High voltage DC/DC converters
- Switch mode power supplies

Package:



Part Number	Package
IV1Q12160T4	TO247-4

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DS}	Drain-Source voltage	1200	V	$V_{GS}=0\text{V}$, $I_D=100\mu\text{A}$	
V_{GS}	Gate-Source voltage	-5 to 20	V	Recommended maximum	
I_D	Drain current (continuous)	20	A	$V_{GS}=20\text{V}$, $T_c=25^\circ\text{C}$	Fig. 21
		16	A	$V_{GS}=20\text{V}$, $T_c=100^\circ\text{C}$	
I_{DM}	Drain current (pulsed)	50	A	Pulse width limited by SOA	Fig. 24
P_{TOT}	Total power dissipation	138	W	$T_c=25^\circ\text{C}$	Fig. 22
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$		
T_J	Operating junction temperature	-55 to 175	$^\circ\text{C}$		
T_L	Solder Temperature	260	$^\circ\text{C}$	Wave soldering only allowed at leads, 1.6mm from case for 10 s	

Thermal Data

Symbol	Parameter	Value	Unit	Note
$R_{\theta(j-c)}$	Thermal Resistance from Junction to Case	1.088	$^\circ\text{C}/\text{W}$	Fig. 23

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
I_{DSS}	Zero gate voltage drain current		5	100	μA	$V_{DS}=1200\text{V}, V_{GS}=0\text{V}$	
I_{GSS}	Gate leakage current		1	± 100	nA	$V_{DS}=0\text{V}, V_{GS}=-5\sim 20\text{V}$	
V_{TH}	Gate threshold voltage		2.9		V	$V_{GS}=V_{DS}, I_D=1.9\text{mA}$	Fig. 8, 9
			1.9			$V_{GS}=V_{DS}, I_D=1.9\text{mA}$ @ $T_c=175^\circ\text{C}$	
R_{ON}	Static drain-source on-resistance		160	195	$\text{m}\Omega$	$V_{GS}=20\text{V}, I_D=10\text{A}$ @ $T_j=25^\circ\text{C}$	Fig. 4, 5, 6, 7
			250		$\text{m}\Omega$	$V_{GS}=20\text{V}, I_D=10\text{A}$ @ $T_j=175^\circ\text{C}$	
C_{iss}	Input capacitance		885		pF	$V_{DS}=800\text{V}, V_{GS}=0\text{V},$ $f=1\text{MHz}, V_{AC}=25\text{mV}$	Fig. 16
C_{oss}	Output capacitance		38		pF		
C_{rss}	Reverse transfer capacitance		2		pF		
E_{oss}	C_{oss} stored energy		16		μJ		Fig. 17
Q_g	Total gate charge		43		nC	$V_{DS}=800\text{V}, I_D=10\text{A},$ $V_{GS}=-5\text{ to }20\text{V}$	Fig. 18
Q_{gs}	Gate-source charge		9		nC		
Q_{gd}	Gate-drain charge		19		nC		
R_g	Gate input resistance		9.5		Ω	$f=1\text{MHz}$	
E_{ON}	Turn-on switching energy		139.3		μJ	$V_{DS}=800\text{V}, I_D=10\text{A},$ $V_{GS}=-2\text{ to }20\text{V},$ $R_{G(\text{ext})}=5.1\Omega,$ $L=450\mu\text{H}$	Fig. 19, 20
E_{OFF}	Turn-off switching energy		39.2		μJ		
$t_{d(\text{on})}$	Turn-on delay time		6.4		ns		
t_r	Rise time		19.4				
$t_{d(\text{off})}$	Turn-off delay time		11.8				
t_f	Fall time		14				

Reverse Diode Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
V_{SD}	Diode forward voltage		4.1		V	$I_{SD}=5A, V_{GS}=0V$	Fig. 10, 11, 12
			3.7		V	$I_{SD}=5A, V_{GS}=0V,$ $T_J=175^\circ\text{C}$	
t_{rr}	Reverse recovery time		33.2		ns	$V_{GS}=-2V/+20V,$ $I_{SD}=10A, V_R=800V,$ $di/dt=1000A/\mu s,$	
Q_{rr}	Reverse recovery charge		101.5		nC		
I_{RRM}	Peak reverse recovery current		5.6		A	$R_{G(ext)}=13.0\Omega$	

Typical Performance (curves)

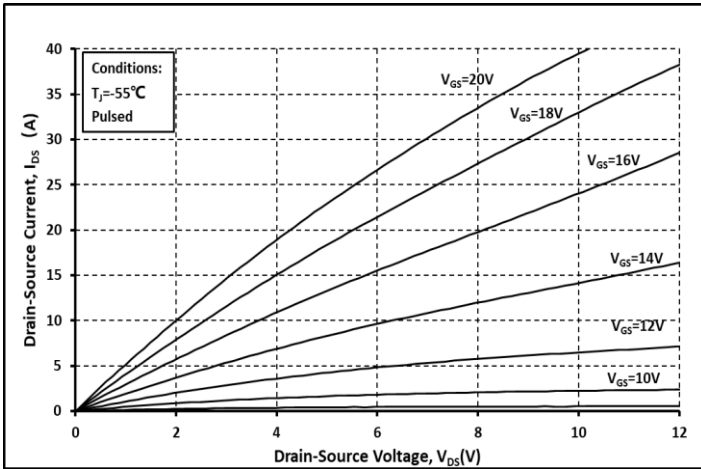


Fig. 1 Output Curve @ $T_j = -55^\circ\text{C}$

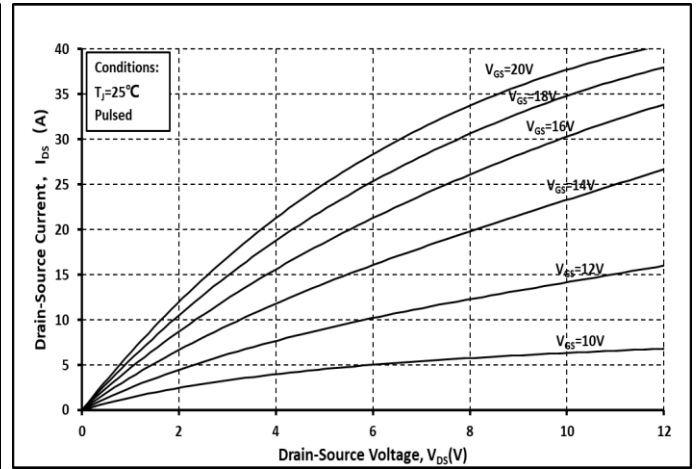


Fig. 2 Output Curve @ $T_j = 25^\circ\text{C}$

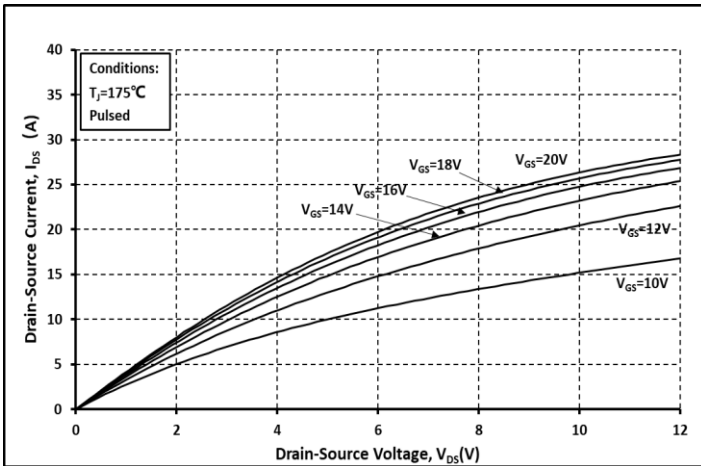


Fig. 3 Output Curve @ $T_j = 175^\circ\text{C}$

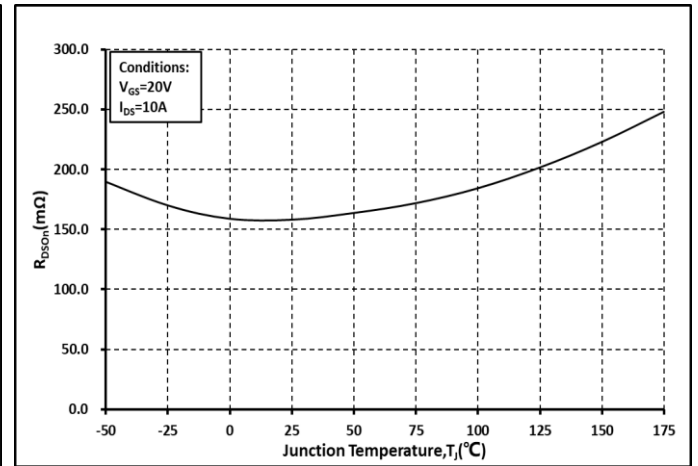


Fig. 4 R_{on} vs. Temperature

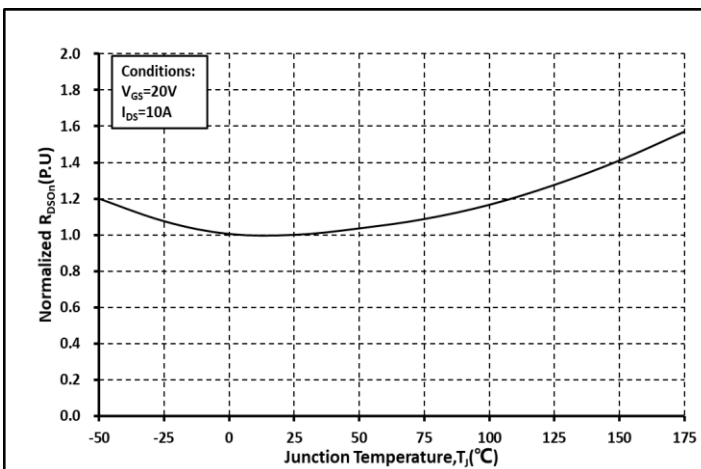


Fig. 5 Normalized R_{on} vs. Temperature

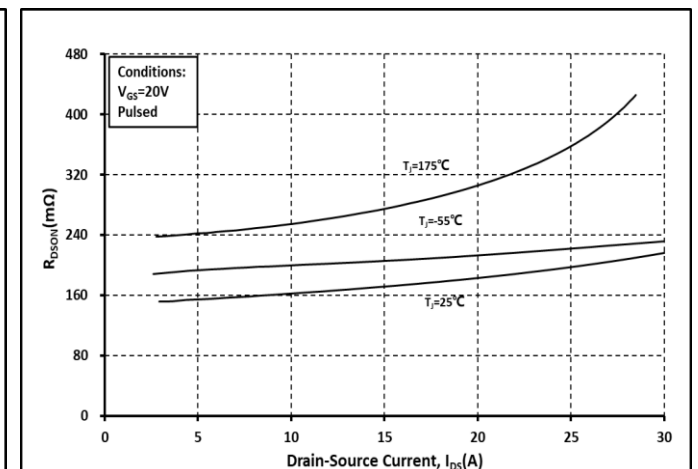


Fig. 6 R_{on} vs. I_{DS} @ Various Temperature

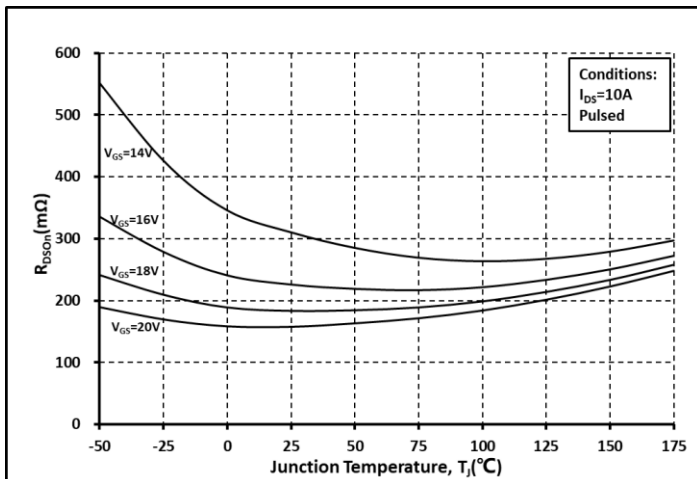


Fig. 7 Ron vs. Temperature @ Various V_{GS}

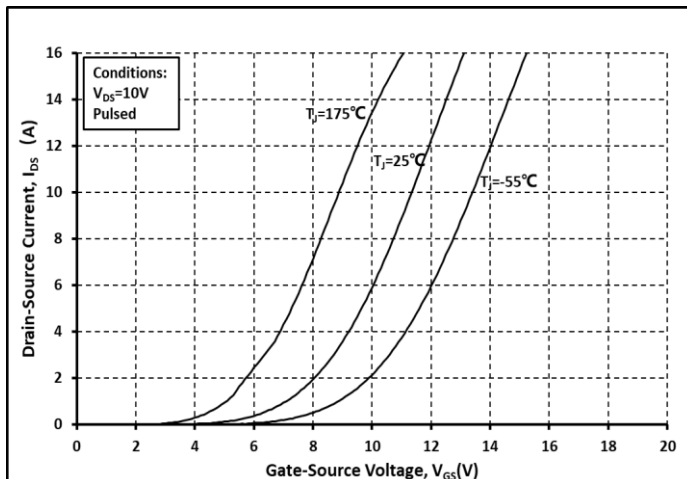


Fig. 8 Transfer Curves @ Various Temperature

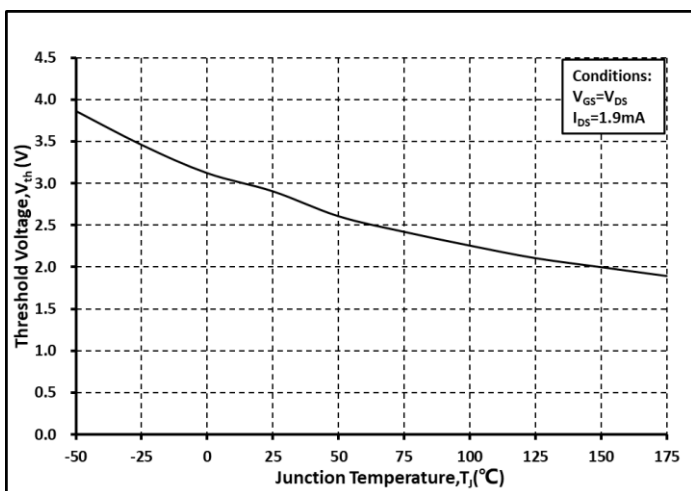


Fig. 9 Threshold Voltage vs. Temperature

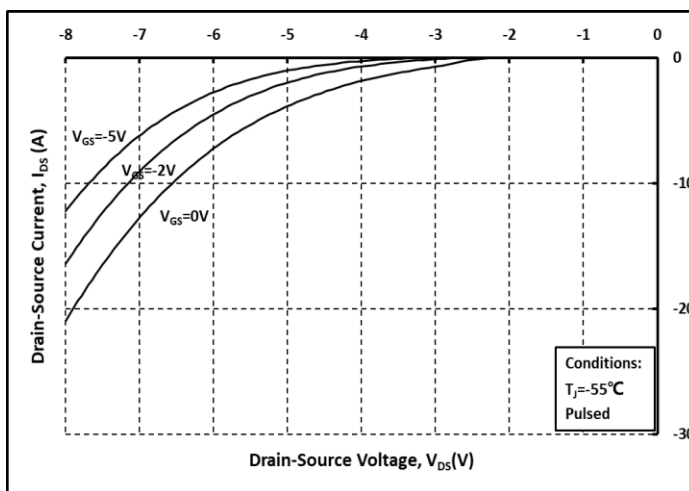


Fig. 10 Body Diode Curves @ $T_J = -55^\circ\text{C}$

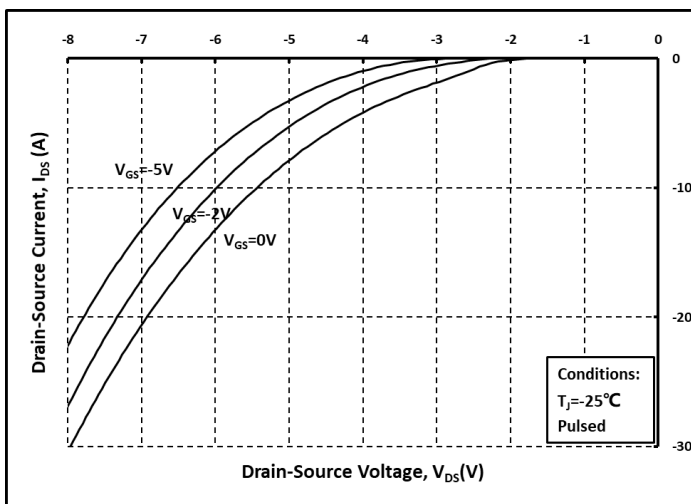


Fig. 11 Body Diode Curves @ $T_J = 25^\circ\text{C}$

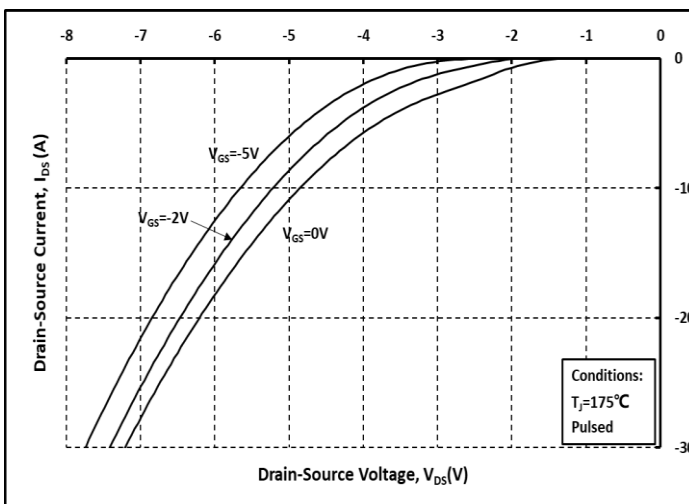


Fig. 12 Body Diode Curves @ $T_J = 175^\circ\text{C}$

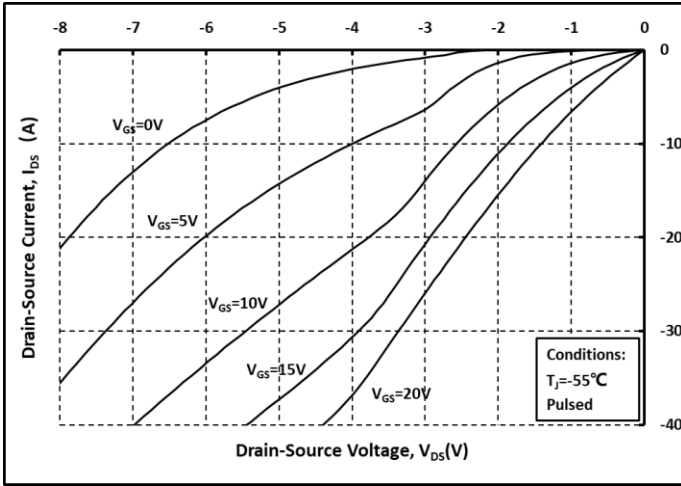


Fig. 13 3rd Quadrant Curves @ $T_j = -55^\circ\text{C}$

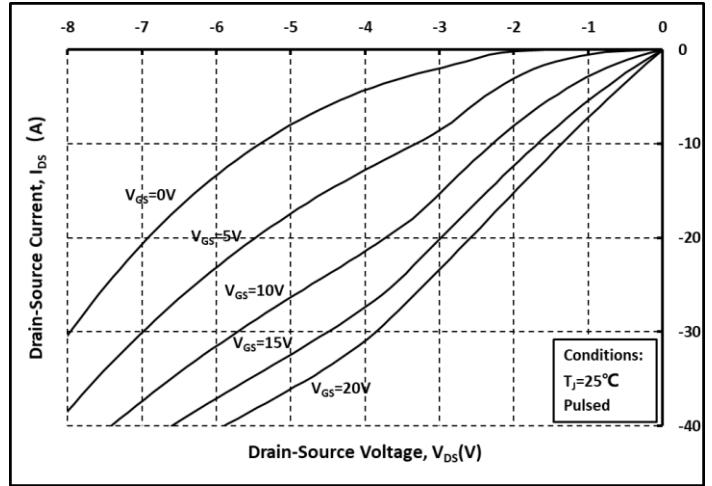


Fig. 14 3rd Quadrant Curves @ $T_j = 25^\circ\text{C}$

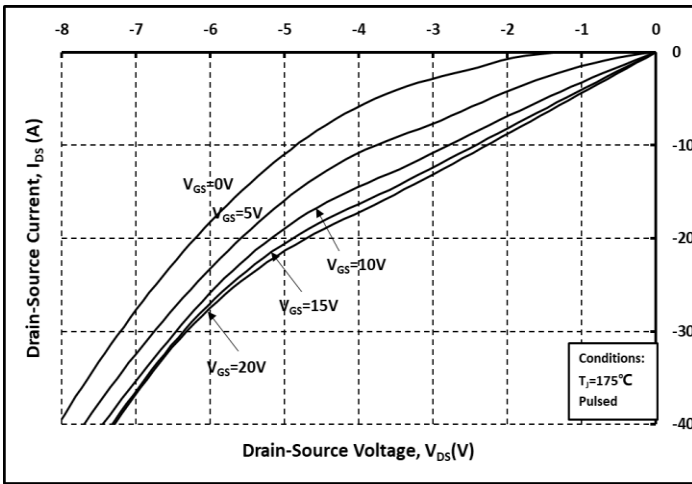


Fig. 15 3rd Quadrant Curves @ $T_j = 175^\circ\text{C}$

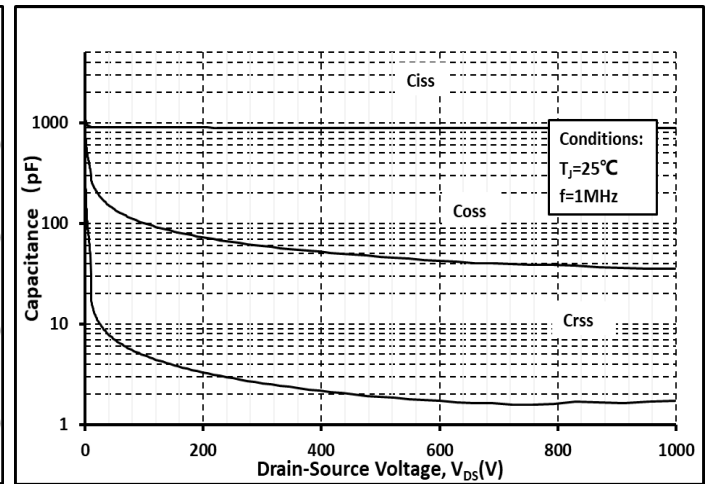


Fig. 16 Capacitance vs. V_{DS}

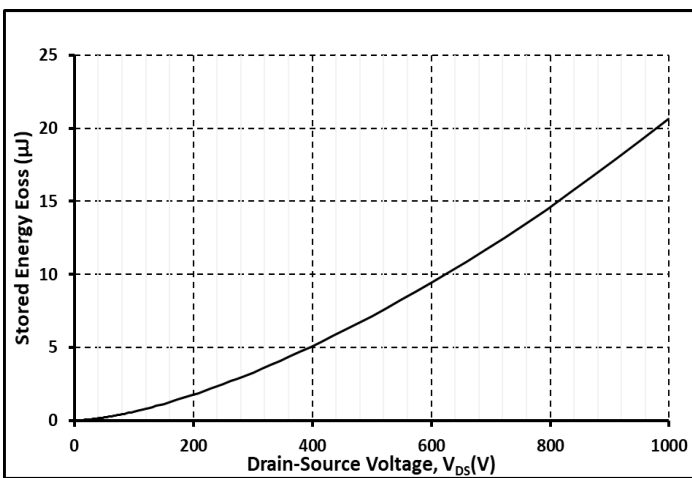


Fig. 17 Output Capacitor Stored Energy

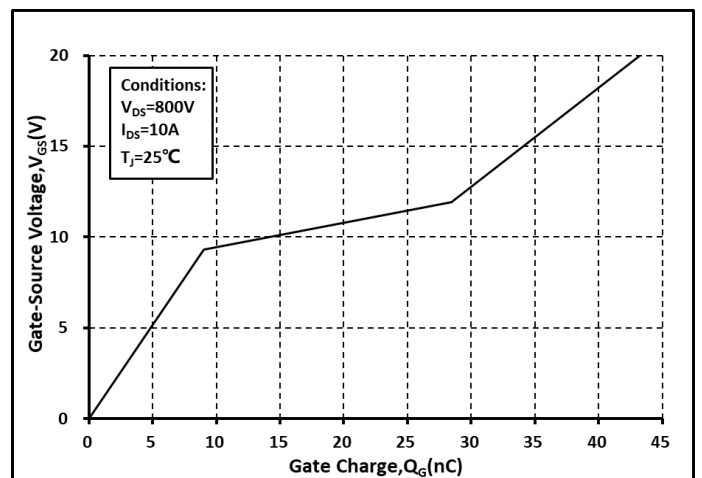


Fig. 18 Gate Charge Characteristics

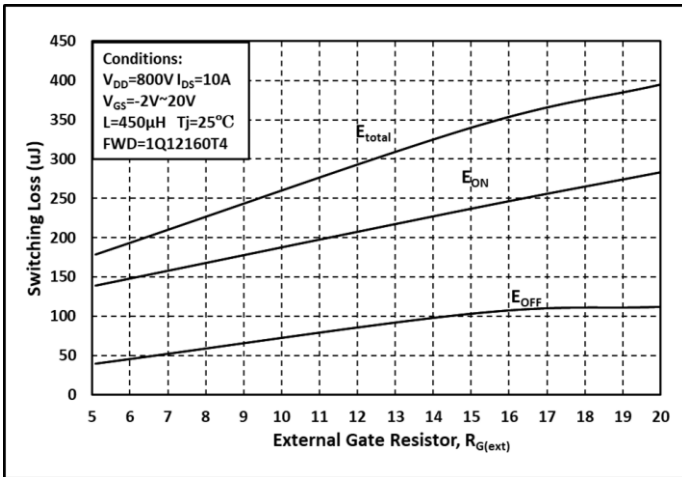


Fig. 19 Switching Energy vs. $R_{G(ext)}$

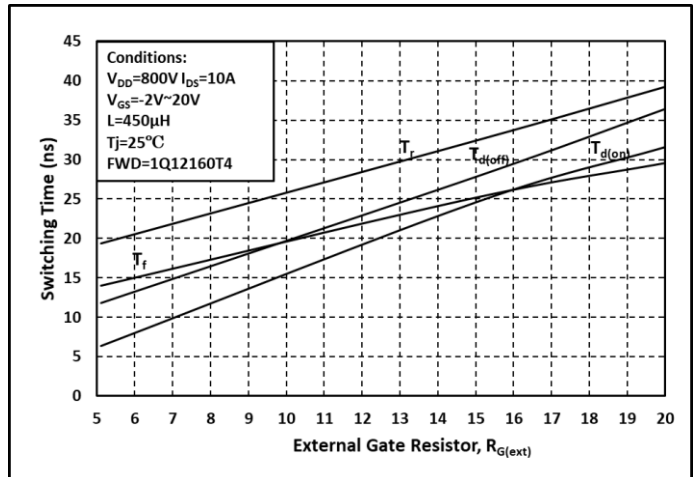


Fig. 20 Switching Times vs. $R_{G(ext)}$

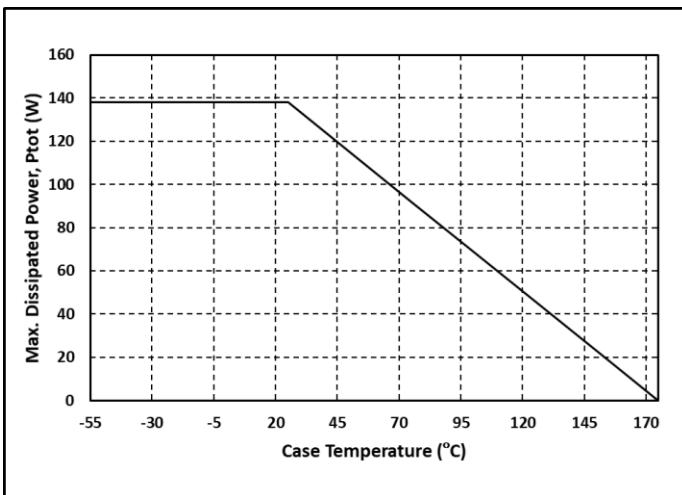


Fig. 21 Continuous Drain Current vs. Case Temperature

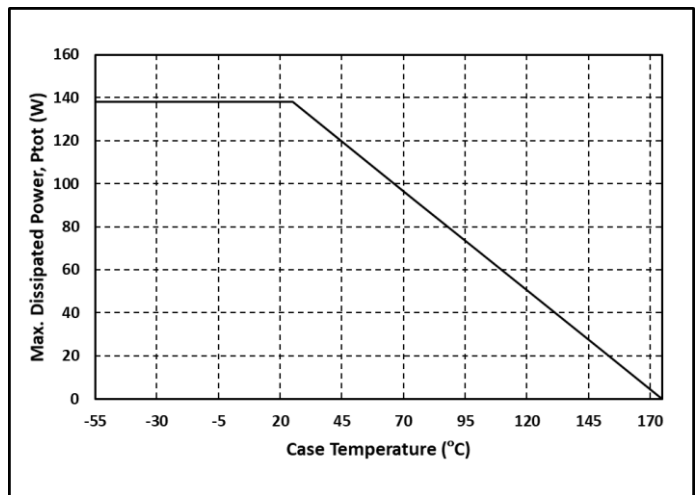


Fig. 22 Max. Power Dissipation Derating vs. Case Temperature

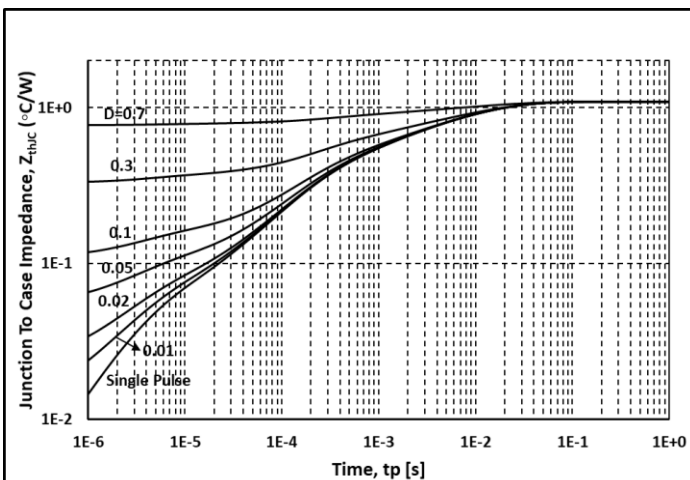


Fig. 23 Thermal Impedance

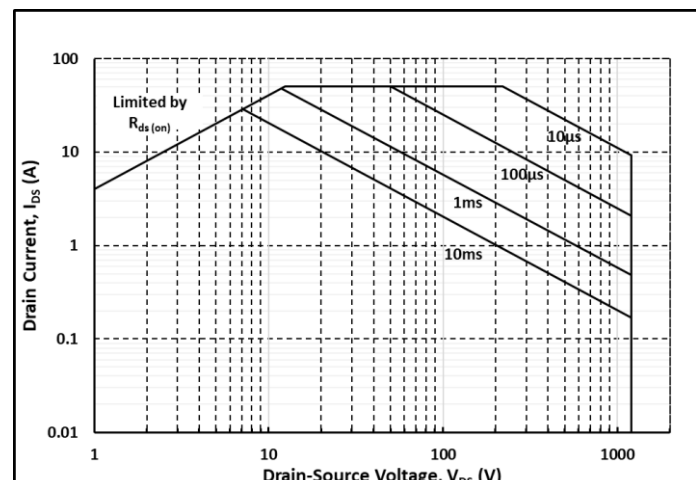
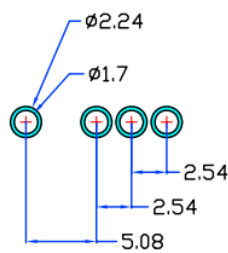
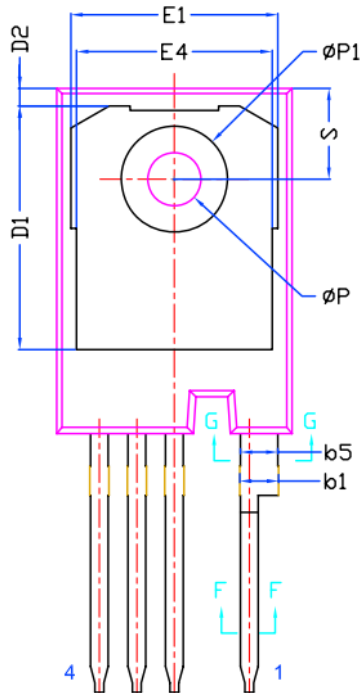
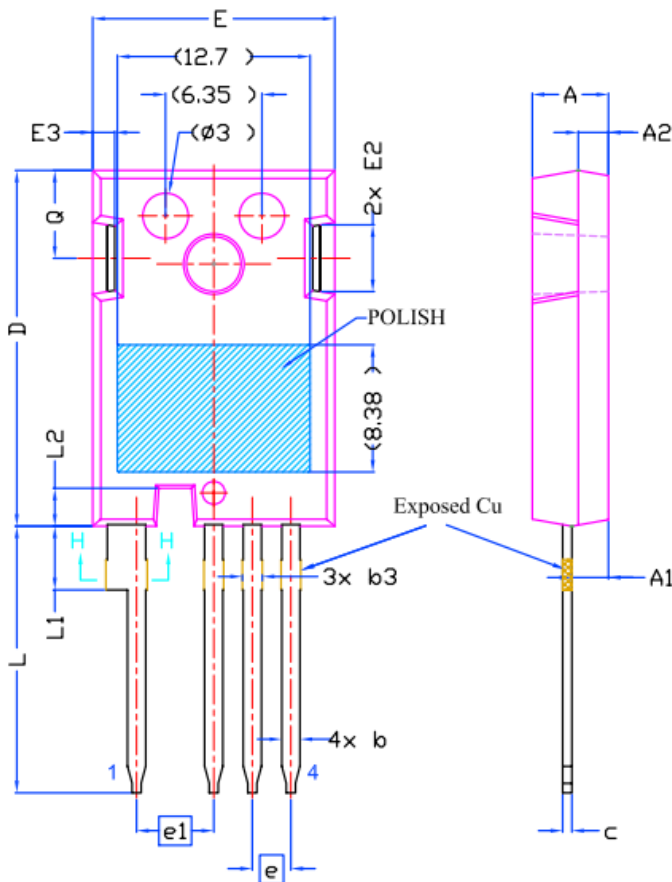
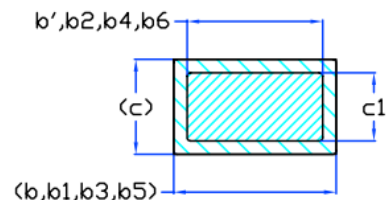


Fig. 24 Safe Operating Area

Package Dimensions



Recommended Solder Pad Layout



Section F--F, G--G, H--H

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	4.83	5.02	5.21
A1	2.29	2.41	2.54
A2	1.91	2.00	2.16
b'	1.07	1.20	1.28
b	1.07	1.20	1.33
b1	2.39	2.67	2.94
b2	2.39	2.67	2.84
b3	1.07	1.30	1.60
b4	1.07	1.30	1.50
b5	2.39	2.53	2.69
b6	2.39	2.53	2.64
c	0.55	0.60	0.68
c1	0.55	0.60	0.65
D	23.30	23.45	23.60
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
E	15.75	15.94	16.13
E1	13.10	14.02	14.15
E2	3.68	4.40	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
e	2.54 BSC		
e1	5.08 BSC		
L	17.31	17.57	17.82
L1	3.97	4.19	4.37
L2	2.35	2.50	2.65
øP	3.51	3.61	3.65
øP1	7.19 REF.		
Q	5.49	5.79	6.00
S	6.04	6.17	6.30

Note:

1. Package Reference: JEDEC TO247, Variation AD
2. All Dimensions are in mm
3. Slot Required, Notch May Be Rounded
4. Dimension D&E Do Not Include Mold Flash

Notes

Current revision is preliminary one, for further information please contact IVCT's Office.
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