Evaluating the ADMV4540, K Band Quadrature Demodulator with Integrated Fractional-N PLL and VCO

FEATURES

- Full feature evaluation board for the ADMV4540
- 5 V operation
- ACE software interface for SPI control

EVALUATION KIT CONTENTS

- ADMV4540-EVALZ evaluation board

EQUIPMENT NEEDED

- 5 V dc power supply
- 2 low noise 3.3 V dc power supplies
- RF signal generator
- Spectrum analyzer(s)
- Low phase noise RF signal generator
- SDP-S controller board
- 2 180° baluns

DOCUMENTS NEEDED

- ADMV4540 data sheet
- ADMV4540-EVALZ user guide (UG-2014)

SOFTWARE NEEDED

- **Analysis | Control | Evaluation (ACE)** software
- ACE Plug-in for the ADMV4540

ADMV4540-EVALZ EVALUATION BOARD PHOTOGRAPH

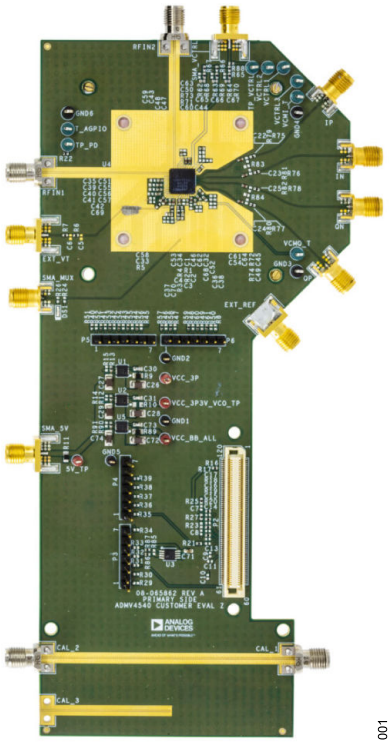


Figure 1.

GENERAL DESCRIPTION

The ADMV4540-EVALZ evaluation board incorporates the ADMV4540 with low noise low dropout (LDO) regulators for 5 V operation. The digital logic can be controlled using the ACE software via the SDP-S microcontroller, which connects with the ADMV4540-EVALZ. The ADMV4540-EVALZ has the option of using either of the two RF inputs (RF_INx). The baseband gain can be controlled using the VCTRL inputs (VCTRL_BBVVAx). The four outputs (QOUTP, QOUTN, IOUTN, and IOUTP) of the ADMV4540 are ac-coupled, and a balun is required for each channel to combine the differential signals.

For full details on the ADMV4540, see the ADMV4540 data sheet, which should be consulted in conjunction with this ADMV4540-EVALZ evaluation board user guide when using this evaluation board.

TABLE OF CONTENTS

Features..... 1
Evaluation Kit Contents..... 1
Equipment Needed.....1
Documents Needed.....1
Software Needed.....1
ADMV4540-EVALZ Evaluation Board Photograph 1
General Description.....1
Evaluation Board Hardware.....3
Evaluation Board Software Quick Start Procedures..... 5
Installing the ACE Software and ADMV4540 Plug-Ins and Drivers.....5
Initial Setup.....5
ADMV4540 Block Diagram and Its Functions..... 7
Using the ADMV4540 CSV Table.....10
Test Results..... 11
Evaluation Board Schematics and Artwork..... 13
Ordering Information.....22
Bill of Materials.....22
Notes.....23

REVISION HISTORY

10/2021—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

The ADMV4540-EVALZ comes with an ADMV4540 chip, and Figure 2 shows the location of this chip on the ADMV4540-EVALZ and the block diagram of the ADMV4540.

The ADMV4540-EVALZ has two RF inputs (RFIN1 and RFIN2) for direct down conversion to four outputs (IP, IN, QN, and QP).

To turn on the ADMV4540-EVALZ, connect the 5 V test point to a 5 V dc power supply and the GND test point to ground. Alternatively, connect the 5 V supply through a coax to the SMA_5V connector. Connect a second dc supply through a coax to the SMA_VCTRL coax connector and set at 0 V (minimum gain). Connect a third dc supply to the VCTRL1 test point and a GND test point to ground. Consult the ADMV4540 data sheet to vary the conversion gain as needed.

For serial peripheral interface (SPI) control, connect the SDP-S board to ADMV4540 P2 connector and then connect a microUSB to USB cable to the SDP-S and the computer. When connected to the computer, the green LED on the SDP-S board turns on.

Connect a signal generator set at 50 MHz, 0 dBm to the EXT_REF coax connector to set the external reference. Connect a 180° balun to IP and IN, and then connect the output to a spectrum analyzer, oscilloscope, or analog-to-digital converter (ADC). Connect another 180° balun to the QP and QN connector, and then connect the output of the balun to another spectrum analyzer, oscilloscope, or ADC.

Finally, connect an RF signal generator to either the RFIN1 or RFIN2, 2.92 mm coax connector.

Figure 3 and Figure 4 show the lab bench setups for the ADMV4540-EVALZ RFINx inputs. Note that I_OUT is the combination of IP and IN, and Q_OUT is the combination of QP and QN in Figure 3 and Figure 4.

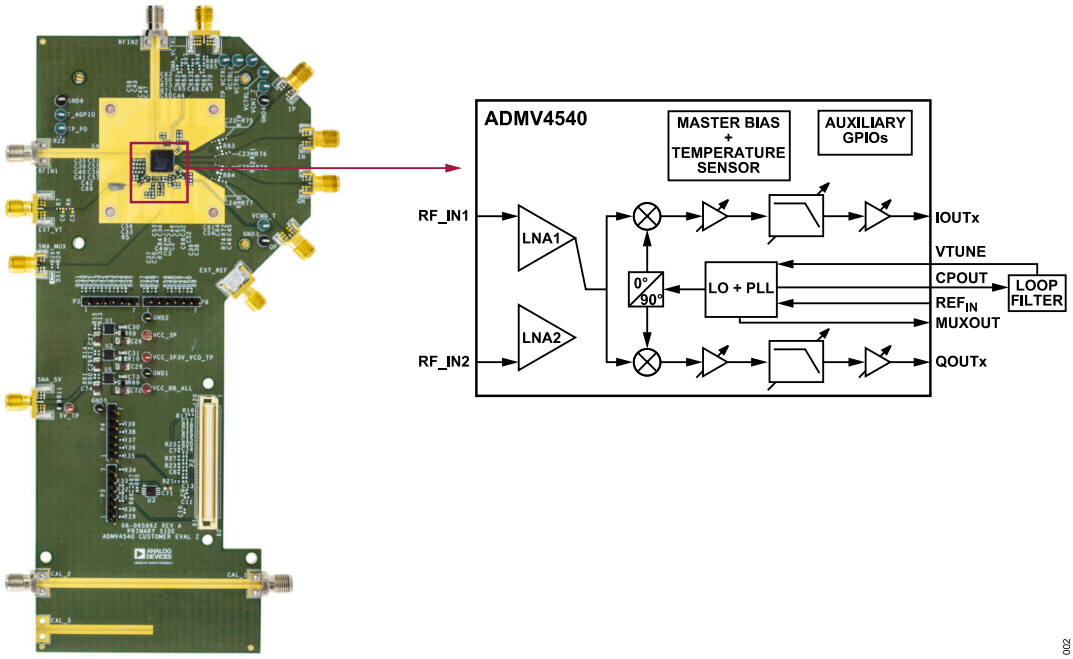


Figure 2. Evaluation Board Configuration

EVALUATION BOARD HARDWARE

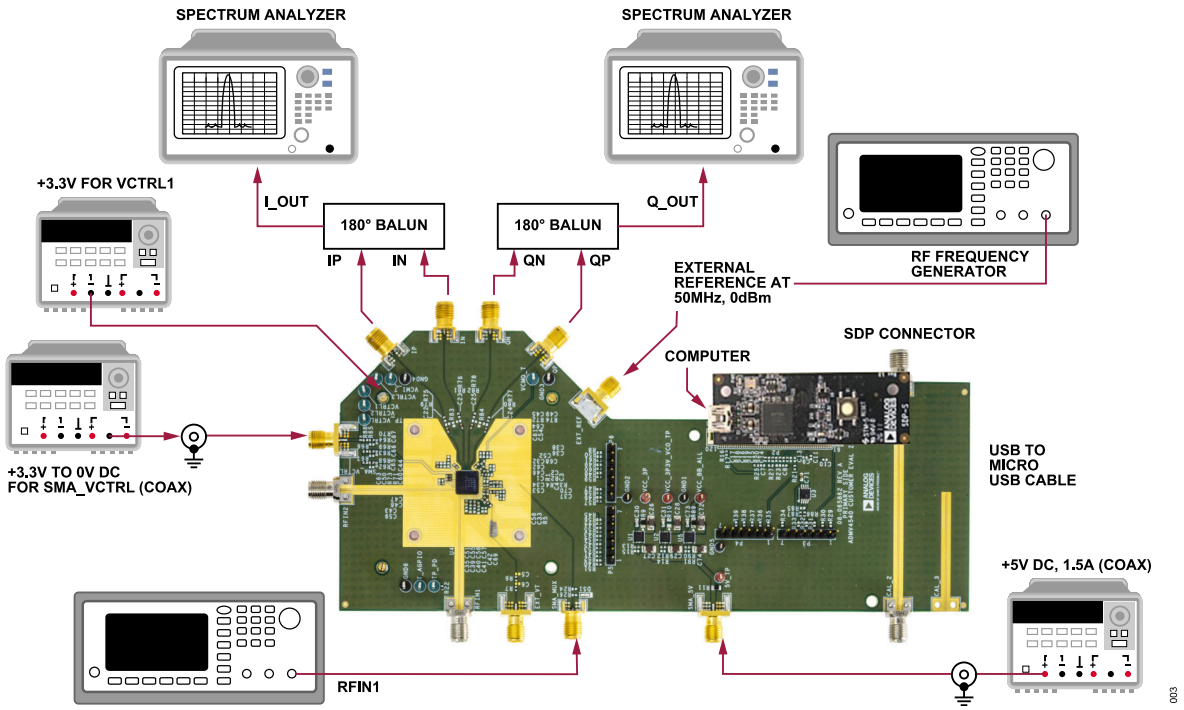


Figure 3. ADMV4540 Lab Bench Setup for the RFIN1 Input

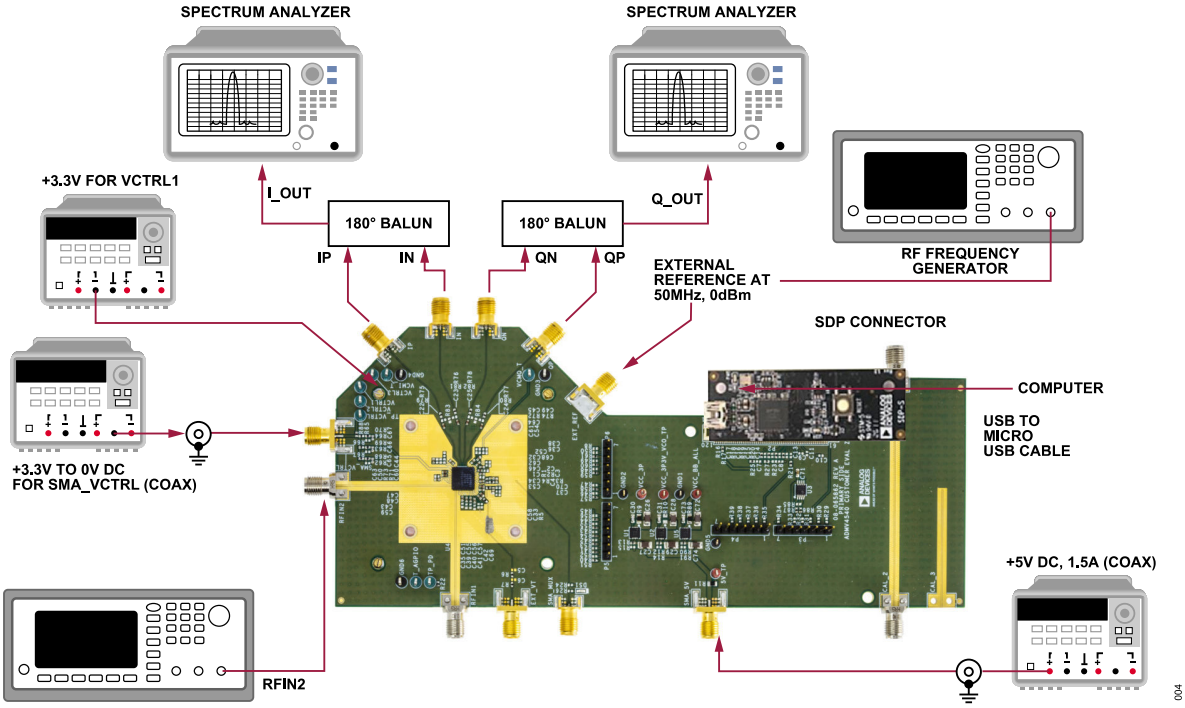


Figure 4. ADMV4540 Lab Bench Setup for the RFIN2 Input

EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE AND ADMV4540 PLUG-INS AND DRIVERS

The ADMV4540-EVALZ software uses the Analog Devices, Inc., Analysis|Control|Evaluation (ACE) software. For instructions on how to install and use the ACE software, go to www.analog.com/ACE.

If the ACE software has already been installed in the computer, make sure it is the latest version as on www.analog.com/ACE. If not, take the following steps:

1. Uninstall the current version of the ACE software on the computer.
2. Delete the ACE folder in **C:\ProgramData\Analog Devices**.
3. Install the latest version of the ACE software by following the instructions on the ACE software page. During installation, ensure that the **SDP Drivers**, **LRF Drivers**, and **.NET 4.8 Drivers** boxes are checked of under the **Select components to install: window** as well (see Figure 5).

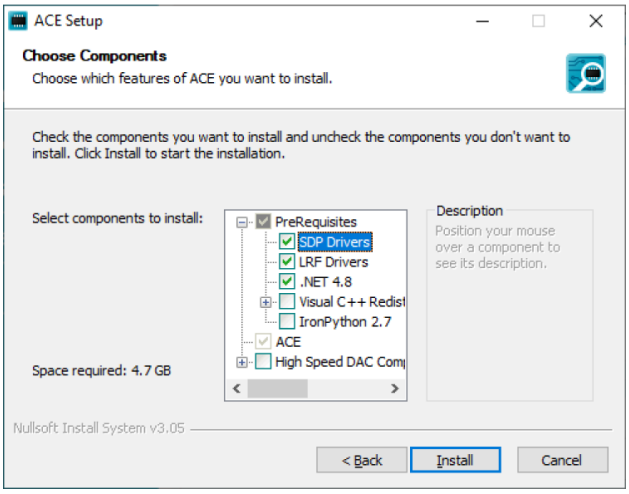


Figure 5. Drivers That Must Be Installed with the ACE Software

After the ACE software installs, download the ADMV4540-EVALZ **ADMV4540.acezip** file provided by Analog Devices.

After the download completes, double-click on the ADMV4540-EVALZ **ADMV4540.acezip** file, and the ADMV4540 plug-in installs within the ACE software.

Once the installation is complete, the ADMV4540-EVALZ evaluation board plug-in appears when the user opens the ACE software (see Figure 6).

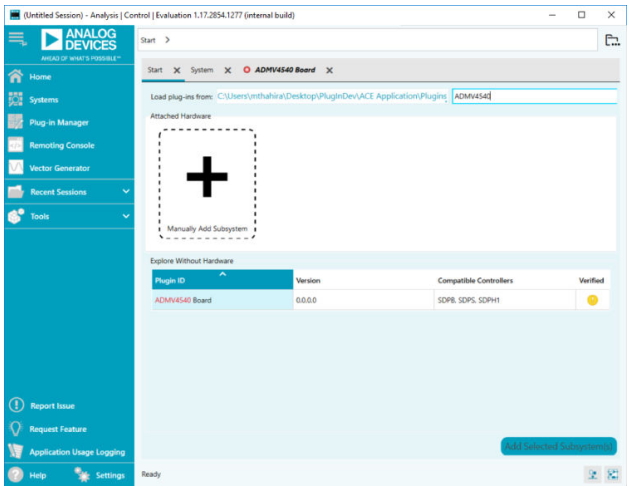


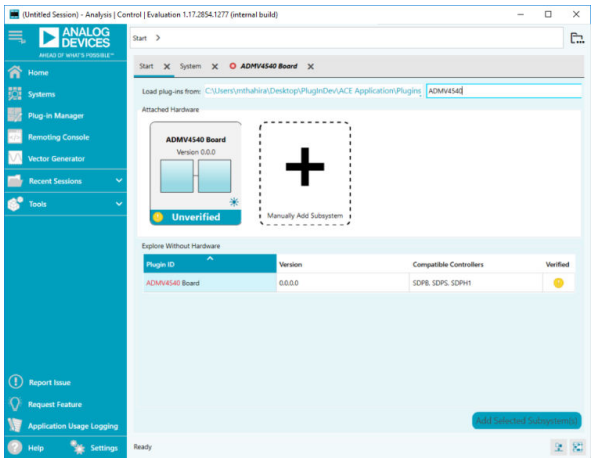
Figure 6. ADMV4540-EVALZ Evaluation Board Plug-In Window After Opening the ACE Software

INITIAL SETUP

To set up the ADMV4540-EVALZ, take the following steps:

1. Connect a USB cable to the PC and then to the USB connector of the SDP-S controller board. Connect the system demonstration platform (SDP-S) board to the ADMV4540-EVALZ through the on-board SDP-S connector on the ADMV4540-EVALZ.
2. Power up the ADMV4540-EVALZ with a 5 V dc supply.
3. Connect a coax cable to a second dc supply and connect it to the SMA_VCTRL coax connector. Set the dc supply to 0 V (minimum gain).
4. Connect a signal generator set at 50 MHz, 0 dBm to the EXT_REF connector.
5. Connect the IP, IN, QN, and QP cables as shown in Figure 3 and Figure 4.
6. Open the ACE software. The ADMV4540-EVALZ (**ADMV4540 Board**) appears in the **Attached Hardware** section (see Figure 7). Double-click on the ADMV4540-EVALZ plug-in. If the device is turned off and on, or if the USB cable is unplugged and plugged in, while the ACE software is open, the user may lose contact with the ADMV4540-EVALZ. If this happens, go to the **System** tab, click the **USB** symbol on the **ADMV4540 Board** subsystem, and then click **Acquire** to establish SPI communication with the ADMV4540-EVALZ again.

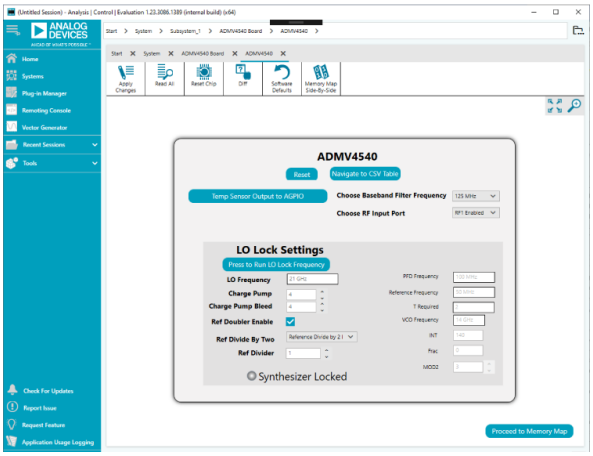
EVALUATION BOARD SOFTWARE QUICK START PROCEDURES



007

Figure 7. Attached Hardware Section when the ADMV4540 Board (ADMV4540-EVALZ Is Connected

7. The **ADMV4540 Block Diagram** in the ACE software then opens (see Figure 8). Note for optimal performance, it is recommended to click **Reset** each time the USB is plugged into the computer.



800

Figure 8. ADMV4540 Block Diagram in the ACE Software

ADMV4540 BLOCK DIAGRAM AND ITS FUNCTIONS

The ADMV4540 ACE plug-in is conveniently organized so that the user can quickly configure the ADMV4540 for lab evaluation. The full screen ADMV4540 block diagram with labels is shown in Figure 9, and Table 1 describes the functionality of each block.

Due to ongoing improvements and enhancements to the ACE software, note that some of the screen images in this user guide may not be the latest versions found in the ACE software.

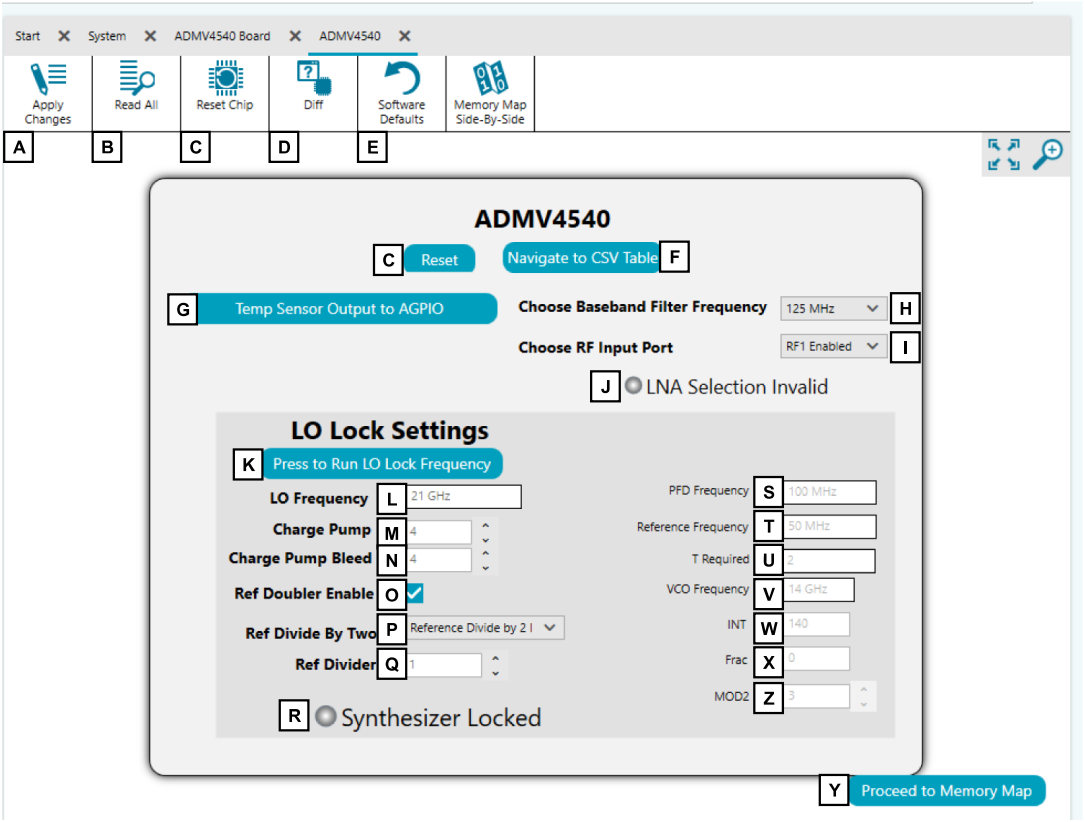


Figure 9. ADMV4540 Block Diagram with Labels

Table 1. ADMV4540 Block Diagram Label Functions (See Figure 9)

Label	Function
A	To apply all of the changed register values to the device, click **Apply Changes** (Label A).
B	To read back all of the SPI registers of the device, click **Read All** (Label B).
C	Click **Reset Chip** (Label C) or the **Reset** button to reset the ADMV4540 and load the SPI start-up settings, 125 MHz filter settings, and lock the synthesizer to 21 GHz.
D	Click **Diff** (Label D) to shows registers that are different on the device.
E	Click **Software Defaults** (Label E) to load the software defaults on to the device, and then click **Apply Changes** (Label A).
F	Click **Navigate to CSV Table** (Label F) to navigate to the CSV table. Refer to the Using the ADMV4540 CSV Table section for more information
G	Click the **Temp Sensor Output to AGPIO** (Label G) to send the temperature sensor output to the AGPIO pin.
H	Use the **Choose Baseband Filter Frequency** drop-down menu (Label H) to choose the appropriate baseband filter corner settings.
I	Use the Choose RF Input Port drop-down menu (Label I) to choose the appropriate RF input.
J	The **LNA Selection Invalid** (Label J) message only appears if both RFIN1 and RFIN2 are enabled through the **Memory Map**. This message does not appear during normal operation of the device.
K	Click **Press to Run LO Lock Frequency** (Label K) to lock the device at the desired frequency entered in the **LO Frequency** (Label L) box.
L	Enter the desired LO frequency in the **LO Frequency** (Label L) box. Ensure that you press**Press to Run LO Lock Frequency** (Label K) after changing the **LO Frequency** value within the box; otherwise, the LO will not change to the desired frequency.
M	Enter the charge pump current in the **Charge Pump** (Label M) box. The charge pump current is set to 4 at startup, by default. If the PFD frequency is set to 50 MHz, change the charge pump current value to 8 and then click the **Press to Run LO Lock Frequency** button.

ADMV4540 BLOCK DIAGRAM AND ITS FUNCTIONS

Table 1. ADMV4540 Block Diagram Label Functions (See Figure 9)

Label	Function
N	The charge pump bleed value is shown in the **Charge Pump Bleed** (Label N) box. The charge pump bleed is a read only field that is set to 4 at startup, by default.
O	Select the **Ref Doubler Enable** (Label O) check box to enable or disable the reference doubler. If the check box is selected, the reference doubler is enabled, and if the check box is not selected, the reference doubler is disabled. When the **Ref Doubler Enable** is selected, click the **Press to Run LO Lock Frequency** button. It is recommended to keep the reference doubler enabled at all times for optimum integrated phase noise performance.
P	Use the **Ref Divide By Two** (Label P) drop-down menu to select enabling or disabling of the reference divide by two. Refer to the ADMV4540 data sheet for more information on how this selection changes the phase frequency detector (PFD) frequency. If the **Ref Divide By Two** pull-down menu changes, click the **Press to Run LO Lock Frequency** button.
Q	To enter the reference divider value, toggle the **Ref Divider** (Label Q) box. **Ref Divider** is set to 1 at startup, by default, or after clicking the **Reset** button (Label C)d. When the**Ref Divider** value changes, click the **Press to Run LO Lock Frequency** button. Refer to the ADMV4540 data sheet for more information on how this selection changes the PFD frequency.
R	The **Synthesizer Locked** (Label R) light turns green if the synthesizer is locked after clicking the **Press to Run LO Lock Frequency** (Label L) button.
S	See the **PFD Frequency** (Label S) box for the PFD frequency, which is a read only field. Refer to the ADMV4540 data sheet for more information on how to calculate the PFD frequency.
T	See the **Reference Frequency** (Label T) box for the reference frequency, which is a read only field and set to 50 MHz at startup, by default.
U	See the **T Required** (Label U) box for the T value, which is a read only field. Refer to the ADMV4540 data sheet for more information on how to calculate the T value.
V	See the **VCO Frequency** (Label V) box for the voltage-controlled oscillator frequency. This is a read only field. The VCO frequency is the LO frequency divided by 1.5.
W	See the **INT Divider** (Label W) box for the integer divider value, which is a read only field. Refer to the ADMV4540 data sheet for more information on how to calculate the INT divider.
X	See the **Frac** (Label X) box for the fractional value, which is a read only field. Refer to the ADMV4540 data sheet for more information on how to calculate the fractional value.
Y	Click **Proceed to Memory Map** (Label Y) to open the ADMV4540 memory map (see Figure 10).
Z	See the **MOD2**(Label Z) box for the MOD2 value, which is a read only field. MOD2 is set to 3 at startup, by default.

ADMV4540 BLOCK DIAGRAM AND ITS FUNCTIONS

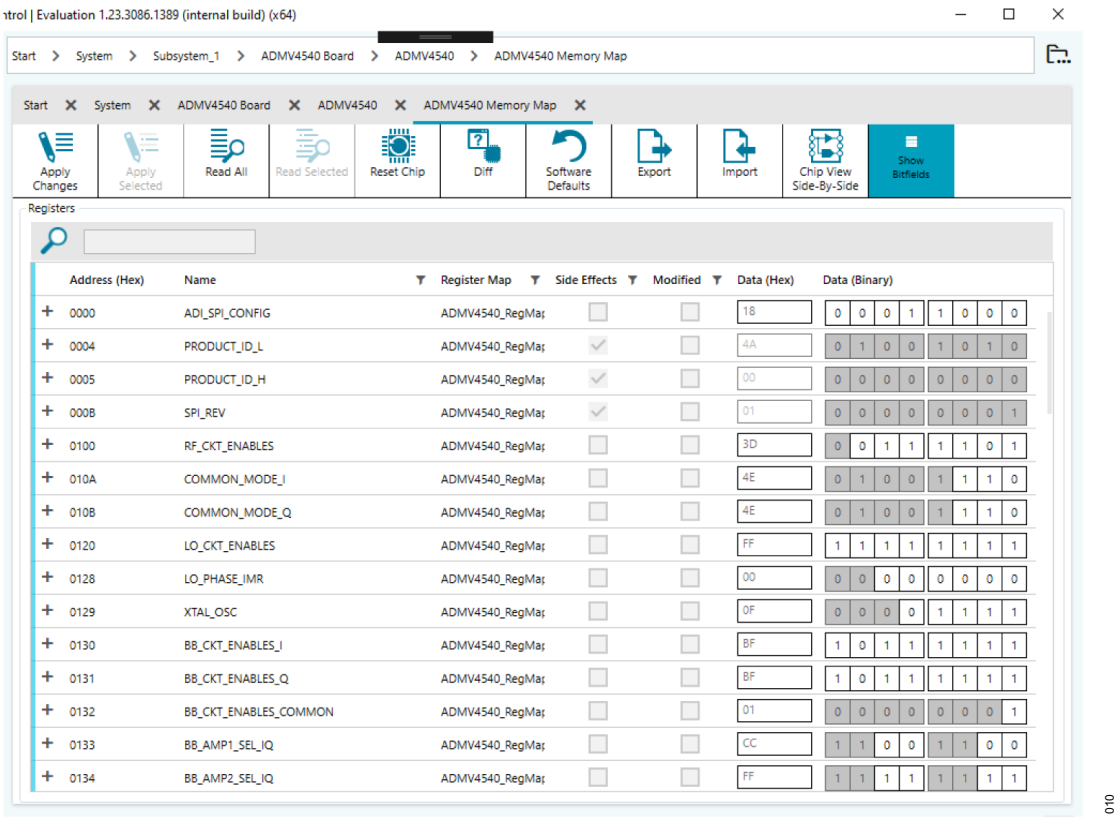


Figure 10. ADMV4540 Memory Map in the ACE Software

ADMV4540 BLOCK DIAGRAM AND ITS FUNCTIONS

USING THE ADMV4540 CSV TABLE

The ADMV4540 CSV table is a quick tool to use to load a .csv file of register settings to program the device or to save the current register settings to a .csv file. The register settings can be saved as hexadecimal (Base 16) or decimal (Base 10) format.

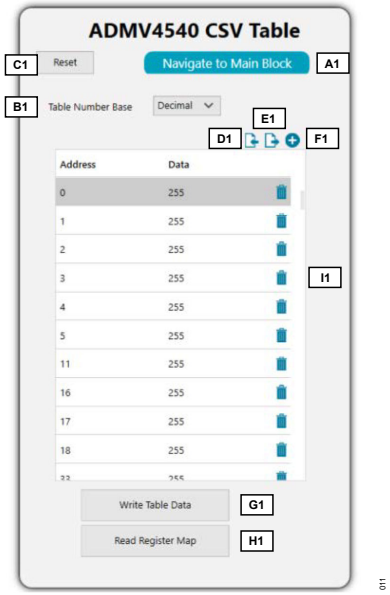


Figure 11. ADMV4540 CSV Table with Labels

Table 2. ADMV4540 CSV Table Block Diagram Label Functions (See Figure 11)

Label	Function
A1	Click **Navigate to Main Block** (Label A1) to navigate to the main chip view (Figure 9).
B1	Click **Table Number** Base (Label B1) to select the appropriate base (Base 16 or Base 10). Note that it is important to select the correct base before importing a .csv file.
C1	Click **Reset** (Label C1) to reset the ADMV4540 and to load the third-order intercept (IP3) settings, gain set settings, and 125 MHz filter settings, and to lock the synthesizer to 21 GHz. Consult the ADMV4540 data sheet for additional information on SPI sequences.
D1	Click **Import CSV**(Label D1) to import a .csv file of register settings. Note that it is important to match the same base as the csv file shown in the **Table Number Base** (Label B1). Note that importing the .csv file does not write these values to the ADMV4540. The first row of the .csv file must have the header **Address** in the first column and **Data** in the second column.
E1	Click **Export CSV**(Label E1) to export a .csv file of the register settings shown in the **CSV Table** (Label I1).
F1	Click **Add Row to CSV Table**(Label F1) to add another row of register settings to the **CSV Table** (Label I1).
G1	Click **Write Table Data** (Label G1) to write the register settings shown in the **CSV Table** (Label I1) to the ADMV4540.
H1	Click **Read Register Map** (Label H1) to read the register settings from all the registers in the ADMV4540 memory map and display these settings in the **CSV Table** (Label I1).
I1	The **CSV Table** (Label I1) displays the registers addresses and data to be written to the device or to be read from the device.

TEST RESULTS

When testing the ADMV4540-EVALZ, the results described in this section are the expected results. VCTRB_BBVVAx = 3.3 V, the LO frequency (f_{LO}) = 17 GHz, the reference frequency (f_{REF}) = 50 MHz, the external single-ended reference power level = 3 dBm, the phase frequency detector (PFD) frequency (f_{PFD}) = 100 MHz, the RF power level = –66 dBm, the I channel and Q channel positive and negative outputs were combined with a 180° balun, and the board traces are not deembedded.

Figure 12 shows the expected results for the I channel and the Q channel with an RF frequency (f_{RF}) of 17.1 GHz and a 125 MHz serial peripheral interface (SPI)-selectable low-pass filter (LPF).

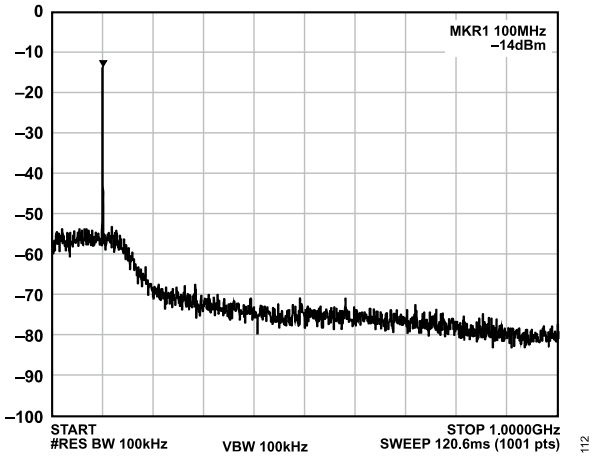


Figure 12. ADMV4540-EVALZ Test Results for f_{RF} = 17.1 GHz and a 125 MHz SPI-Selectable LPF

Figure 13 shows the expected results for the I channel and the Q channel with an f_{RF} of 17.2 GHz and a 125 MHz SPI-selectable LPF.

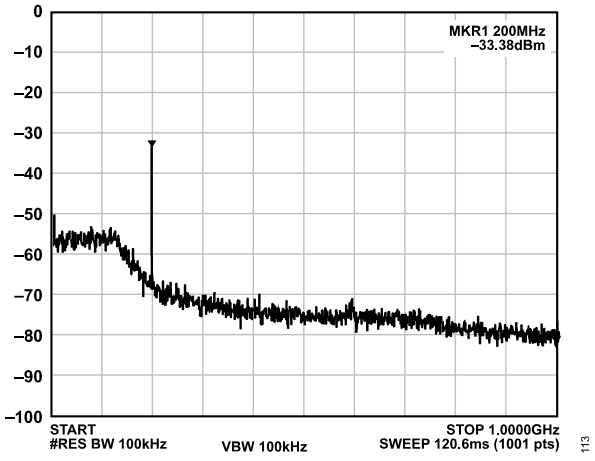


Figure 13. ADMV4540-EVALZ Test Results for f_{RF} = 17.2 GHz and a 125 MHz SPI-Selectable LPF

Figure 14 shows the expected results for the I channel and the Q channel with an f_{RF} of 17.2 GHz and a 250 MHz SPI-selectable LPF.

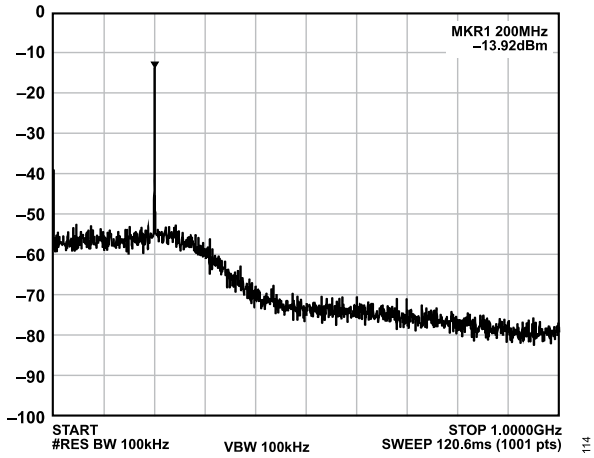


Figure 14. ADMV4540-EVALZ Test Results for f_{RF} = 17.2 GHz and a 250 MHz SPI-Selectable LPF

Figure 15 shows the expected results for the I channel and the Q channel with an f_{RF} of 17.4 GHz and a 250 MHz SPI-selectable LPF.

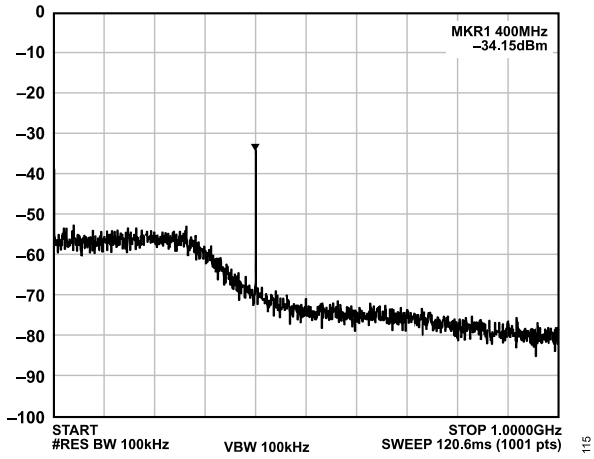


Figure 15. ADMV4540-EVALZ Test Results for f_{RF} = 17.4 GHz and a 250 MHz SPI-Selectable LPF

TEST RESULTS

Figure 16 shows the expected results for the I channel and the Q channel with an f_{RF} of 17.4 GHz and a 500 MHz SPI-selectable LPF.

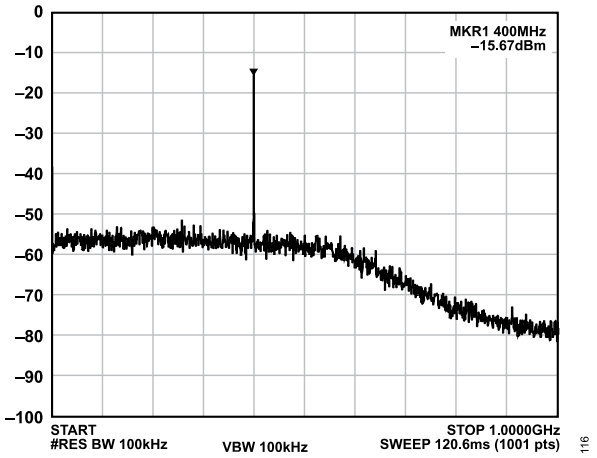


Figure 16. ADMV4540-EVALZ Test Results for f_{RF} = 17.4 GHz and a 500 MHz SPI-Selectable LPF

Figure 17 shows the expected results for the I channel and the Q channel with an f_{RF} of 17.8 GHz and a 500 MHz SPI-selectable LPF.

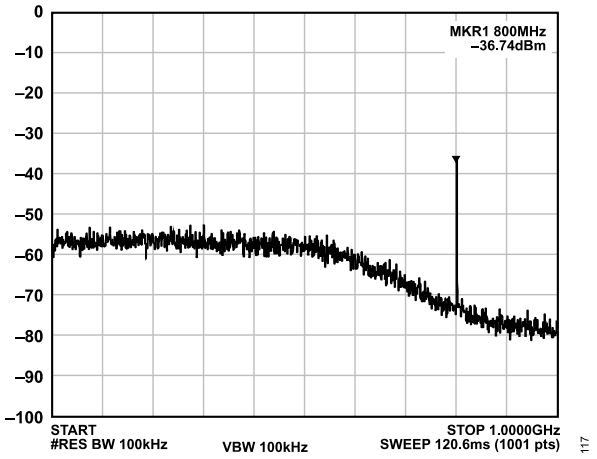


Figure 17. ADMV4540-EVALZ Test Results for f_{RF} = 17.8 GHz and a 500 MHz SPI-Selectable LPF

Figure 18 shows the expected results for the I channel and the Q channel with an f_{RF} of 17.8 GHz and a bypass SPI-selectable LPF.

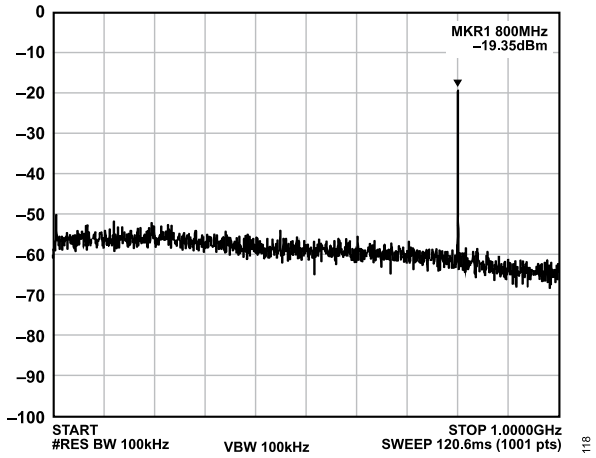


Figure 18. ADMV4540-EVALZ Test Results for f_{RF} = 17.8 GHz and a Bypass SPI-Selectable LPF

EVALUATION BOARD SCHEMATICS AND ARTWORK

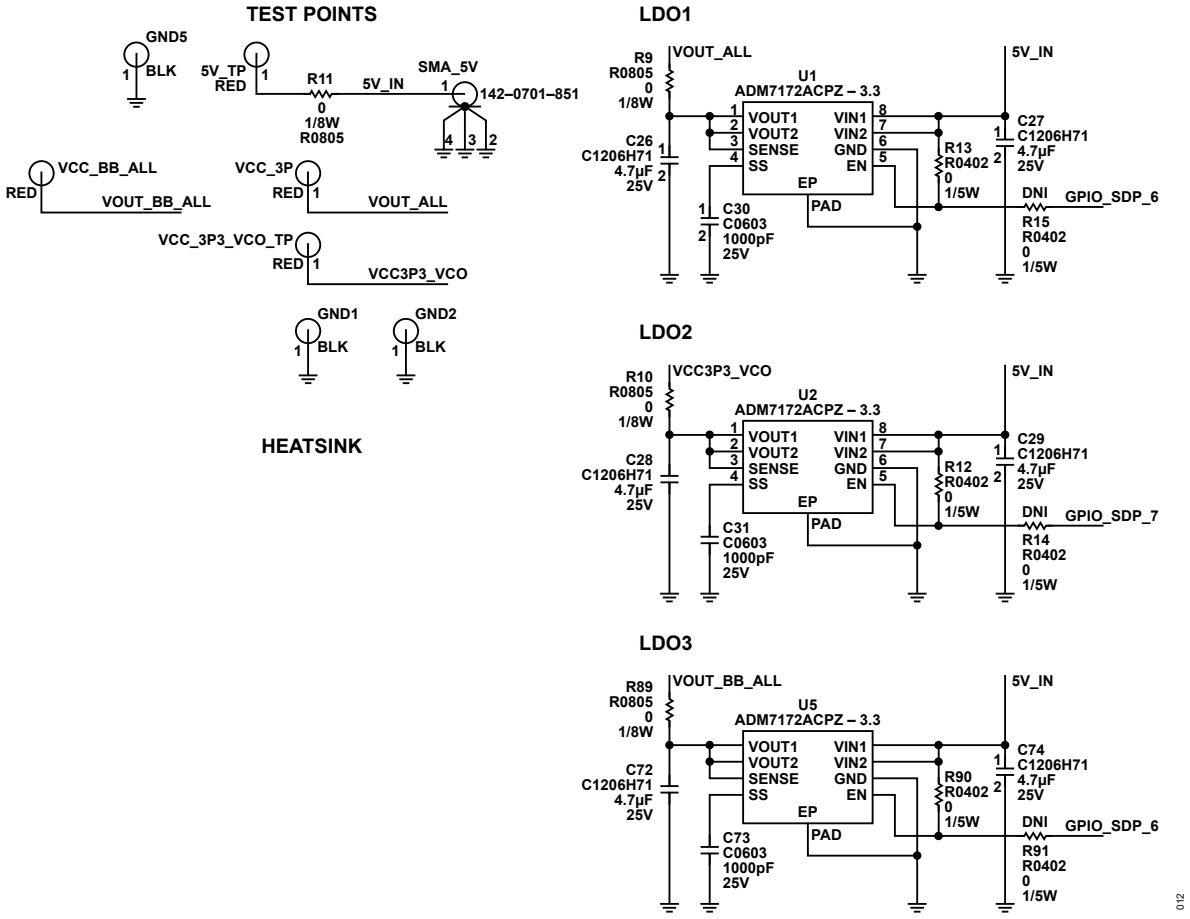


Figure 19. ADMV4540-EVALZ Evaluation Board Schematic, Page 1

EVALUATION BOARD SCHEMATICS AND ARTWORK

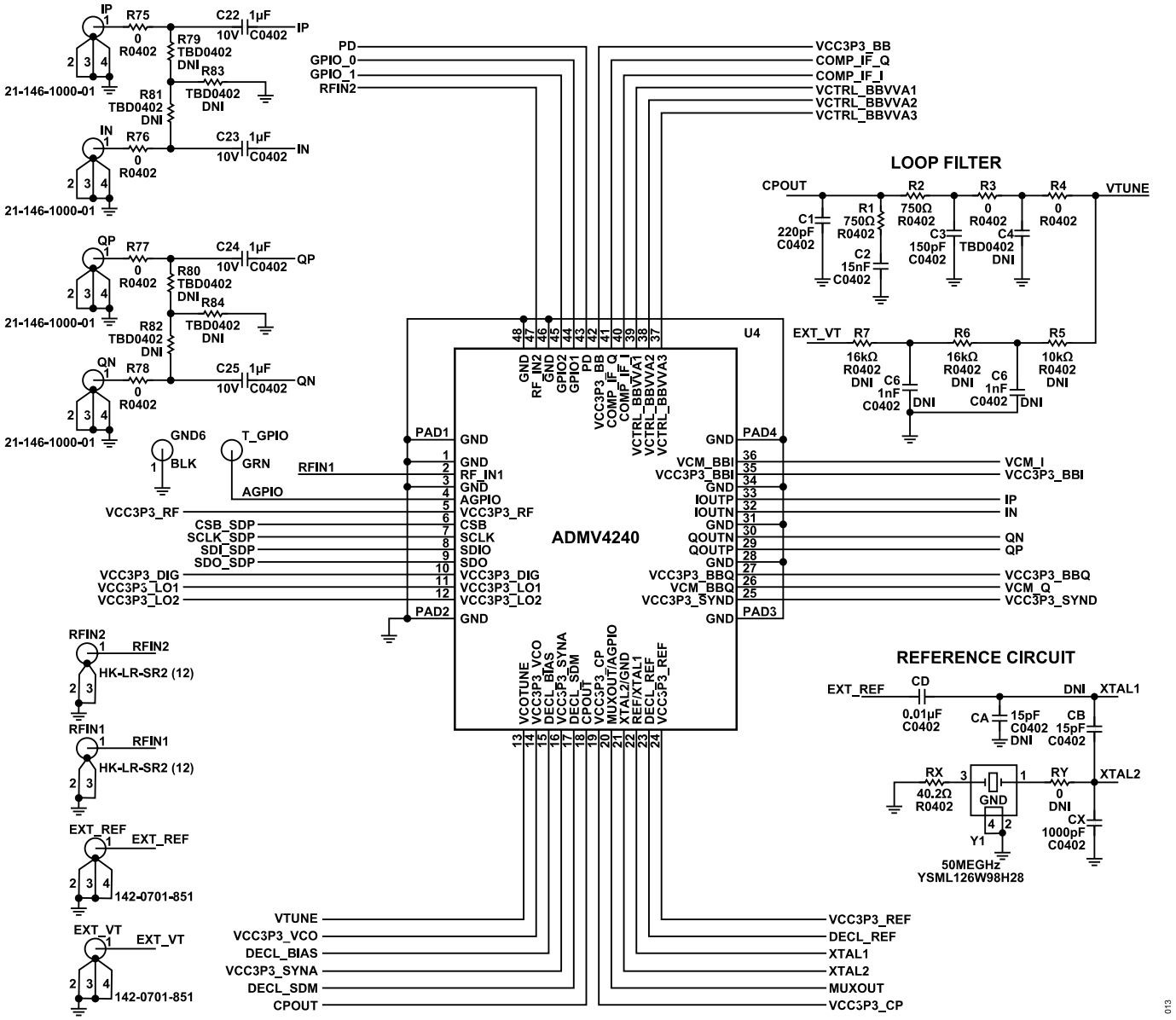


Figure 20. ADMV4540-EVALZ Evaluation Board Schematic, Page 2

EVALUATION BOARD SCHEMATICS AND ARTWORK

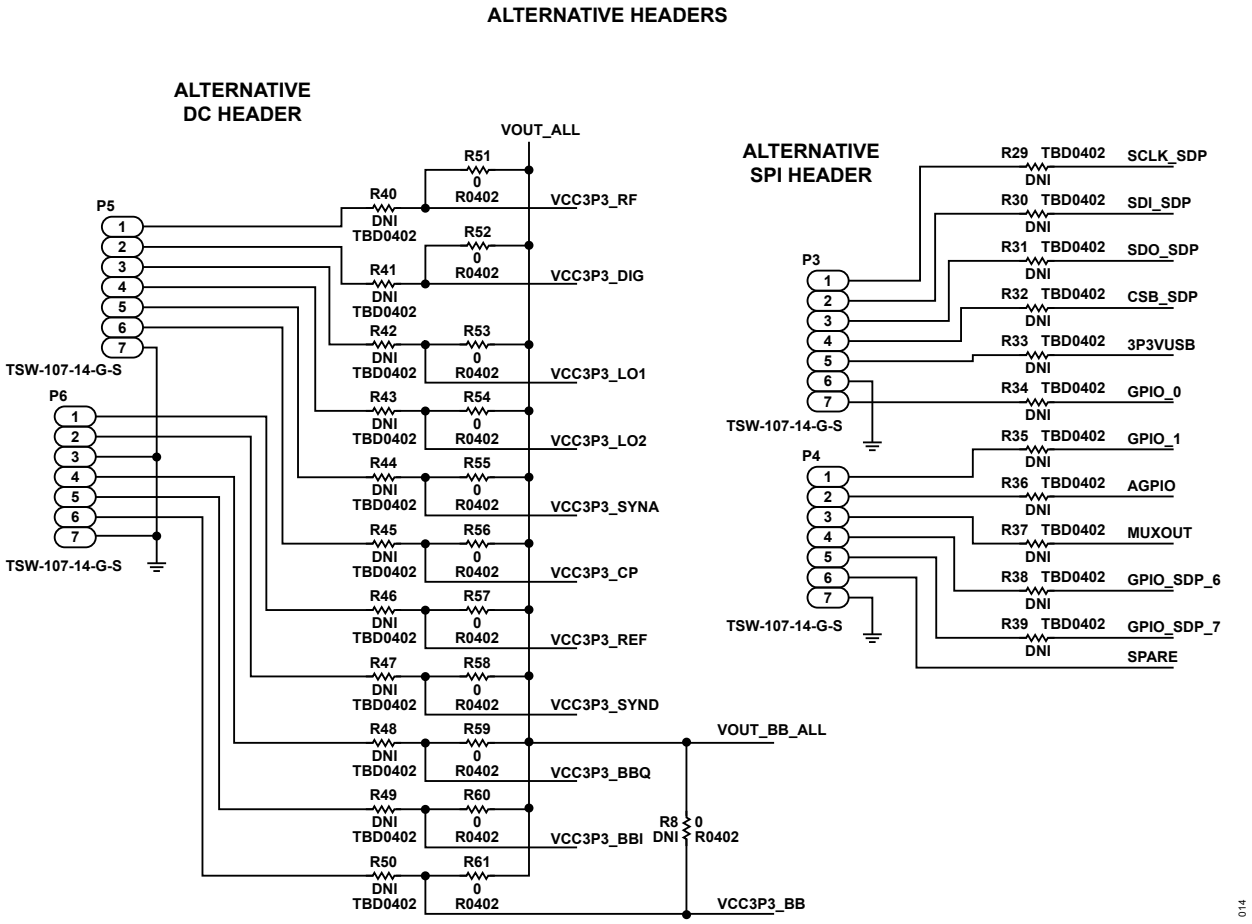


Figure 21. ADMV4540-EVALZ Evaluation Board Schematic, Page 3

EVALUATION BOARD SCHEMATICS AND ARTWORK

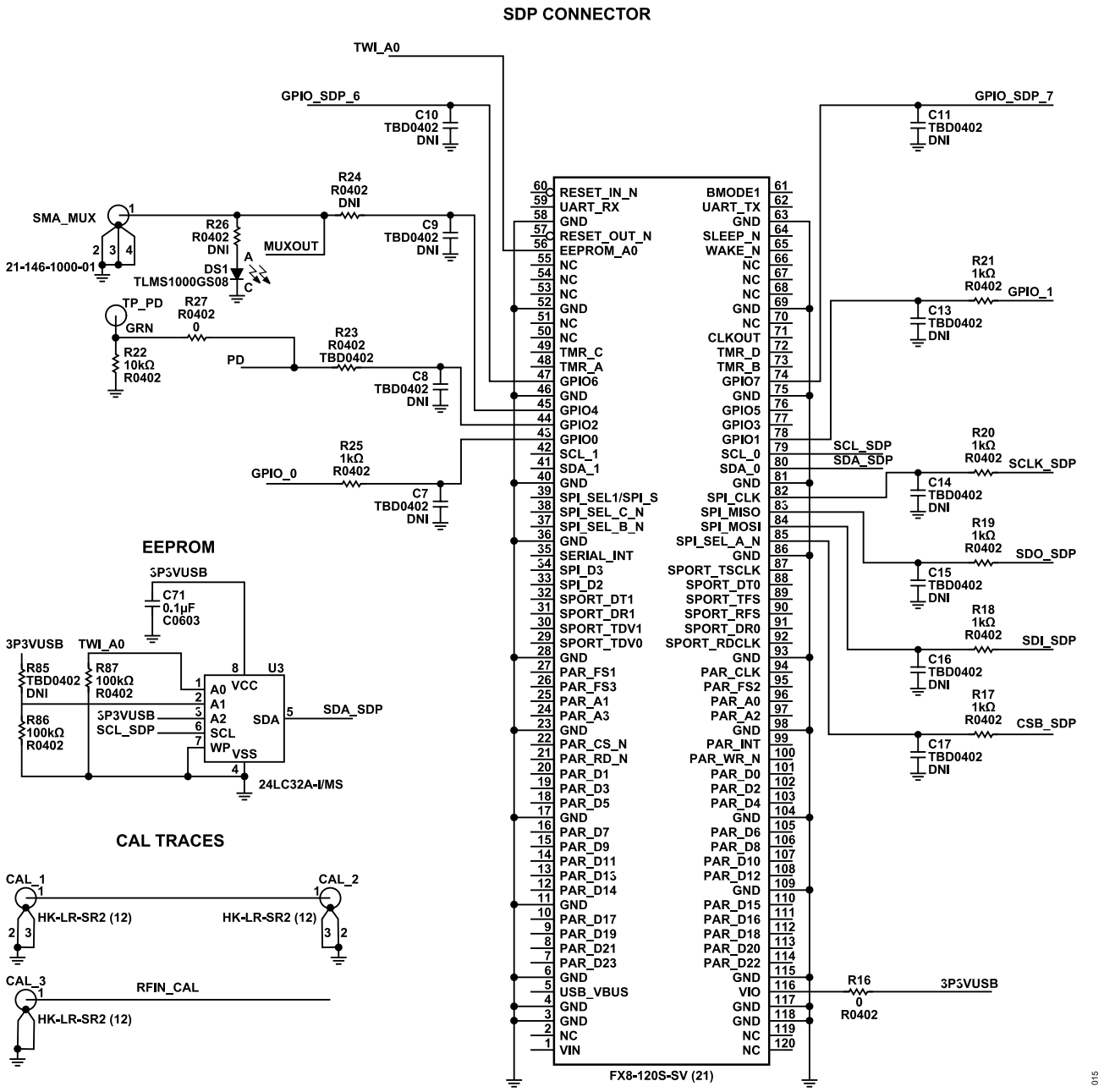


Figure 22. ADMV4540-EVALZ Evaluation Board Schematic, Page 4

EVALUATION BOARD SCHEMATICS AND ARTWORK

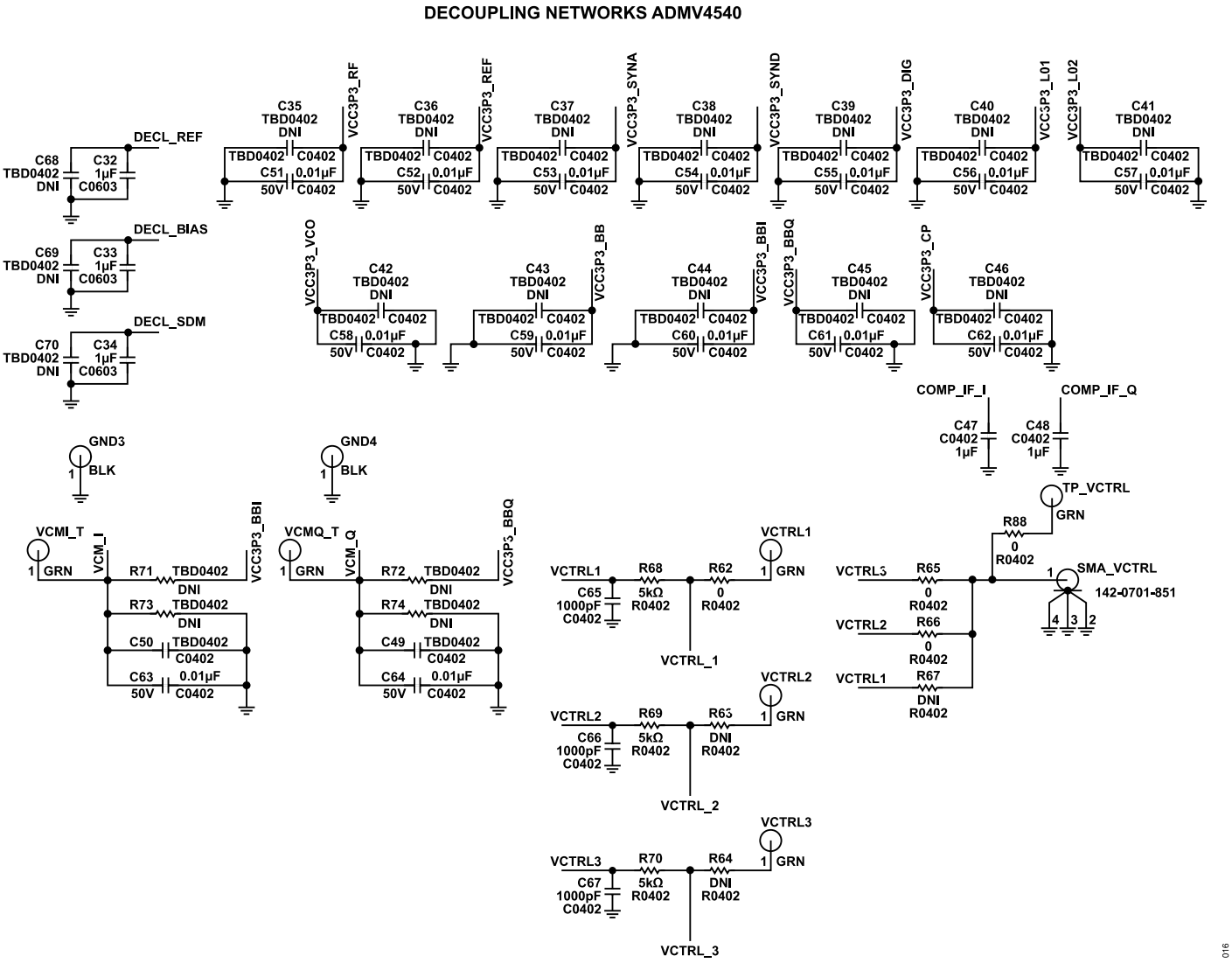


Figure 23. ADMV4540-EVALZ Evaluation Board Schematic, Page 5

EVALUATION BOARD SCHEMATICS AND ARTWORK

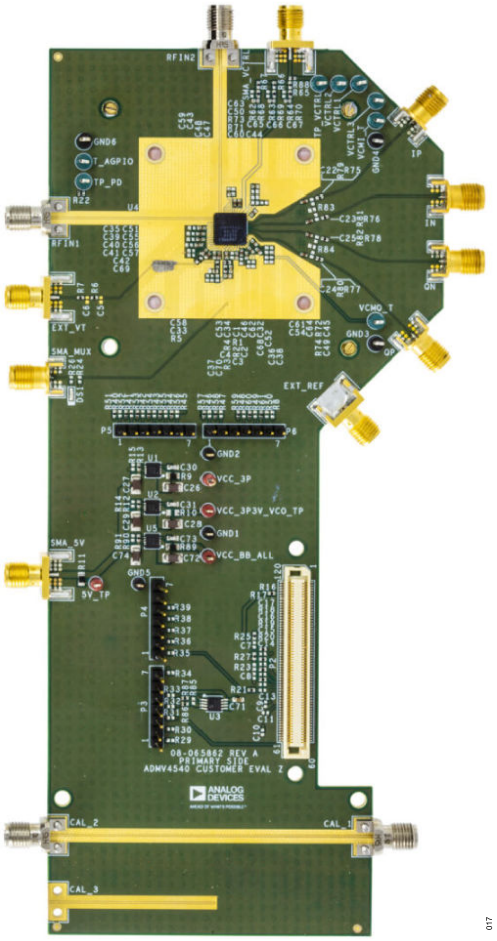


Figure 24. ADMV4540-EVALZ Evaluation Board Top

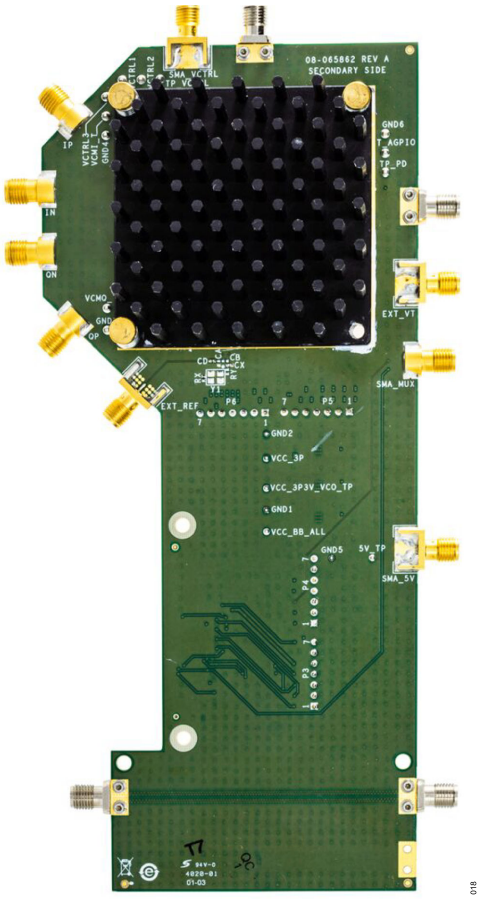


Figure 25. ADMV4540-EVALZ Evaluation Board Bottom

EVALUATION BOARD SCHEMATICS AND ARTWORK

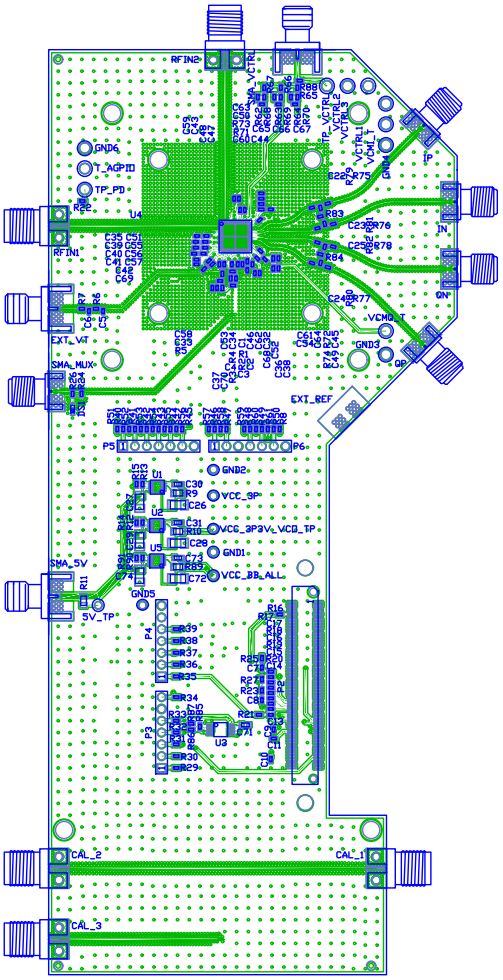


Figure 26. ADMV4540-EVALZEvaluation Board Top Layer

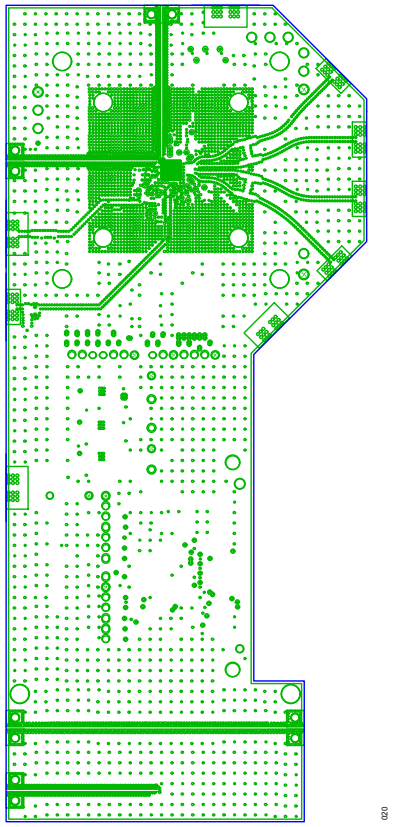


Figure 27. ADMV4540-EVALZ Evaluation Board Second Layer

EVALUATION BOARD SCHEMATICS AND ARTWORK

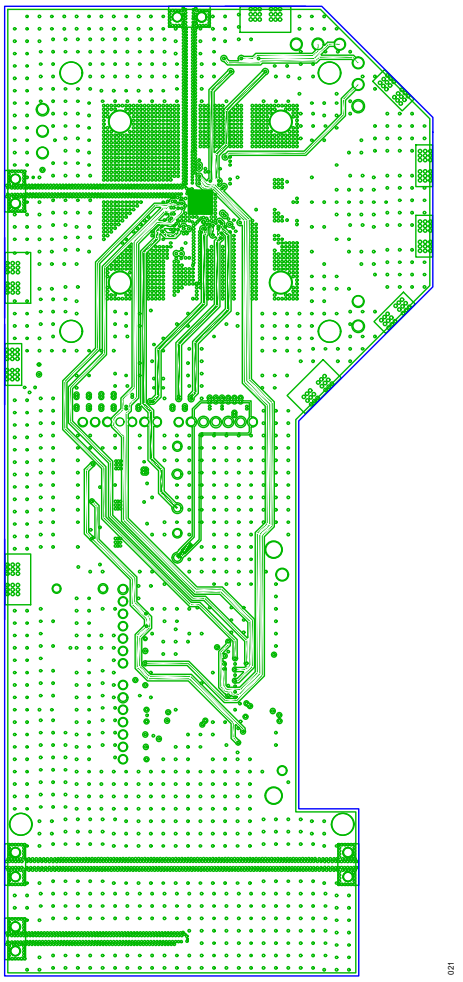


Figure 28. ADMV4540-EVALZ Evaluation Board Third Layer

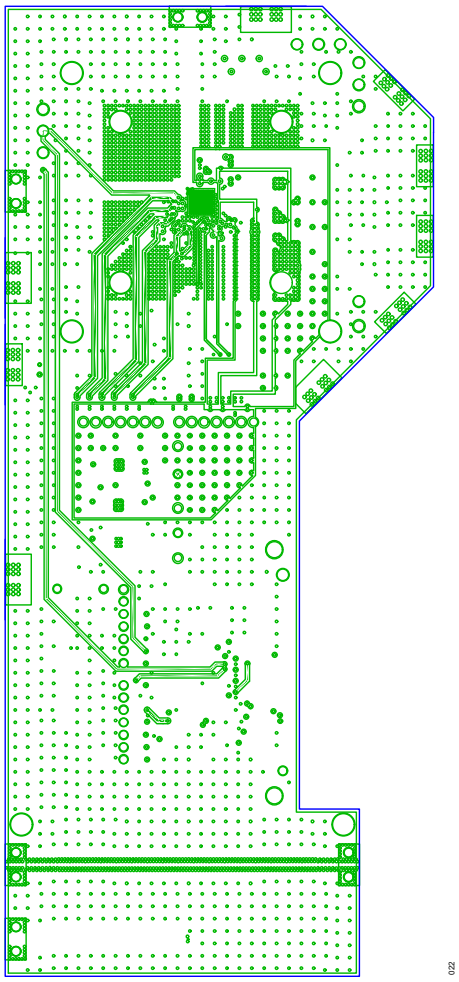


Figure 29. ADMV4540-EVALZ Evaluation Board Fourth Layer

EVALUATION BOARD SCHEMATICS AND ARTWORK

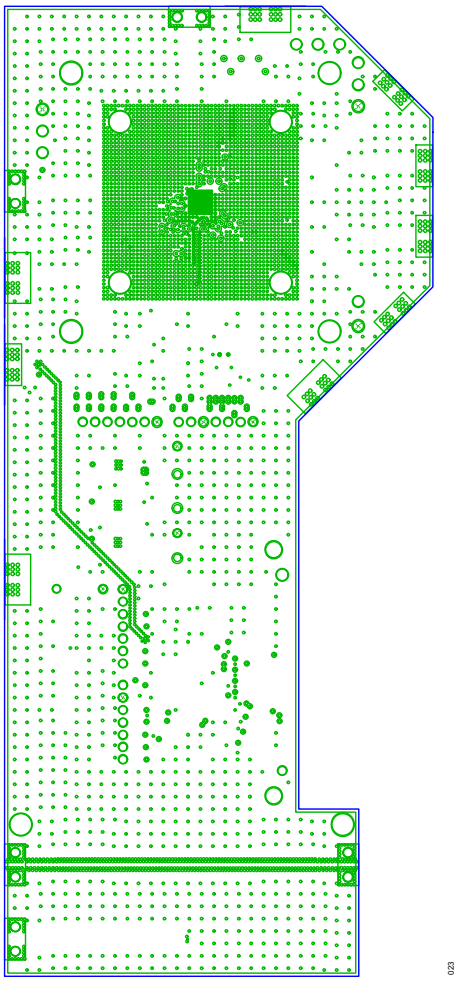


Figure 30. ADMV4540-EVALZ Evaluation Board Fifth Layer

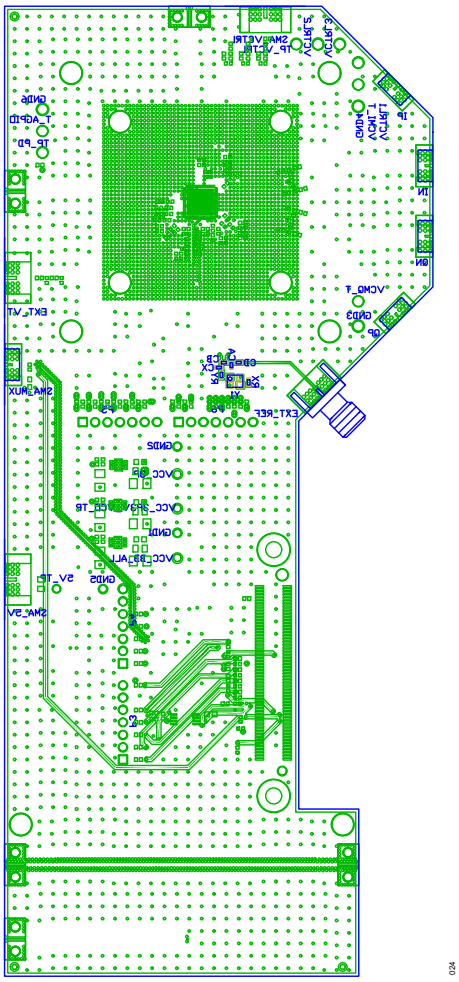


Figure 31. ADMV4540-EVALZ Evaluation Board Sixth Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 3. ADMV4540-EVALZ Configuration Options

Components	Description	Manufacturer
PCB	Printed circuit board	Analog Devices supplied
5V_TP, VCC_3P, VCC_3P3V_VCO_TP, VCC_BB_ALL	Red test points, CNKEY5001TP	Keystone Electronics
C1	220 pF ceramic capacitor, 50 V, C0402	KEMET
C3	150 pF ceramic capacitor, 50 V C0402	KEMET
C2	15 nF ceramic capacitor, 15 nF, 50 V, 10%, X7R, C0402	Samsung
C22 to C25, C32 to C34, C47, C48	1 µF ceramic capacitors, 10 V, C0402	Murata
C26 to C29, C72, C74	4.7 µF ceramic capacitors, 25VC1206H71	KEMET
C30, C31, C73	1000 pF ceramic capacitors, 25 V, C0603	AVX Corporation
C51 to C64, CD	0.01 µF ceramic capacitors, 50 V, C0402	Murata
C65 to C67, CX	1000 pF ceramic capacitors, 50 V, C0402	Murata
C71	0.1 µF ceramic capacitor, 50 V C0603	Murata
CAL_1 to CAL_3, RFIN1, RFIN2	CONN-PCB, 2.92 mm coax, HK-LR-SR2(12), CNHRSH2_4-LR-SR2	Hirose Electric Company
DS1	Red light emitting diode (LED), surface-mount device (SMD), 0603, TLMS1000GS08, LED0603	Vishay
EXT_REF, EXT_VT, SMA_5V, SMA_VCTRL	CONN-PCB jacks, 142-0701-851, CNSMA10G62THK_EDGE	Cinch
GND1, GND2, GND5	Black test points, CNKEY5001TP	Keystone Electronics
GND3, GND4, GND6	Black test points, CNLOOPTP	Components Corporation
IN, IP, QN, QP, SMA_MUX	CONN-PCB jacks, Subminiture A (SMA), 21-146-1000-01, CNSMA20G62THK_EDGE	SRI Connector Gage Co.
P2	CONN-PCB vertical type receptor, FX8-120S-SV(21), CNHRSFX8-120S-SV_A	HRS
P3 to P6	CONN-PCB 7 position male, TSW-107-14-G-S, CNTHMHDR1X7L700W100H433	Samtec, Inc.
R1, R2	750 Ω resistors, SMD, R0402	Vishay
R9 to R11, R89	0 Ω resistors, SMD, R0805	Vishay
R3, R4, R12, R13, R16, R27, R51 to R62, R65, R66, R75 to R78, R88, R90	0 Ω resistors, SMD, R0402	Vishay
R17 to R20	33 Ω resistors, SMD, R0402	Panasonic
R21, R25	1 kΩ resistors, SMD, R0402	Panasonic
R22	10 kΩ resistor, SMD, R0402	Vishay
R68 to R70	8.2 kΩ resistors, SMD, R0402	Panasonic
R86, R87	100 kΩ resistors, SMD, R0402	Panasonic
RX	40.2 Ω resistor, SMD, R0402	Panasonic
TP_PD, TP_VCTRL, T_AGPIO, VCMI_T, VCMQ_T, VCTRL1, VCTRL2, VCTRL3	Green test points, CNLOOPTP	Components Corporation
U1, U2, U5	6.5 V, 2 A, ultralow noise, high power supply rejection ratio (PSRR), fast transient response CMOS LDO, 3.3 V output voltage, ADM7172ACPZ-3.3, DFN8_3X3_PAD2_44X1_6_A	Analog Devices
U3	IC 32KBIT serial EEPROM, 24LC32A-I/MS, MSOP8	Microchip Technology
U4	K band quadrature demodulator with integrated fractional-N phase-locked loop (PLL) and voltage controlled oscillator (VCO), ADMV4540ACCZ, LGA48_7X7_4PAD	Analog Devices
Y1	12 pF, IC crystal, NX3225SA, 50 MHz, YSML126W98H28	Nihon Dempa Kogyo Corporation, Ltd.

ORDERING INFORMATION

NOTES

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.