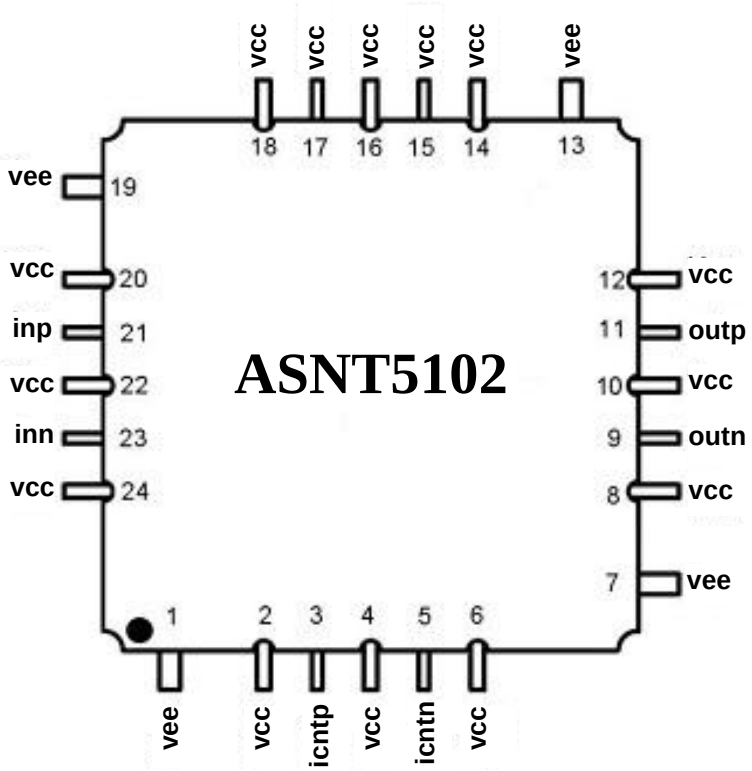
ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
2790 Skypark Drive Suite 112, Torrance, CA 90505

Offices: 310-530-9400 / Fax: 310-530-9402
www.adsantec.com

ASNT5102-KMC
DC-32.5*GHz* Clock Phase Shifter

- DC to 32.5*GHz* tunable clock phase shifter
- Delay adjustment range of 105*ps*
- Exhibits low jitter and limited temperature variation over industrial temperature range
- 2.0G*Hz* of bandwidth for the phase adjustment tuning port
- Ideal for high speed proof-of-concept prototyping
- Fully differential CML input interface
- Fully differential CML output interface with 600*mV* single-ended swing
- Power consumption: 1100*mW*
- Single +3.3*V* or -3.3*V* power supply
- Fabricated in SiGe for high performance, yield, and reliability
- Custom CQFP 24-pin package



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DESCRIPTION

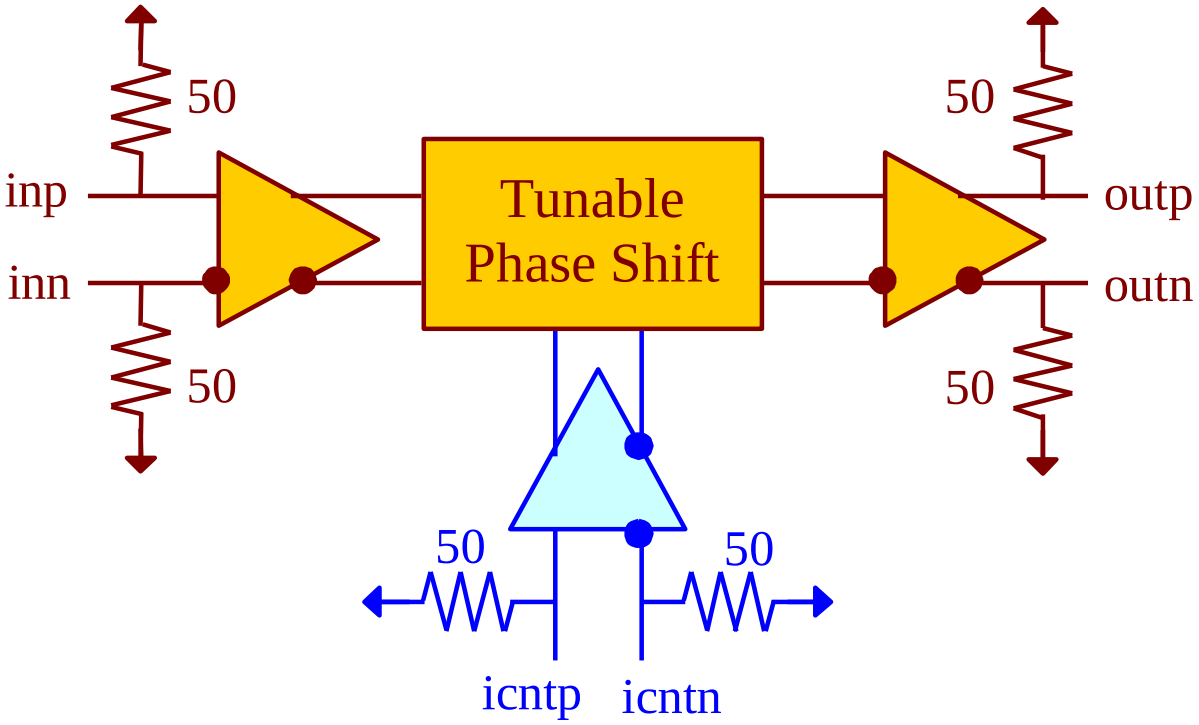

Fig. 1. Functional Block Diagram

ASNT5102-KMC is a clock variable delay line fabricated in SiGe technology. The IC shown in Fig. 1 provides an adjustable delay of its differential output signal outp/outn in relation to its input signal inp/inn. The delay is controlled through a wide-band differential tuning port icntp/icntn.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

Due to an extremely low jitter, the part is suitable for use in high-speed measurement / test equipment.

Delay Control Port

The delay is controlled through a wide-band differential tuning port icntp/icntn. The delay control diagram is shown in Fig. 2.

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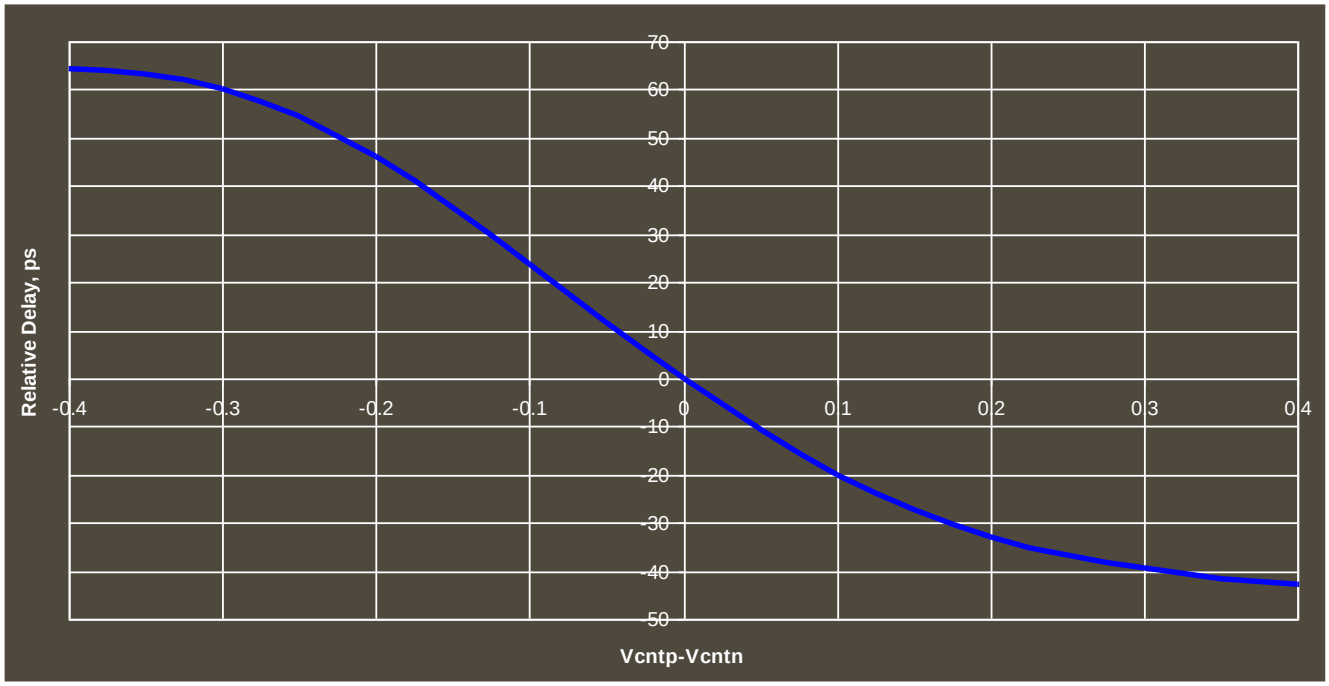

Fig. 2. Delay Control Diagram

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POWER SUPPLY CONFIGURATION

The ASNT5102-KMC can operate with either a negative supply (vcc = 0.0*V*=ground and vee = -3.3*V*), or a positive supply (vcc = +3.3*V* and vee = 0.0*V*=ground). In case of a positive supply, all I/Os need AC termination when connected to any devices with 50*Ohm* termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume vcc = 0.0*V* and vee = -3.3*V*.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All voltage limits are referenced to ground.

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		1.3	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
inp	21	CML input	Differential high-speed signal inputs with internal SE 50*Ohm* termination to vcc
inn	23		
icntp	3	CML input	Differential low-speed control inputs with internal SE 50*Ohm* termination to vcc
icntn	5		
outp	11	CML output	Differential high-speed signal outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
outn	9		

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V* or 0)	2, 4, 6, 8, 10, 12, 14, 15, 16, 17, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)	1, 7, 13, 19

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee	330	335	350	*mA*	
Power consumption		875		*mW*	
Junction temperature	-25	50	125	*°C*	
HS Input Signal (inp/inn)					
Frequency	DC		32.5	*GHz*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Signal (outp/outn)					
Frequency	DC		32.5	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc-0.6		*V*	With external 50*Ohm* DC termination
Rise/Fall times	11		13	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	For clock signal
Output-to-Input Delay					
Adjustment range		105		*ps*	For the full range of **icntp/icntn** control signals
Absolute delay stability	-10		10	*ps*	0-125°C
Phase Shift Control port (icntp/icntn)					
Bandwidth	DC		2.0	*GHz*	
SE voltage level	vcc-400		vcc	*mV*	Half control range when the opposite pin is at vcc
SE voltage level	vcc-800		vcc	*mV*	Full control range when the opposite pin is at vcc-0.4*V*
Differential swing	0		800	*mV*	Peak-peak, full control range
CM Level		vcc-(Diff. swing)/4		*V*	In differential mode

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the vcc plain, which is ground for a negative supply, or power for a positive supply.

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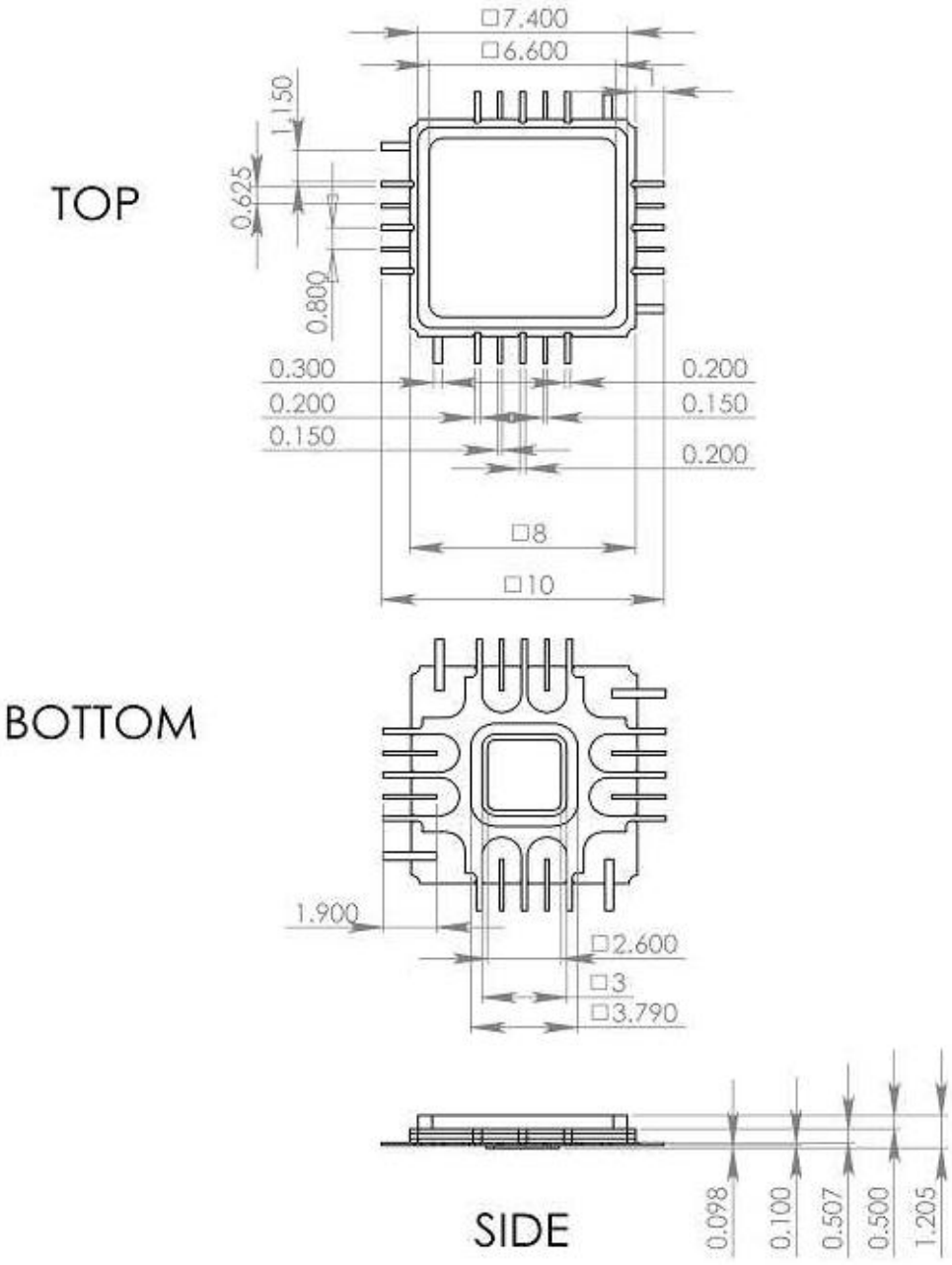

Fig. 3. CQFP 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT5102-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

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REVISION HISTORY

Revision	Date	Changes
2.8.2	01-2020	Updated Package Information
2.7.2	07-2019	Updated Letterhead
2.7.1	08-2016	Corrected power and current consumption values Revised package information section
2.6.1	09-2014	Revised maximum frequency of operation Revised electrical characteristics table
2.5.1	12-2013	Corrected comment in Electrical Characteristics
2.4.1	06-2013	Corrected control diagram Corrected electrical characteristics table
2.3.1	03-2013	Corrected terminal functions Corrected shift range values Added delay control diagram
2.2.1	02-2013	Corrected title Corrected description Added delay control diagram Corrected terminal functions Corrected electrical characteristics Added package mechanical drawing
2.1.1	09-2012	Corrected shift range values Corrected format
2.0	02-2012	Revised functional block diagram section Revised description section Added power supply configuration text Revised terminal functions section Revised electrical characteristics section Added absolute maximum ratings table Added package information section Added revision history table
1.0	03-2009	First release