

Dual N-Channel Enhancement Mode Power MOSFET

Description

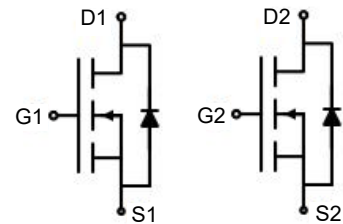
The G2K3N10L6 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

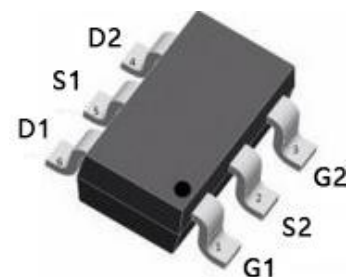
- V_{DS} 100V
- I_D (at $V_{GS} = 10V$) 3A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 220m Ω
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 230m Ω
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



SOT-23-6

Ordering Information

Device	Package	Marking	Packaging
G2K3N10L6	SOT-23-6 Dual	G2K3N10	30pcs/Tube

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current	I_D	3	A
Pulsed Drain Current (note1)	I_{DM}	12	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	1.67	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$

Thermal Resistance

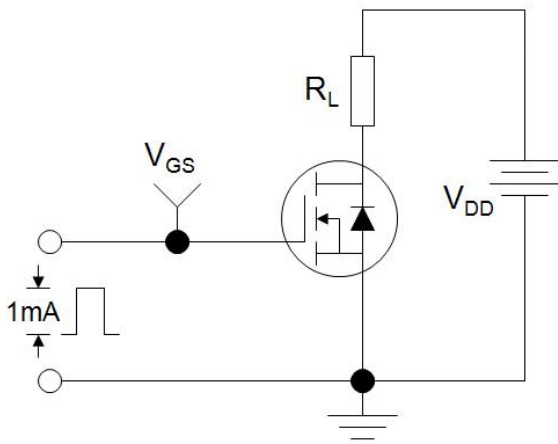
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	75	$^\circ\text{C/W}$

Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.6	2.2	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 2A$	--	180	220	m Ω
		$V_{GS} = 4.5V, I_D = 2A$	--	190	230	
Forward Transconductance	g_{FS}	$V_{GS} = 5V, I_D = 2A$	--	6	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 50V,$ $f = 1.0\text{MHz}$	--	536	--	pF
Output Capacitance	C_{oss}		--	103	--	
Reverse Transfer Capacitance	C_{rss}		--	52	--	
Total Gate Charge	Q_g	$V_{DD} = 50V,$ $I_D = 2A,$ $V_{GS} = 4.5V$	--	4.8	--	nC
Gate-Source Charge	Q_{gs}		--	1.2	--	
Gate-Drain Charge	Q_{gd}		--	1.7	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 50V,$ $I_D = 2A,$ $R_G = 6\Omega$	--	52	--	ns
Turn-on Rise Time	t_r		--	12	--	
Turn-off Delay Time	$t_{d(off)}$		--	17	--	
Turn-off Fall Time	t_f		--	10	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	3	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 2A, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = 2A, V_{GS} = 0V$ $di/dt = 500A/\mu s$	--	91	--	nC
Reverse Recovery Time	T_{rr}		--	28	--	ns

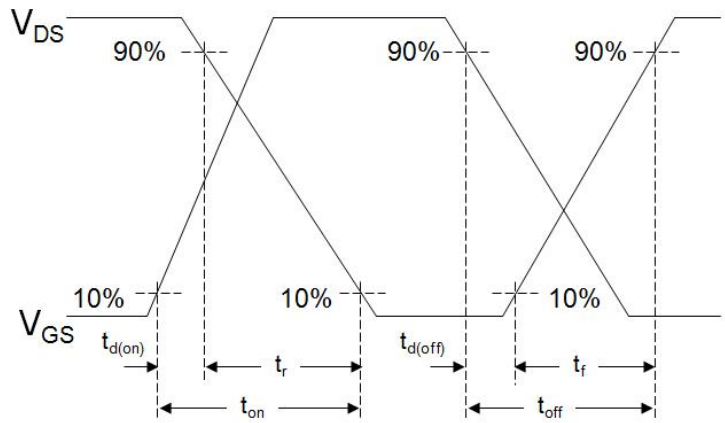
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

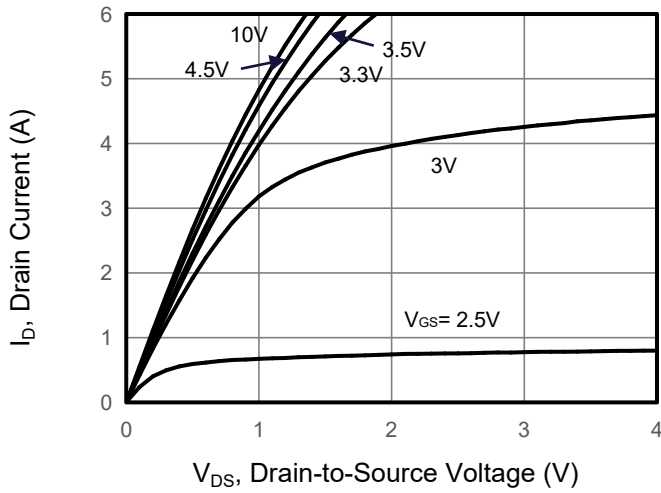


Figure 2. Transfer Characteristics

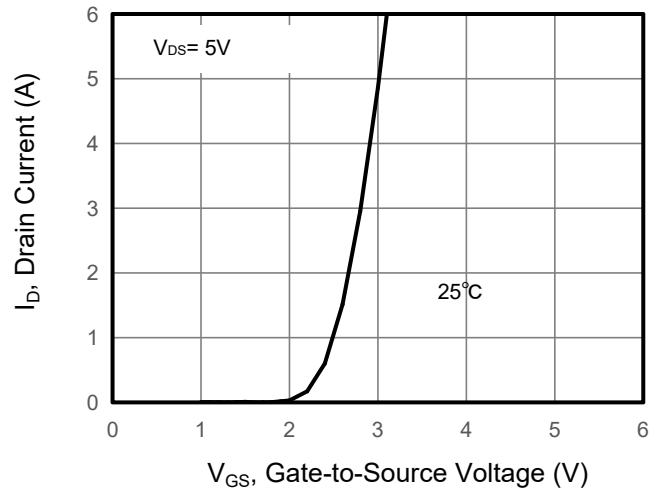


Figure 3. Drain Source On Resistance

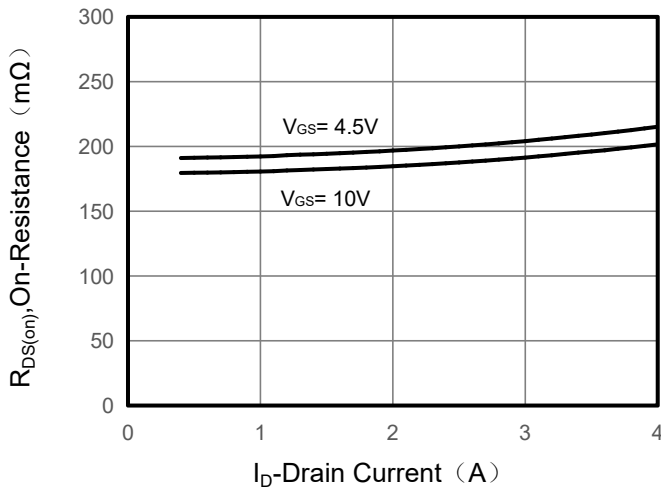


Figure 4. Gate Charge

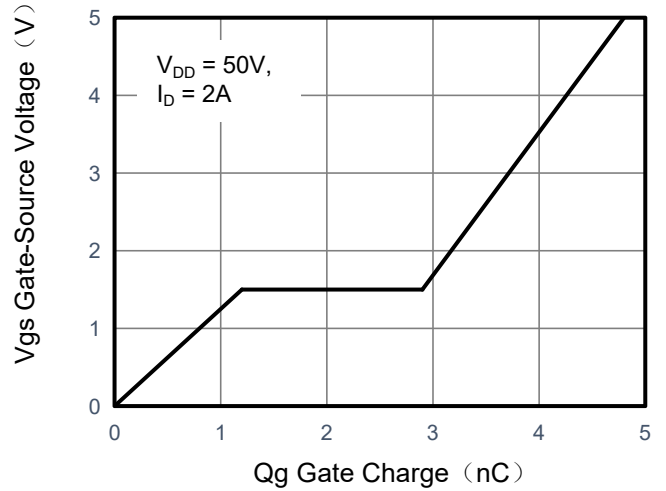


Figure 5. Capacitance

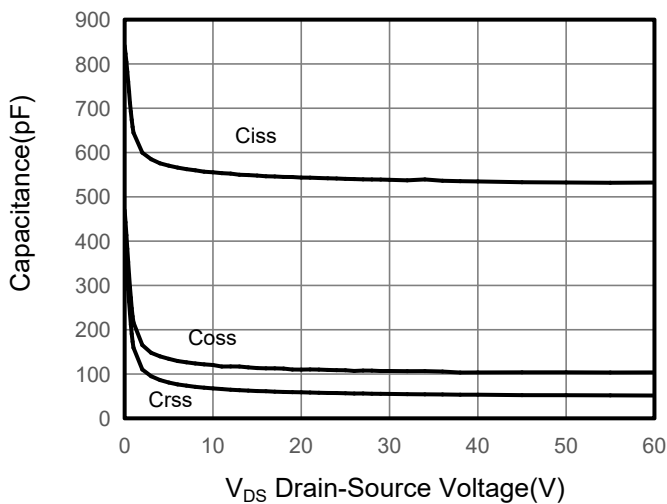
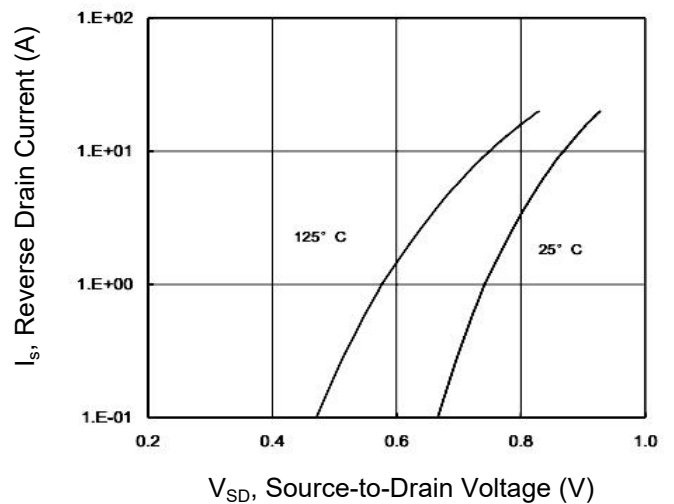


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

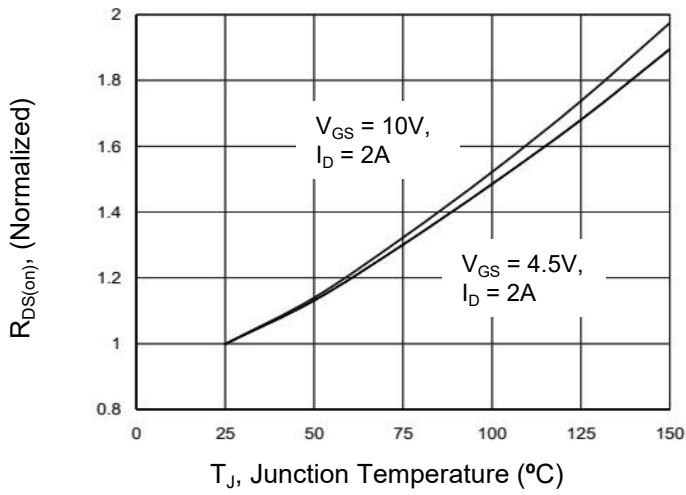


Figure 8. Safe Operation Area

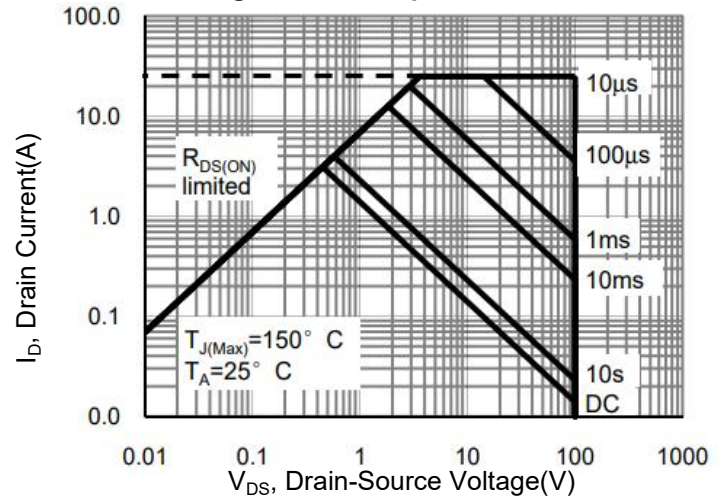
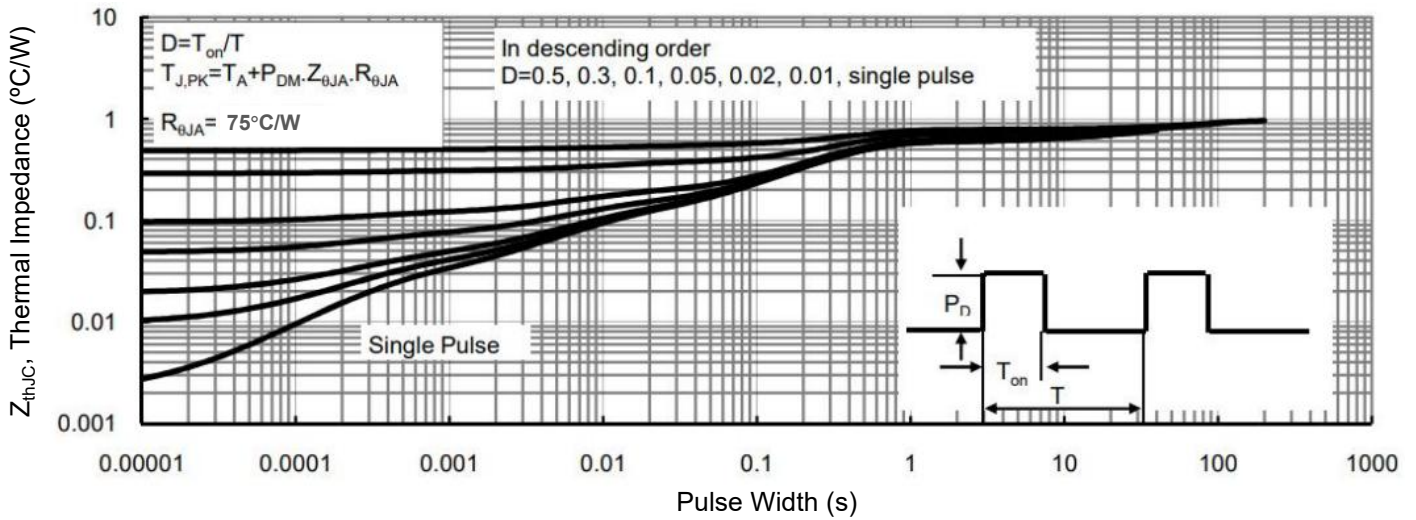
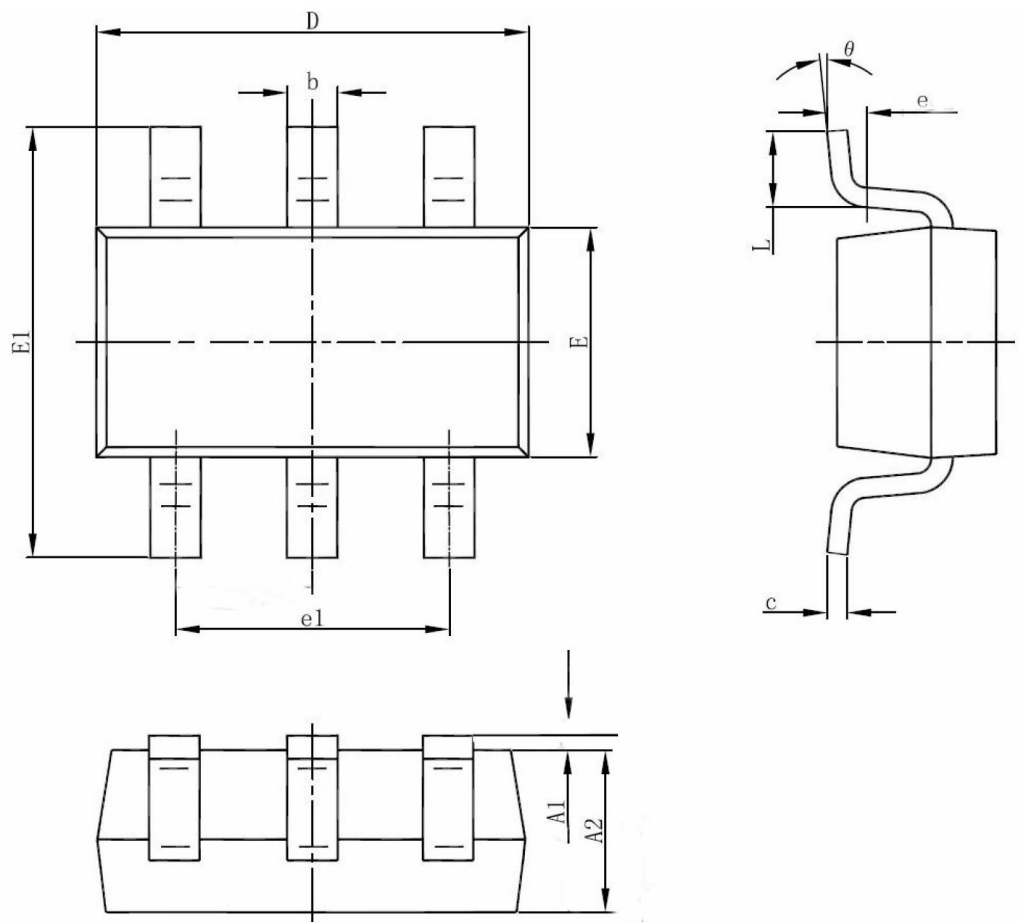


Figure 9. Normalized Maximum Transient Thermal Impedance



SOT-23-6 Dual Package Information



DIM	MIN	NOM	MAX
A1	0.00	-	0.10
A2	1.00	1.10	1.20
b	0.30	0.40	0.50
c	0.10	0.15	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
E1	2.60	2.80	3.00
e	0.2GAUGE PLANE		
e1	-	1.90	-
L	0.30	0.45	0.60
θ	0°	-	8°
All Dimensions in mm			