U_FPGA_IO
FPGA_IO.SchDoc

U_B2B_Connector
B2B_Connector.SchDoc

U_FPGA_MGT
FPGA_MGT.SchDoc

U_POWER
POWER.SchDoc

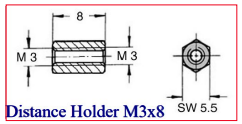
U_FPGA_MISC
FPGA_MISC.SchDoc

U_Revision
Revision Changes.SchDoc

Special notes:

Top of Board


Screw M3x4



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Screw M3x6

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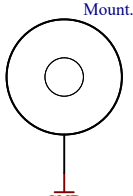
GND

Serial
Serial
Serialnumber 6,3 x 6.3mm

S/N
SN 1 0R 2 GND
0R

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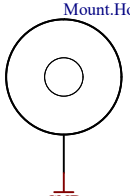
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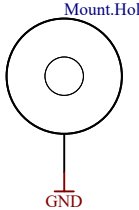
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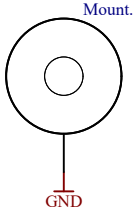
LOGO1
TE Logo PRINT Layer
LOGO PRINT

Mount.Hole 3.2mm

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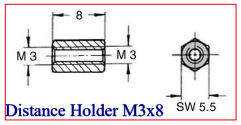
Screw M3x4



Distance Holder M3x8


Screw M3x6

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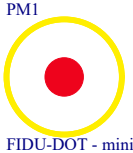
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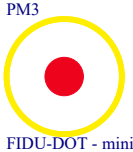
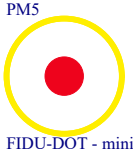
PM2

FIDU-DOT - mini

PM3

FIDU-DOT - mini

PM4

FIDU-DOT - mini

PM5

FIDU-DOT - mini

PM6

FIDU-DOT - mini

Assembly variant	35-2I
Created by	
Modified by	
Modified at	
SVN Revision	8634

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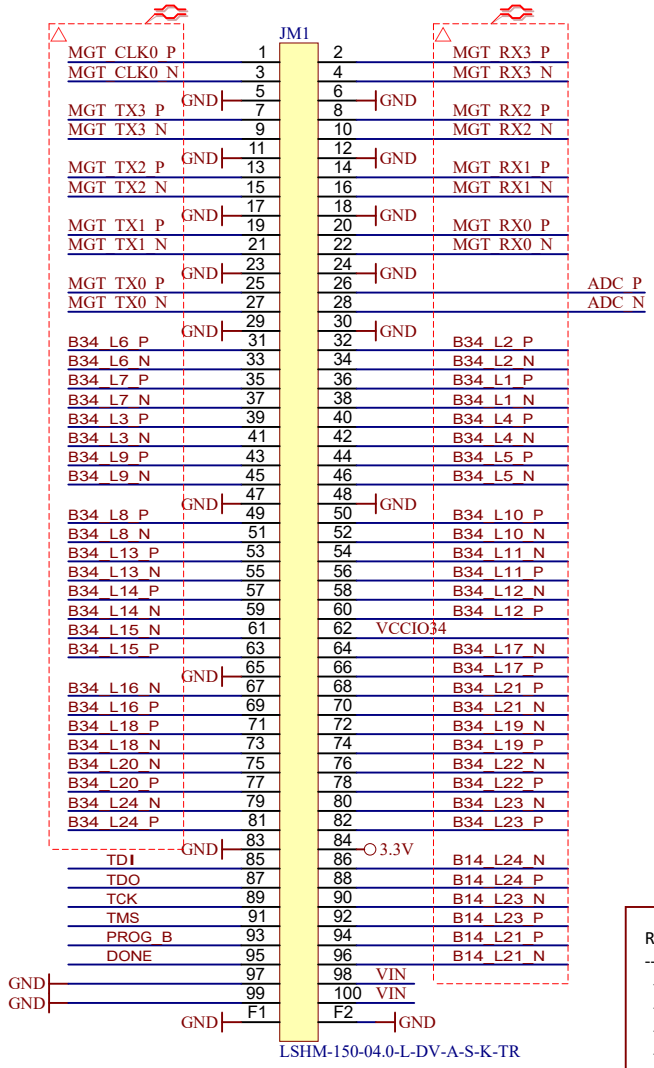
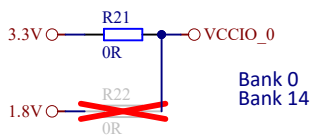
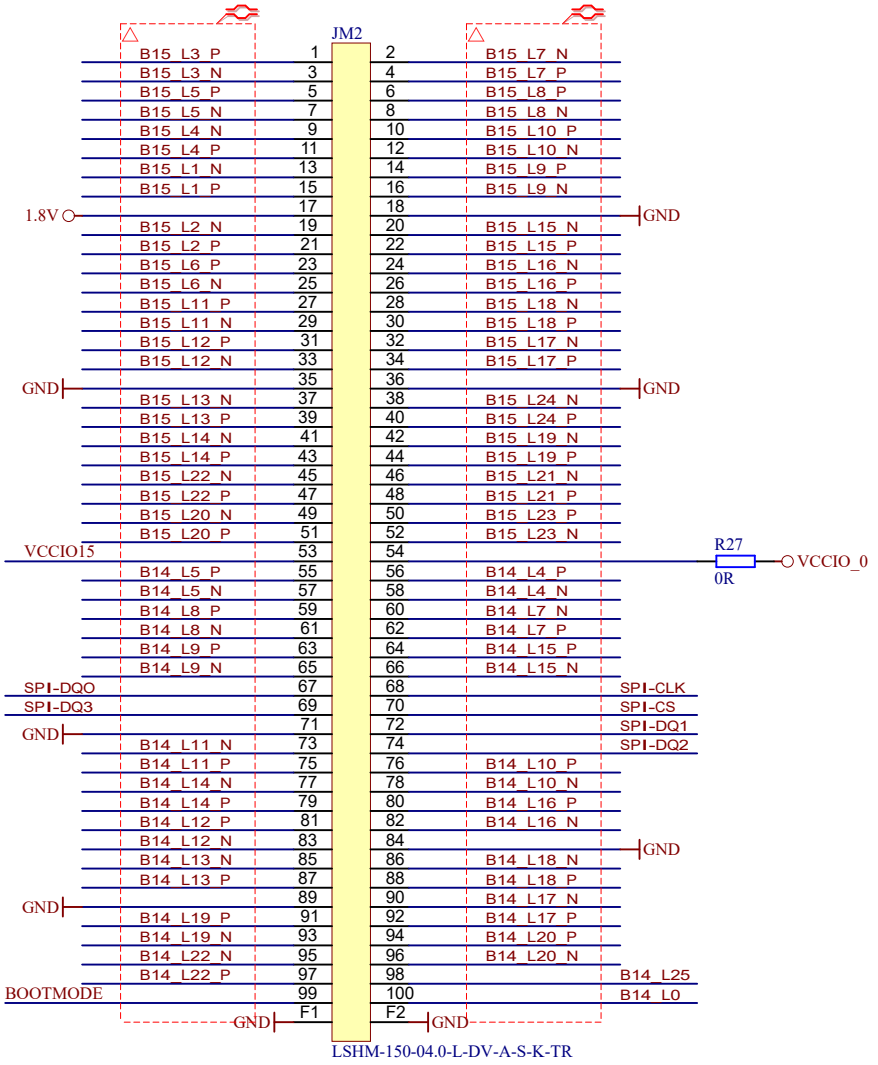
Title:	TE0714		
A4	Number:	TE0714 35-2I	Rev. 03
Date: 2019-02-14	Copyright: Trenz Electronic GmbH / TT		Page1 of 7
Filename:	TE0714.SchDoc		



R21	R22	R24	R25	R27	*JM2 pin 54 function
+	-	+	-	+	3.3V Power OUTPUT
-	+	-	+	+	1.8V Power OUTPUT
-	-	+	-	+	2.5V/3.3V Power Input
-	-	-	+	+	1.8V Power Input
?	?	?	?	-	Not connected





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Date: 2019-02-14	Copyright: Trenz Electronic GmbH / TT		Page2 of 7
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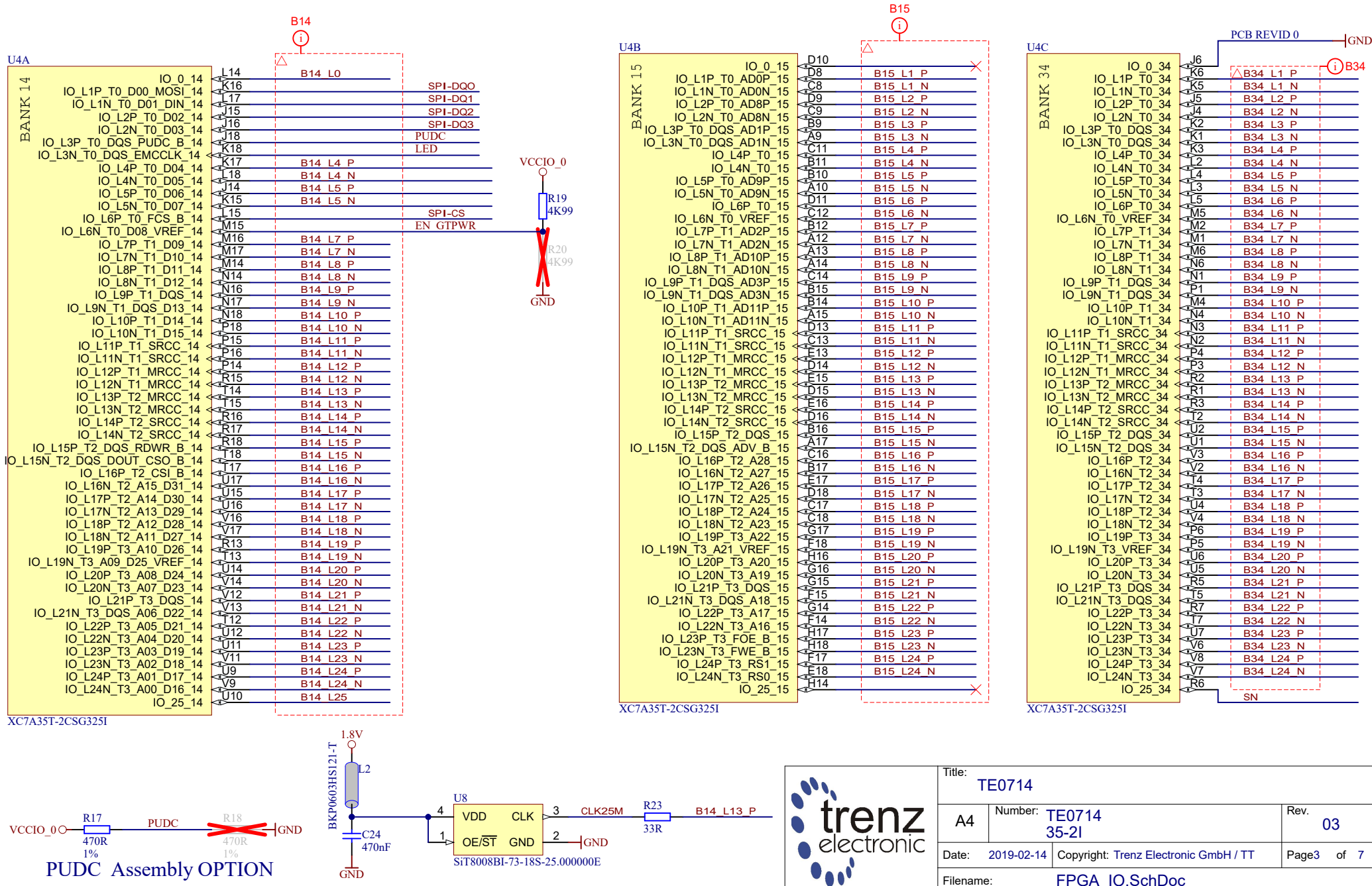
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U4A
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IO_L1N_T0_D01_DIN_14 L17 SPI-DQ1
IO_L2P_T0_D02_14 J15 SPI-DQ2
IO_L2N_T0_D03_14 J16 SPI-DQ3
IO_L3P_T0_DQS_PUDC_B_14 J18 PUDC
IO_L3N_T0_DQS_EMCCLK_14 K18 LED
IO_L4P_T0_D04_14 K17 B14_L4_P
IO_L4N_T0_D05_14 L18 B14_L4_N
IO_L5P_T0_D06_14 J14 B14_L5_P
IO_L5N_T0_D07_14 K15 B14_L5_N
IO_L6P_T0_FCS_B_14 L15 SPI-CS
IO_L6N_T0_D08_VREF_14 M15 EN_GTPWR
IO_L7P_T1_D09_14 M16 B14_L7_P
IO_L7N_T1_D10_14 M17 B14_L7_N
IO_L8P_T1_D11_14 M14 B14_L8_P
IO_L8N_T1_D12_14 N14 B14_L8_N
IO_L9P_T1_DQS_14 N16 B14_L9_P
IO_L9N_T1_DQS_D13_14 N17 B14_L9_N
IO_L10P_T1_D14_14 N18 B14_L10_P
IO_L10N_T1_D15_14 P18 B14_L10_N
IO_L11P_T1_SRCC_14 P15 B14_L11_P
IO_L11N_T1_SRCC_14 P16 B14_L11_N
IO_L12P_T1_MRCC_14 P14 B14_L12_P
IO_L12N_T1_MRCC_14 R15 B14_L12_N
IO_L13P_T2_MRCC_14 T14 B14_L13_P
IO_L13N_T2_MRCC_14 T15 B14_L13_N
IO_L14P_T2_SRCC_14 R16 B14_L14_P
IO_L14N_T2_SRCC_14 R17 B14_L14_N
IO_L15P_T2_DQS_RDWR_B_14 R18 B14_L15_P
IO_L15N_T2_DQS_DOUT_CSO_B_14 T18 B14_L15_N
IO_L16P_T2_CSI_B_14 T17 B14_L16_P
IO_L16N_T2_A15_D31_14 U17 B14_L16_N
IO_L17P_T2_A14_D30_14 U15 B14_L17_P
IO_L17N_T2_A13_D29_14 U16 B14_L17_N
IO_L18P_T2_A12_D28_14 V16 B14_L18_P
IO_L18N_T2_A11_D27_14 V17 B14_L18_N
IO_L19P_T3_A10_D26_14 R13 B14_L19_P
IO_L19N_T3_A09_D25_VREF_14 T13 B14_L19_N
IO_L20P_T3_A08_D24_14 U14 B14_L20_P
IO_L20N_T3_A07_D23_14 V14 B14_L20_N
IO_L21P_T3_DQS_14 V12 B14_L21_P
IO_L21N_T3_DQS_A06_D22_14 V13 B14_L21_N
IO_L22P_T3_A05_D21_14 T12 B14_L22_P
IO_L22N_T3_A04_D20_14 U12 B14_L22_N
IO_L23P_T3_A03_D19_14 U11 B14_L23_P
IO_L23N_T3_A02_D18_14 V11 B14_L23_N
IO_L24P_T3_A01_D17_14 V9 B14_L24_P
IO_L24N_T3_A00_D16_14 V9 B14_L24_N
IO_25_14 U10 B14_L25
XC7A35T-2CSG325I
VCCIO_0
R19 4K99
R20 4K99
GND
B15
U4B
BANK 15
IO_0_15 D10
IO_L1P_T0_AD0P_15 D8 B15_L1_P
IO_L1N_T0_AD0N_15 C8 B15_L1_N
IO_L2P_T0_AD8P_15 D9 B15_L2_P
IO_L2N_T0_AD8N_15 C9 B15_L2_N
IO_L3P_T0_DQS_AD1P_15 B9 B15_L3_P
IO_L3N_T0_DQS_AD1N_15 A9 B15_L3_N
IO_L4P_T0_15 C11 B15_L4_P
IO_L4N_T0_15 B11 B15_L4_N
IO_L5P_T0_AD9P_15 B10 B15_L5_P
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IO_L11N_T1_SRCC_15 C13 B15_L11_N
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IO_L23P_T3_FOE_B_15 H17 B15_L23_P
IO_L23N_T3_FWE_B_15 H18 B15_L23_N
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IO_L24N_T3_RS0_15 F18 B15_L24_N
IO_25_15 H14
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U4C
BANK 34
PCB REVID 0
GND
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IO_L1N_T0_34 K5 B34_L1_N
IO_L2P_T0_34 J5 B34_L2_P
IO_L2N_T0_34 J4 B34_L2_N
IO_L3P_T0_DQS_34 K2 B34_L3_P
IO_L3N_T0_DQS_34 K1 B34_L3_N
IO_L4P_T0_34 K3 B34_L4_P
IO_L4N_T0_34 J2 B34_L4_N
IO_L5P_T0_34 L4 B34_L5_P
IO_L5N_T0_34 L3 B34_L5_N
IO_L6P_T0_34 L5 B34_L6_P
IO_L6N_T0_VREF_34 M5 B34_L6_N
IO_L7P_T1_34 M2 B34_L7_P
IO_L7N_T1_34 M1 B34_L7_N
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VCCIO_0
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PUDC
R18 470R 1%
GND
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L2
C24 470nF
GND
U8
VDD CLK
OE/ST GND
SiT8008BI-73-18S-25.000000E
CLK25M
R23 33R
B14_L13_P
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Title: TE0714
A4
Number: TE0714 35-2I
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Date: 2019-02-14
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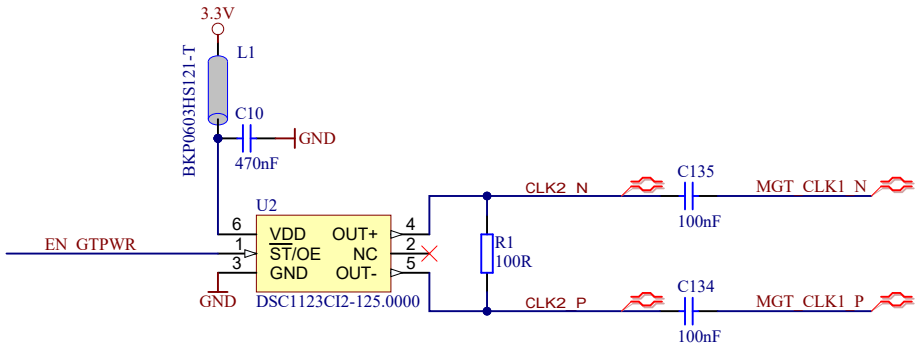
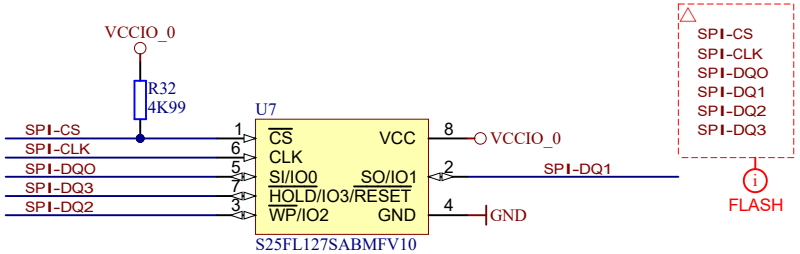
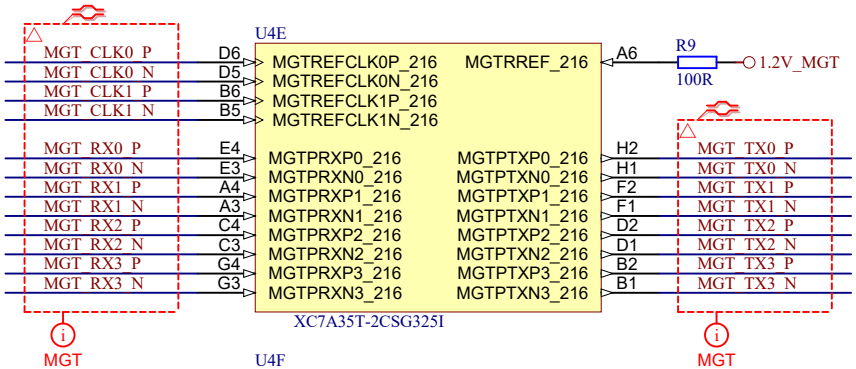
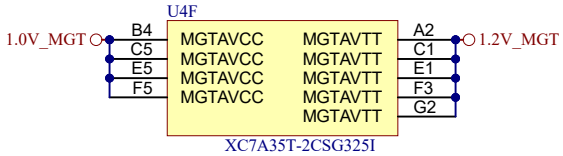
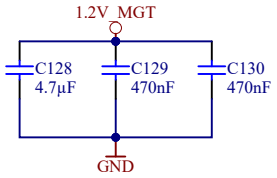
Filename: FPGA_IO.SchDoc

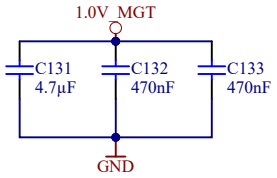












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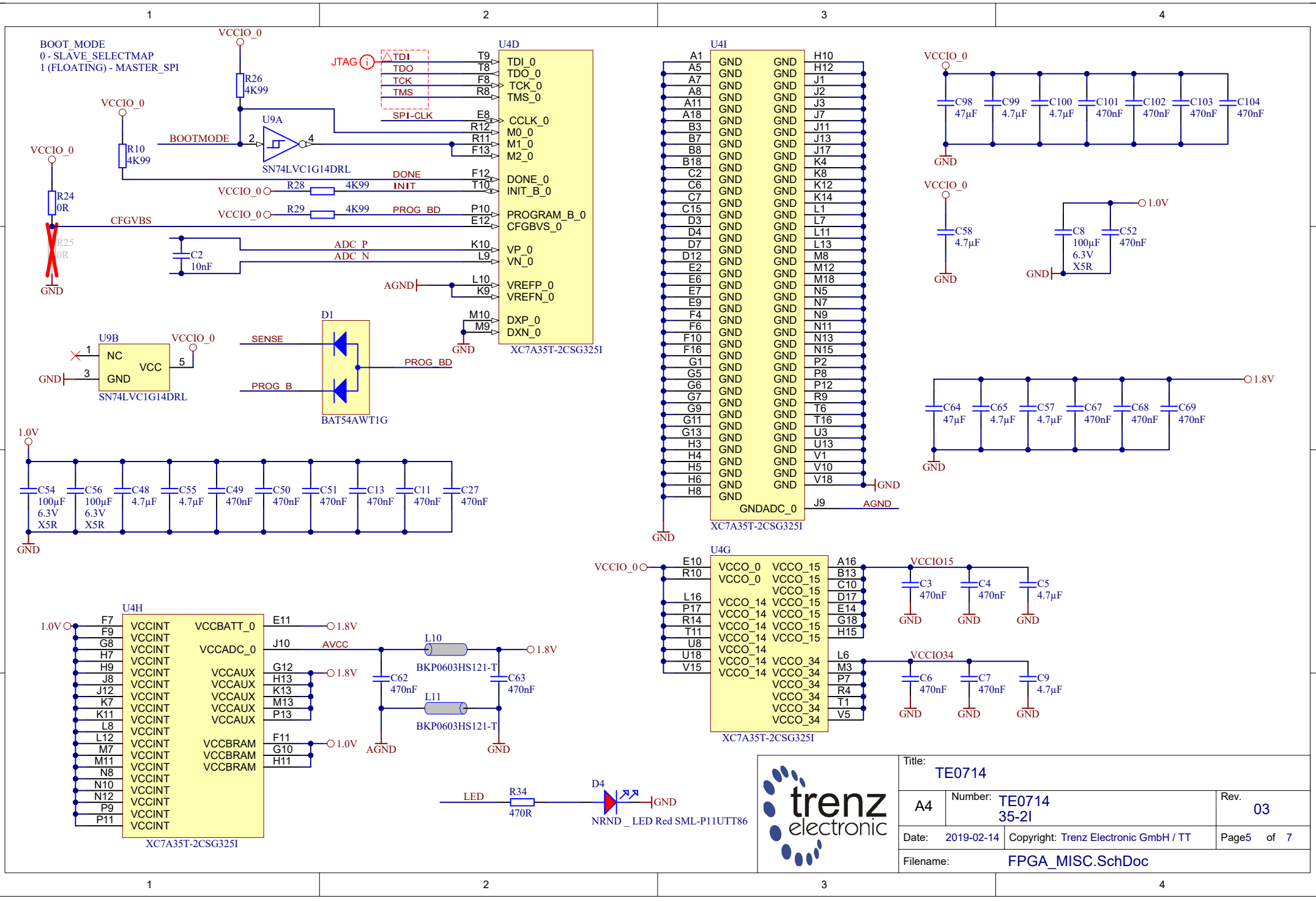

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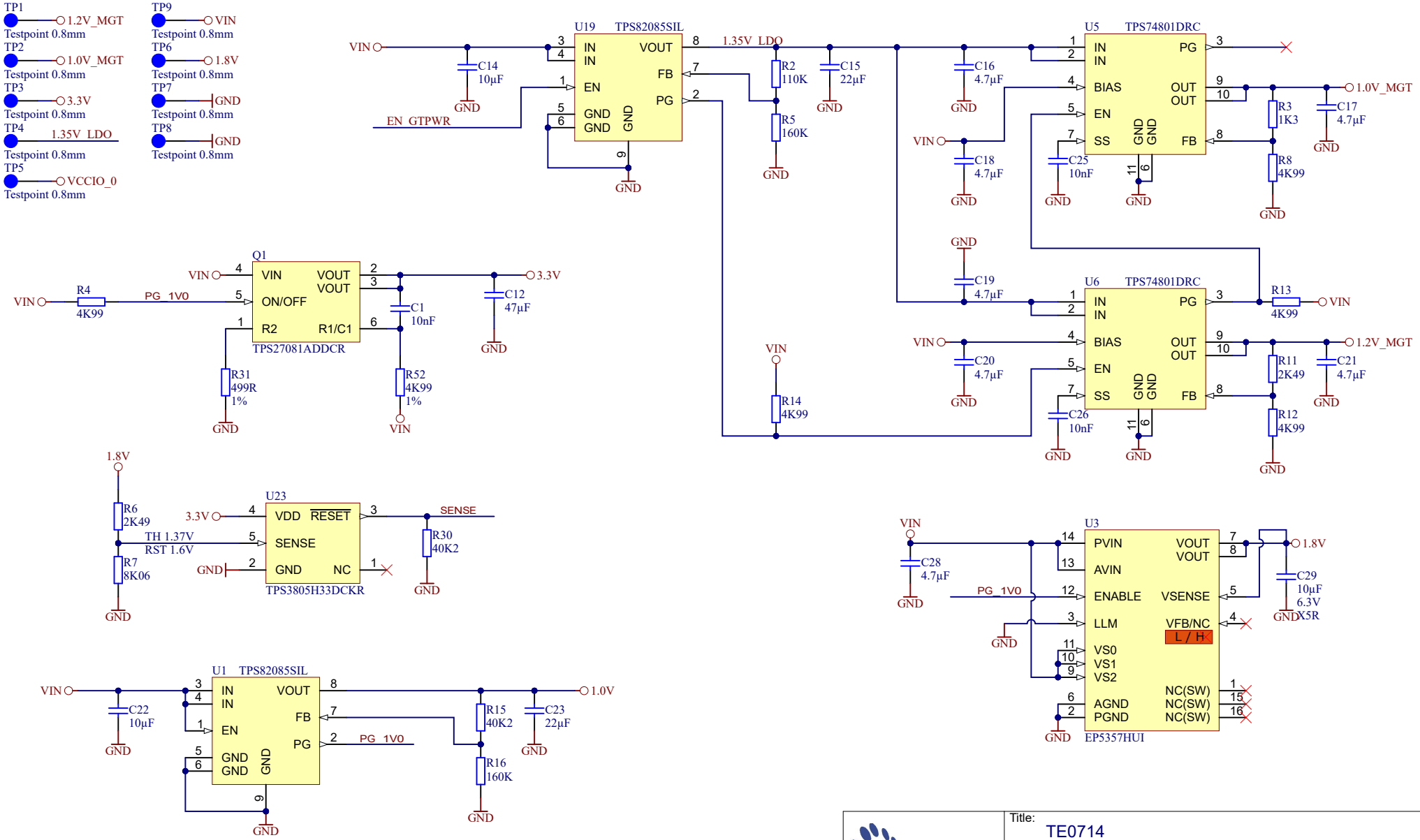

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Changes REV 02:

1. Added 0 ohm strap option to supply VCCIO0 on B2B connector
2. Added PCB Revision sense support. PCB Revision readout possible from HDL Design
3. Updated FPGA pin PROG_B connection. TPS3805H33 push-pull output RESET_N not affected on baseboard circuit, connected to PROG_B.
4. C8, C54, C56 updated to 100uF for variant 50-2I
5. Added testpoints

Changes REV 02A (12.2018):

1. New FLASH memory U7 S25FL127SABMFV10

Changes REV 03:

1) Changed obsolete component U3 (LXDC2HL18A-052 -> EP5357HUI)
2) DXP/DXN connected to GND (recommendation UG475, p31)
3) Added serial number to silk
4) Changed obsolet component Q1 (TPS27082LDDCR ->TPS27081ADDCR)
5) Full update LIB
6) Optimized testpoints placement

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