LSM6DSO16IS

Datasheet

iNEMO inertial module: always-on 3-axis accelerometer and 3-axis gyroscope with ISPU - intelligent sensor processing unit

LGA-14L
(2.5 x 3.0 x 0.83 mm) typ.

Product status link
LSM6DSO16IS

Product summary	
Order code	LSM6DSO16ISTR
Temperature range [°C]	-40 to +85
Package	LGA-14L (2.5 x 3 x 0.83 mm)
Packing	Tape and reel

Product resources
TN0018 (Design and soldering)

Product label
SUSTAINABLE TECHNOLOGY

Features

- 3-axis accelerometer with selectable full scale: ±2/±4/±8/±16 *g*
- 3-axis gyroscope with selectable full scale: ±125/±250/±500/±1000/±2000 dps
- Embedded ISPU: ultra-low-power, high-performance programmable core to execute signal processing and AI algorithms in the edge for a seamless digital-life experience
- Low-power consumption: 0.59 mA in high-performance mode, 0.46 mA in low-power mode (gyroscope + accelerometer only, ISPU not included)
- Low noise: 70 µg/√Hz in high-performance mode
- Sensor hub feature to efficiently collect data from additional external sensors (up to 4 external sensors)
- SPI / I²C serial interface
- Analog supply voltage: 1.71 V to 3.6 V with independent IO supply (1.62 V)
- Temperature range from -40 to +85 °C
- Embedded temperature sensor
- Compact footprint: 2.5 mm x 3 mm x 0.83 mm
- ECOPACK and RoHS compliant

Applications

- Complex motion detection and gesture recognition
- Activity recognition and tracking
- IoT and connected devices
- Wearables and smart watches for sports and personal health
- Smart pens, gaming and remote controllers

Description

The LSM6DSO16IS is a system-in-package featuring a 3-axis digital accelerometer and a 3-axis digital gyroscope, boosting performance at 0.59 mA in high-performance mode and enabling always-on low-power features for optimal motion results in personal electronics and IoT solutions.

The LSM6DSO16IS has a full-scale acceleration range of ±2/±4/±8/±16 *g* and an angular rate range of ±125/±250/±500/±1000/±2000 dps. The module features programmable interrupts and an on-chip sensor hub which includes up to 6 sensors: the internal accelerometer & gyroscope and 4 external sensors.

The LSM6DSO16IS embeds a new ST category of processing, ISPU (intelligent sensor processing unit) to support real-time applications that rely on sensor data. The ISPU is an ultra-low-power, high-performance programmable core which can execute signal processing and AI algorithms in the edge. The main benefits of the ISPU are C programming and an enhanced ecosystem with libraries and 3rd party tools/IDE.

Its optimized ultra-low-power hardware circuitry for real-time execution of the algorithms is a state-of-the-art feature for any personal electronics, from wearable accessories to high-end applications.

The LSM6DSO16IS is available in a plastic land grid array (LGA) package.

1 Overview

The LSM6DSO16IS is a system-in-package featuring a high-performance 3-axis digital accelerometer and 3-axis digital gyroscope which embeds an **ISPU (intelligent sensor processing unit)**.

ISPU is the new ST category of processing: it is an ultra-low-power, high-performance programmable core with high computational efficiency which can execute signal processing and AI algorithms on the real-time data from the sensor(s). It is compatible with the most common tools to enable flexible development and supports both machine learning and deep learning, offering broad options and freedom for programming.

ISPU is equipped with 32 KB of program RAM, 8 KB of data RAM and an FPU supporting addition, subtraction, and multiplication.

The LSM6DSO16IS features programmable interrupts and an on-chip sensor hub which includes up to six sensors: two internal (accelerometer and gyroscope) and four external sensors.

The sensor hub is accessible from the ISPU.

Like the entire portfolio of MEMS sensor modules, the LSM6DSO16IS leverages the robust and mature in-house manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the characteristics of the sensing element.

The LSM6DSO16IS is available in a small plastic land grid array (LGA) package of 2.5 x 3.0 x 0.83 mm to address ultra-compact solutions.

2 ISPU (intelligent sensor processing unit)

The LSM6DSO16IS embeds a general-purpose core, a new ST category of processing, called ISPU (intelligent sensor processing unit). The ISPU is based on STRED architecture, a proprietary architecture developed by STMicroelectronics. Its optimized ultra-low-power hardware circuitry for the real-time execution of the algorithms is a state-of-the-art feature for any personal electronics, from wearable accessories to high-end applications (for example, smartwatches, convertible laptops, smartphones, and so on).

A toolchain allows developing in C code and loading any custom program in the core, with the only limitation being the available memory size of the program.

Several algorithms running on the ISPU can generate interrupts to wake up the host processor accordingly.

The ISPU core includes an 8 KB RAM for data storage and a dedicated 32 KB RAM for program memory in order to have maximum configurability. The program of the ISPU, hosted in volatile memory, should be loaded at power-up of the device by an external host through the SPI/I²C interface.

The LSM6DSO16IS is internally organized as follows:

- the sensor core (with 8-bit registers) which communicates with the user over the SPI or I²C and handles the sensor features (from settings to outputs)
- the processing core: ISPU which is based on 32-bit registers and communicates with the user through the 8-bit interface registers of the sensor core

The registers that enable the exchange between the ISPU and the sensor core are:

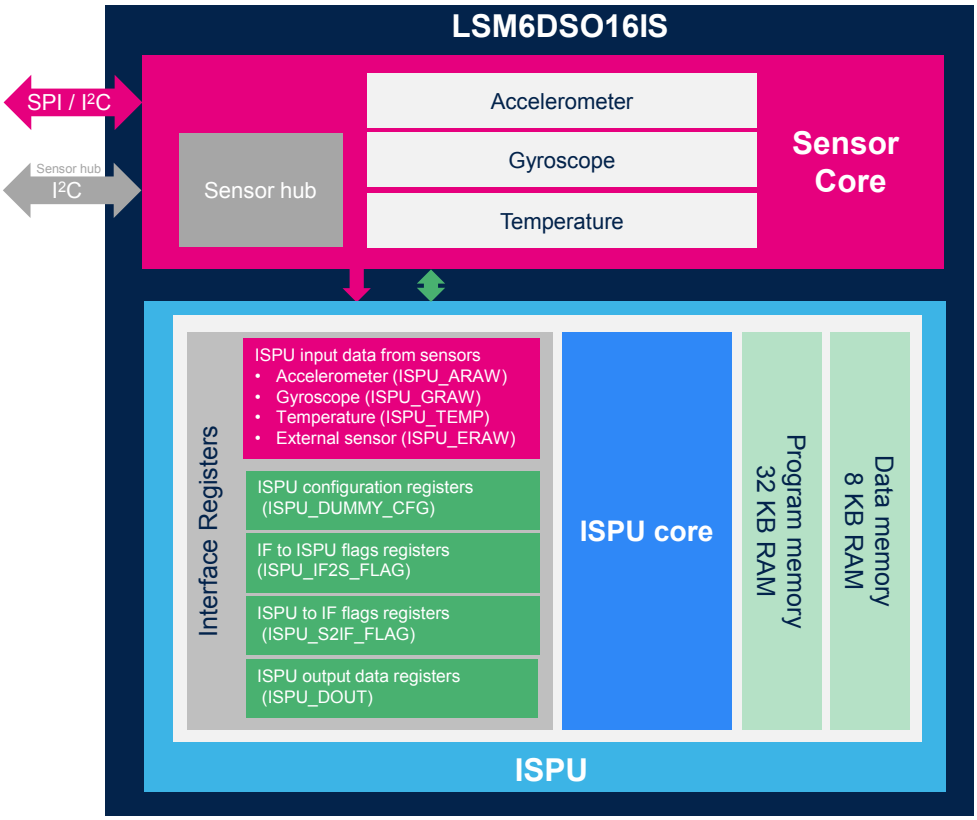
- ISPU reading accelerometer data ISPU_ARAW_X_L (6880h), ISPU_ARAW_X_H (6881h), ISPU_ARAW_Y_L (6884h), ISPU_ARAW_Y_H (6885h), ISPU_ARAW_Z_L (6888h), ISPU_ARAW_Z_H (6889h)
- ISPU reading gyroscope data ISPU_GRAW_X_L (688Ch), ISPU_GRAW_X_H (688Dh), ISPU_GRAW_Y_L (6890h), ISPU_GRAW_Y_L (6891h), ISPU_GRAW_Z_L (6894h), ISPU_GRAW_Z_H (6895h)
- ISPU reading external sensor data ISPU_ERAW_0_L (6898h), ISPU_ERAW_0_H (6899h), ISPU_ERAW_1_L (689Ch), ISPU_ERAW_1_H (689Dh), ISPU_ERAW_2_L (68A0h), ISPU_ERAW_2_H (68A1h)
- ISPU reading temperature sensor data ISPU_TEMP_L (68A4h), ISPU_TEMP_H (68A5h)

The data in the registers above comes from physical sensors (accelerometer, gyroscope, temperature and external sensors) in 16-bit two’s complement format, without any decoding.

There are 64-byte registers for general-purpose output data coming from the ISPU in registers ISPU_DOUT_00_L (10h), ISPU_DOUT_00_H (11h) through ISPU_DOUT_31_L (4Eh), ISPU_DOUT_31_H (4Fh).

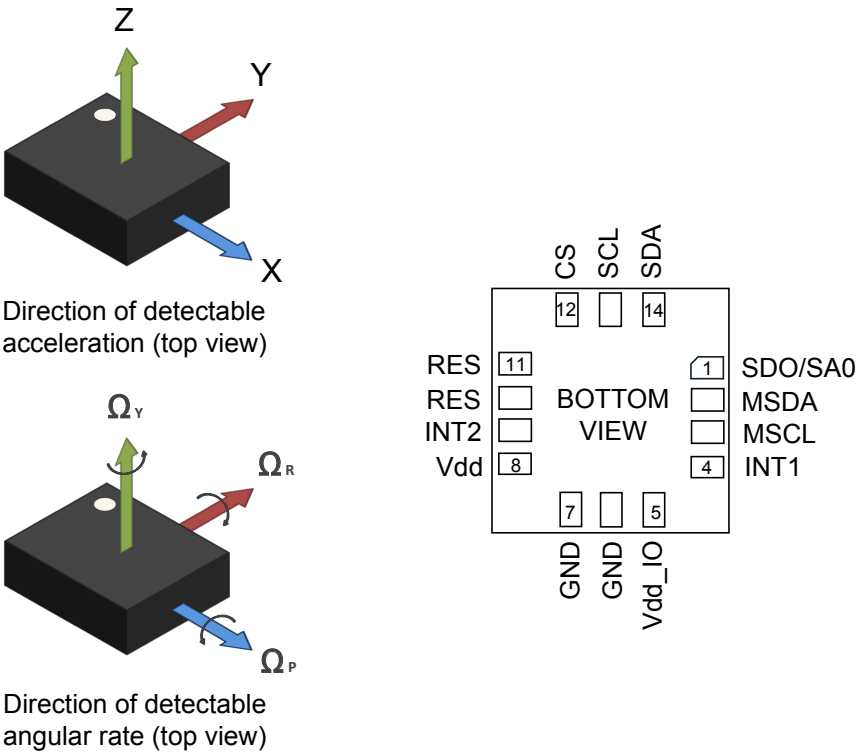
The device also provides four sets of 16-bit registers which can be used for loading input data (like algorithm configuration) for the ISPU in registers ISPU_DUMMY_CFG_1_L (73h) and ISPU_DUMMY_CFG_1_H (74h) through ISPU_DUMMY_CFG_4_L (79h) and ISPU_DUMMY_CFG_4_H (7Ah).

Figure 1. ISPU block diagram



3 Pin description

Figure 2. Pin connections

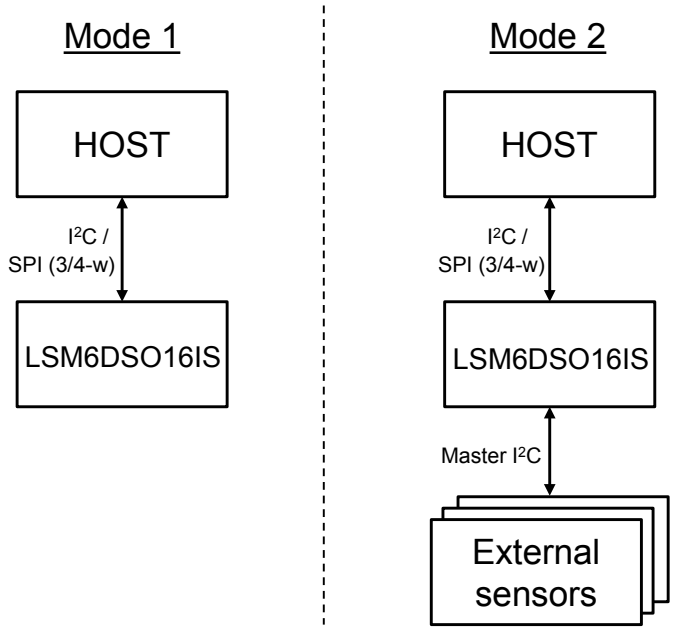


3.1 Pin connections

The LSM6DSO16IS offers flexibility to connect the pins in order to have two different mode connections and functionalities. In detail:

- **Mode 1**: I²C or SPI (3- and 4-wire) serial interface is available.
- **Mode 2**: I²C or SPI (3- and 4-wire) serial interface and I²C interface master for external sensor connections are available.

Figure 3. LSM6DSO16IS connection modes



In the following table each mode is described for the pin connections and function.

Table 1. Pin description

Pin#	Name	Mode 1 function	Mode 2 function
1	SDO/SA0	SPI 4-wire interface serial data output (SDO) I²C least significant bit of the device address (SA0)	
2	MSDA	Connect to Vdd_IO or GND	I²C serial data master (MSDA)
3	MSCL	Connect to Vdd_IO or GND	I²C serial clock master (MSCL)
4	INT1	Programmable interrupt 1	
5	Vdd_IO(1)	Power supply for I/O pins	
6	GND	0 V supply	
7	GND	0 V supply	
8	Vdd(1)	Power supply	
9	INT2	Programmable interrupt 2	Programmable interrupt 2 (INT2) I²C master external synchronization signal (MDRDY)
10	RES	Leave unconnected(2)	
11	RES	Connect to Vdd_IO or leave unconnected(2)	
12	CS	I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	
13	SCL	I²C serial clock (SCL) SPI serial port clock (SPC)	
14	SDA	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	

1. *Recommended 100 nF filter capacitor.*
2. *Leave pin electrically unconnected and soldered to PCB.*

4 Module specifications

4.1 Mechanical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

Table 2. Mechanical characteristics

Symbol	Parameter	Test conditions	Min. (1)	Typ. (2)	Max. (1)	Unit
LA_FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
G_FS	Angular rate measurement range			±125		dps
				±250		
				±500		
				±1000		
				±2000		
LA_So	Linear acceleration sensitivity(3)	FS = ±2 *g*		0.061		mg/LSB
		FS = ±4 *g*		0.122		
		FS = ±8 *g*		0.244		
		FS = ±16 *g*		0.488		
G_So	Angular rate sensitivity(3)	FS = ±125 dps		4.375		mdps/LSB
		FS = ±250 dps		8.75		
		FS = ±500 dps		17.50		
		FS = ±1000 dps		35		
		FS = ±2000 dps		70		
G_So%	Sensitivity tolerance(4)	at component level, T = 25 °C		±1		%
LA_So%	Sensitivity tolerance(4)	at component level, T = 25 °C		±1		%
LA_SoDr	Linear acceleration sensitivity change vs. temperature(5)	from -40° to +85°		±0.01		%/°C
G_SoDr	Angular rate sensitivity change vs. temperature(5)	from -40° to +85°		±0.01		%/°C
LA_TyOff	Linear acceleration zero-*g* level offset accuracy(4)	T = 25 °C		±40		mg
G_TyOff	Angular rate zero-rate level(4)	T = 25 °C		±3		dps
LA_OffDr	Linear acceleration zero-*g* level change vs. temperature(5)	from -40° to +85°		±0.1		mg/ °C
G_OffDr	Angular rate typical zero-rate level change vs. temperature(5)	from -40° to +85°		±0.015		dps/°C
Rn	Rate noise density in high-performance mode(6)			3.4		mdps/√Hz
RnRMS	Gyroscope RMS noise in low-power mode(7)			75		mdps
An	Acceleration noise density in high-performance mode(8)	FS = ±2 *g*		70		µg/√Hz
		FS = ±4 *g*		75		
		FS = ±8 *g*		85		
		FS = ±16 *g*		110		
RMS	Acceleration RMS noise in low-power mode(9)(10)	FS = ±2 *g*		1.8		mg(RMS)
		FS = ±4 *g*		2.0		
		FS = ±8 *g*		2.4		

Symbol	Parameter	Test conditions	Min. (1)	Typ.(2)	Max. (1)	Unit
RMS	Acceleration RMS noise in low-power mode(9)(10)	FS = ±16 *g*		3.0		mg(RMS)
LA_ODR	Linear acceleration output data rate			1.6(11) 12.5 26 52 104 208 416 833 1667 3333 6667		Hz
G_ODR	Angular rate output data rate			12.5 26 52 104 208 416 833 1667 3333 6667		
Vst	Linear acceleration self-test output change(12)(13)(14)		50		1700	mg
	Angular rate self-test output change(15)(16)	FS = ±250 dps	20		80	dps
		FS = ±2000 dps	150		700	dps
Top	Operating temperature range		-40		+85	°C

1. *Min/Max values are based on characterization results at 3σ on a limited number of samples, not tested in production and not guaranteed.*
2. *Typical specifications are not guaranteed.*
3. *Sensitivity values after factory calibration test and trimming.*
4. *Values after factory calibration test and trimming.*
5. *Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples. Not measured during final test for production.*
6. *Gyroscope rate noise density in high-performance mode is independent of the ODR and FS setting.*
7. *Gyroscope RMS noise in low-power mode is independent of the ODR and FS setting.*
8. *Accelerometer noise density in high-performance mode is independent of the ODR.*
9. *Accelerometer RMS noise in low-power mode is independent of the ODR.*
10. *Noise RMS related to BW = ODR/2.*
11. *This ODR is available when the accelerometer is in low-power mode.*
12. *The sign of the linear acceleration self-test output change is defined by the STx_XL bits in a dedicated register for all axes.*
13. *The linear acceleration self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 0.061 mg at ±2 g full scale.*
14. *Accelerometer self-test limits are full-scale independent.*
15. *The sign of the angular rate self-test output change is defined by the STx_G bits in a dedicated register for all axes.*
16. *The angular rate self-test output change is defined with the device in stationary condition as the absolute value of: OUTPUT[LSb] (self-test enabled) - OUTPUT[LSb] (self-test disabled). 1LSb = 70 mdps at ±2000 dps full scale.*

4.2 Electrical characteristics

@ Vdd = 1.8 V, T = 25 °C, unless otherwise noted.

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
Vdd	Supply voltage		1.71	1.8	3.6	V
Vdd_IO	Power supply for I/O		1.62		3.6	V
IddHP	Gyroscope and accelerometer current consumption in high-performance mode(3)			595		µA
IddLP	Gyroscope and accelerometer current consumption in low-power mode(3)	ODR = 208 Hz		465		µA
G_IddHP	Gyroscope current consumption in high-performance mode(3)			490		µA
G_IddLP	Gyroscope current consumption in low-power mode(3)	ODR = 52 Hz ODR = 12.5 Hz		320 290		µA
LA_IddHP	Accelerometer current consumption in high-performance mode(3)			180		µA
LA_IddLP	Accelerometer current consumption in low-power mode(3)	ODR = 52 Hz ODR = 1.6 Hz		37 15		µA
IddPD	Gyroscope and accelerometer current consumption during power-down			6		µA
Ton	Turn-on time			35		ms
V_{IH}	Digital high-level input voltage		0.7 * Vdd_IO			V
V_{IL}	Digital low-level input voltage				0.3 * Vdd_IO	V
V_{OH}	High-level output voltage	I_{OH} = 4 mA(4)	Vdd_IO - 0.2			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA(4)			0.2	V
Top	Operating temperature range		-40		+85	°C

1. *Min/Max values are based on characterization results at 3σ on a limited number of samples, not tested in production and not guaranteed.*
2. *Typical specifications are not guaranteed.*
3. *Current consumption is intended for accelerometer and gyroscope sensors only, ISPU consumption is not taken into account.*
4. *4 mA is the maximum driving capability, that is, the maximum DC current that can be sourced/sunk by the digital pin in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.*

4.3 Temperature sensor characteristics

@ Vdd = 1.8 V, T = 25 °C unless otherwise noted.

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.(1)	Typ.(2)	Max.(1)	Unit
TODR(3)	Temperature refresh rate			52		Hz
Toff	Temperature offset(4)		-15		+15	°C
TSen	Temperature sensitivity			256		LSB/°C
TST	Temperature stabilization time(5)				500	µs
T_ADC_res	Temperature ADC resolution			16		bit
Top	Operating temperature range		-40		+85	°C

1. *Min/Max values are based on characterization results at 3σ on a limited number of samples, not tested in production and not guaranteed.*
2. *Typical specifications are not guaranteed.*
3. *When the accelerometer is in low-power mode and the gyroscope part is turned off, the TODR value is equal to the accelerometer ODR.*
4. *The output of the temperature sensor is 0 LSB (typ.) at 25 °C.*
5. *Time from power ON to valid data based on characterization data.*

4.4 Communication interface characteristics

4.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top. @ Vdd_IO = 1.8 V, T = 25 °C unless otherwise noted.

Table 5. SPI slave timing values

Symbol	Parameter	Value(1)			Unit
		Min	Typ	Max	
$f_{c(SPC)}$	SPI clock frequency			10	MHz
$t_{c(SPC)}$	SPI clock period			100	ns
$t_{high(SPC)}$	SPI clock high	45			
$t_{low(SPC)}$	SPI clock low	45			
$t_{su(CS)}$	CS setup time (mode 3)	5			
	CS setup time (mode 0)	20			
$t_{h(CS)}$	CS hold time (mode 3)	20			
	CS hold time (mode 0)	20			
$t_{su(SI)}$	SDI input setup time	5			
$t_{h(SI)}$	SDI input hold time	15			
$t_{v(SO)}$	SDO valid output time		15	25	
$t_{dis(SO)}$	SDO output disable time			50	
C_{load}	Bus capacitance			100	pF

1. *Values are evaluated at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production*

Figure 4. SPI slave timing in mode 0

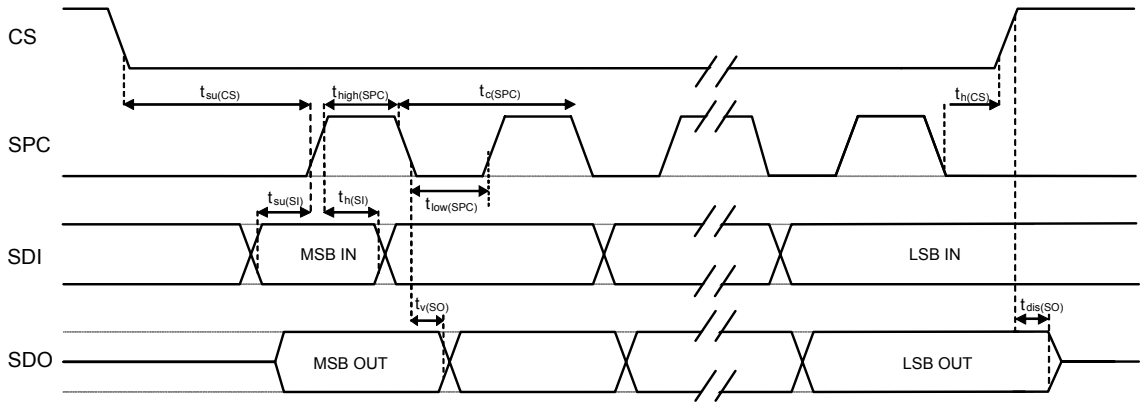
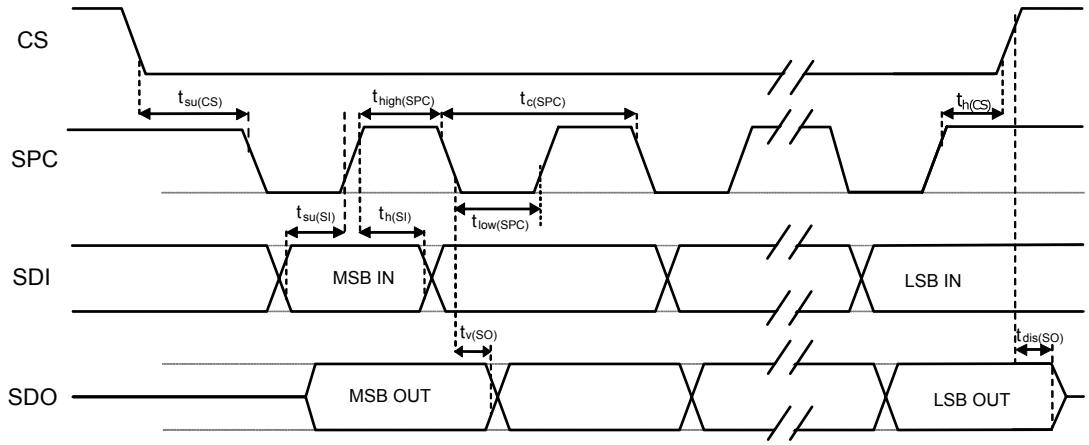


Figure 5. SPI slave timing in mode 3



Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both input and output ports.

4.4.2 I²C - inter-IC control interface

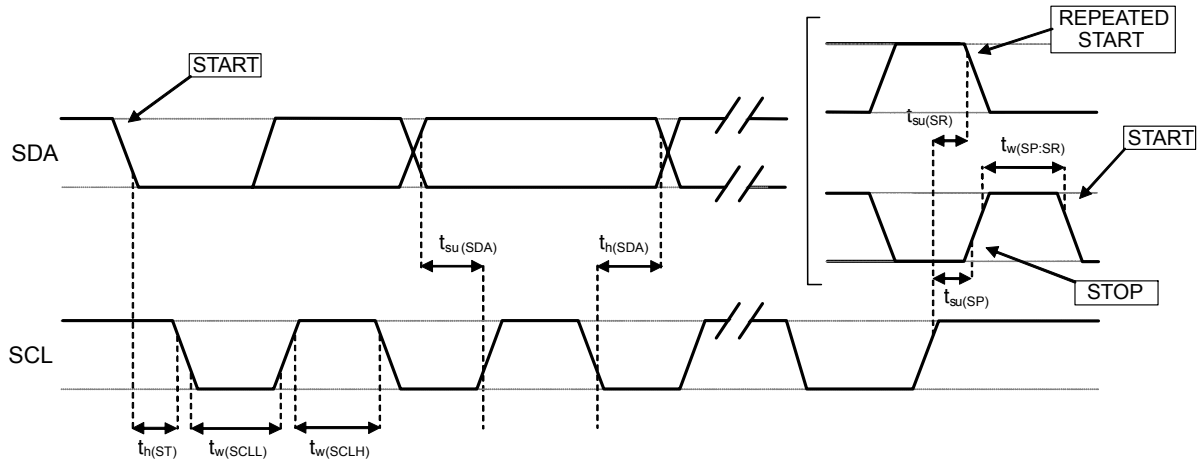
Subject to general operating conditions for Vdd and Top.

Table 6. I²C slave timing values

Symbol	Parameter	I²C fast mode(1)(2)		I²C fast mode plus(1)(2)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	400	0	1000	kHz
$t_{w(SCLL)}$	SCL clock low time	1.3		0.5		µs
$t_{w(SCLH)}$	SCL clock high time	0.6		0.26		
$t_{su(SDA)}$	SDA setup time	100		50		ns
$t_{h(SDA)}$	SDA data hold time	0	0.9	0		µs
$t_{h(ST)}$	START/REPEATED START condition hold time	0.6		0.26		
$t_{su(SR)}$	REPEATED START condition setup time	0.6		0.26		
$t_{su(SP)}$	STOP condition setup time	0.6		0.26		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	1.3		0.5		
	Data valid time		0.9		0.45	
	Data valid acknowledge time		0.9		0.45	
C_B	Capacitive load for each bus line		400		550	pF

1. *Data based on standard I²C protocol requirement, not tested in production.*
2. *Data for I²C fast mode and I²C fast mode plus have been validated by characterization, not tested in production.*

Figure 6. I²C slave timing diagram



Note: Measurement points are done at 0.3·Vdd_IO and 0.7·Vdd_IO for both ports.

4.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration *g* for 0.2 ms	10,000	*g*
ESD	Electrostatic discharge protection (HBM)	2	kV
Vin	Input voltage on any control pin (including CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

4.6 Terminology

4.6.1 Sensitivity

Linear acceleration sensitivity can be determined, for example, by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors (see Table 2).

An angular rate gyroscope is a device that produces a positive-going digital output for counterclockwise rotation around the axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time (see Table 2).

4.6.2 Zero-*g* and zero-rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface measures 0 *g* on both the X-axis and Y-axis, whereas the Z-axis measures 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as a two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in Table 2. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Zero-rate level describes the actual output signal if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time (see Table 2).

5 Digital interfaces

5.1 I²C/SPI interface

The registers embedded inside the LSM6DSO16IS may be accessed through both the I²C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode. The device is compatible with SPI modes 0 and 3.

The serial interfaces are mapped onto the same pins. To select/exploit the I²C interface, the CS line must be tied high (that is, connected to Vdd_IO).

Table 8. Serial interface pin description

Pin name	Pin description
CS	Enables SPI I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)
SCL/SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
SDA/SDI/SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO/SA0	SPI serial data output (SDO) I²C less significant bit of the device address

5.1.1 I²C serial interface

The LSM6DSO16IS I²C is a bus slave. The I²C is employed to write the data to the registers, whose content can also be read back.

The relevant I²C terminology is provided in the table below.

Table 9. I²C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I²C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both the lines are high.

The I²C interface is implemented with fast mode (400 kHz) I²C standards as well as with fast mode plus (1000 kHz).

In order to disable the I²C block, (I2C_disable) = 1 must be written in CTRL4_C (13h).

5.1.1.1 I²C operation

The transaction on the bus is started through a start (ST) signal. A start condition is defined as a high to low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LSM6DSO16IS is 110101xb. The SDO/SA0 pin can be used to modify the less significant bit of the device address. If the SDO/SA0 pin is connected to the supply voltage, LSb is 1 (address 1101011b); else if the SDO/SA0 pin is connected to ground, the LSb value is 0 (address 1101010b). This solution permits to connect and address two different inertial modules to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LSM6DSO16IS behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit subaddress (SUB) is transmitted. The increment of the address is configured by the CTRL3_C (12h) (IF_INC).

The slave address is completed with a read/write bit. If the bit is 1 (read), a repeated start (SR) condition must be issued after the two subaddress bytes. If the bit is 0 (write) the master transmits to the slave with direction unchanged. Table 10 explains how the SAD + read/write bit pattern is composed, listing all the possible configurations.

Table 10. SAD + read/write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 11. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 12. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 13. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 14. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a slave receiver doesn't acknowledge the slave address (that is, it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low to high transition on the SDA line while the SCL line is high is defined as a stop condition. Each data transfer must be terminated by the generation of a stop (SP) condition.

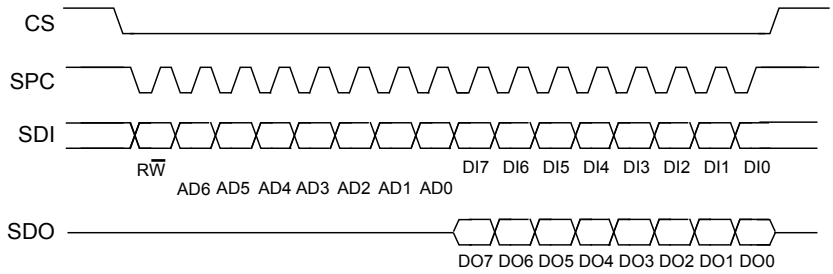
In the presented communication format MAK is master acknowledge and NMAK is no master acknowledge.

5.1.2 SPI bus interface

The LSM6DSO16IS SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface communicates to the application using 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 7. Read and write protocol (in mode 3)



CS enables the serial port and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are, respectively, the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: $\overline{RW}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip drives **SDO** at the start of bit 8.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written into the device (MSb first).

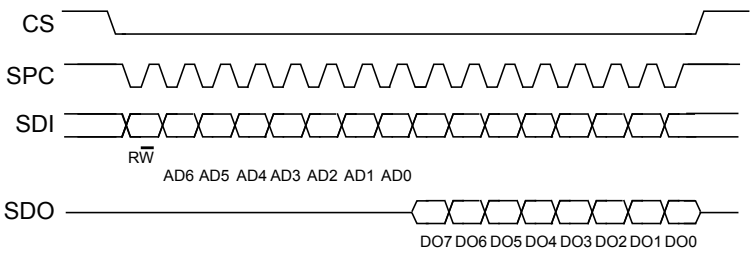
bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods are added. When the CTRL3_C (12h) (IF_INC) bit is 0, the address used to read/write data remains the same for every block. When the CTRL3_C (12h) (IF_INC) bit is 1, the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.1.2.1 SPI read

Figure 8. SPI read protocol (in mode 3)



The SPI read command is performed with 16 clock pulses. A multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

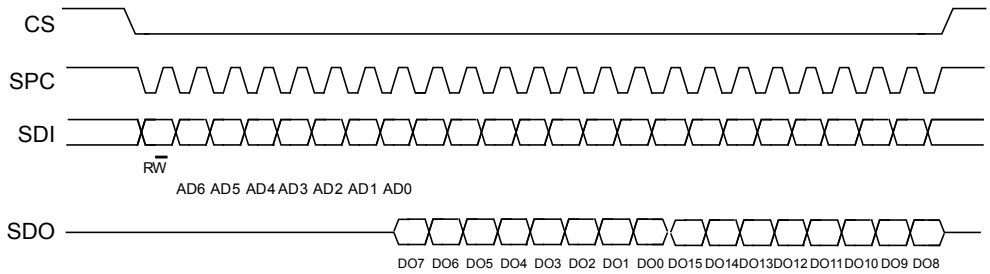
bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

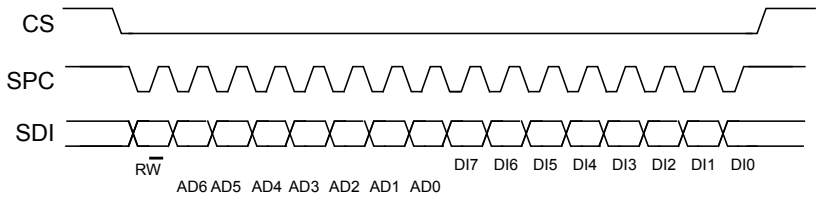
bit 16-...: data DO(...-8). Further data in multiple byte reads.

Figure 9. Multiple byte SPI read protocol (2-byte example) (in mode 3)



5.1.2.2 SPI write

Figure 10. **SPI write protocol (in mode 3)**



The SPI write command is performed with 16 clock pulses. A multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

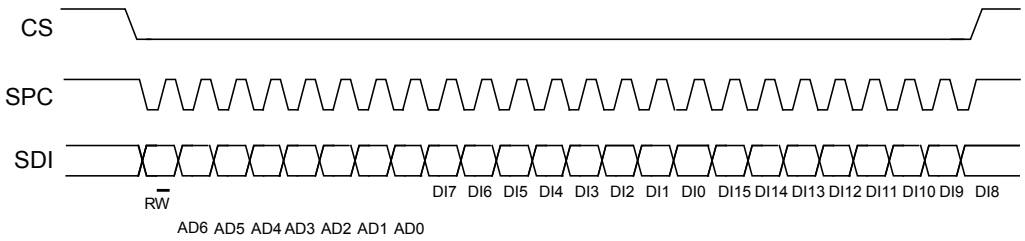
bit 0: WRITE bit. The value is 0.

bit 1 -7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

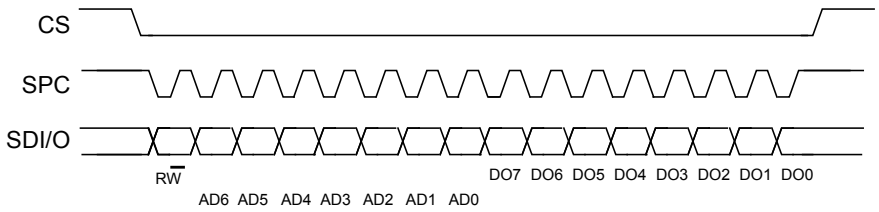
Figure 11. **Multiple byte SPI write protocol (2-byte example) (in mode 3)**



5.1.2.3 *SPI read in 3-wire mode*

A 3-wire mode is entered by setting the CTRL3_C (12h) (SIM) bit equal to 1 (SPI serial interface mode selection).

Figure 12. SPI read protocol in 3-wire mode (in mode 3)



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that is read from the device (MSb first).

A multiple read command is also available in 3-wire mode.

5.2 Master I²C interface

If the LSM6DSO16IS is configured in mode 2, a master I²C line is available. The master serial interface is mapped in the following dedicated pins.

Table 15. Master I²C pin details

Pin name	Pin description
MSCL	I²C serial clock master
MSDA	I²C serial data master
MDRDY	I²C master external synchronization signal

6 Functionality

6.1 Operating modes

In the LSM6DSO16IS, the accelerometer and the gyroscope can be turned on/off independently of each other and are allowed to have different ODRs and power modes.

The LSM6DSO16IS has three operating modes available:

- only accelerometer active and gyroscope in power-down
- only gyroscope active and accelerometer in power-down
- both accelerometer and gyroscope sensors active with independent ODR

The accelerometer is activated from power-down by writing ODR_XL[3:0] in CTRL1_XL (10h) while the gyroscope is activated from power-down by writing ODR_G[3:0] in CTRL2_G (11h). For combo-mode the ODRs are totally independent.

6.2 Accelerometer power modes

In the LSM6DSO16IS, the accelerometer can be configured in three different operating modes: power-down, low-power, and high-performance mode. The operating mode selected depends on the value of the XL_HM_MODE bit in CTRL6_C (15h). If XL_HM_MODE is set to 0, high-performance mode is valid for all ODRs (from 12.5 Hz up to 6667 Hz).

To enable low-power mode, the XL_HM_MODE bit has to be set to 1. Low-power mode is available for ODRs of 1.6, 12.5, 26, 52, 104, 208 Hz.

6.3 Gyroscope power modes

In the LSM6DSO16IS, the gyroscope can be configured in three different operating modes: power-down, low-power, and high-performance mode. The operating mode selected depends on the value of the G_HM_MODE bit in CTRL7_G (16h). If G_HM_MODE is set to 0, high-performance mode is valid for all ODRs (from 12.5 Hz up to 6667 Hz).

To enable low-power mode, the G_HM_MODE bit has to be set to 1. Low-power mode is available for ODRs of 12.5, 26, 52, 104, 208 Hz.

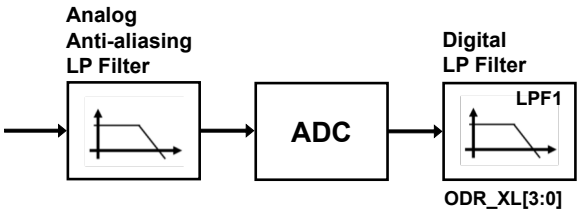
6.4 Block diagram of filters

6.4.1 Block diagram of the accelerometer filters

In the LSM6DSO16IS, the filtering chain for the accelerometer part is composed of the following:

- Analog filter (anti-aliasing)
- Digital low-pass filter (LPF1)

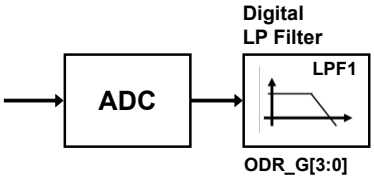
Figure 13. Accelerometer filters



6.4.2 Block diagram of the gyroscope filter

In the LSM6DSO16IS, the filtering chain for the gyroscope part is composed of a digital low-pass filter (LPF1).

Figure 14. Gyroscope filter



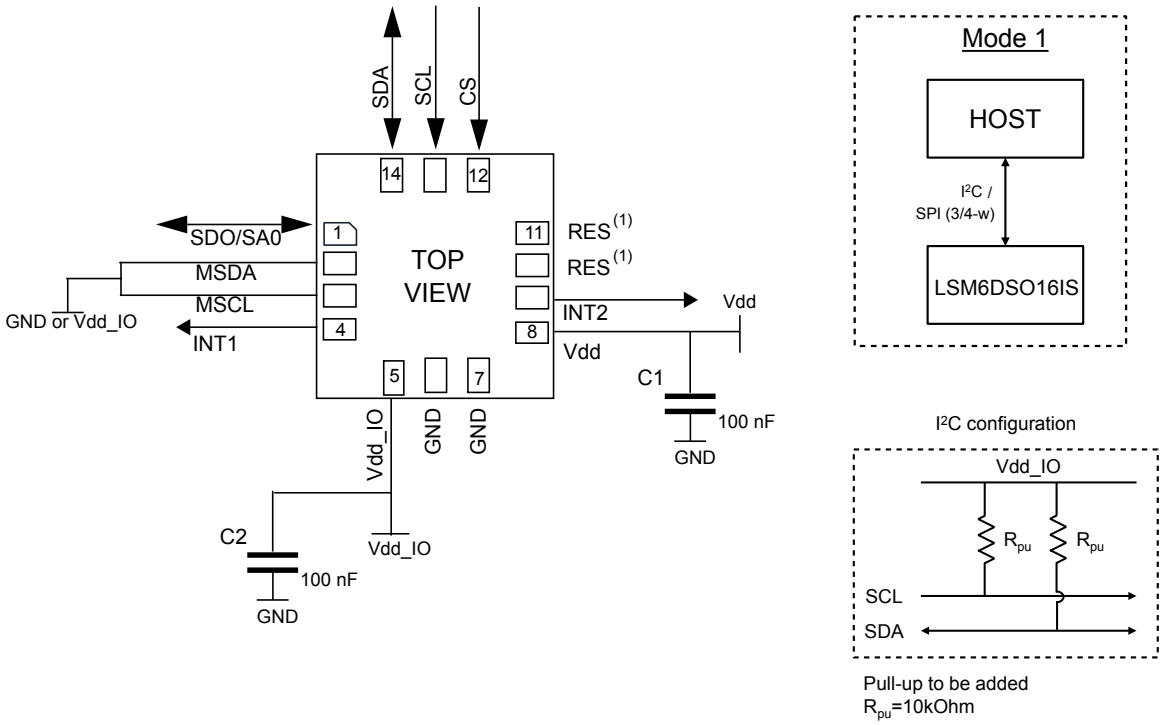
6.5 Temperature sensor

The temperature is available in OUT_TEMP_L (20h), OUT_TEMP_H (21h) stored as two's complement data. Refer to Table 4. Temperature sensor characteristics for the conversion factor.

7 Application hints

7.1 LSM6DSO16IS electrical connections in mode 1

Figure 15. **LSM6DSO16IS electrical connections in mode 1**



1. Leave pin electrically unconnected and soldered to PCB.

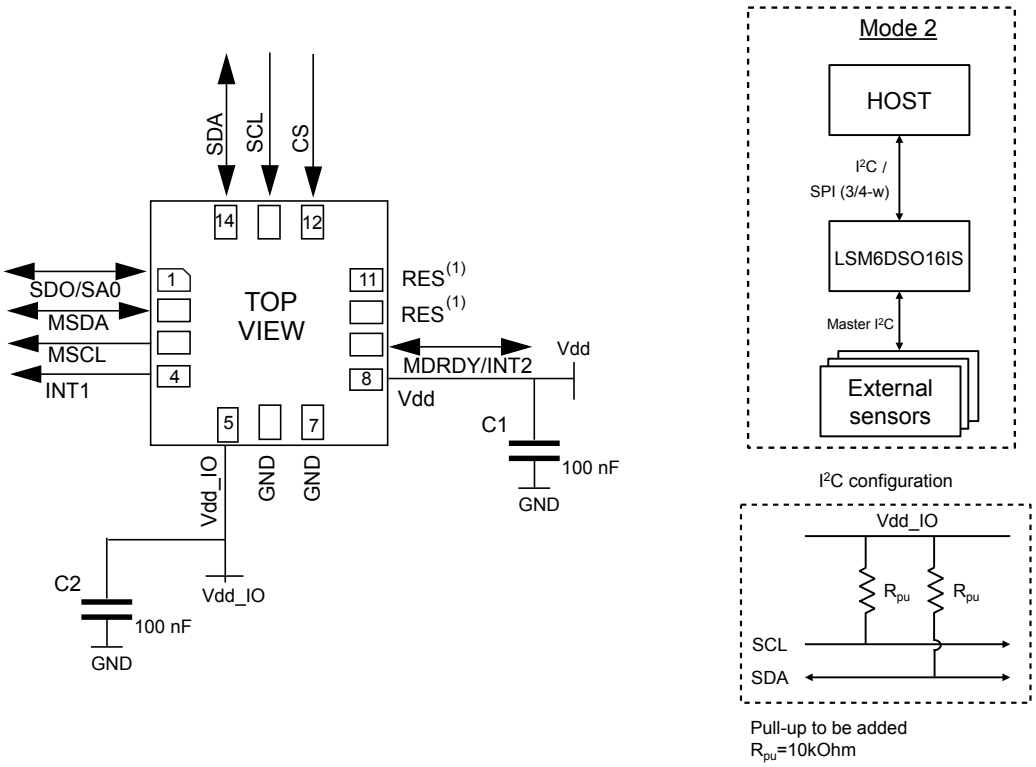
The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C interface.

7.2 LSM6DSO16IS electrical connections in mode 2

Figure 16. LSM6DSO16IS electrical connections in mode 2



1. Leave pin electrically unconnected and soldered to PCB.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration/angular rate data is selectable and accessible through the SPI/I²C primary interface.

The functions, the threshold and the timing of the two interrupt pins for each sensor can be completely programmed by the user through the SPI/I²C primary interface.

Table 16. Internal pin status

Pin #	Name	Mode 1 function	Mode 2 function	Pin status - mode 1	Pin status - mode 2
1	SDO	SPI 4-wire interface serial data output (SDO)	SPI 4-wire interface serial data output (SDO)	Default: input without pull-up Pull-up is enabled if bit SDO_PU_EN = 1 in PIN_CTRL (02h).	Default: input without pull-up Pull-up is enabled if bit SDO_PU_EN = 1 in PIN_CTRL (02h).
	SA0	I²C least significant bit of the device address (SA0)	I²C least significant bit of the device address (SA0)		
2	MSDA	Connect to Vdd_IO or GND	I²C serial data master (MSDA)	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in MASTER_CONFIG (14h) in the sensor hub registers (see Note to enable pull-up).	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in MASTER_CONFIG (14h) in the sensor hub registers (see Note to enable pull-up).
3	MSCL	Connect to Vdd_IO or GND	I²C serial clock master (MSCL)	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in MASTER_CONFIG (14h) in the sensor hub registers (see Note to enable pull-up).	Default: input without pull-up Pull-up is enabled if bit SHUB_PU_EN = 1 in MASTER_CONFIG (14h) in the sensor hub registers (see Note to enable pull-up).
4	INT1	Programmable interrupt 1	Programmable interrupt 1	Default: input with pull-down(1)	Default: input with pull-down(1)
5	Vdd_IO	Power supply for I/O pins	Power supply for I/O pins		
6	GND	0 V supply	0 V supply		
7	GND	0 V supply	0 V supply		
8	Vdd	Power supply	Power supply		
9	INT2	Programmable interrupt 2 (INT2)	Programmable interrupt 2 (INT2) / I²C master external synchronization signal (MDRDY)	Default: output forced to ground	Default: output forced to ground
10	RES	Leave unconnected	Leave unconnected		
11	RES	Connect to Vdd_IO or leave unconnected	Connect to Vdd_IO or leave unconnected		
12	CS	I²C/SPI mode selection (1:SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	I²C/SPI mode selection (1:SPI idle mode / I²C communication enabled; 0: SPI communication mode / I²C disabled)	Default: input with pull-up	Default: input with pull-up
13	SCL	I²C serial clock (SCL) / SPI serial port clock (SPC)	I²C serial clock (SCL) / SPI serial port clock (SPC)	Default: input without pull-up	Default: input without pull-up
14	SDA	I²C serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	I²C serial data (SDA) / SPI serial data input (SDI) / 3-wire interface serial data output (SDO)	Default: input without pull-up	Default: input without pull-up

1. *INT1 must be set to 0 or left unconnected during power-on.*

Internal pull-up value is from 30 kΩ to 50 kΩ, depending on Vdd_IO.

Note: The procedure to enable the pull-up on pins 2 and 3 is as follows:

1. From the primary I²C/SPI interface: write 40h in register at address 01h (enable access to the sensor hub registers)

2. From the primary I²C/SPI interface: write 08h in register at address 14h (enable the pull-up on pins 2 and 3)

3. From the primary I²C/SPI interface: write 00h in register at address 01h (disable access to the sensor hub registers)

8 Register mapping

The table given below provides a list of the 8/16-bit registers embedded in the device and the corresponding addresses.

All these registers are accessible from the primary SPI/I²C interface only.

Table 17. Registers address map

Name	Type	Register address		Default
		Hex	Binary	
FUNC_CFG_ACCESS	R/W	01	00000001	00000000
PIN_CTRL	R/W	02	00000010	00111111
RESERVED	-	03-0A		
DRDY_PULSED_REG	R/W	0B	00001011	00000000
RESERVED	-	0C		
INT1_CTRL	R/W	0D	00001101	00000000
INT2_CTRL	R/W	0E	00001110	00000000
WHO_AM_I	R	0F	00001111	00100010
CTRL1_XL	R/W	10	00010000	00000000
CTRL2_G	R/W	11	00010001	00000000
CTRL3_C	R/W	12	00010010	00000100
CTRL4_C	R/W	13	00010011	00000000
CTRL5_C	R/W	14	00010100	00000000
CTRL6_C	R/W	15	00010101	00000000
CTRL7_G	R/W	16	00010110	00000000
RESERVED	-	17		
CTRL9_C	R/W	18	00011000	11100000
CTRL10_C	R/W	19	00011001	00000000
ISPU_INT_STATUS0_MAINPAGE	R	1A	00011010	output
ISPU_INT_STATUS1_MAINPAGE	R	1B	00011011	output
ISPU_INT_STATUS2_MAINPAGE	R	1C	00011100	output
ISPU_INT_STATUS3_MAINPAGE	R	1D	00011101	output
STATUS_REG	R	1E	00011110	output
RESERVED	-	1F		
OUT_TEMP_L	R	20	00100000	output
OUT_TEMP_H	R	21	00100001	output
OUTX_L_G	R	22	00100010	output
OUTX_H_G	R	23	00100011	output
OUTY_L_G	R	24	00100100	output
OUTY_H_G	R	25	00100101	output
OUTZ_L_G	R	26	00100110	output
OUTZ_H_G	R	27	00100111	output
OUTX_L_A	R	28	00101000	output
OUTX_H_A	R	29	00101001	output

Name	Type	Register address		Default
		Hex	Binary	
OUTY_L_A	R	2A	00101010	output
OUTY_H_A	R	2B	00101011	output
OUTZ_L_A	R	2C	00101100	output
OUTZ_H_A	R	2D	00101101	output
RESERVED	-	2E-38		
STATUS_MASTER_ MAINPAGE	R	39	00111001	output
RESERVED	-	3A-3F		
TIMESTAMP0	R	40	01000000	output
TIMESTAMP1	R	41	01000001	output
TIMESTAMP2	R	42	01000010	output
TIMESTAMP3	R	43	01000011	output
RESERVED	-	44-5D		
MD1_CFG	R/W	5E	01011110	00000000
MD2_CFG	R/W	5F	01011111	00000000
INTERNAL_FREQ_FINE	R	63	01100011	output
ISPU_DUMMY_CFG_1_L	R/W	73	01110011	00000000
ISPU_DUMMY_CFG_1_H	R/W	74	01110100	00000000
ISPU_DUMMY_CFG_2_L	R/W	75	01110101	00000000
ISPU_DUMMY_CFG_2_H	R/W	76	01110110	00000000
ISPU_DUMMY_CFG_3_L	R/W	77	01110111	00000000
ISPU_DUMMY_CFG_3_H	R/W	78	01111000	00000000
ISPU_DUMMY_CFG_4_L	R/W	79	01111001	00000000
ISPU_DUMMY_CFG_4_H	R/W	7A	01111010	00000000

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

9 Register description

The device contains a set of registers which are used to control its behavior and to retrieve linear acceleration, angular rate and temperature data. The register addresses, made up of 7 bits, are used to identify them and to write the data through the serial interface.

9.1 FUNC_CFG_ACCESS (01h)

Enable ISPU / sensor hub functions register (R/W)

Table 18. FUNC_CFG_ACCESS register

ISPU_REG_ACCESS	SHUB_REG_ACCESS	0(1)	0(1)	0(1)	0(1)	SW_RESET_ISPU	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 19. FUNC_CFG_ACCESS register description

ISPU_REG_ACCESS	Enables access to the ISPU interaction registers(1). Default value: 0
SHUB_REG_ACCESS	Enables access to the sensor hub (I²C master) registers(2). Default value: 0
SW_RESET_ISPU	Software reset of ISPU core. Set the bit to 1 to activate the reset sequence and immediately write back to 0 (this bit is not automatically cleared). Default value: 0

1. *Details regarding the ISPU interaction registers are available in Section 10 ISPU interaction register mapping and Section 11 ISPU interaction register description.*
2. *Details concerning the sensor hub registers are available in Section 14 Sensor hub register mapping and Section 15 Sensor hub register description.*

9.2 PIN_CTRL (02h)

SDO pin pull-up register (R/W)

Table 20. PIN_CTRL register

0(1)	SDO_PU_EN	1(2)	1(2)	1(2)	1(2)	1(2)	1(2)

1. *This bit must be set to 0 for the correct operation of the device.*
2. *This bit must be set to 1 for the correct operation of the device.*

Table 21. PIN_CTRL register description

SDO_PU_EN	Enables pull-up on SDO pin. (0: SDO pin pull-up disconnected (default); 1: SDO pin with pull-up)

9.3 DRDY_PULSED_REG (0Bh)

Pulsed data-ready mode register (R/W)

Table 22. DRDY_PULSED_REG register

DRDY_ PULSED	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 23. DRDY_PULSED_REG register description

DRDY_PULSED	Enables pulsed data-ready mode. (0: Data-ready latched mode (returns to 0 only after an interface reading) (default); 1: Data-ready pulsed mode (the data-ready pulses are 75 µs long))

9.4 INT1_CTRL (0Dh)

INT1 pin control register (R/W)

The output of the INT1 pin is the OR combination of the signals selected here and in register MD1_CFG (5Eh).

Table 24. INT1_CTRL register

0(1)	0(1)	0(1)	0(1)	0(1)	INT1_ BOOT	INT1_ DRDY_G	INT1_ DRDY_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 25. INT1_CTRL register description

INT1_ BOOT	Boot status available on the INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_G	Enables gyroscope data-ready interrupt on the INT1 pin. Default value: 0 (0: disabled; 1: enabled)
INT1_DRDY_XL	Enables accelerometer data-ready interrupt on the INT1 pin. Default value: 0 (0: disabled; 1: enabled)

9.5 INT2_CTRL (0Eh)

INT2 pin control register (R/W)

The output of the INT2 pin is the OR combination of the signals selected here and in register MD2_CFG (5Fh).

Table 26. INT2_CTRL register

INT2_SLEEP_ISPU	0(1)	0(1)	0(1)	0(1)	INT2_DRDY_TEMP	INT2_DRDY_G	INT2_DRDY_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 27. INT2_CTRL register description

INT2_SLEEP_ISPU	Enables ISPU sleep state signal on the INT2 pin. Default value: 0 (0: disabled; 1: enabled) When enabled: • INT2 low: ISPU is running; • INT2 high: ISPU is in sleep state.
INT2_DRDY_TEMP	Enables temperature sensor data-ready interrupt on the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_G	Enables gyroscope data-ready interrupt on the INT2 pin. Default value: 0 (0: disabled; 1: enabled)
INT2_DRDY_XL	Enables accelerometer data-ready interrupt on the INT2 pin. Default value: 0 (0: disabled; 1: enabled)

9.6 WHO_AM_I (0Fh)

WHO_AM_I register (R). This is a read-only register. Its value is fixed at 22h.

Table 28. WHO_AM_I register

0	0	1	0	0	0	1	0

9.7 CTRL1_XL (10h)

Control register 1 (R/W)

Table 29. CTRL1_XL register

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	FS1_XL	FS0_XL	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 30. CTRL1_XL register description

ODR_XL[3:0]	Accelerometer ODR selection (see Table 31).
FS[1:0]_XL	Accelerometer full-scale selection (see Table 32).

Table 31. Accelerometer ODR configuration setting

ODR_XL3	ODR_XL2	ODR_XL1	ODR_XL0	ODR selection [Hz] when XL_HM_MODE = 1 in CTRL6_C (15h)	ODR selection [Hz] when XL_HM_MODE = 0 in CTRL6_C (15h)
0	0	0	0	Power-down	Power-down
1	0	1	1	1.6 Hz (low power)	12.5 Hz (high performance)
0	0	0	1	12.5 Hz (low power)	12.5 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (low power)	104 Hz (high performance)
0	1	0	1	208 Hz (low power)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1667 Hz (high performance)	1667 Hz (high performance)
1	0	0	1	3333 Hz (high performance)	3333 Hz (high performance)
1	0	1	0	6667 Hz (high performance)	6667 Hz (high performance)
1	0	1	1	Reserved	Reserved
1	1	x	x	Reserved	Reserved

Table 32. Accelerometer full-scale selection

FS[1:0]_XL	Full scale
00 (default)	±2 *g*
01	±16 *g*
10	±4 *g*
11	±8 *g*

9.8 CTRL2_G (11h)

Control register 2 (R/W)

Table 33. CTRL2_G register

ODR_G3	ODR_G2	ODR_G1	ODR_G0	FS1_G	FS0_G	FS_125	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 34. CTRL2_G register description

ODR_G[3:0]	Gyroscope output data rate selection. Default value: 0000 (Refer to Table 35)
FS[1:0]_G	Gyroscope chain full-scale selection. Default value: 00 (00: ±250 dps; 01: ±500 dps; 10: ±1000 dps; 11: ±2000 dps)
FS_125	Gyroscope chain full-scale selection for ±125 dps. Default value: 0 (0: FS selected through bits FS[1:0]_G; 1: FS set to ±125 dps)

Table 35. Gyroscope ODR configuration setting

ODR_G3	ODR_G2	ODR_G1	ODR_G0	ODR selection [Hz] when G_HM_MODE = 1 in CTRL7_G (16h)	ODR selection [Hz] when G_HM_MODE = 0 in CTRL7_G (16h)
0	0	0	0	Power-down	Power-down
0	0	0	1	12.5 Hz (low power)	12.5 Hz (high performance)
0	0	1	0	26 Hz (low power)	26 Hz (high performance)
0	0	1	1	52 Hz (low power)	52 Hz (high performance)
0	1	0	0	104 Hz (low power)	104 Hz (high performance)
0	1	0	1	208 Hz (low power)	208 Hz (high performance)
0	1	1	0	416 Hz (high performance)	416 Hz (high performance)
0	1	1	1	833 Hz (high performance)	833 Hz (high performance)
1	0	0	0	1667 Hz (high performance)	1667 Hz (high performance)
1	0	0	1	3333 Hz (high performance)	3333 Hz (high performance)
1	0	1	0	6667 Hz (high performance)	6667 Hz (high performance)
1	0	1	1	Reserved	Reserved
1	1	x	x	Reserved	Reserved

9.9 CTRL3_C (12h)

Control register 3 (R/W)

Table 36. CTRL3_C register

BOOT	BDU	H_LACTIVE	PP_OD	SIM	IF_INC	0(1)	SW_RESET

1. *This bit must be set to 0 for the correct operation of the device.*

Table 37. CTRL3_C register description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers are not updated until MSB and LSB have been read)
H_LACTIVE	Interrupt activation level. Default value: 0 (0: interrupt output pins active-high; 1: interrupt output pins active-low)
PP_OD	Push-pull/open-drain selection on INT1 and INT2 pins. This bit must be set to 0 when H_LACTIVE is set to 1. Default value: 0 (0: push-pull mode; 1: open-drain mode)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)
IF_INC	Register address automatically incremented during a multiple byte access with a serial interface (I²C or SPI). Default value: 1 (0: disabled; 1: enabled)
SW_RESET	Software reset. Default value: 0 (0: normal mode; 1: reset device) This bit is automatically cleared.

9.10 CTRL4_C (13h)

Control register 4 (R/W)

Table 38. CTRL4_C register

0(1)	SLEEP_G	INT2_on_INT1	0(1)	0(1)	I2C_disable	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 39. CTRL4_C register description

SLEEP_G	Enables gyroscope sleep mode. Default value: 0 (0: disabled; 1: enabled)
INT2_on_INT1	Enables all interrupt signals available on INT1 pin. Default value: 0 (0: interrupt signals divided between INT1 and INT2 pins; 1: all interrupt signals in logic or on INT1 pin)
I2C_disable	Disables I²C interface. Default value: 0 (0: SPI and I²C interfaces enabled (default); 1: I²C interface disabled)

9.11 CTRL5_C (14h)

Control register 5 (R/W)

Table 40. CTRL5_C register

0(1)	0(1)	0(1)	0(1)	ST1_G	ST0_G	ST1_XL	ST0_XL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 41. CTRL5_C register description

ST[1:0]_G	Enables angular rate sensor self-test. Default value: 00 (00: Self-test disabled; Other: refer to Table 42)
ST[1:0]_XL	Enables linear acceleration sensor self-test. Default value: 00 (00: Self-test disabled; Other: refer to Table 43)

Table 42. Angular rate sensor self-test mode selection

ST1_G	ST0_G	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Not allowed
1	1	Negative sign self-test

Table 43. Linear acceleration sensor self-test mode selection

ST1_XL	ST0_XL	Self-test mode
0	0	Normal mode
0	1	Positive sign self-test
1	0	Negative sign self-test
1	1	Not allowed

9.12 CTRL6_C (15h)

Control register 6 (R/W)

Table 44. CTRL6_C register

0(1)	0(1)	0(1)	XL_ HM_MODE	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 45. CTRL6_C register description

XL_HM_MODE	Disables high-performance operating mode for the accelerometer. Default value: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)

9.13 CTRL7_G (16h)

Control register 7 (R/W)

Table 46. CTRL7_G register

G_ HM_MODE	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 47. CTRL7_G register description

G_HM_MODE	Disables high-performance operating mode for gyroscope. Default: 0 (0: high-performance operating mode enabled; 1: high-performance operating mode disabled)

9.14 CTRL9_C (18h)

Control register 9 (R/W)

Table 48. CTRL9_C register

ISPU_ RATE_3	ISPU_ RATE_2	ISPU_ RATE_1	ISPU_ RATE_0	0(1)	0(1)	ISPU_ BDU_1	ISPU_ BDU_0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 49. CTRL9_C register description

ISPU_RATE_[3:0]	ISPU IRQ rate selection. (0000: power-down (default); 0001: 12.5 Hz; 0010: 26 Hz; 0011: 52 Hz; 0100: 104 Hz; 0101: 208 Hz; 0110: 416 Hz; 0111: 833 Hz; 1000: 1667 Hz; 1001: 3333 Hz; 1010: 6667 Hz; 1011-1111: reserved)
ISPU_BDU_[1:0]	Block data update (BDU) for ISPU output registers. Based on output data format, different configurations must be used, see Table 50

Table 50. Configurations for block data update

ISPU_BDU_[1:0]	ISPU_DOUT_00_L to ISPU_DOUT_15_H	ISPU_DOUT_16_L to ISPU_DOUT_31_H
00	BDU disabled	BDU disabled
01	BDU on 2 bytes (16 outputs)	BDU on 4 bytes (8 outputs)
10	BDU on 2 bytes (16 outputs)	BDU on 2 bytes (16 outputs)
11	BDU on 4 bytes (8 outputs)	BDU on 4 bytes (8 outputs)

9.15 CTRL10_C (19h)

Control register 10 (R/W)

Table 51. CTRL10_C register

0(1)	0(1)	TIMESTAMP_EN	0(1)	0(1)	ISPU_CLK_SEL	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 52. CTRL10_C register description

TIMESTAMP_EN	Enables timestamp counter. Default value: 0 (0: disabled; 1: enabled) The counter is readable in TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h).
ISPU_CLK_SEL	Selects the ISPU core clock frequency: 0: core clock frequency set to 5 MHz (default) 1: core clock frequency set to 10 MHz

9.16 ISPU_INT_STATUS0_MAINPAGE (1Ah), ISPU_INT_STATUS1_MAINPAGE (1Bh), ISPU_INT_STATUS2_MAINPAGE (1Ch), ISPU_INT_STATUS3_MAINPAGE (1Dh)

ISPU interrupt status registers (R)

Table 53. ISPU_INT_STATUS0_MAINPAGE output register

IA_ISPU_7	IA_ISPU_6	IA_ISPU_5	IA_ISPU_4	IA_ISPU_3	IA_ISPU_2	IA_ISPU_1	IA_ISPU_0

Table 54. ISPU_INT_STATUS1_MAINPAGE output register

IA_ISPU_15	IA_ISPU_14	IA_ISPU_13	IA_ISPU_12	IA_ISPU_11	IA_ISPU_10	IA_ISPU_9	IA_ISPU_8

Table 55. ISPU_INT_STATUS2_MAINPAGE output register

IA_ISPU_23	IA_ISPU_22	IA_ISPU_21	IA_ISPU_20	IA_ISPU_19	IA_ISPU_18	IA_ISPU_17	IA_ISPU_16

Table 56. ISPU_INT_STATUS3_MAINPAGE output register

0	0	IA_ISPU_29	IA_ISPU_28	IA_ISPU_27	IA_ISPU_26	IA_ISPU_25	IA_ISPU_24

Table 57. ISPU_INT_STATUS_MAINPAGE output register description

IA_ISPU_[29:0]	Generic interrupt flags from ISPU.

9.17 STATUS_REG (1Eh)

Status register (R)

Table 58. STATUS_REG register

TIMESTAMP_ ENDCOUNT	0	0	0	0	TDA	GDA	XLDA

Table 59. STATUS_REG register description

TIMESTAMP_ENDCOUNT	Alerts timestamp overflow within 6.4 ms.
TDA	Temperature new data available. Default: 0 (0: no set of data is available at temperature sensor output; 1: a new set of data is available at temperature sensor output)
GDA	Gyroscope new data available. Default value: 0 (0: no set of data available at gyroscope output; 1: a new set of data is available at gyroscope output)
XLDA	Accelerometer new data available. Default value: 0 (0: no set of data available at accelerometer output; 1: a new set of data is available at accelerometer output)

9.18 OUT_TEMP_L (20h), OUT_TEMP_H (21h)

Temperature data output register (R). The value is expressed as a 16-bit word in two's complement.

Table 60. OUT_TEMP_L register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 61. OUT_TEMP_H register

Temp15	Temp14	Temp13	Temp12	Temp11	Temp10	Temp9	Temp8

Table 62. OUT_TEMP register description

Temp[15:0]	Temperature sensor output data. The value is expressed as two's complement sign extended on the MSB.

9.19 OUTX_L_G (22h) and OUTX_H_G (23h)

Angular rate sensor pitch axis (X) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale and ODR settings (CTRL2_G (11h)) of the gyroscope.

Table 63. OUTX_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 64. OUTX_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 65. OUTX_H_G register description

D[15:0]	Gyroscope chain pitch axis (X) angular rate output value.

9.20 OUTY_L_G (24h) and OUTY_H_G (25h)

Angular rate sensor roll axis (Y) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale and ODR settings (CTRL2_G (11h)) of the gyroscope.

Table 66. OUTY_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 67. OUTY_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 68. OUTY_H_G register description

D[15:0]	Gyroscope chain roll axis (Y) angular rate output value.

9.21 OUTZ_L_G (26h) and OUTZ_H_G (27h)

Angular rate sensor yaw axis (Z) angular rate output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale and ODR settings (CTRL2_G (11h)) of the gyroscope.

Table 69. OUTZ_L_G register

D7	D6	D5	D4	D3	D2	D1	D0

Table 70. OUTZ_H_G register

D15	D14	D13	D12	D11	D10	D9	D8

Table 71. OUTZ_H_G register description

D[15:0]	Gyroscope chain yaw axis (Z) angular rate output value.

9.22 OUTX_L_A (28h) and OUTX_H_A (29h)

Linear acceleration sensor X-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale and ODR settings (CTRL1_XL (10h)) of the accelerometer.

Table 72. OUTX_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 73. OUTX_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 74. OUTX_H_A register description

D[15:0]	Accelerometer chain X-axis linear acceleration output value.

9.23 OUTY_L_A (2Ah) and OUTY_H_A (2Bh)

Linear acceleration sensor Y-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale and ODR settings (CTRL1_XL (10h)) of the accelerometer.

Table 75. OUTY_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 76. OUTY_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 77. OUTY_H_A register description

D[15:0]	Accelerometer chain Y-axis linear acceleration output value.

9.24 OUTZ_L_A (2Ch) and OUTZ_H_A (2Dh)

Linear acceleration sensor Z-axis output register (R). The value is expressed as a 16-bit word in two's complement.

Data are according to the full-scale and ODR settings (CTRL1_XL (10h)) of the accelerometer.

Table 78. OUTZ_L_A register

D7	D6	D5	D4	D3	D2	D1	D0

Table 79. OUTZ_H_A register

D15	D14	D13	D12	D11	D10	D9	D8

Table 80. OUTZ_H_A register description

D[15:0]	Accelerometer chain Z-axis linear acceleration output value.

9.25 STATUS_MASTER_MAINPAGE (39h)

Sensor hub status register (R)

Table 81. STATUS_MASTER_MAINPAGE register

WR_ONCE_DONE	SLAVE3_NACK	SLAVE2_NACK	SLAVE1_NACK	SLAVE0_NACK	0	0	SENS_HUB_ENDOP

Table 82. STATUS_MASTER_MAINPAGE register description

WR_ONCE_DONE	When the bit WRITE_ONCE in MASTER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on slave 0 has been performed and completed. Default value: 0
SLAVE3_NACK	This bit is set to 1 if Not acknowledge occurs on slave 3 communication. Default value: 0
SLAVE2_NACK	This bit is set to 1 if Not acknowledge occurs on slave 2 communication. Default value: 0
SLAVE1_NACK	This bit is set to 1 if Not acknowledge occurs on slave 1 communication. Default value: 0
SLAVE0_NACK	This bit is set to 1 if Not acknowledge occurs on slave 0 communication. Default value: 0
SENS_HUB_ENDOP	Sensor hub communication status. Default value: 0 (0: sensor hub communication not concluded; 1: sensor hub communication concluded)

9.26 TIMESTAMP0 (40h), TIMESTAMP1 (41h), TIMESTAMP2 (42h), and TIMESTAMP3 (43h)

Timestamp first data output register (R). The value is expressed as a 32-bit word and the bit resolution is 25 µs.
These registers are also accessible from ISPU at address 6940h, 6941h, 6942h, 6943h (R).

Table 83. TIMESTAMP0 output register

D7	D6	D5	D4	D3	D2	D1	D0

Table 84. TIMESTAMP1 output register

D15	D14	D13	D12	D11	D10	D9	D8

Table 85. TIMESTAMP2 output register

D23	D22	D21	D20	D19	D18	D17	D16

Table 86. TIMESTAMP3 output register

D31	D30	D29	D28	D27	D26	D25	D24

Table 87. TIMESTAMP output register description

D[31:0]	Timestamp output registers: 1LSB = 25 µs.

9.27 MD1_CFG (5Eh)

Functions routing to INT1 pin register (R/W)

Table 88. MD1_CFG register

0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	INT1_ ISPU	INT1_SHUB

1. *This bit must be set to 0 for the correct operation of the device.*

Table 89. MD1_CFG register description

INT1_ISPU	Routing ISPU event to INT1. Default value: 0 (0: routing ISPU event to INT1 disabled; 1: routing ISPU event to INT1 enabled)
INT1_SHUB	Routing sensor hub communication concluded event to INT1. Default value: 0 (0: routing sensor hub communication concluded event to INT1 disabled; 1: routing sensor hub communication concluded event to INT1 enabled)

9.28 MD2_CFG (5Fh)

Functions routing to INT2 pin register (R/W)

Table 90. MD2_CFG register

0(1)	0(1)	0(1)	0(1)	0(1)	0(1)	INT2_ ISPU	INT2_ TIMESTAMP

1. *This bit must be set to 0 for the correct operation of the device.*

Table 91. MD2_CFG register description

INT2_ISPU	Routing ISPU event to INT2. Default value: 0 (0: routing ISPU event to INT2 disabled; 1: routing ISPU event to INT2 enabled)
INT2_TIMESTAMP	Enables routing the alert for timestamp overflow within 6.4 ms to the INT2 pin.

9.29 INTERNAL_FREQ_FINE (63h)

Internal frequency register (R)

Table 92. INTERNAL_FREQ_FINE register

FREQ_ FINE7	FREQ_ FINE6	FREQ_ FINE5	FREQ_ FINE4	FREQ_ FINE3	FREQ_ FINE2	FREQ_ FINE1	FREQ_ FINE0

Table 93. INTERNAL_FREQ_FINE register description

FREQ_FINE[7:0]	Difference in percentage of the effective ODR (and timestamp rate) with respect to the typical. Step: 0.15%. 8-bit format, two's complement.

9.30 ISPU_DUMMY_CFG_1_L (73h) and ISPU_DUMMY_CFG_1_H (74h)

General-purpose input configuration register for ISPU (R/W). This register is also accessible from ISPU at address 6974h, 6975h (R).

Table 94. ISPU_DUMMY_CFG_1_L register

ISPU_DUMMY_CFG_1_7	ISPU_DUMMY_CFG_1_6	ISPU_DUMMY_CFG_1_5	ISPU_DUMMY_CFG_1_4	ISPU_DUMMY_CFG_1_3	ISPU_DUMMY_CFG_1_2	ISPU_DUMMY_CFG_1_1	ISPU_DUMMY_CFG_1_0

Table 95. ISPU_DUMMY_CFG_1_H register

ISPU_DUMMY_CFG_1_15	ISPU_DUMMY_CFG_1_14	ISPU_DUMMY_CFG_1_13	ISPU_DUMMY_CFG_1_12	ISPU_DUMMY_CFG_1_11	ISPU_DUMMY_CFG_1_10	ISPU_DUMMY_CFG_1_9	ISPU_DUMMY_CFG_1_8

Table 96. ISPU_DUMMY_CFG_1 register description

ISPU_DUMMY_CFG_1_[15:0]	Input configuration register 1 for ISPU.

9.31 ISPU_DUMMY_CFG_2_L (75h) and ISPU_DUMMY_CFG_2_H (76h)

General-purpose input configuration register for ISPU (R/W). This register is also accessible from ISPU at address 6976h, 6977h (R).

Table 97. ISPU_DUMMY_CFG_2_L register

ISPU_DUMMY_CFG_2_7	ISPU_DUMMY_CFG_2_6	ISPU_DUMMY_CFG_2_5	ISPU_DUMMY_CFG_2_4	ISPU_DUMMY_CFG_2_3	ISPU_DUMMY_CFG_2_2	ISPU_DUMMY_CFG_2_1	ISPU_DUMMY_CFG_2_0

Table 98. ISPU_DUMMY_CFG_2_H register

ISPU_DUMMY_CFG_2_15	ISPU_DUMMY_CFG_2_14	ISPU_DUMMY_CFG_2_13	ISPU_DUMMY_CFG_2_12	ISPU_DUMMY_CFG_2_11	ISPU_DUMMY_CFG_2_10	ISPU_DUMMY_CFG_2_9	ISPU_DUMMY_CFG_2_8

Table 99. ISPU_DUMMY_CFG_2 register description

ISPU_DUMMY_CFG_2_[15:0]	Input configuration register 2 for ISPU.

9.32 ISPU_DUMMY_CFG_3_L (77h) and ISPU_DUMMY_CFG_3_H (78h)

General-purpose input configuration register for ISPU (R/W). This register is also accessible from ISPU at address 6978h, 6979h (R).

Table 100. ISPU_DUMMY_CFG_3_L register

ISPU_DUMMY_CFG_3_7	ISPU_DUMMY_CFG_3_6	ISPU_DUMMY_CFG_3_5	ISPU_DUMMY_CFG_3_4	ISPU_DUMMY_CFG_3_3	ISPU_DUMMY_CFG_3_2	ISPU_DUMMY_CFG_3_1	ISPU_DUMMY_CFG_3_0

Table 101. ISPU_DUMMY_CFG_3_H register

ISPU_DUMMY_CFG_3_15	ISPU_DUMMY_CFG_3_14	ISPU_DUMMY_CFG_3_13	ISPU_DUMMY_CFG_3_12	ISPU_DUMMY_CFG_3_11	ISPU_DUMMY_CFG_3_10	ISPU_DUMMY_CFG_3_9	ISPU_DUMMY_CFG_3_8

Table 102. ISPU_DUMMY_CFG_3 register description

ISPU_DUMMY_CFG_3_[15:0]	Input configuration register 3 for ISPU.

9.33 ISPU_DUMMY_CFG_4_L (79h) and ISPU_DUMMY_CFG_4_H (7Ah)

General-purpose input configuration register for ISPU (R/W). This register is also accessible from ISPU at address 697Ah, 697Bh (R).

Table 103. ISPU_DUMMY_CFG_4_L register

ISPU_DUMMY_CFG_4_7	ISPU_DUMMY_CFG_4_6	ISPU_DUMMY_CFG_4_5	ISPU_DUMMY_CFG_4_4	ISPU_DUMMY_CFG_4_3	ISPU_DUMMY_CFG_4_2	ISPU_DUMMY_CFG_4_1	ISPU_DUMMY_CFG_4_0

Table 104. ISPU_DUMMY_CFG_4_H register

ISPU_DUMMY_CFG_4_15	ISPU_DUMMY_CFG_4_14	ISPU_DUMMY_CFG_4_13	ISPU_DUMMY_CFG_4_12	ISPU_DUMMY_CFG_4_11	ISPU_DUMMY_CFG_4_10	ISPU_DUMMY_CFG_4_9	ISPU_DUMMY_CFG_4_8

Table 105. ISPU_DUMMY_CFG_4 register description

ISPU_DUMMY_CFG_4_[15:0]	Input configuration register 4 for ISPU.

10 ISPU interaction register mapping

The table given below provides a list of the registers for the ISPU functions available in the device and the corresponding addresses.

When the ISPU_REG_ACCESS bit is set to 1 in FUNC_CFG_ACCESS (01h), the ISPU interaction registers are accessible **over the I²C/SPI interface** with the address indicated in the first column (IF address) of the table below.

These registers are also accessible from ISPU through the address indicated in the second column (ISPU address), regardless of the ISPU_REG_ACCESS bit configuration.

Table 106. Register map - ISPU interaction registers

IF address (hex)	ISPU address (hex)	Bytes	Name	IF access	ISPU access
02	6802	1	ISPU_CONFIG	R/W	R
04	6804	1	ISPU_STATUS	R	R/W
08	-	1	ISPU_MEM_SEL	R/W	No
09-0A	-	2	ISPU_MEM_ADDR	R/W	No
0B	-	1	ISPU_MEM_DATA	R/W	No
0C-0D	680C-680D	2	ISPU_IF2S_FLAG	R/W, set only	R/W, clear only
0E-0F	680E-680F	2	ISPU_S2IF_FLAG	R/W, clear only	R/W, set only
10-11	6810-6811	2	ISPU_DOUT_00	R	R/W
12-13	6812-6813	2	ISPU_DOUT_01	R	R/W
14-15	6814-6815	2	ISPU_DOUT_02	R	R/W
16-17	6816-6817	2	ISPU_DOUT_03	R	R/W
18-19	6818-6819	2	ISPU_DOUT_04	R	R/W
1A-1B	681A-681B	2	ISPU_DOUT_05	R	R/W
1C-1D	681C-681C	2	ISPU_DOUT_06	R	R/W
1E-1F	681E-681F	2	ISPU_DOUT_07	R	R/W
20-21	6820-6821	2	ISPU_DOUT_08	R	R/W
22-23	6822-6823	2	ISPU_DOUT_09	R	R/W
24-25	6824-6825	2	ISPU_DOUT_10	R	R/W
26-27	6826-6827	2	ISPU_DOUT_11	R	R/W
28-29	6828-6829	2	ISPU_DOUT_12	R	R/W
2A-2B	682A-682B	2	ISPU_DOUT_13	R	R/W
2C-2D	682C-682D	2	ISPU_DOUT_14	R	R/W
2E-2F	682E-682F	2	ISPU_DOUT_15	R	R/W
30-31	6830-6831	2	ISPU_DOUT_16	R	R/W
32-33	6832-6833	2	ISPU_DOUT_17	R	R/W
34-35	6834-6835	2	ISPU_DOUT_18	R	R/W
36-37	6836-6837	2	ISPU_DOUT_19	R	R/W
38-39	6838-6839	2	ISPU_DOUT_20	R	R/W
3A-3B	683A-683B	2	ISPU_DOUT_21	R	R/W
3C-3D	683C-683D	2	ISPU_DOUT_22	R	R/W
3E-3F	683E-683F	2	ISPU_DOUT_23	R	R/W
40-41	6840-6841	2	ISPU_DOUT_24	R	R/W

IF address (hex)	ISPU address (hex)	Bytes	Name	IF access	ISPU access
42-43	6842-6843	2	ISPU_DOUT_25	R	R/W
44-45	6844-6845	2	ISPU_DOUT_26	R	R/W
46-47	6846-6847	2	ISPU_DOUT_27	R	R/W
48-49	6848-6849	2	ISPU_DOUT_28	R	R/W
4A-4B	684A-684B	2	ISPU_DOUT_29	R	R/W
4C-4D	684C-684D	2	ISPU_DOUT_30	R	R/W
4E-4F	684E-684F	2	ISPU_DOUT_31	R	R/W
50-53	6850-6853	4	ISPU_INT1_CTRL	R/W	R
54-57	6854-6857	4	ISPU_INT2_CTRL	R/W	R
58-5B	6858-685B	4	ISPU_INT_STATUS	R	R/W
70-73	6870-6873	4	ISPU_ALGO	R/W	R, clear only

Table 107. Register map - ISPU to external resources

ISPU address (hex)	Bytes	Name	ISPU access
6940-6941	2	TIMESTAMP0 (40h), TIMESTAMP1 (41h) Section 9.26	R
6942-6943	2	TIMESTAMP2 (42h), TIMESTAMP3 (43h) Section 9.26	R
6974-6975	2	ISPU_DUMMY_CFG_1_L (73h) and ISPU_DUMMY_CFG_1_H (74h)	R
6976-6977	2	ISPU_DUMMY_CFG_2_L (75h) and ISPU_DUMMY_CFG_2_H (76h)	R
6978-6979	2	ISPU_DUMMY_CFG_3_L (77h) and ISPU_DUMMY_CFG_3_H (78h)	R
697A-697B	2	ISPU_DUMMY_CFG_4_L (79h) and ISPU_DUMMY_CFG_4_H (7Ah)	R

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

11 ISPU interaction register description

11.1 ISPU_CONFIG (02h)

ISPU configuration register (R/W). This register is also accessible from ISPU at address 6802h (R).

Table 108. ISPU_CONFIG register

0(1)	0(1)	0(1)	LATCHED	0(1)	0(1)	CLK_DIS	ISPU_ RST_N

1. *This bit must be set to 0 for the correct operation of the device.*

Table 109. ISPU_CONFIG register description

LATCHED	Configures the interrupt generation. (0: interrupt pulsed; 1: interrupt latched)
CLK_DIS	When active, stops the clock of ISPU.
ISPU_RST_N	ISPU active-low reset.

11.2 ISPU_STATUS (04h)

ISPU status register (R). This register is also accessible from ISPU at address 6804h (R/W).

Table 110. ISPU_STATUS register

0(1)	0(1)	0(1)	0(1)	0(1)	BOOT_END	0(1)	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 111. ISPU_STATUS register description

BOOT_END	End of ISPU boot procedure.

11.3 ISPU_MEM_SEL (08h)

ISPU memory selection register (R/W)

Table 112. ISPU_MEM_SEL register

0(1)	READ_ MEM_EN	0(1)	0(1)	0(1)	0(1)	0(1)	MEM_SEL

1. *This bit must be set to 0 for the correct operation of the device.*

Table 113. ISPU_MEM_SEL register description

READ_MEM_EN	Enables reading from program or data memories. Default value: 0 (0: disabled; 1: enabled)
MEM_SEL	Selects the memory to be accessed. Default value: 0 (0: data RAM memory is selected; 1: program RAM memory is selected)

11.4 ISPU_MEM_ADDR1 (09h), ISPU_MEM_ADDR0 (0Ah)

ISPU memory address register (R/W)

Table 114. ISPU_MEM_ADDR1 register

MEM_ADDR_15	MEM_ADDR_14	MEM_ADDR_13	MEM_ADDR_12	MEM_ADDR_11	MEM_ADDR_10	MEM_ADDR_9	MEM_ADDR_8

Table 115. ISPU_MEM_ADDR0 register

MEM_ADDR_7	MEM_ADDR_6	MEM_ADDR_5	MEM_ADDR_4	MEM_ADDR_3	MEM_ADDR_2	MEM_ADDR_1	MEM_ADDR_0

Table 116. ISPU_MEM_ADDR register description

MEM_ADDR_[15:0]	Memory address to be read/written.

11.5 ISPU_MEM_DATA (0Bh)

ISPU memory data register (R/W)

Table 117. ISPU_MEM_DATA register

MEM_DATA_7	MEM_DATA_6	MEM_DATA_5	MEM_DATA_4	MEM_DATA_3	MEM_DATA_2	MEM_DATA_1	MEM_DATA_0

Table 118. ISPU_MEM_DATA register description

MEM_DATA_[7:0]	Byte to write to memory in write transaction or data read from memory in read transaction.

11.6 ISPU_IF2S_FLAG_L (0Ch), ISPU_IF2S_FLAG_H (0Dh)

Interface to ISPU register (R/W, set only). This register is also accessible from ISPU at address 680Ch, 680Dh (R/W, clear only).

Table 119. ISPU_IF2S_FLAG_L register

IF2S_7	IF2S_6	IF2S_5	IF2S_4	IF2S_3	IF2S_2	IF2S_1	IF2S_0

Table 120. ISPU_IF2S_FLAG_H register

IF2S_15	IF2S_14	IF2S_13	IF2S_12	IF2S_11	IF2S_10	IF2S_9	IF2S_8

Table 121. ISPU_IF2S_FLAG register description

IF2S_[15:0]	16-bit general purpose bits which can be set from the interface and cleared by ISPU.

11.7 ISPU_S2IF_FLAG_L (0Eh), ISPU_S2IF_FLAG_H (0Fh)

ISPU to interface register (R/W, clear only). This register is also accessible from ISPU at address 680Eh, 680Fh (R/W, set only).

Table 122. ISPU_S2IF_FLAG_L register

S2IF_7	S2IF_6	S2IF_5	S2IF_4	S2IF_3	S2IF_2	S2IF_1	S2IF_0

Table 123. ISPU_S2IF_FLAG_H register

S2IF_15	S2IF_14	S2IF_13	S2IF_12	S2IF_11	S2IF_10	S2IF_9	S2IF_8

Table 124. ISPU_S2IF_FLAG register description

S2IF_[15:0]	16-bit general purpose bits which can be set from ISPU and cleared by the interface.

11.8 ISPU_DOUT_00_L (10h), ISPU_DOUT_00_H (11h)

ISPU output register 0 (R). This register is also accessible from ISPU at address 6810h, 6811h (R/W).

Table 125. ISPU_DOUT_00_L register

DOUT0_7	DOUT0_6	DOUT0_5	DOUT0_4	DOUT0_3	DOUT0_2	DOUT0_1	DOUT0_0

Table 126. ISPU_DOUT_00_H register

DOUT0_15	DOUT0_14	DOUT0_13	DOUT0_12	DOUT0_11	DOUT0_10	DOUT0_9	DOUT0_8

Table 127. ISPU_DOUT_00 register description

DOUT0_[15:0]	General-purpose output.

11.9 ISPU_DOUT_01_L (12h), ISPU_DOUT_01_H (13h)

ISPU output register 1 (R). This register is also accessible from ISPU at address 6812h, 6813h (R/W).

Table 128. ISPU_DOUT_01_L registers

DOUT1_7	DOUT1_6	DOUT1_5	DOUT1_4	DOUT1_3	DOUT1_2	DOUT1_1	DOUT1_0

Table 129. ISPU_DOUT_01_H registers

DOUT1_15	DOUT1_14	DOUT1_13	DOUT1_12	DOUT1_11	DOUT1_10	DOUT1_9	DOUT1_8

Table 130. ISPU_DOUT_01 register description

DOUT1_[15:0]	General-purpose output.

11.10 ISPU_DOUT_02_L (14h), ISPU_DOUT_02_H (15h)

ISPU output register 2 (R). This register is also accessible from ISPU at address 6814h, 6815h (R/W).

Table 131. ISPU_DOUT_02_L register

DOUT2_7	DOUT2_6	DOUT2_5	DOUT2_4	DOUT2_3	DOUT2_2	DOUT2_1	DOUT2_0

Table 132. ISPU_DOUT_02_H register

DOUT2_15	DOUT2_14	DOUT2_13	DOUT2_12	DOUT2_11	DOUT2_10	DOUT2_9	DOUT2_8

Table 133. ISPU_DOUT_02 register description

DOUT2_[15:0]	General-purpose output.

11.11 ISPU_DOUT_03_L (16h), ISPU_DOUT_03_H (17h)

ISPU output register 3 (R). This register is also accessible from ISPU at address 6816h, 6817h (R/W).

Table 134. ISPU_DOUT_03_L register

DOUT3_7	DOUT3_6	DOUT3_5	DOUT3_4	DOUT3_3	DOUT3_2	DOUT3_1	DOUT3_0

Table 135. ISPU_DOUT_03_H register

DOUT3_15	DOUT3_14	DOUT3_13	DOUT3_12	DOUT3_11	DOUT3_10	DOUT3_9	DOUT3_8

Table 136. ISPU_DOUT_03 register description

DOUT3_[15:0]	General-purpose output.

11.12 ISPU_DOUT_04_L (18h), ISPU_DOUT_04_H (19h)

ISPU output register 4 (R). This register is also accessible from ISPU at address 6818h, 6819h (R/W).

Table 137. ISPU_DOUT_04_L register

DOUT4_7	DOUT4_6	DOUT4_5	DOUT4_4	DOUT4_3	DOUT4_2	DOUT4_1	DOUT4_0

Table 138. ISPU_DOUT_04_H register

DOUT4_15	DOUT4_14	DOUT4_13	DOUT4_12	DOUT4_11	DOUT4_10	DOUT4_9	DOUT4_8

Table 139. ISPU_DOUT_04 register description

DOUT4_[15:0]	General-purpose output.

11.13 ISPU_DOUT_05_L (1Ah), ISPU_DOUT_05_H (1Bh)

ISPU output register 5 (R). This register is also accessible from ISPU at address 681Ah, 681Bh (R/W).

Table 140. ISPU_DOUT_05_L register

DOUT5_7	DOUT5_6	DOUT5_5	DOUT5_4	DOUT5_3	DOUT5_2	DOUT5_1	DOUT5_0

Table 141. ISPU_DOUT_05_H register

DOUT5_15	DOUT5_14	DOUT5_13	DOUT5_12	DOUT5_11	DOUT5_10	DOUT5_9	DOUT5_8

Table 142. ISPU_DOUT_05 register description

DOUT5_[15:0]	General-purpose output.

11.14 ISPU_DOUT_06_L (1Ch), ISPU_DOUT_06_H (1Dh)

ISPU output register 6 (R). This register is also accessible from ISPU at address 681Ch, 681Dh (R/W).

Table 143. ISPU_DOUT_06_L register

DOUT6_7	DOUT6_6	DOUT6_5	DOUT6_4	DOUT6_3	DOUT6_2	DOUT6_1	DOUT6_0

Table 144. ISPU_DOUT_06_H register

DOUT6_15	DOUT6_14	DOUT6_13	DOUT6_12	DOUT6_11	DOUT6_10	DOUT6_9	DOUT6_8

Table 145. ISPU_DOUT_06 register description

DOUT6_[15:0]	General-purpose output.

11.15 ISPU_DOUT_07_L (1Eh), ISPU_DOUT_07_H (1Fh)

ISPU output register 7 (R). This register is also accessible from ISPU at address 681Eh, 681Fh (R/W).

Table 146. ISPU_DOUT_07_L register

DOUT7_7	DOUT7_6	DOUT7_5	DOUT7_4	DOUT7_3	DOUT7_2	DOUT7_1	DOUT7_0

Table 147. ISPU_DOUT_07_H register

DOUT7_15	DOUT7_14	DOUT7_13	DOUT7_12	DOUT7_11	DOUT7_10	DOUT7_9	DOUT7_8

Table 148. ISPU_DOUT_07 register description

DOUT7_[15:0]	General-purpose output.

11.16 ISPU_DOUT_08_L (20h), ISPU_DOUT_08_H (21h)

ISPU output register 8 (R). This register is also accessible from ISPU at address 6820h, 6821h (R/W).

Table 149. ISPU_DOUT_08_L register

DOUT8_7	DOUT8_6	DOUT8_5	DOUT8_4	DOUT8_3	DOUT8_2	DOUT8_1	DOUT8_0

Table 150. ISPU_DOUT_08_H register

DOUT8_15	DOUT8_14	DOUT8_13	DOUT8_12	DOUT8_11	DOUT8_10	DOUT8_9	DOUT8_8

Table 151. ISPU_DOUT_08 register description

DOUT8_[15:0]	General-purpose output.

11.17 ISPU_DOUT_09_L (22h), ISPU_DOUT_09_H (23h)

ISPU output register 9 (R). This register is also accessible from ISPU at address 6822h, 6823h (R/W).

Table 152. ISPU_DOUT_09_L register

DOUT9_7	DOUT9_6	DOUT9_5	DOUT9_4	DOUT9_3	DOUT9_2	DOUT9_1	DOUT9_0

Table 153. ISPU_DOUT_09_H register

DOUT9_15	DOUT9_14	DOUT9_13	DOUT9_12	DOUT9_11	DOUT9_10	DOUT9_9	DOUT9_8

Table 154. ISPU_DOUT_09 register description

DOUT9_[15:0]	General-purpose output.

11.18 ISPU_DOUT_10_L (24h), ISPU_DOUT_10_H (25h)

ISPU output register 10 (R). This register is also accessible from ISPU at address 6824h, 6825h (R/W).

Table 155. ISPU_DOUT_10_L register

DOUT10_7	DOUT10_6	DOUT10_5	DOUT10_4	DOUT10_3	DOUT10_2	DOUT10_1	DOUT10_0

Table 156. ISPU_DOUT_10_H register

DOUT10_15	DOUT10_14	DOUT10_13	DOUT10_12	DOUT10_11	DOUT10_10	DOUT10_9	DOUT10_8

Table 157. ISPU_DOUT_10 register description

DOUT10_[15:0]	General-purpose output.

11.19 ISPU_DOUT_11_L (26h), ISPU_DOUT_11_H (27h)

ISPU output register 11 (R). This register is also accessible from ISPU at address 6826h, 6827h (R/W).

Table 158. ISPU_DOUT_11_L register

DOUT11_7	DOUT11_6	DOUT11_5	DOUT11_4	DOUT11_3	DOUT11_2	DOUT11_1	DOUT11_0

Table 159. ISPU_DOUT_11_H register

DOUT11_15	DOUT11_14	DOUT11_13	DOUT11_12	DOUT11_11	DOUT11_10	DOUT11_9	DOUT11_8

Table 160. ISPU_DOUT_11 register description

DOUT11_[15:0]	General-purpose output.

11.20 ISPU_DOUT_12_L (28h), ISPU_DOUT_12_H (29h)

ISPU output register 12 (R). This register is also accessible from ISPU at address 6828h, 6829h (R/W).

Table 161. ISPU_DOUT_12_L register

DOUT12_7	DOUT12_6	DOUT12_5	DOUT12_4	DOUT12_3	DOUT12_2	DOUT12_1	DOUT12_0

Table 162. ISPU_DOUT_12_H register

DOUT12_15	DOUT12_14	DOUT12_13	DOUT12_12	DOUT12_11	DOUT12_10	DOUT12_9	DOUT12_8

Table 163. ISPU_DOUT_12 register description

DOUT12_[15:0]	General-purpose output.

11.21 ISPU_DOUT_13_L (2Ah), ISPU_DOUT_13_H (2Bh)

ISPU output register 13 (R). This register is also accessible from ISPU at address 682Ah, 682Bh (R/W).

Table 164. ISPU_DOUT_13_L register

DOUT13_7	DOUT13_6	DOUT13_5	DOUT13_4	DOUT13_3	DOUT13_2	DOUT13_1	DOUT13_0

Table 165. ISPU_DOUT_13_H register

DOUT13_15	DOUT13_14	DOUT13_13	DOUT13_12	DOUT13_11	DOUT13_10	DOUT13_9	DOUT13_8

Table 166. ISPU_DOUT_13 register description

DOUT13_[15:0]	General-purpose output.

11.22 ISPU_DOUT_14_L (2Ch), ISPU_DOUT_14_H (2Dh)

ISPU output register 14 (R). This register is also accessible from ISPU at address 682Ch, 682Dh (R/W).

Table 167. ISPU_DOUT_14_L register

DOUT14_7	DOUT14_6	DOUT14_5	DOUT14_4	DOUT14_3	DOUT14_2	DOUT14_1	DOUT14_0

Table 168. ISPU_DOUT_14_H register

DOUT14_15	DOUT14_14	DOUT14_13	DOUT14_12	DOUT14_11	DOUT14_10	DOUT14_9	DOUT14_8

Table 169. ISPU_DOUT_14 register description

DOUT14_[15:0]	General-purpose output.

11.23 ISPU_DOUT_15_L (2Eh), ISPU_DOUT_15_H (2Fh)

ISPU output register 15 (R). This register is also accessible from ISPU at address 682Eh, 682Fh (R/W).

Table 170. ISPU_DOUT_15_L register

DOUT15_7	DOUT15_6	DOUT15_5	DOUT15_4	DOUT15_3	DOUT15_2	DOUT15_1	DOUT15_0

Table 171. ISPU_DOUT_15_H register

DOUT15_15	DOUT15_14	DOUT15_13	DOUT15_12	DOUT15_11	DOUT15_10	DOUT15_9	DOUT15_8

Table 172. ISPU_DOUT_15 register description

DOUT15_[15:0]	General-purpose output.

11.24 ISPU_DOUT_16_L (30h), ISPU_DOUT_16_H (31h)

ISPU output register 16 (R). This register is also accessible from ISPU at address 6830h, 6831h (R/W).

Table 173. ISPU_DOUT_16_L register

DOUT16_7	DOUT16_6	DOUT16_5	DOUT16_4	DOUT16_3	DOUT16_2	DOUT16_1	DOUT16_0

Table 174. ISPU_DOUT_16_H register

DOUT16_15	DOUT16_14	DOUT16_13	DOUT16_12	DOUT16_11	DOUT16_10	DOUT16_9	DOUT16_8

Table 175. ISPU_DOUT_16 register description

DOUT16_[15:0]	General-purpose output.

11.25 ISPU_DOUT_17_L (32h), ISPU_DOUT_17_H (33h)

ISPU output register 17 (R). This register is also accessible from ISPU at address 6832h, 6833h (R/W).

Table 176. ISPU_DOUT_17_L register

DOUT17_7	DOUT17_6	DOUT17_5	DOUT17_4	DOUT17_3	DOUT17_2	DOUT17_1	DOUT17_0

Table 177. ISPU_DOUT_17_H register

DOUT17_15	DOUT17_14	DOUT17_13	DOUT17_12	DOUT17_11	DOUT17_10	DOUT17_9	DOUT17_8

Table 178. ISPU_DOUT_17 register description

DOUT17_[15:0]	General-purpose output.

11.26 ISPU_DOUT_18_L (34h), ISPU_DOUT_18_H (35h)

ISPU output register 18 (R). This register is also accessible from ISPU at address 6834h, 6835h (R/W).

Table 179. ISPU_DOUT_18_L register

DOUT18_7	DOUT18_6	DOUT18_5	DOUT18_4	DOUT18_3	DOUT18_2	DOUT18_1	DOUT18_0

Table 180. ISPU_DOUT_18_H register

DOUT18_15	DOUT18_14	DOUT18_13	DOUT18_12	DOUT18_11	DOUT18_10	DOUT18_9	DOUT18_8

Table 181. ISPU_DOUT_18 register description

DOUT18_[15:0]	General-purpose output.

11.27 ISPU_DOUT_19_L (36h), ISPU_DOUT_19_H (37h)

ISPU output register 19 (R). This register is also accessible from ISPU at address 6836h, 6837h (R/W).

Table 182. ISPU_DOUT_19_L register

DOUT19_7	DOUT19_6	DOUT19_5	DOUT19_4	DOUT19_3	DOUT19_2	DOUT19_1	DOUT19_0

Table 183. ISPU_DOUT_19_H register

DOUT19_15	DOUT19_14	DOUT19_13	DOUT19_12	DOUT19_11	DOUT19_10	DOUT19_9	DOUT19_8

Table 184. ISPU_DOUT_19 register description

DOUT19_[15:0]	General-purpose output.

11.28 ISPU_DOUT_20_L (38h), ISPU_DOUT_20_H (39h)

ISPU output register 20 (R). This register is also accessible from ISPU at address 6838h, 6839h (R/W).

Table 185. ISPU_DOUT_20_L register

DOUT20_7	DOUT20_6	DOUT20_5	DOUT20_4	DOUT20_3	DOUT20_2	DOUT20_1	DOUT20_0

Table 186. ISPU_DOUT_20_H register

DOUT20_15	DOUT20_14	DOUT20_13	DOUT20_12	DOUT20_11	DOUT20_10	DOUT20_9	DOUT20_8

Table 187. ISPU_DOUT_20 register description

DOUT20_[15:0]	General-purpose output.

11.29 ISPU_DOUT_21_L (3Ah), ISPU_DOUT_21_H (3Bh)

ISPU output register 21 (R). This register is also accessible from ISPU at address 683Ah, 683Bh (R/W).

Table 188. ISPU_DOUT_21_L register

DOUT21_7	DOUT21_6	DOUT21_5	DOUT21_4	DOUT21_3	DOUT21_2	DOUT21_1	DOUT21_0

Table 189. ISPU_DOUT_21_H register

DOUT21_15	DOUT21_14	DOUT21_13	DOUT21_12	DOUT21_11	DOUT21_10	DOUT21_9	DOUT21_8

Table 190. ISPU_DOUT_21 register description

DOUT21_[15:0]	General-purpose output.

11.30 ISPU_DOUT_22_L (3Ch), ISPU_DOUT_22_H (3Dh)

ISPU output register 22 (R). This register is also accessible from ISPU at address 683Ch, 683Dh (R/W).

Table 191. ISPU_DOUT_22_L register

DOUT22_7	DOUT22_6	DOUT22_5	DOUT22_4	DOUT22_3	DOUT22_2	DOUT22_1	DOUT22_0

Table 192. ISPU_DOUT_22_H register

DOUT22_15	DOUT22_14	DOUT22_13	DOUT22_12	DOUT22_11	DOUT22_10	DOUT22_9	DOUT22_8

Table 193. ISPU_DOUT_22 register description

DOUT22_[15:0]	General-purpose output.

11.31 ISPU_DOUT_23_L (3Eh), ISPU_DOUT_23_H (3Fh)

ISPU output register 23 (R). This register is also accessible from ISPU at address 683Eh, 683Fh (R/W).

Table 194. ISPU_DOUT_23_L register

DOUT23_7	DOUT23_6	DOUT23_5	DOUT23_4	DOUT23_3	DOUT23_2	DOUT23_1	DOUT23_0

Table 195. ISPU_DOUT_23_L register

DOUT23_15	DOUT23_14	DOUT23_13	DOUT23_12	DOUT23_11	DOUT23_10	DOUT23_9	DOUT23_8

Table 196. ISPU_DOUT_23 register description

DOUT23_[15:0]	General-purpose output.

11.32 ISPU_DOUT_24_L (40h), ISPU_DOUT_24_H (41h)

ISPU output register 24 (R). This register is also accessible from ISPU at address 6840h, 6841h (R/W).

Table 197. ISPU_DOUT_24_L register

DOUT24_7	DOUT24_6	DOUT24_5	DOUT24_4	DOUT24_3	DOUT24_2	DOUT24_1	DOUT24_0

Table 198. ISPU_DOUT_24_H register

DOUT24_15	DOUT24_14	DOUT24_13	DOUT24_12	DOUT24_11	DOUT24_10	DOUT24_9	DOUT24_8

Table 199. ISPU_DOUT_24 register description

DOUT24_[15:0]	General-purpose output.

11.33 ISPU_DOUT_25_L (42h), ISPU_DOUT_25_H (43h)

ISPU output register 25 (R). This register is also accessible from ISPU at address 6842h, 6843h (R/W).

Table 200. ISPU_DOUT_25_L register

DOUT25_7	DOUT25_6	DOUT25_5	DOUT25_4	DOUT25_3	DOUT25_2	DOUT25_1	DOUT25_0

Table 201. ISPU_DOUT_25_H register

DOUT25_15	DOUT25_14	DOUT25_13	DOUT25_12	DOUT25_11	DOUT25_10	DOUT25_9	DOUT25_8

Table 202. ISPU_DOUT_25 register description

DOUT25_[15:0]	General-purpose output.

11.34 ISPU_DOUT_26_L (44h), ISPU_DOUT_26_H (45h)

ISPU output register 26 (R). This register is also accessible from ISPU at address 6844h, 6845h (R/W).

Table 203. ISPU_DOUT_26_L register

DOUT26_7	DOUT26_6	DOUT26_5	DOUT26_4	DOUT26_3	DOUT26_2	DOUT26_1	DOUT26_0

Table 204. ISPU_DOUT_26_H register

DOUT26_15	DOUT26_14	DOUT26_13	DOUT26_12	DOUT26_11	DOUT26_10	DOUT26_9	DOUT26_8

Table 205. ISPU_DOUT_26 register description

DOUT26_[15:0]	General-purpose output.

11.35 ISPU_DOUT_27_L (46h), ISPU_DOUT_27_H (47h)

ISPU output register 27 (R). This register is also accessible from ISPU at address 6846h, 6847h (R/W).

Table 206. ISPU_DOUT_27_L register

DOUT27_7	DOUT27_6	DOUT27_5	DOUT27_4	DOUT27_3	DOUT27_2	DOUT27_1	DOUT27_0

Table 207. ISPU_DOUT_27_H register

DOUT27_15	DOUT27_14	DOUT27_13	DOUT27_12	DOUT27_11	DOUT27_10	DOUT27_9	DOUT27_8

Table 208. ISPU_DOUT_27 register description

DOUT27_[15:0]	General-purpose output.

11.36 ISPU_DOUT_28_L (48h), ISPU_DOUT_28_H (49h)

ISPU output register 28 (R). This register is also accessible from ISPU at address 6848h, 6849h (R/W).

Table 209. ISPU_DOUT_28_L register

DOUT28_7	DOUT28_6	DOUT28_5	DOUT28_4	DOUT28_3	DOUT28_2	DOUT28_1	DOUT28_0

Table 210. ISPU_DOUT_28_H register

DOUT28_15	DOUT28_14	DOUT28_13	DOUT28_12	DOUT28_11	DOUT28_10	DOUT28_9	DOUT28_8

Table 211. ISPU_DOUT_28 register description

DOUT28_[15:0]	General-purpose output.

11.37 ISPU_DOUT_29_L (4Ah), ISPU_DOUT_29_H (4Bh)

ISPU output register 29 (R). This register is also accessible from ISPU at address 684Ah, 684Bh (R/W).

Table 212. ISPU_DOUT_29_L register

DOUT29_7	DOUT29_6	DOUT29_5	DOUT29_4	DOUT29_3	DOUT29_2	DOUT29_1	DOUT29_0

Table 213. ISPU_DOUT_29_H register

DOUT29_15	DOUT29_14	DOUT29_13	DOUT29_12	DOUT29_11	DOUT29_10	DOUT29_9	DOUT29_8

Table 214. ISPU_DOUT_29 register description

DOUT29_[15:0]	General-purpose output.

11.38 ISPU_DOUT_30_L (4Ch), ISPU_DOUT_30_H (4Dh)

ISPU output register 30 (R). This register is also accessible from ISPU at address 684Ch, 684Dh (R/W).

Table 215. ISPU_DOUT_30_L register

DOUT30_7	DOUT30_6	DOUT30_5	DOUT30_4	DOUT30_3	DOUT30_2	DOUT30_1	DOUT30_0

Table 216. ISPU_DOUT_30_H register

DOUT30_15	DOUT30_14	DOUT30_13	DOUT30_12	DOUT30_11	DOUT30_10	DOUT30_9	DOUT30_8

Table 217. ISPU_DOUT_30 register description

DOUT30_[15:0]	General-purpose output.

11.39 ISPU_DOUT_31_L (4Eh), ISPU_DOUT_31_H (4Fh)

ISPU output register 31 (R). This register is also accessible from ISPU at address 684Eh, 684Fh (R/W).

Table 218. ISPU_DOUT_31_L register

DOUT31_7	DOUT31_6	DOUT31_5	DOUT31_4	DOUT31_3	DOUT31_2	DOUT31_1	DOUT31_0

Table 219. ISPU_DOUT_31_H register

DOUT31_15	DOUT31_14	DOUT31_13	DOUT31_12	DOUT31_11	DOUT31_10	DOUT31_9	DOUT31_8

Table 220. ISPU_DOUT_31 register description

DOUT31_[15:0]	General-purpose output.

11.40 ISPU_INT1_CTRL0 (50h), ISPU_INT1_CTRL1 (51h), ISPU_INT1_CTRL2 (52h), ISPU_INT1_CTRL3 (53h)

ISPU INT1 configuration register (R/W). This register is also accessible from ISPU at address 6850h, 6851h, 6852h, 6853h (R).

Table 221. ISPU_INT1_CTRL0 register

ISPU_INT1_CTRL7	ISPU_INT1_CTRL6	ISPU_INT1_CTRL5	ISPU_INT1_CTRL4	ISPU_INT1_CTRL3	ISPU_INT1_CTRL2	ISPU_INT1_CTRL1	ISPU_INT1_CTRL0

Table 222. ISPU_INT1_CTRL1 register

ISPU_INT1_CTRL15	ISPU_INT1_CTRL14	ISPU_INT1_CTRL13	ISPU_INT1_CTRL12	ISPU_INT1_CTRL11	ISPU_INT1_CTRL10	ISPU_INT1_CTRL9	ISPU_INT1_CTRL8

Table 223. ISPU_INT1_CTRL2 register

ISPU_INT1_CTRL23	ISPU_INT1_CTRL22	ISPU_INT1_CTRL21	ISPU_INT1_CTRL20	ISPU_INT1_CTRL19	ISPU_INT1_CTRL18	ISPU_INT1_CTRL17	ISPU_INT1_CTRL16

Table 224. ISPU_INT1_CTRL3 register

0	0	ISPU_INT1_CTRL29	ISPU_INT1_CTRL28	ISPU_INT1_CTRL27	ISPU_INT1_CTRL26	ISPU_INT1_CTRL25	ISPU_INT1_CTRL24

Table 225. ISPU_INT1_CTRL register description

ISPU_INT1_CTRL[29:0]	Routing 30-bit interrupt flags (in ISPU_INT_STATUS registers) to the INT1 pin. INT1_ISPU must be set to 1 also.

11.41 ISPU_INT2_CTRL0 (54h), ISPU_INT2_CTRL1 (55h), ISPU_INT2_CTRL2 (56h), ISPU_INT2_CTRL3 (57h)

ISPU INT2 configuration register (R/W). This register is also accessible from ISPU at address 6854h, 6855h, 6856h, 6857h (R).

Table 226. ISPU_INT2_CTRL0 register

ISPU_INT2_CTRL7	ISPU_INT2_CTRL6	ISPU_INT2_CTRL5	ISPU_INT2_CTRL4	ISPU_INT2_CTRL3	ISPU_INT2_CTRL2	ISPU_INT2_CTRL1	ISPU_INT2_CTRL0

Table 227. ISPU_INT2_CTRL1 register

ISPU_INT2_CTRL15	ISPU_INT2_CTRL14	ISPU_INT2_CTRL13	ISPU_INT2_CTRL12	ISPU_INT2_CTRL11	ISPU_INT2_CTRL10	ISPU_INT2_CTRL9	ISPU_INT2_CTRL8

Table 228. ISPU_INT2_CTRL2 register

ISPU_INT2_CTRL23	ISPU_INT2_CTRL22	ISPU_INT2_CTRL21	ISPU_INT2_CTRL20	ISPU_INT2_CTRL19	ISPU_INT2_CTRL18	ISPU_INT2_CTRL17	ISPU_INT2_CTRL16

Table 229. ISPU_INT2_CTRL3 register

0	0	ISPU_INT2_CTRL29	ISPU_INT2_CTRL28	ISPU_INT2_CTRL27	ISPU_INT2_CTRL26	ISPU_INT2_CTRL25	ISPU_INT2_CTRL24

Table 230. ISPU_INT2_CTRL register description

ISPU_INT2_CTRL[29:0]	Routing 30-bit interrupt flags (in ISPU_INT_STATUS registers) to the INT2 pin. INT2_ISPU must be set to 1 also.

11.42 ISPU_INT_STATUS0 (58h), ISPU_INT_STATUS1 (59h), ISPU_INT_STATUS2 (5Ah), ISPU_INT_STATUS3 (5Bh)

ISPU interrupt status register (R). This register is also accessible from ISPU at address 6858h, 6859h, 685Ah, 685Bh (R/W).

Table 231. ISPU_INT_STATUS0 register

ISPU_INT_STATUS7	ISPU_INT_STATUS6	ISPU_INT_STATUS5	ISPU_INT_STATUS4	ISPU_INT_STATUS3	ISPU_INT_STATUS2	ISPU_INT_STATUS1	ISPU_INT_STATUS0

Table 232. ISPU_INT_STATUS1 register

ISPU_INT_STATUS15	ISPU_INT_STATUS14	ISPU_INT_STATUS13	ISPU_INT_STATUS12	ISPU_INT_STATUS11	ISPU_INT_STATUS10	ISPU_INT_STATUS9	ISPU_INT_STATUS8

Table 233. ISPU_INT_STATUS2 register

ISPU_INT_STATUS23	ISPU_INT_STATUS22	ISPU_INT_STATUS21	ISPU_INT_STATUS20	ISPU_INT_STATUS19	ISPU_INT_STATUS18	ISPU_INT_STATUS17	ISPU_INT_STATUS16

Table 234. ISPU_INT_STATUS3 register

0	0	ISPU_INT_STATUS29	ISPU_INT_STATUS28	ISPU_INT_STATUS27	ISPU_INT_STATUS26	ISPU_INT_STATUS25	ISPU_INT_STATUS24

Table 235. ISPU_INT_STATUS register description

ISPU_INT_STATUS[29:0]	30-bit interrupt flags.

11.43 ISPU_ALGO0 (70h), ISPU_ALGO1 (71h), ISPU_ALGO2 (72h), ISPU_ALGO3 (73h)

ISPU algorithm register (R/W). This register is also accessible from ISPU at address 6870h, 6871h, 6872h, 6873h (R).

Table 236. ISPU_ALGO0 register

ISPU_ ALGO7	ISPU_ ALGO6	ISPU_ ALGO5	ISPU_ ALGO4	ISPU_ ALGO3	ISPU_ ALGO2	ISPU_ ALGO1	ISPU_ ALGO0

Table 237. ISPU_ALGO1 register

ISPU_ ALGO15	ISPU_ ALGO14	ISPU_ ALGO13	ISPU_ ALGO12	ISPU_ ALGO11	ISPU_ ALGO10	ISPU_ ALGO9	ISPU_ ALGO8

Table 238. ISPU_ALGO2 register

ISPU_ ALGO23	ISPU_ ALGO22	ISPU_ ALGO21	ISPU_ ALGO20	ISPU_ ALGO19	ISPU_ ALGO18	ISPU_ ALGO17	ISPU_ ALGO16

Table 239. ISPU_ALGO3 register

0	0	ISPU_ ALGO29	ISPU_ ALGO28	ISPU_ ALGO27	ISPU_ ALGO26	ISPU_ ALGO25	ISPU_ ALGO24

Table 240. ISPU_ALGO register description

ISPU_ALGO[29:0]	Enable configurations in order to run up to 30 independent algorithms.

12 ISPU functions register mapping

The table given below provides a list of the registers internally available in the ISPU core.

Table 241. Register map - ISPU functions internally available

ISPU address (hex)	Bytes	Name	IF access	ISPU access
6800	1	ISPU_GLB_CALL_EN	No	R/W
685C	1	ISPU_INT_PIN	No	R/W
6880-6881	2	ISPU_ARAW_X	No	R
6884-6885	2	ISPU_ARAW_Y	No	R
6888-6889	2	ISPU_ARAW_Z	No	R
688C-688D	2	ISPU_GRAW_X	No	R
6890-6891	2	ISPU_GRAW_Y	No	R
6894-6895	2	ISPU_GRAW_Z	No	R
6898-6899	2	ISPU_ERAW_0	No	R
689C-689D	2	ISPU_ERAW_1	No	R
68A0-68A1	2	ISPU_ERAW_2	No	R
68A4-68A5	2	ISPU_TEMP	No	R
68B8-68BB	4	ISPU_CALL_EN	No	R/W
6948-6949	2	ISPU_DTIME_0	No	R
694A-694B	2	ISPU_DTIME_1	No	R

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

13 ISPU functions register description

13.1 ISPU_GLB_CALL_EN (6800h)

ISPU read/write access (6800h)

Table 242. ISPU_GLB_CALL_EN registers

-	-	-	-	-	-	-	ISPU_GLB_CALL_EN

Table 243. ISPU_GLB_CALL_EN register description

ISPU_GLB_CALL_EN	Enables internal interrupt generation to run algorithm routines.

13.2 ISPU_INT_PIN (685Ch)

ISPU read/write access (685Ch)

Table 244. ISPU_INT_PIN registers

0	0	0	0	0	0	INT2	INT1

Table 245. ISPU_INT_PIN register description

INT2	Flag for interrupt generation on INT2 pin.
INT1	Flag for interrupt generation on INT1 pin.

13.3 ISPU_ARAW_X_L (6880h), ISPU_ARAW_X_H (6881h)

ISPU read access (6880h, 6881h)

Table 246. ISPU_ARAW_X_L register

ISPU_ARAW_X_7	ISPU_ARAW_X_6	ISPU_ARAW_X_5	ISPU_ARAW_X_4	ISPU_ARAW_X_3	ISPU_ARAW_X_2	ISPU_ARAW_X_1	ISPU_ARAW_X_0

Table 247. ISPU_ARAW_X_H register

ISPU_ARAW_X_15	ISPU_ARAW_X_14	ISPU_ARAW_X_13	ISPU_ARAW_X_12	ISPU_ARAW_X_11	ISPU_ARAW_X_10	ISPU_ARAW_X_9	ISPU_ARAW_X_8

Table 248. ISPU_ARAW_X register description

ISPU_ARAW_X_[15:0]	Accelerometer X-axis output expressed in two’s complement.

13.4 ISPU_ARAW_Y_L (6884h), ISPU_ARAW_Y_H (6885h)

ISPU read access (6884h, 6885h)

Table 249. ISPU_ARAW_Y_L register

ISPU_ ARAW_Y_7	ISPU_ ARAW_Y_6	ISPU_ ARAW_Y_5	ISPU_ ARAW_Y_4	ISPU_ ARAW_Y_3	ISPU_ ARAW_Y_2	ISPU_ ARAW_Y_1	ISPU_ ARAW_Y_0

Table 250. ISPU_ARAW_Y_H register

ISPU_ ARAW_Y_15	ISPU_ ARAW_Y_14	ISPU_ ARAW_Y_13	ISPU_ ARAW_Y_12	ISPU_ ARAW_Y_11	ISPU_ ARAW_Y_10	ISPU_ ARAW_Y_9	ISPU_ ARAW_Y_8

Table 251. ISPU_ARAW_Y register description

ISPU_ARAW_Y_[15:0]	Accelerometer Y-axis output expressed in two's complement.

13.5 ISPU_ARAW_Z_L (6888h), ISPU_ARAW_Z_H (6889h)

ISPU read access (6888h, 6889h)

Table 252. ISPU_ARAW_Z_L register

ISPU_ ARAW_Z_7	ISPU_ ARAW_Z_6	ISPU_ ARAW_Z_5	ISPU_ ARAW_Z_4	ISPU_ ARAW_Z_3	ISPU_ ARAW_Z_2	ISPU_ ARAW_Z_1	ISPU_ ARAW_Z_0

Table 253. ISPU_ARAW_Z_H register

ISPU_ ARAW_Z_15	ISPU_ ARAW_Z_14	ISPU_ ARAW_Z_13	ISPU_ ARAW_Z_12	ISPU_ ARAW_Z_11	ISPU_ ARAW_Z_10	ISPU_ ARAW_Z_9	ISPU_ ARAW_Z_8

Table 254. ISPU_ARAW_Z register description

ISPU_ARAW_Z_[15:0]	Accelerometer Z-axis output expressed in two's complement.

13.6 ISPU_GRAW_X_L (688Ch), ISPU_GRAW_X_H (688Dh)

ISPU read access (688Ch, 688Dh)

Table 255. ISPU_GRAW_X_L register

ISPU_ GRAW_X_7	ISPU_ GRAW_X_6	ISPU_ GRAW_X_5	ISPU_ GRAW_X_4	ISPU_ GRAW_X_3	ISPU_ GRAW_X_2	ISPU_ GRAW_X_1	ISPU_ GRAW_X_0

Table 256. ISPU_GRAW_X_H register

ISPU_ GRAW_X_15	ISPU_ GRAW_X_14	ISPU_ GRAW_X_13	ISPU_ GRAW_X_12	ISPU_ GRAW_X_11	ISPU_ GRAW_X_10	ISPU_ GRAW_X_9	ISPU_ GRAW_X_8

Table 257. ISPU_GRAW_X register description

ISPU_GRAW_X_[15:0]	Gyroscope pitch axis output expressed in two's complement.

13.7 ISPU_GRAW_Y_L (6890h), ISPU_GRAW_Y_L (6891h)

ISPU read access (6890h, 6891h)

Table 258. ISPU_GRAW_Y_L registers

ISPU_ GRAW_Y_7	ISPU_ GRAW_Y_6	ISPU_ GRAW_Y_5	ISPU_ GRAW_Y_4	ISPU_ GRAW_Y_3	ISPU_ GRAW_Y_2	ISPU_ GRAW_Y_1	ISPU_ GRAW_Y_0

Table 259. ISPU_GRAW_Y_H registers

ISPU_ GRAW_Y_15	ISPU_ GRAW_Y_14	ISPU_ GRAW_Y_13	ISPU_ GRAW_Y_12	ISPU_ GRAW_Y_11	ISPU_ GRAW_Y_10	ISPU_ GRAW_Y_9	ISPU_ GRAW_Y_8

Table 260. ISPU_GRAW_Y register description

ISPU_GRAW_Y_[15:0]	Gyroscope roll axis output expressed in two's complement.

13.8 ISPU_GRAW_Z_L (6894h), ISPU_GRAW_Z_H (6895h)

ISPU read access (6894h, 6895h)

Table 261. ISPU_GRAW_Z_L registers

ISPU_ GRAW_Z_7	ISPU_ GRAW_Z_6	ISPU_ GRAW_Z_5	ISPU_ GRAW_Z_4	ISPU_ GRAW_Z_3	ISPU_ GRAW_Z_2	ISPU_ GRAW_Z_1	ISPU_ GRAW_Z_0

Table 262. ISPU_GRAW_Z_H registers

ISPU_ GRAW_Z_15	ISPU_ GRAW_Z_14	ISPU_ GRAW_Z_13	ISPU_ GRAW_Z_12	ISPU_ GRAW_Z_11	ISPU_ GRAW_Z_10	ISPU_ GRAW_Z_9	ISPU_ GRAW_Z_8

Table 263. ISPU_GRAW_Z register description

ISPU_GRAW_Z_[15:0]	Gyroscope yaw axis output expressed in two's complement.

13.9 ISPU_ERAW_0_L (6898h), ISPU_ERAW_0_H (6899h)

ISPU read access (6898h, 6899h)

Table 264. ISPU_ERAW_0_L registers

ISPU_ ERAW_0_7	ISPU_ MERAW_0_6	ISPU_ ERAW_0_5	ISPU_ ERAW_0_4	ISPU_ ERAW_0_3	ISPU_ ERAW_0_2	ISPU_ ERAW_0_1	ISPU_ ERAW_0_0

Table 265. ISPU_ERAW_0_H registers

ISPU_ ERAW_0_15	ISPU_ ERAW_0_14	ISPU_ ERAW_0_13	ISPU_ ERAW_0_12	ISPU_ ERAW_0_11	ISPU_ ERAW_0_10	ISPU_ ERAW_0_9	ISPU_ ERAW_0_8

Table 266. ISPU_ERAW_0 register description

ISPU_ERAW_0_[15:0]	External sensor data from SENSOR_HUB_1 and SENSOR_HUB_2.

13.10 ISPU_ERAW_1_L (689Ch), ISPU_ERAW_1_H (689Dh)

ISPU read access (689Ch, 689Dh)

Table 267. ISPU_ERAW_1_L register

ISPU_ ERAW_1_7	ISPU_ ERAW_1_6	ISPU_ MRAW_Y_5	ISPU_ ERAW_1_4	ISPU_ ERAW_1_3	ISPU_ ERAW_1_2	ISPU_ ERAW_1_1	ISPU_ ERAW_1_0

Table 268. ISPU_ERAW_1_H register

ISPU_ ERAW_1_15	ISPU_ ERAW_1_14	ISPU_ ERAW_1_13	ISPU_ ERAW_1_12	ISPU_ ERAW_1_11	ISPU_ ERAW_1_10	ISPU_ ERAW_1_9	ISPU_ ERAW_1_8

Table 269. ISPU_ERAW_1 register description

ISPU_ERAW_1_[15:0]	External sensor data from SENSOR_HUB_3 and SENSOR_HUB_4.

13.11 ISPU_ERAW_2_L (68A0h), ISPU_ERAW_2_H (68A1h)

ISPU read access (68A0h, 68A1h)

Table 270. ISPU_ERAW_2_L register

ISPU_ ERAW_2_7	ISPU_ ERAW_2_6	ISPU_ ERAW_2_5	ISPU_ ERAW_2_4	ISPU_ ERAW_2_3	ISPU_ ERAW_2_2	ISPU_ ERAW_2_1	ISPU_ ERAW_2_0

Table 271. ISPU_ERAW_2_H register

ISPU_ ERAW_2_15	ISPU_ ERAW_2_14	ISPU_ ERAW_2_13	ISPU_ ERAW_2_12	ISPU_ ERAW_2_11	ISPU_ ERAW_2_10	ISPU_ ERAW_2_9	ISPU_ ERAW_2_8

Table 272. ISPU_ERAW_2 register description

ISPU_ERAW_2_[15:0]	External sensor data from SENSOR_HUB_5 and SENSOR_HUB_6.

13.12 ISPU_TEMP_L (68A4h), ISPU_TEMP_H (68A5h)

ISPU read access (68A4h, 68A5h)

Table 273. ISPU_TEMP_L register

ISPU_ TEMP_7	ISPU_ TEMP_6	ISPU_ TEMP_5	ISPU_ TEMP_4	ISPU_ TEMP_3	ISPU_ TEMP_2	ISPU_ TEMP_1	ISPU_ TEMP_0

Table 274. ISPU_TEMP_H register

ISPU_ TEMP_15	ISPU_ TEMP_14	ISPU_ TEMP_13	ISPU_ TEMP_12	ISPU_ TEMP_11	ISPU_ TEMP_10	ISPU_ TEMP_9	ISPU_ TEMP_8

Table 275. ISPU_TEMP register description

ISPU_TEMP_[15:0]	Temperature sensor output expressed in two’s complement.

13.13 ISPU_CALL_EN_0 (68B8h), ISPU_CALL_EN_1 (68B9h), ISPU_CALL_EN_2 (68BAh), ISPU_CALL_EN_3 (68BBh)

ISPU read/write access (68B8h, 68B9h, 68BAh, 68BBh)

Table 276. ISPU_CALL_EN_0 register

ISPU_CALL_ ALGO_6	ISPU_CALL_ ALGO_5	ISPU_CALL_ ALGO_4	ISPU_CALL_ ALGO_3	ISPU_CALL_ ALGO_2	ISPU_CALL_ ALGO1	ISPU_CALL_ ALGO_0	0(1)

1. *This bit must be set to 0 for the correct operation of the device.*

Table 277. ISPU_CALL_EN_1 register

ISPU_CALL_ ALGO_14	ISPU_CALL_ ALGO_13	ISPU_CALL_ ALGO_12	ISPU_CALL_ ALGO_11	ISPU_CALL_ ALGO_10	ISPU_CALL_ ALGO_9	ISPU_CALL_ ALGO_8	ISPU_CALL_ ALGO_7

Table 278. ISPU_CALL_EN_2 register

ISPU_CALL_ ALGO_22	ISPU_CALL_ ALGO_21	ISPU_CALL_ ALGO_20	ISPU_CALL_ ALGO_19	ISPU_CALL_ ALGO_18	ISPU_CALL_ ALGO_17	ISPU_CALL_ ALGO_16	ISPU_CALL_ ALGO_15

Table 279. ISPU_CALL_EN_3 register

0(1)	ISPU_CALL_ ALGO_29	ISPU_CALL_ ALGO_28	ISPU_CALL_ ALGO_27	ISPU_CALL_ ALGO_26	ISPU_CALL_ ALGO_25	ISPU_CALL_ ALGO_24	ISPU_CALL_ ALGO_23

1. *This bit must be set to 0 for the correct operation of the device.*

Table 280. ISPU_CALL_EN register description

ISPU_CALL_ALGO_[29:0]	If bit i=1, IRQ is generated for the execution of ISPU_ALGO_(i-1). After it is written to 1, it remains at 1 until the ISPU_ALGO_(i-1) routine is completed.

13.14 ISPU_DTIME_0_L (6948h), ISPU_DTIME_0_H (6949h), ISPU_DTIME_1_L (694Ah), ISPU_DTIME_1_H (694Bh)

ISPU read access (6948h, 6949h, 694Ah, 694Bh)

Table 281. ISPU_DTIME_0_L output register

ISPU_ DTIME_7	ISPU_ DTIME_6	ISPU_ DTIME_5	ISPU_ DTIME_4	ISPU_ DTIME_3	ISPU_ DTIME_2	ISPU_ DTIME_1	ISPU_ DTIME_0

Table 282. ISPU_DTIME_0_H output register

ISPU_ DTIME_15	ISPU_ DTIME_14	ISPU_ DTIME_13	ISPU_ DTIME_12	ISPU_ DTIME_11	ISPU_ DTIME_10	ISPU_ DTIME_9	ISPU_ DTIME_8

Table 283. ISPU_DTIME_1_L output register

ISPU_ DTIME_23	ISPU_ DTIME_22	ISPU_ DTIME_21	ISPU_ DTIME_20	ISPU_ DTIME_19	ISPU_ DTIME_18	ISPU_ DTIME_17	ISPU_ DTIME_16

Table 284. ISPU_DTIME_1_H output register

ISPU_ DTIME_31	ISPU_ DTIME_30	ISPU_ DTIME_29	ISPU_ DTIME_28	ISPU_ DTIME_27	ISPU_ DTIME_26	ISPU_ DTIME_25	ISPU_ DTIME_24

Table 285. ISPU_DTIME output register description

ISPU_DTIME_[31:0]	Actual delta time at 104 Hz (expressed in seconds): it is represented as a single precision floating-point number.

14 Sensor hub register mapping

The table given below provides a list of the registers for the sensor hub functions available in the device and the corresponding addresses. The sensor hub registers are accessible when bit SHUB_REG_ACCESS is set to 1 in FUNC_CFG_ACCESS (01h).

Table 286. Registers address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
SENSOR_HUB_1	R	02	00000010	output	
SENSOR_HUB_2	R	03	00000011	output	
SENSOR_HUB_3	R	04	00000100	output	
SENSOR_HUB_4	R	05	00000101	output	
SENSOR_HUB_5	R	06	00000110	output	
SENSOR_HUB_6	R	07	00000111	output	
SENSOR_HUB_7	R	08	00001000	output	
SENSOR_HUB_8	R	09	00001001	output	
SENSOR_HUB_9	R	0A	00001010	output	
SENSOR_HUB_10	R	0B	00001011	output	
SENSOR_HUB_11	R	0C	00001100	output	
SENSOR_HUB_12	R	0D	00001101	output	
SENSOR_HUB_13	R	0E	00001110	output	
SENSOR_HUB_14	R	0F	00001111	output	
SENSOR_HUB_15	R	10	00010000	output	
SENSOR_HUB_16	R	11	00010001	output	
SENSOR_HUB_17	R	12	00010010	output	
SENSOR_HUB_18	R	13	00010011	output	
MASTER_CONFIG	R/W	14	00010100	00000000	
SLV0_ADD	R/W	15	00010101	00000000	
SLV0_SUBADD	R/W	16	00010110	00000000	
SLV0_CONFIG	R/W	17	00010111	00000000	
SLV1_ADD	R/W	18	00011000	00000000	
SLV1_SUBADD	R/W	19	00011001	00000000	
SLV1_CONFIG	R/W	1A	00011010	00000000	
SLV2_ADD	R/W	1B	00011011	00000000	
SLV2_SUBADD	R/W	1C	00011100	00000000	
SLV2_CONFIG	R/W	1D	00011101	00000000	
SLV3_ADD	R/W	1E	00011110	00000000	
SLV3_SUBADD	R/W	1F	00011111	00000000	
SLV3_CONFIG	R/W	20	00100000	00000000	
DATAWRITE_SLV0	R/W	21	00100001	00000000	
STATUS_MASTER	R	22	00100010	output	

Reserved registers must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

15 Sensor hub register description

15.1 SENSOR_HUB_1 (02h)

Sensor hub output register (R)

First byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 287. SENSOR_HUB_1 register

Sensor Hub1_7	Sensor Hub1_6	Sensor Hub1_5	Sensor Hub1_4	Sensor Hub1_3	Sensor Hub1_2	Sensor Hub1_1	Sensor Hub1_0

Table 288. SENSOR_HUB_1 register description

SensorHub1_[7:0]	First byte associated to external sensors.

15.2 SENSOR_HUB_2 (03h)

Sensor hub output register (R)

Second byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 289. SENSOR_HUB_2 register

Sensor Hub2_7	Sensor Hub2_6	Sensor Hub2_5	Sensor Hub2_4	Sensor Hub2_3	Sensor Hub2_2	Sensor Hub2_1	Sensor Hub2_0

Table 290. SENSOR_HUB_2 register description

SensorHub2_[7:0]	Second byte associated to external sensors.

15.3 SENSOR_HUB_3 (04h)

Sensor hub output register (R)

Third byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 291. SENSOR_HUB_3 register

Sensor Hub3_7	Sensor Hub3_6	Sensor Hub3_5	Sensor Hub3_4	Sensor Hub3_3	Sensor Hub3_2	Sensor Hub3_1	Sensor Hub3_0

Table 292. SENSOR_HUB_3 register description

SensorHub3_[7:0]	Third byte associated to external sensors.

15.4 SENSOR_HUB_4 (05h)

Sensor hub output register (R)

Fourth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 293. SENSOR_HUB_4 register

Sensor Hub4_7	Sensor Hub4_6	Sensor Hub4_5	Sensor Hub4_4	Sensor Hub4_3	Sensor Hub4_2	Sensor Hub4_1	Sensor Hub4_0

Table 294. SENSOR_HUB_4 register description

SensorHub4_[7:0]	Fourth byte associated to external sensors.

15.5 SENSOR_HUB_5 (06h)

Sensor hub output register (R)

Fifth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 295. SENSOR_HUB_5 register

Sensor Hub5_7	Sensor Hub5_6	Sensor Hub5_5	Sensor Hub5_4	Sensor Hub5_3	Sensor Hub5_2	Sensor Hub5_1	Sensor Hub5_0

Table 296. SENSOR_HUB_5 register description

SensorHub5_[7:0]	Fifth byte associated to external sensors.

15.6 SENSOR_HUB_6 (07h)

Sensor hub output register (R)

Sixth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 297. SENSOR_HUB_6 register

Sensor Hub6_7	Sensor Hub6_6	Sensor Hub6_5	Sensor Hub6_4	Sensor Hub6_3	Sensor Hub6_2	Sensor Hub6_1	Sensor Hub6_0

Table 298. SENSOR_HUB_6 register description

SensorHub6_[7:0]	Sixth byte associated to external sensors.

15.7 SENSOR_HUB_7 (08h)

Sensor hub output register (R)

Seventh byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 299. SENSOR_HUB_7 register

Sensor Hub7_7	Sensor Hub7_6	Sensor Hub7_5	Sensor Hub7_4	Sensor Hub7_3	Sensor Hub7_2	Sensor Hub7_1	Sensor Hub7_0

Table 300. SENSOR_HUB_7 register description

SensorHub7_[7:0]	Seventh byte associated to external sensors.

15.8 SENSOR_HUB_8 (09h)

Sensor hub output register (R)

Eighth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 301. SENSOR_HUB_8 register

Sensor Hub8_7	Sensor Hub8_6	Sensor Hub8_5	Sensor Hub8_4	Sensor Hub8_3	Sensor Hub8_2	Sensor Hub8_1	Sensor Hub8_0

Table 302. SENSOR_HUB_8 register description

SensorHub8_[7:0]	Eighth byte associated to external sensors.

15.9 SENSOR_HUB_9 (0Ah)

Sensor hub output register (R)

Ninth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 303. SENSOR_HUB_9 register

Sensor Hub9_7	Sensor Hub9_6	Sensor Hub9_5	Sensor Hub9_4	Sensor Hub9_3	Sensor Hub9_2	Sensor Hub9_1	Sensor Hub9_0

Table 304. SENSOR_HUB_9 register description

SensorHub9_[7:0]	Ninth byte associated to external sensors.

15.10 SENSOR_HUB_10 (0Bh)

Sensor hub output register (R)

Tenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 305. SENSOR_HUB_10 register

Sensor Hub10_7	Sensor Hub10_6	Sensor Hub10_5	Sensor Hub10_4	Sensor Hub10_3	Sensor Hub10_2	Sensor Hub10_1	Sensor Hub10_0

Table 306. SENSOR_HUB_10 register description

SensorHub10_[7:0]	Tenth byte associated to external sensors.

15.11 SENSOR_HUB_11 (0Ch)

Sensor hub output register (R)

Eleventh byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 307. SENSOR_HUB_11 register

Sensor Hub11_7	Sensor Hub11_6	Sensor Hub11_5	Sensor Hub11_4	Sensor Hub11_3	Sensor Hub11_2	Sensor Hub11_1	Sensor Hub11_0

Table 308. SENSOR_HUB_11 register description

SensorHub11_[7:0]	Eleventh byte associated to external sensors.

15.12 SENSOR_HUB_12 (0Dh)

Sensor hub output register (R)

Twelfth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 309. SENSOR_HUB_12 register

Sensor Hub12_7	Sensor Hub12_6	Sensor Hub12_5	Sensor Hub12_4	Sensor Hub12_3	Sensor Hub12_2	Sensor Hub12_1	Sensor Hub12_0

Table 310. SENSOR_HUB_12 register description

SensorHub12_[7:0]	Twelfth byte associated to external sensors.

15.13 SENSOR_HUB_13 (0Eh)

Sensor hub output register (R)

Thirteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 311. SENSOR_HUB_13 register

Sensor Hub13_7	Sensor Hub13_6	Sensor Hub13_5	Sensor Hub13_4	Sensor Hub13_3	Sensor Hub13_2	Sensor Hub13_1	Sensor Hub13_0

Table 312. SENSOR_HUB_13 register description

SensorHub13_[7:0]	Thirteenth byte associated to external sensors.

15.14 SENSOR_HUB_14 (0Fh)

Sensor hub output register (R)

Fourteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 313. SENSOR_HUB_14 register

Sensor Hub14_7	Sensor Hub14_6	Sensor Hub14_5	Sensor Hub14_4	Sensor Hub14_3	Sensor Hub14_2	Sensor Hub14_1	Sensor Hub14_0

Table 314. SENSOR_HUB_14 register description

SensorHub14_[7:0]	Fourteenth byte associated to external sensors.

15.15 SENSOR_HUB_15 (10h)

Sensor hub output register (R)

Fifteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 315. SENSOR_HUB_15 register

Sensor Hub15_7	Sensor Hub15_6	Sensor Hub15_5	Sensor Hub15_4	Sensor Hub15_3	Sensor Hub15_2	Sensor Hub15_1	Sensor Hub15_0

Table 316. SENSOR_HUB_15 register description

SensorHub15_[7:0]	Fifteenth byte associated to external sensors.

15.16 SENSOR_HUB_16 (11h)

Sensor hub output register (R)

Sixteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 317. SENSOR_HUB_16 register

Sensor Hub16_7	Sensor Hub16_6	Sensor Hub16_5	Sensor Hub16_4	Sensor Hub16_3	Sensor Hub16_2	Sensor Hub16_1	Sensor Hub16_0

Table 318. SENSOR_HUB_16 register description

SensorHub16_[7:0]	Sixteenth byte associated to external sensors.

15.17 SENSOR_HUB_17 (12h)

Sensor hub output register (R)

Seventeenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 319. SENSOR_HUB_17 register

Sensor Hub17_7	Sensor Hub17_6	Sensor Hub17_5	Sensor Hub17_4	Sensor Hub17_3	Sensor Hub17_2	Sensor Hub17_1	Sensor Hub17_0

Table 320. SENSOR_HUB_17 register description

SensorHub17_[7:0]	Seventeenth byte associated to external sensors.

15.18 SENSOR_HUB_18 (13h)

Sensor hub output register (R)

Eighteenth byte associated to external sensors. The content of the register is consistent with the SLVx_CONFIG number of read operation configurations (for external sensors from x = 0 to x = 3).

Table 321. SENSOR_HUB_18 register

Sensor Hub18_7	Sensor Hub18_6	Sensor Hub18_5	Sensor Hub18_4	Sensor Hub18_3	Sensor Hub18_2	Sensor Hub18_1	Sensor Hub18_0

Table 322. SENSOR_HUB_18 register description

SensorHub18_[7:0]	Eighteenth byte associated to external sensors.

15.19 MASTER_CONFIG (14h)

Master configuration register (R/W)

Table 323. MASTER_CONFIG register

RST_MASTER_REGS	WRITE_ONCE	START_CONFIG	PASS_THROUGH_MODE	SHUB_PU_EN	MASTER_ON	AUX_SENS_ON_1	AUX_SENS_ON_0

Table 324. MASTER_CONFIG register description

RST_MASTER_REGS	Resets master logic and output registers. Must be set to 1 and then set it to 0. Default value: 0
WRITE_ONCE	Slave 0 write operation is performed only at the first sensor hub cycle. Default value: 0 (0: write operation for each sensor hub cycle; 1: write operation only for the first sensor hub cycle)
START_CONFIG	Selects sensor hub trigger signal. Default value: 0 (0: sensor hub trigger signal is the accelerometer/gyro data-ready; 1: sensor hub trigger signal is external to INT2 pin)
PASS_THROUGH_MODE	I²C interface pass-through. Default value: 0 (0: pass-through disabled; 1: pass-through enabled, main I²C line is short-circuited with the auxiliary line)
SHUB_PU_EN	Enables master I²C pull-up. Default value: 0 (0: internal pull-up on auxiliary I²C line disabled; 1: internal pull-up on auxiliary I²C line enabled)
MASTER_ON	Enables sensor hub I²C master. Default: 0 (0: master I²C of sensor hub disabled; 1: master I²C of sensor hub enabled)
AUX_SENS_ON_[1:0]	Number of external sensors to be read by the sensor hub. (00: one sensor; 01: two sensors; 10: three sensors; 11: four sensors)

15.20 SLV0_ADD (15h)

I²C slave address of the first external sensor (sensor 1) register (R/W)

Table 325. SLV0_ADD register

slave0_ add6	slave0_ add5	slave0_ add4	slave0_ add3	slave0_ add2	slave0_ add1	slave0_ add0	rw_0

Table 326. SLV0_ADD register description

slave0_add[6:0]	I²C slave address of sensor 1 that can be read by the sensor hub. Default value: 0000000
rw_0	Read/write operation on sensor 1. Default value: 0 (0: write operation; 1: read operation)

15.21 SLV0_SUBADD (16h)

Address of register on the first external sensor (sensor 1) register (R/W)

Table 327. SLV0_SUBADD register

slave0_ reg7	slave0_ reg6	slave0_ reg5	slave0_ reg4	slave0_ reg3	slave0_ reg2	slave0_ reg1	slave0_ reg0

Table 328. SLV0_SUBADD register description

slave0_reg[7:0]	Address of register on sensor1 that has to be read/written according to the rw_0 bit value in SLV0_ADD (15h). Default value: 00000000

15.22 SLV0_CONFIG (17h)

First external sensor (sensor 1) configuration and sensor hub settings register (R/W)

Table 329. SLV0_CONFIG register

SHUB_ ODR_1	SHUB_ ODR_0	0(1)	0(1)	0(1)	Slave0_ numop2	Slave0_ numop1	Slave0_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 330. SLV0_CONFIG register description

SHUB_ODR_[1:0]	Rate at which the master communicates. Default value: 00 (00: 104 Hz (or at the maximum ODR between the accelerometer and gyro if it is less than 104 Hz); 01: 52 Hz (or at the maximum ODR between the accelerometer and gyro if it is less than 52 Hz); 10: 26 Hz (or at the maximum ODR between the accelerometer and gyro if it is less than 26 Hz); 11: 12.5 Hz (or at the maximum ODR between the accelerometer and gyro if it is less than 12.5 Hz)
Slave0_numop[2:0]	Number of read operations on sensor 1. Default value: 000

15.23 SLV1_ADD (18h)

I²C slave address of the second external sensor (sensor 2) register (R/W)

Table 331. SLV1_ADD register

Slave1_ add6	Slave1_ add5	Slave1_ add4	Slave1_ add3	Slave1_ add2	Slave1_ add1	Slave1_ add0	r_1

Table 332. SLV1_ADD register description

Slave1_add[6:0]	I²C slave address of sensor 2 that can be read by the sensor hub. Default value: 0000000
r_1	Enables read operation on sensor 2. Default value: 0 (0: read operation disabled; 1: read operation enabled)

15.24 SLV1_SUBADD (19h)

Address of register on the second external sensor (sensor 2) register (R/W)

Table 333. SLV1_SUBADD register

Slave1_ reg7	Slave1_ reg6	Slave1_ reg5	Slave1_ reg4	Slave1_ reg3	Slave1_ reg2	Slave1_ reg1	Slave1_ reg0

Table 334. SLV1_SUBADD register description

Slave1_reg[7:0]	Address of register on sensor 2 that has to be read/written according to the r_1 bit value in SLV1_ADD (18h).

15.25 SLV1_CONFIG (1Ah)

Second external sensor (sensor 2) configuration register (R/W)

Table 335. SLV1_CONFIG register

0(1)	0(1)	0(1)	0(1)	0(1)	Slave1_ numop2	Slave1_ numop1	Slave1_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 336. SLV1_CONFIG register description

Slave1_numop[2:0]	Number of read operations on sensor 2. Default value: 000

15.26 SLV2_ADD (1Bh)

I²C slave address of the third external sensor (sensor 3) register (R/W)

Table 337. SLV2_ADD register

Slave2_ add6	Slave2_ add5	Slave2_ add4	Slave2_ add3	Slave2_ add2	Slave2_ add1	Slave2_ add0	r_2

Table 338. SLV2_ADD register description

Slave2_add[6:0]	I²C slave address of sensor 3 that can be read by the sensor hub.
r_2	Enables read operation on sensor 3. Default value: 0 (0: read operation disabled; 1: read operation enabled)

15.27 SLV2_SUBADD (1Ch)

Address of register on the third external sensor (sensor 3) register (R/W)

Table 339. SLV2_SUBADD register

Slave2_ reg7	Slave2_ reg6	Slave2_ reg5	Slave2_ reg4	Slave2_ reg3	Slave2_ reg2	Slave2_ reg1	Slave2_ reg0

Table 340. SLV2_SUBADD register description

Slave2_reg[7:0]	Address of register on sensor 3 that has to be read/written according to the r_2 bit value in SLV2_ADD (1Bh).

15.28 SLV2_CONFIG (1Dh)

Third external sensor (sensor 3) configuration register (R/W)

Table 341. SLV2_CONFIG register

0(1)	0(1)	0(1)	0(1)	0(1)	Slave2_ numop2	Slave2_ numop1	Slave2_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 342. SLV2_CONFIG register description

Slave2_numop[2:0]	Number of read operations on sensor 3. Default value: 000

15.29 SLV3_ADD (1Eh)

I²C slave address of the fourth external sensor (sensor 4) register (R/W)

Table 343. SLV3_ADD register

Slave3_ add6	Slave3_ add5	Slave3_ add4	Slave3_ add3	Slave3_ add2	Slave3_ add1	Slave3_ add0	r_3

Table 344. SLV3_ADD register description

Slave3_add[6:0]	I²C slave address of sensor 4 that can be read by the sensor hub.
r_3	Enables read operation on sensor 4. Default value: 0 (0: read operation disabled; 1: read operation enabled)

15.30 SLV3_SUBADD (1Fh)

Address of register on the fourth external sensor (sensor 4) register (R/W)

Table 345. SLV3_SUBADD register

Slave3_ reg7	Slave3_ reg6	Slave3_ reg5	Slave3_ reg4	Slave3_ reg3	Slave3_ reg2	Slave3_ reg1	Slave3_ reg0

Table 346. SLV3_SUBADD register description

Slave3_reg[7:0]	Address of register on sensor 4 that has to be read according to the r_3 bit value in SLV3_ADD (1Eh).

15.31 SLV3_CONFIG (20h)

Fourth external sensor (sensor 4) configuration register (R/W)

Table 347. SLV3_CONFIG register

0(1)	0(1)	0(1)	0(1)	0(1)	Slave3_ numop2	Slave3_ numop1	Slave3_ numop0

1. *This bit must be set to 0 for the correct operation of the device.*

Table 348. SLV3_CONFIG register description

Slave3_numop[2:0]	Number of read operations on sensor 4. Default value: 000

15.32 DATAWRITE_SLV0 (21h)

Data to be written into the slave device register (R/W)

Table 349. DATAWRITE_SLV0 register

Slave0_ dataw7	Slave0_ dataw6	Slave0_ dataw5	Slave0_ dataw4	Slave0_ dataw3	Slave0_ dataw2	Slave0_ dataw1	Slave0_ dataw0

Table 350. DATAWRITE_SLV0 register description

Slave0_dataw[7:0]	Data to be written into the slave 0 device according to the rw_0 bit in register SLV0_ADD (15h). Default value: 00000000

15.33 STATUS_MASTER (22h)

Sensor hub source register (R)

Table 351. STATUS_MASTER register

WR_ONCE _DONE	SLAVE3_ NACK	SLAVE2_ NACK	SLAVE1_ NACK	SLAVE0_ NACK	0	0	SENS_HUB _ENDOP

Table 352. STATUS_MASTER register description

WR_ONCE_DONE	When the bit WRITE_ONCE in MASTER_CONFIG (14h) is configured as 1, this bit is set to 1 when the write operation on slave 0 has been performed and completed. Default value: 0
SLAVE3_NACK	This bit is set to 1 if Not acknowledge occurs on slave 3 communication. Default value: 0
SLAVE2_NACK	This bit is set to 1 if Not acknowledge occurs on slave 2 communication. Default value: 0
SLAVE1_NACK	This bit is set to 1 if Not acknowledge occurs on slave 1 communication. Default value: 0
SLAVE0_NACK	This bit is set to 1 if Not acknowledge occurs on slave 0 communication. Default value: 0
SENS_HUB_ENDOP	Sensor hub communication status. Default value: 0 (0: sensor hub communication not concluded; 1: sensor hub communication concluded)

16 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

16.1 Soldering information

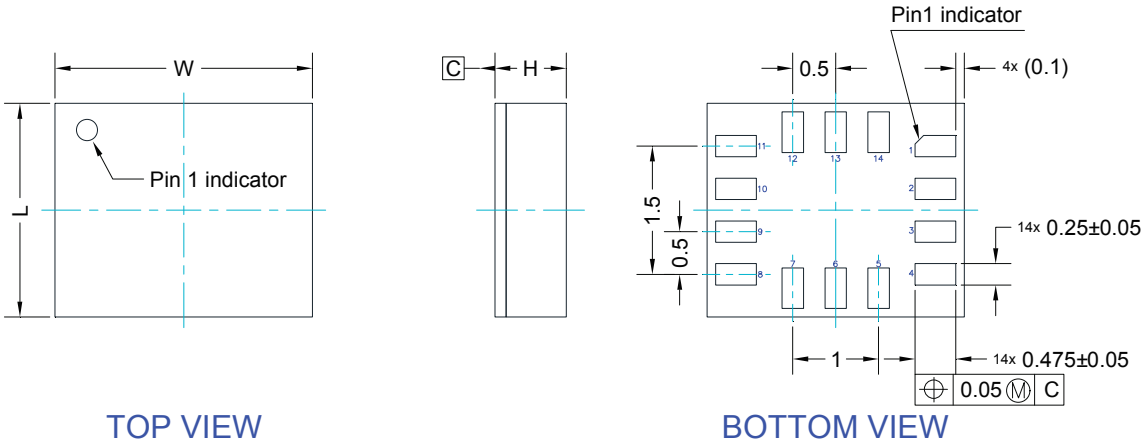
The LGA package is compliant with the ECOPACK and RoHS standard.

It is qualified for soldering heat resistance according to JEDEC J-STD-020.

For land pattern and soldering recommendations, consult technical note TN0018 available on www.st.com.

16.2 LGA-14L package information

Figure 17. LGA-14L 2.5 x 3.0 x 0.86 mm package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

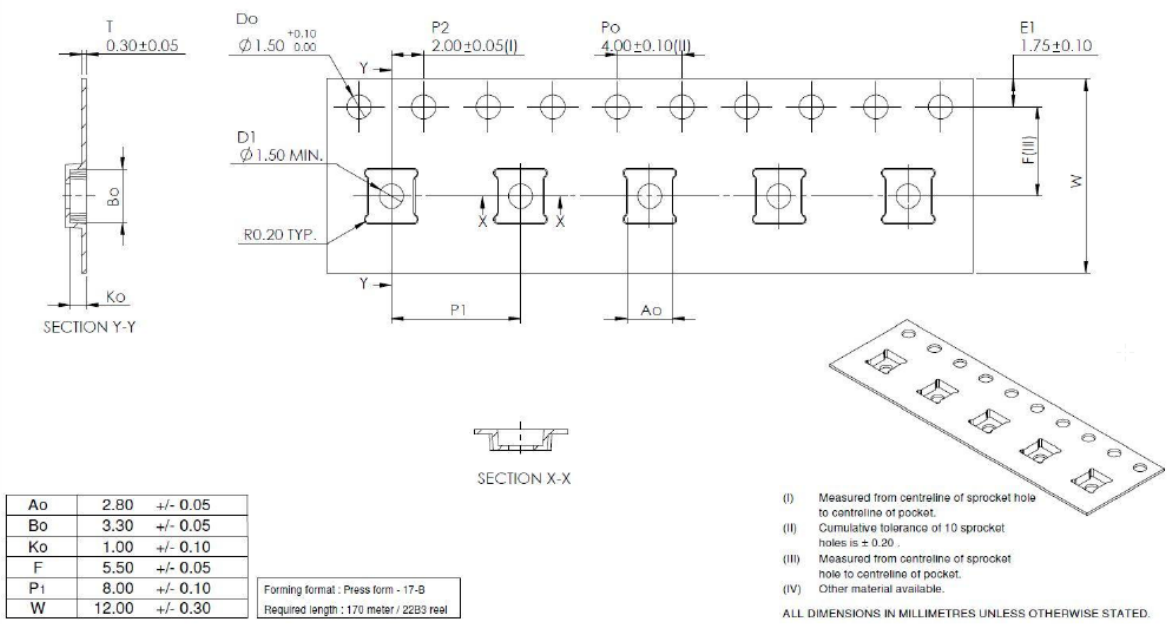
OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.1
Width [W]	3.00	±0.1
Height [H]	0.86	MAX

DM00249496_5

16.3 LGA-14 packing information

Figure 18. **Carrier tape information for LGA-14 package**



Ao	2.80	+/- 0.05
Bo	3.30	+/- 0.05
Ko	1.00	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press form - 17-B
Required length : 170 meter / 22B3 reel

Figure 19. **LGA-14 package orientation in carrier tape**

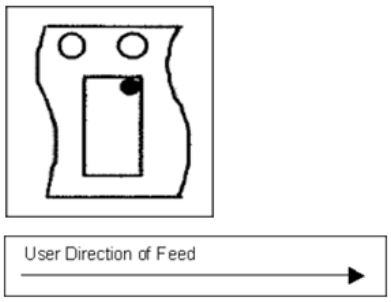


Figure 20. **Reel information for carrier tape of LGA-14 package**

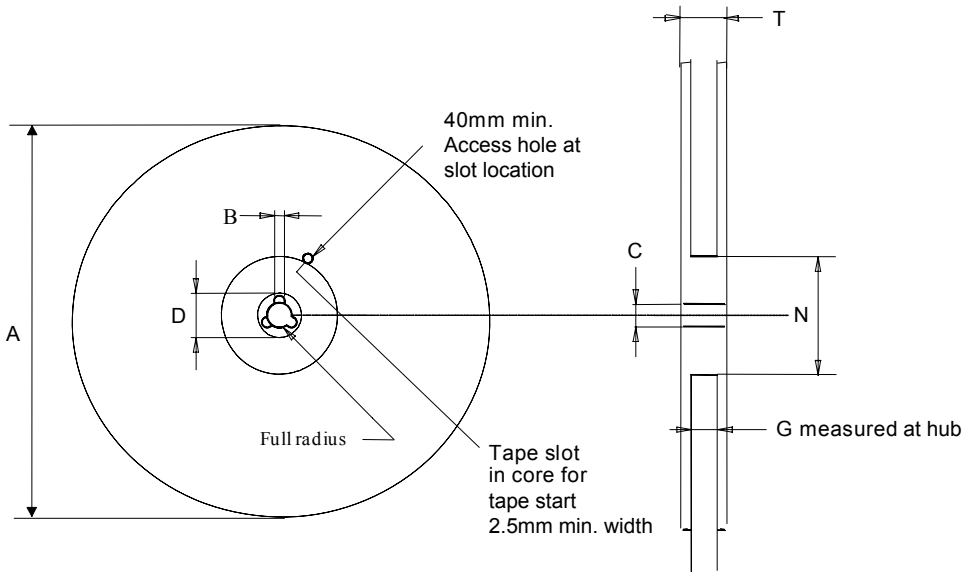


Table 353. **Reel dimensions for carrier tape of LGA-14 package**

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

Revision history

Table 354. **Document revision history**

Date	Version	Changes
22-Dec-2021	1	Initial release
01-Jun-2022	2	First public release

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