TAS6422E-Q1 75-W, 2-MHz Digital Input 2-Channel Automotive Class-D Audio Amplifier with Load Dump Protection and I²C Diagnostics

Texas Instruments
Burr-Brown Audio

1 Features

- AEC-Q100 Qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C T_A
- Advanced load diagnostics
  - DC Diagnostics run without input clocks
  - AC Diagnostic for tweeter detection with impedance and phase response
- Easily meets CISPR25-L5 EMC specifications
- Audio inputs
  - 2 Channel I²S or 4/8-channel TDM input
  - Input sample rates: 44.1 kHz, 48 kHz, 96 kHz
  - Input formats: 16-bit to 32-bit I²S, and TDM
- Audio Outputs
  - Two-channel bridge-tied load (BTL)
  - Single-channel parallel BTL (PBTL)
  - Up to 2.1 MHz output switching frequency
  - 45 W, 10% THD+N Into 2 Ω at 14.4 V BTL
  - 75 W, 10% THD+N Into 4 Ω at 25 V BTL
  - 150W, 10% THD+N Into 2 Ω at 25V PBTL
- Audio performance into 4 Ω at 14.4 V BTL
  - THD+N < 0.02% at 1 W
  - 42 μV_{RMS} output noise
  - –90 dB crosstalk
- Load diagnostics
  - Output open and shorted load
  - Output-to-battery or ground shorts
  - Line output detection up to 6 kΩ
  - Host-independent operation
- Protection
  - Output current limiting and short protection
  - 40 V Load dump
  - Open ground and power tolerant
  - DC offset
  - Over-temperature
  - Undervoltage and overvoltage
- General Operation
  - 4.5 V to 18 V supply voltage
  - I²C Control with 4 address options
  - Latched & Non-Latched Clip Detect
  - Enhanced EMI Management

2 Applications

- Automotive head unit
- Automotive external amplifier

3 Description

The TAS6422E-Q1 device is a two-channel digital-input Class-D audio amplifier that implements a 2.1 MHz PWM switching frequency enabling a cost-optimized solution in a very small PCB size, full operation down to 4.5 V for start/stop events, and exceptional sound quality with up to 40 kHz audio bandwidth.

The devices adds EMI management features including spread-spectrum to assist in system level EMI challenges.

The output switching frequency can be set either above the AM band, which eliminates AM-band interferences and reduces output filtering and cost, or below the AM band to optimize efficiency.

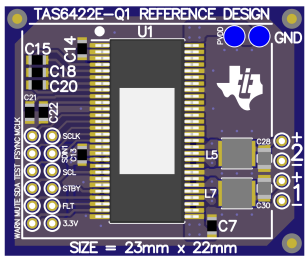
The device has a built-in load diagnostic function for detecting and diagnosing misconnected outputs as well as detection of AC-coupled tweeters to help to reduce test time during the manufacturing process.

The TAS6422E-Q1 Class-D audio amplifier is designed for use in automotive head units and external amplifier modules. For pin compatible one, two and four-channel devices see the the Device Options table.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TAS6422E-Q1	HSSOP (56)	18.41 mm × 7.49 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



PCB AREA

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2020) to Revision A (December 2020)	Page
• Changed the data sheet From: *Advanced Information* To: *Production* data	1

5 Device Options

Part Number	Channel Count	Power-Supply Voltage Range	Channel Current Limit (Typ)	Non-Latching Clip Detect WARN Pin(1)	Output Power per channel / 10% THD			
					4 Ω / BTL 14.4 V	4 Ω / BTL Max Voltage	2 Ω / BTL 14.4 V	2 Ω / PBTL Max Voltage
TAS6424-Q1	4	4.5 V to 26.4 V	6.5 A	N	27 W	75 W at 25 V	45 W	150 W at 25 V
TAS6424M-Q1	4	4.5 V to 18 V	6.5 A	N	27 W	45 W at 18 V	45 W	80 W at 18 V
TAS6424L-Q1	4	4.5 V to 18 V	4.8 A	N	27 W	45 W at 18 V	27 W	80 W at 18 V
TAS6422-Q1	2	4.5 V to 26.4 V	6.5 A	N	27 W	75 W at 25 V	45 W	150 W at 25 V
TAS6421-Q1	1	4.5 V to 26.4 V	6.5 A	Y	27 W	75 W at 25 V	45 W	N/A
TAS6424LS-Q1	4	4.5 V to 18 V	4.8 A	Y	27 W	75 W at 25 V	27 W	80 W at 18 V
TAS6424MS-Q1	4	4.5 V to 18 V	6.5 A	Y	27 W	45 W at 18 V	45 W	80 W at 18 V
TAS6422E-Q1	2	4.5 V to 26.4 V	6.5 A	Y	27 W	75 W at 25 V	45 W	150 W at 25 V

(1) Register configurable function. N = Latched clip detect only. Y = Supports both latched and non-latched clip detect .

6 Pin Configuration and Functions

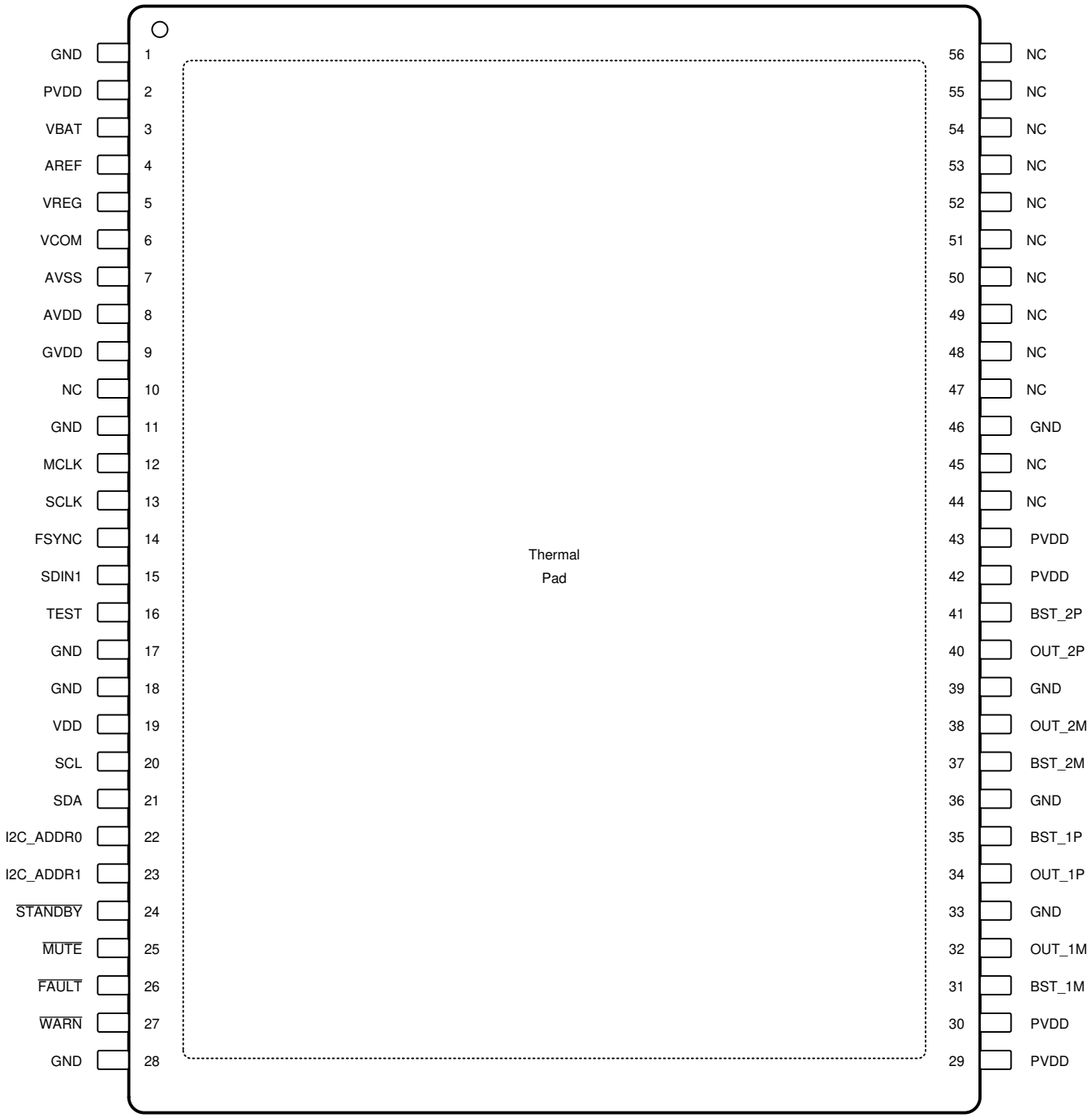


Figure 6-1. DKQ Package, 56-Pin HSSOP With Exposed Thermal Pad, Top View

Table 6-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
AREF	4	PWR	VREG and VCOM bypass capacitor return
AVDD	8	PWR	Voltage regulator bypass. Connect 1 µF capacitor from AVDD to AVSS
AVSS	7	PWR	AVDD bypass capacitor return
BST_1M	31	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_1P	35	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2M	37	PWR	Bootstrap capacitor connection pins for high-side gate driver
BST_2P	41	PWR	Bootstrap capacitor connection pins for high-side gate driver
$\overline{\text{FAULT}}$	26	DO	Reports a fault (active low, open drain), 100 kΩ internal pull-up resistor
FSYNC	14	DI	Audio frame clock input
GND	1, 11, 17, 18, 28, 33, 36, 39, 46	GND	Ground
GVDD	9	PWR	Gate drive voltage regulator derived from VBAT input pin. Connect 2.2 µF capacitor to GND
I2C_ADDR0	22	DI	I^2C address pins. Refer to I^2C Addresses
I2C_ADDR1	23		
MCLK	12	DI	Audio master clock input
$\overline{\text{MUTE}}$	25	DI	Mutes the device outputs (active low) while keeping output FETs switching at 50%, 100 kΩ internal pull-down resistor
NC	10, 44, 45, 47, 48, 49, 50, 51, 52, 53, 54, 55, 56	NC	Not connected or pulled to ground
OUT_1M	32	NO	Negative output for the channel
OUT_1P	34	PO	Positive output for the channel
OUT_2M	38	NO	Negative output for the channel
OUT_2P	40	PO	Positive output for the channel
PVDD	2, 29, 30, 42, 43	PWR	PVDD voltage input (can be connected to battery). Bulk capacitor and bypass capacitor required
SCL	20	DI	I^2C clock input
SCLK	13	DI	Audio bit and serial clock input
SDA	21	DI/O	I^2C data input and output
SDIN1	15	DI	TDM data input and audio I^2S data input for channels 1 and 2
$\overline{\text{STANDBY}}$	24	DI	Enables low power standby state (active Low), 100 kΩ internal pull-down resistor
TEST	16	DI	Internal test pin, connect to GND
VBAT	3	PWR	Battery voltage input
VCOM	6	PWR	Bias voltage
VDD	19	PWR	3.3-V external supply voltage
VREG	5	PWR	Voltage regulator bypass
$\overline{\text{WARN}}$	27	DO	Reports a warning (active low, open drain), 100-kΩ internal pull-up resistor
Thermal Pad	—	GND	Provides both electrical and thermal connection for the device. Heatsink must be connected to GND.

(1) GND = ground, PWR = power, PO = positive output, NO = negative output, DI = digital input, DO = digital output, DI/O = digital input and output, NC = no connection

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
PVDD, VBAT	DC supply voltage relative to GND		-0.3	30	V
VMAX	Transient supply voltage: PVDD, VBAT	t ≤ 400 ms exposure	-1	40	V
VRAMP	Supply-voltage ramp rate: PVDD, VBAT			75	V/ms
VDD	DC supply voltage relative to GND		-0.3	3.5	V
IMAX	Maximum current per pin (PVDD, VBAT, OUT_xP, OUT_xM, GND)			±8	A
IMAX_PULSED	Pulsed supply current per PVDD pin (one shot)	t < 100 ms		±12	A
VLOGIC	Input voltage for logic pins (SCL, SDA, SDIN1, SDIN2, MCLK, BCLK, LRCLK, MUTE,/STANDBY, I2C_ADDRx)		-0.3	VDD + 0.5	A
VGND	Maximum voltage between GND pins		-0.3	0.3	V
T_J	Maximum operating junction temperature		-55	150	°C
T_{stg}	Storage temperature		-55	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±3000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 22, 23 and 44)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordancewith the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
PVDD	Output FET Supply Voltage Range	Relative to GND, Speaker load impedance ≥ 4 Ohm BTL / ≥ 2 Ohm PBTL	4.5		26.4	V
PVDD	Output FET Supply Voltage Range	Relative to GND, Speaker load impedance < 4 Ohm BTL / < 2 Ohm PBTL	4.5		20	V
VBAT	Battery Supply Voltage Input	Relative to GND	4.5	14.4	18	
VDD	DC Logic supply	Relative to GND	3.0	3.3	3.5	
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature	An adequate thermal design is required	–40		150	
R_L	Minimum speaker load impedance	BTL Mode	2	4		Ω
		PBTL Mode	1	2		
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
C_{Bypass}	External capacitance on bypass pins	Pin 2, 3, 5, 6, 8, 19		1		µF
C_{GVDD}	External capacitance on GVDD pins	Pin 9		2.2		µF

			MIN	TYP	MAX	UNIT
C_{OUT}	External capacitance to GND on OUT pins	Limit set by DC-diagnostic timing		1	3.3	µF
L_O	Output filter inductance	Minimum inductance at I_{SD} current levels	1			µH

7.4 Thermal Information

THERMAL METRIC(1)		TAS6422E-Q1(2)
		DKQ(HSSOP)
		56 PINS
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.6
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.8
$R_{\theta JB}$	Junction-to-board thermal resistance	18.1
Ψ_{JT}	Junction-to-top characterization parameter	0.3
Ψ_{JB}	Junction-to-board characterization parameter	18.1
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
(2) JEDEC Standard 4 Layer PCB

7.5 Electrical Characteristics

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_{Load} = 4 Ω, Pout = 1 W/ch, f = 1kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I^2C settings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All channels playing, no audio input		36	45	mA
I_{VBAT_IDLE}	VBAT idle current	All channels playing, no audio input		56	62	mA
I_{PVDD_STBY}	PVDD standby current	$\overline{STANDBY}$ Active, VDD = 0 V		1	2	µA
I_{VBAT_STBY}	VBAT standby current	$\overline{STANDBY}$ Active, VDD = 0 V		4	6	µA
I_{VDD}	VDD supply current	All channels playing, –60-dB signal		15	18	mA
OUTPUT POWER						
P_{O_BTL}	Output power per channel, BTL	4 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	20	22		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	25	27		
		2 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	34	40		
		2 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	42	45		
		4 Ω, PVDD = 25 V, THD+N = 1%, T_C = 75°C	50	55		
		4 Ω, PVDD = 25 V, THD+N = 10%, T_C = 75°C	70	75		

7.5 Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_{Load} = 4 Ω, Pout = 1 W/ch, f = 1kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I^2C settings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_{O_PBTL}	Output power per channel in parallel mode, PBTL	2 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	35	40		W
		2 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	45	50		
		1 Ω, PVDD = 14.4 V, THD+N = 1%, T_C = 75°C	66	80		
		1 Ω, PVDD = 14.4 V, THD+N = 10%, T_C = 75°C	80	90		
		2 Ω, PVDD = 25 V, THD+N = 1%, T_C = 75°C	98	120		
		2 Ω, PVDD = 25 V, THD+N = 10%, T_C = 75°C	138	150		
EFF_P	Power efficiency	4 channels operating, 25 W output power/ch 4 Ω load, PVDD = 14.4 V, T_C = 25°C		0.86		
AUDIO PERFORMANCE						
V_n	Output noise voltage	Zero input, A-weighting, gain level 1, PVDD = 14.4 V		42		μV
		Zero input, A-weighting, gain level 2, PVDD = 14.4 V		55		
		Zero input, A-weighting, gain level 3, PVDD = 25 V		67		
		Zero input, A-weighting, gain level 4, PVDD = 25 V		85		
GAIN	Peak Output Voltage/dBFS	Gain level 1, Register 0x01, bit 1-0 = 00		7.5		V/FS
		Gain level 2, Register 0x01, bit 1-0 = 01		15		
		Gain level 3, Register 0x01, bit 1-0 = 10		21		
		Gain level 4, Register 0x01, bit 1-0 = 11		29		
Crosstalk	Channel crosstalk			-90		dB
PSRR	Power-supply rejection ratio	PVDD = 14.4 V_{dc} + 1 V_{RMS}, f = 1 kHz		75		dB
THD+N	Total harmonic distortion + noise			0.02		
G_{CH}	Channel-to-channel gain variation		-0.5	0	0.5	dB
LINE OUTPUT PERFROMANCE						
$V_{n\_LINEOUT}$	LINE output noise voltage	Zero input, A-weighting, channel set to LINE MODE		42		μV
$V_{O\_LINEOUT}$	LINE output voltage	0 dB input, channel set to LINE MODE		5.5		VRMS
THD+N	Line output total harmonic distortion + noise	V_O = 2 V_{RMS} , channel set to LINE MODE		0.01		
DIGITAL INPUT PINS						
V_{IH}	Input logic level high		70			%VDD
V_{IL}	Input logic level low				30	%VDD
I_{IH}	Input logic current, high	V_I = VDD			15	μA
I_{IL}	Input logic current, low	V_I = 0			-15	μA
PWM OUTPUT STAGE						

7.5 Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_{Load} = 4 Ω, Pout = 1 W/ch, f = 1kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I^2C settings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(on)}$	FET drain-to-source resistance	Not including bond wire and package resistance		90		mΩ
OVER VOLTAGE (OV) PROTECTIONI						
V_{PVDD_OV}	PVDD overvoltage shutdown		27.0	27.8	28.8	V
$V_{PVDD\_OV\_HYS}$	PVDD overvoltage shutdown hysteresis			0.8		V
V_{VBAT_OV}	VBAT overvoltage shutdown		20	21.5	23	V
$V_{VBAT\_OV\_HYS}$	VBAT overvoltage shutdown hysteresis			0.6		
UNDER VOLTAGE (UV) PROTECTIONI						
$VBAT_{UV}$	VBAT undervoltage shutdown			4	4.5	V
$VBAT_{UV\_HYS}$	VBAT undervoltage shutdown hysteresis			0.2		V
$PVDD_{UV}$	PVDD undervoltage shutdown			4	4.5	V
$PVDD_{UV\_HYS}$	PVDD undervoltage shutdown hysteresis			0.2		V
BYPASS VOLTAGES						
V_{GVDD}	Gate drive bypass pin voltage			7		V
V_{AVDD}	Analog bypass pin voltage			6		V
V_{VCOM}	Common bypass pin voltage			2.5		V
V_{VREG}	Regulator bypass pin voltage			5.5		V
POWER-ON RESET(POR)						
V_{POR}	VDD voltage for POR			2.1	2.7	V
V_{POR_HYS}	VDD POR recovery hysteresis voltage			0.5		V
OVER TEMPERATURE (OT) PROTECTION						
$OTW_{(i)}$	Channel overtemperature warning			150		°C
$OTSD_{(i)}$	Channel overtemperature shutdown			175		°C
OTW	Global junction overtemperature warning			130		°C
OTSD	Global junction overtemperature shutdown			160		°C
OT_{HYS}	Overtemperature hysteresis			15		°C
LOAD OVER CURRENT PROTECTION						
I_{LIM}	Overcurrent cycle-by-cycle limit	OC Level 1	4.0	4.8		A
		OC Level 2	6.0	6.5		A
I_{SD}	Overcurrent shutdown	OC Level 1, Any short to supply, ground, or other channels		7		A
		OC Level 2, Any short to supply, ground, or other channels		9		A
MUTE MODE						
G_{MUTE}	Output attenuation			100		dB
CLICK AND POP						
V_{CP}	Output click and pop voltage	ITU-R 2k filter, High-Z/MUTE to Play, Play to Mute/High-Z		7		mV
DC OFFSET						
V_{OFFSET}	Output offset voltage			2	5	mV
DC DETECT						

7.5 Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_{Load} = 4 Ω, Pout = 1 W/ch, f = 1kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I^2C settings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC_{FAULT}	Output DC fault protection			2	2.5	V
DIGITAL OUTPUT PINS						
V_{OH}	Output voltage for logic level high	I = ±2 mA	90			%VDD
V_{OL}	Output voltage for logic level low	I = ±2 mA			10	%VDD
$t_{DELAY\_CLIPDET}$	Signal delay when output clipping detected				20	µs
LOAD DIAGNOSTICS						
S2P	Maximum resistance to detect a short from OUT pin(s) to PVDD				500	Ω
S2G	Maximum resistance to detect a short from OUT pin(s) to ground				200	Ω
SL	Shorted load detection tolerance	Other channels in Hi-Z			±0.5	Ω
OL	Open load	Other channels in Hi-Z	40	70		Ω
t_{DC_DIAG}	DC diagnostic time	All 2 Channels		140		ms
LO	Line output				6	kΩ
t_{LINE_DIAG}	Line output diagnostic time			40		ms
AC_{IMP}	AC impedance accuracy	Offset			±0.5	Ω
		Gain linearity, f = 19 kHz, R_L = 2 Ω to 16 Ω			0.25	
t_{AC_DIAG}	AC diagnostic time	All 2 Channels		250		ms
I2C_ADDR PINS						
t_{I2C_ADDR}	Time delay needed for I2C address set-up			300		µs
I2C CONTROL PORT						
t_{BUS}	Bus free time between start and stop conditions		1.3			µs
t_{HOLD1}	Hold time, SCL to SDA		0			ns
t_{HOLD2}	Hold time, start condition to SCL		0.6			µs
t_{START}	I2C startup time after VDD power on reset				12	ms
t_{RISE}	Rise time, SCL and SDA				300	ns
t_{FALL}	Fall time, SCL and SDA				300	ns
t_{SU1}	Setup, SDA to SCL		100			ns
t_{SU2}	Setup, SCL to start condition		0.6			µs
t_{SU3}	Setup, SCL to stop condition		0.6			µs
$t_{W(H)}$	Required pulse duration SCL high		0.6			µs
$t_{W(L)}$	Required pulse duration SCL low		1.3			µs
SERIAL AUDIO PORT						
$MCLK_{DC}$, $SCLK_{DC}$	Allowable input clock duty cycle		0.45	0.5	0.55	
f_{MCLK}	Supported MCLK frequencies	128, 256, or 512	128		512	xFS
f_{MCLK_Max}	Maximum frequency				25	MHz
t_{SCY}	SCLK pulse cycle time		40			ns
t_{SCL}	SCLK pulse-with LOW		16			ns
t_{SCH}	SCLK pulse-with HIGH		16			ns
$t_{RISE/FALL}$	Rise and fall time			<5		ns

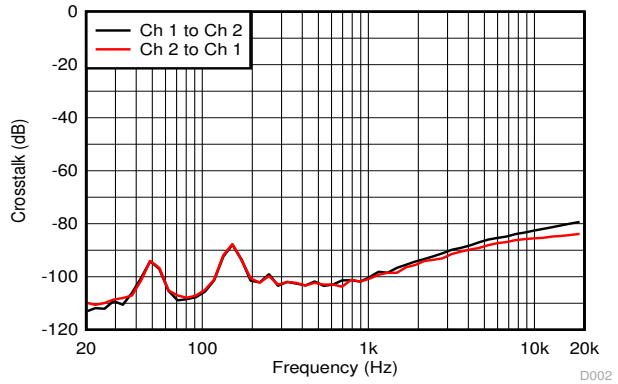
7.5 Electrical Characteristics (continued)

Test conditions (unless otherwise noted): T_C = 25°C, PVDD = VBAT = 14.4 V, VDD = 3.3 V, R_{Load} = 4 Ω, Pout = 1 W/ch, f = 1kHz, f_{SW} = 2.11 MHz, AES17 Filter, default I^2C settings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SF}	Required FSYNC to SCLK rising edge		8			ns
t_{FS}	FSYNC rising edge to SCLK edge		8			ns
t_{DS}	DATA set-up time		8			ns
t_{DH}	DATA hold time		8			ns
c_i	Input capacitance, pins MCLK, SCLK, FSYNC, SDIN1				10	pf
t_{LA}	Latency from input to output measured in FSYNC sample count	FSYNC = 44.1 kHz or 48 kHz			30	
		FSYNC = 96 kHz			12	

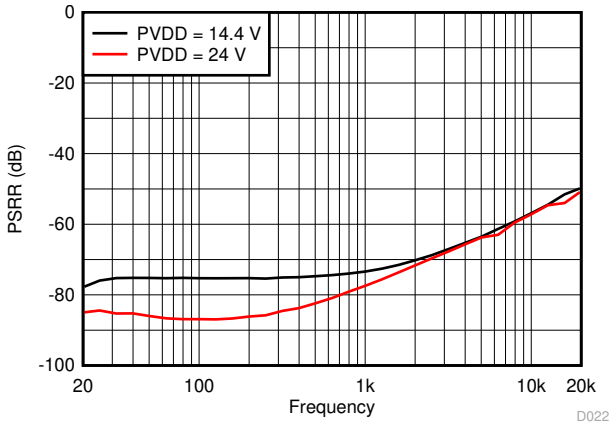
7.6 Typical Characteristics

T_A = 25 °C, VBAT = PVDD = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, f_s = 48 kHz, AES17 filter, default I^2C settings, see Figure 10-2 and Figure 10-3 (unless otherwise noted)



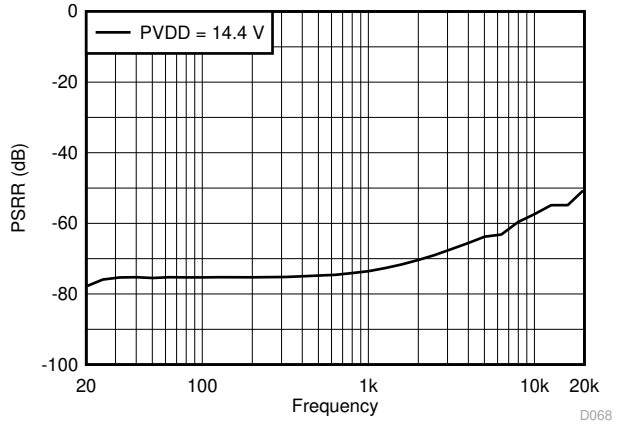
P_O = 1 W

Figure 7-1. Crosstalk vs Frequency



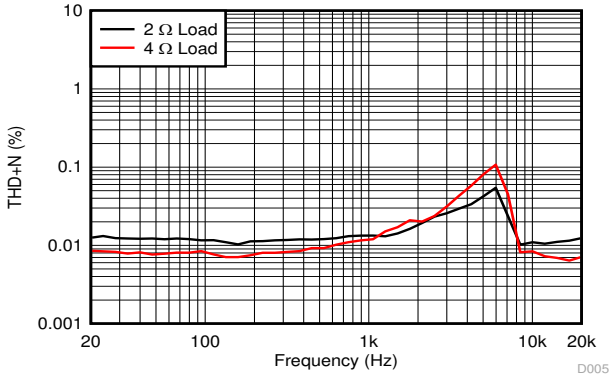
P_O = 1 W

Figure 7-2. PVDD PSRR vs Frequency



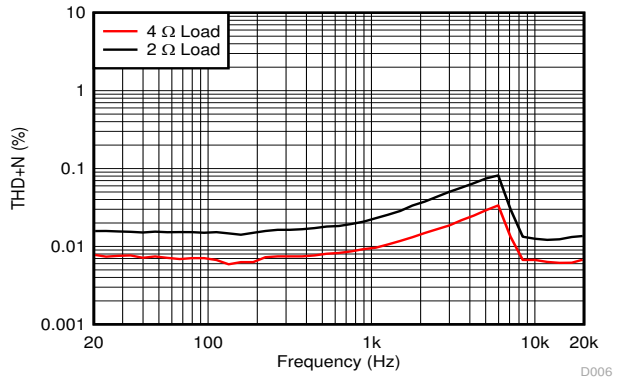
P_O = 1 W

Figure 7-3. VBAT + PVDD PSRR vs Frequency



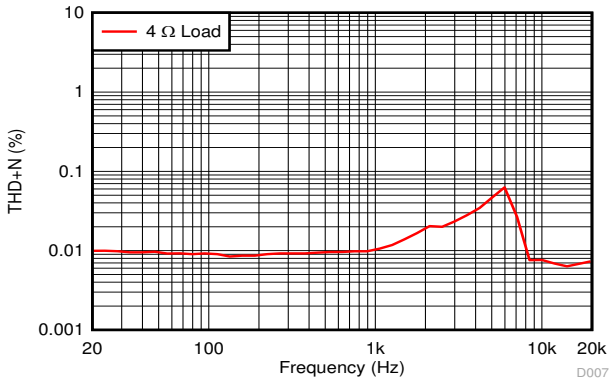
P_O = 1 W f_{SW} = 384 kHz

Figure 7-4. THD+N vs Frequency



P_O = 1 W f_{SW} = 2.1 MHz

Figure 7-5. THD+N vs Frequency

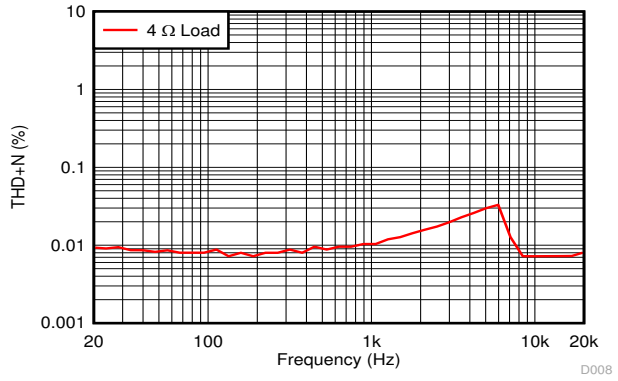


P_O = 1 W f_{SW} = 384 kHz PVDD = 24V

Figure 7-6. THD+N vs Frequency

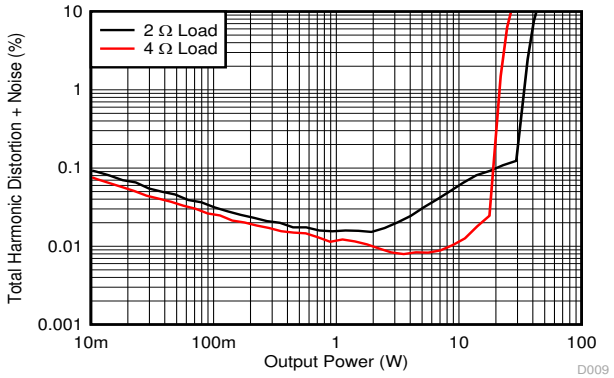
7.6 Typical Characteristics (continued)

T_A = 25 °C, VBAT = PVDD = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, f_s = 48 kHz, AES17 filter, default I^2C settings, see Figure 10-2 and Figure 10-3 (unless otherwise noted)



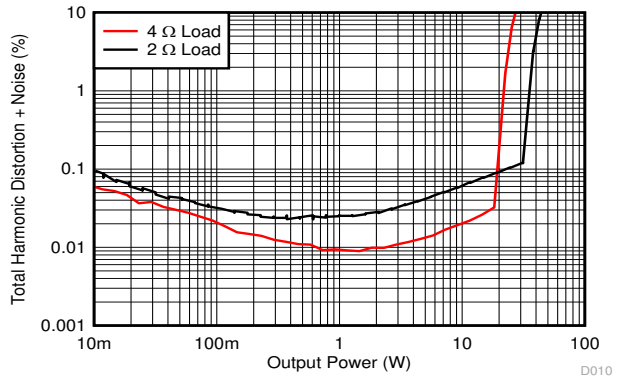
P_O = 1 W f_{SW} = 2.1 MHz PVDD = 24V

Figure 7-7. THD+N vs Frequency



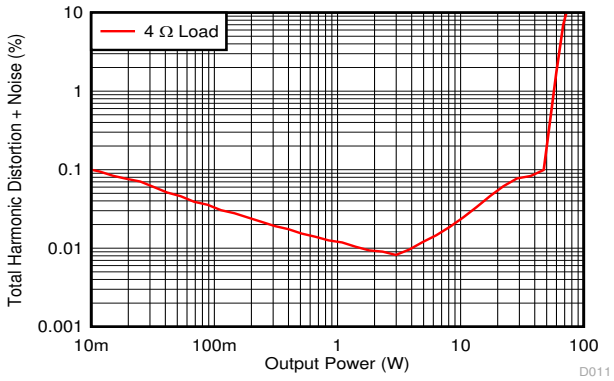
f_{SW} = 384 kHz

Figure 7-8. THD+N vs Power



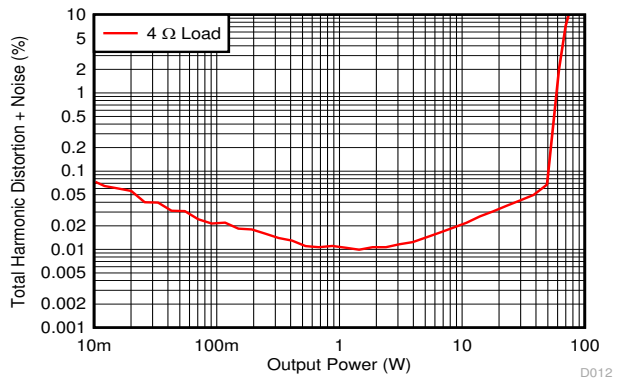
f_{SW} = 2.1 MHz

Figure 7-9. THD+N vs Power



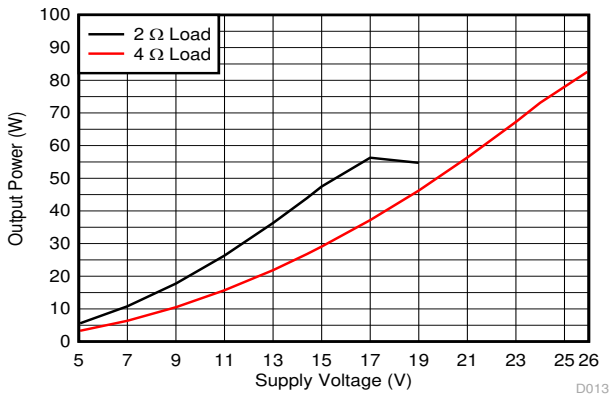
f_{SW} = 384 kHz PVDD = 24 V

Figure 7-10. THD+N vs Power



f_{SW} = 2.1 MHz PVDD = 24 V

Figure 7-11. THD+N vs Power

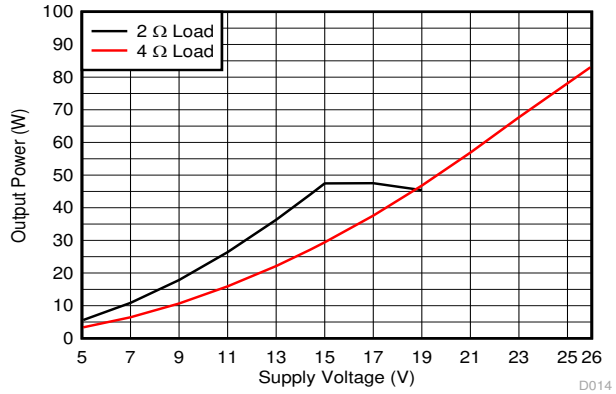


10% THD f_{SW} = 384 kHz

Figure 7-12. Output Power vs Supply Voltage

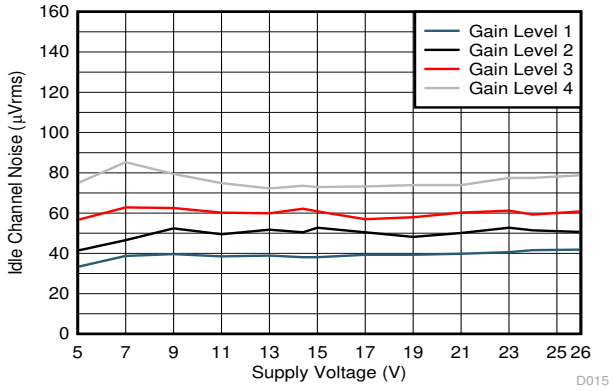
7.6 Typical Characteristics (continued)

T_A = 25 °C, VBAT = PVDD = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, f_s = 48 kHz, AES17 filter, default I^2C settings, see Figure 10-2 and Figure 10-3 (unless otherwise noted)



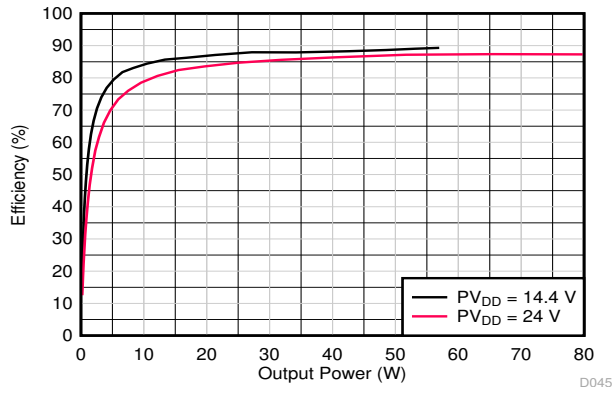
10% THD f_{SW} = 2.1 MHz

Figure 7-13. Output Power vs Supply Voltage



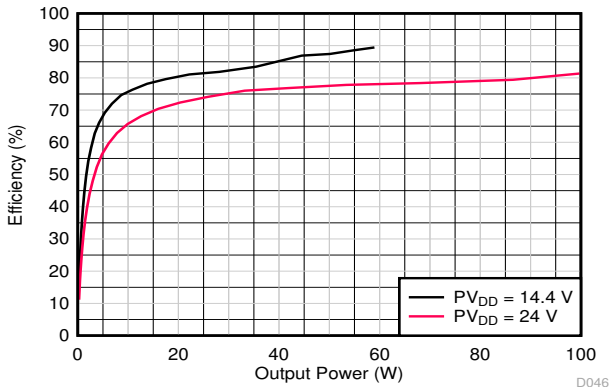
A-weighted Noise f_{SW} = 2.1 MHz

Figure 7-14. Noise vs Supply voltage



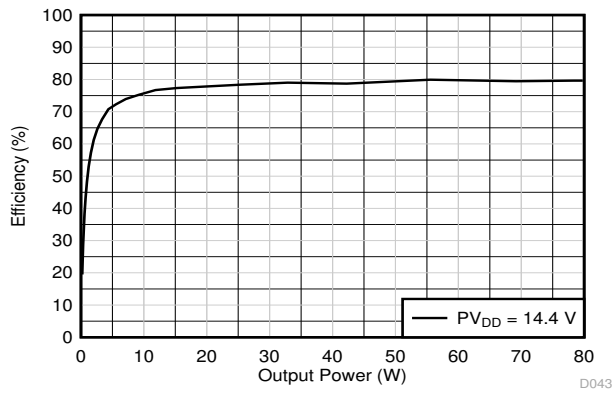
4 Ω f_{SW} = 384 kHz

Figure 7-15. Power Efficiency vs Total Output Power



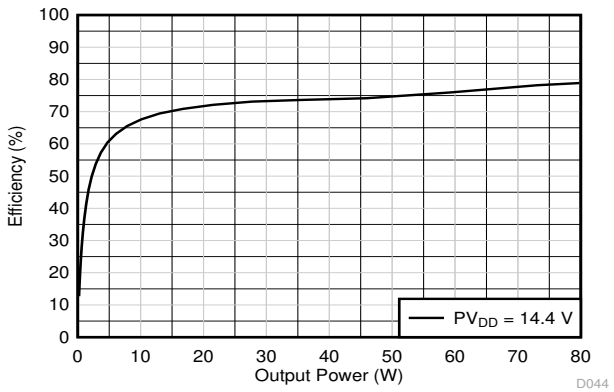
4 Ω f_{SW} = 2.1 MHz

Figure 7-16. Power Efficiency vs Total Output Power



2 Ω f_{SW} = 384 kHz

Figure 7-17. Power Efficiency vs Total Output Power



2 Ω f_{SW} = 2.1 MHz

Figure 7-18. Power Efficiency vs Total Output Power

7.6 Typical Characteristics (continued)

T_A = 25 °C, VBAT = PVDD = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, f_s = 48 kHz, AES17 filter, default I^2C settings, see Figure 10-2 and Figure 10-3 (unless otherwise noted)

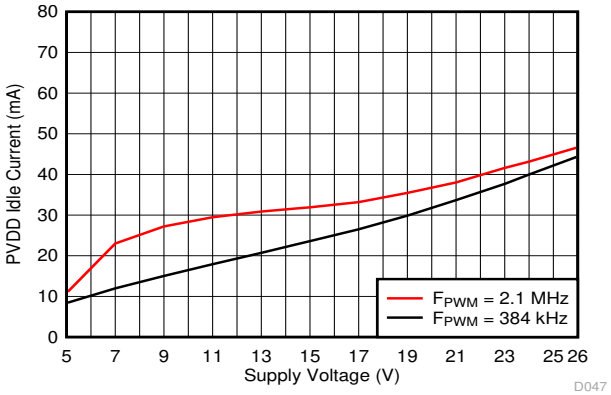


Figure 7-19. PVDD Idle Current vs Voltage

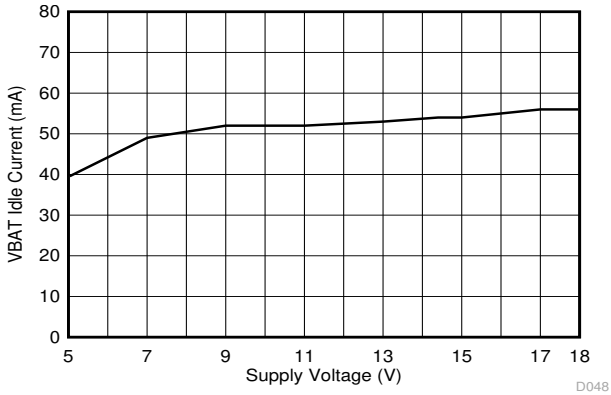


Figure 7-20. VBAT Idle Current vs Voltage

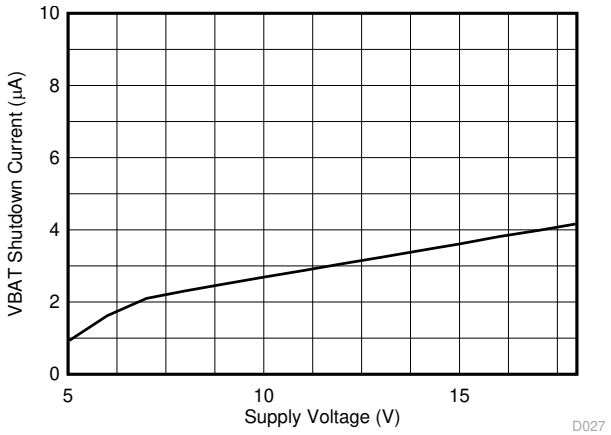
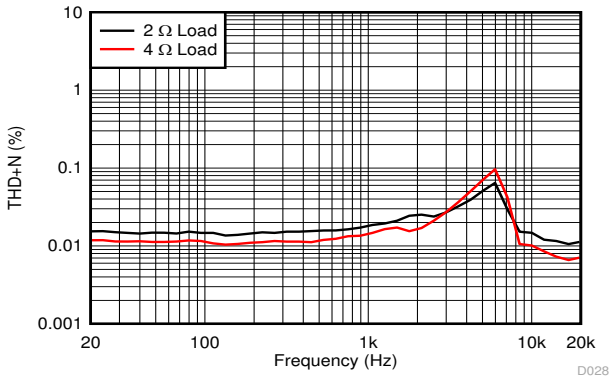
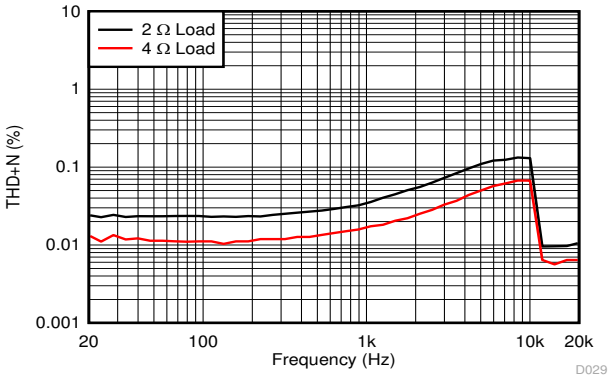


Figure 7-21. VBAT Standby Current vs Voltage



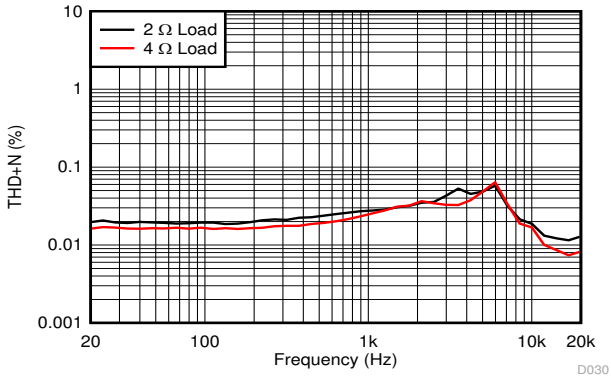
P_O = 1 W f_{SW} = 384 kHz

Figure 7-22. PBTL THD+N vs Frequency



P_O = 1 W f_{SW} = 2.1 MHz

Figure 7-23. PBTL THD+N vs Frequency

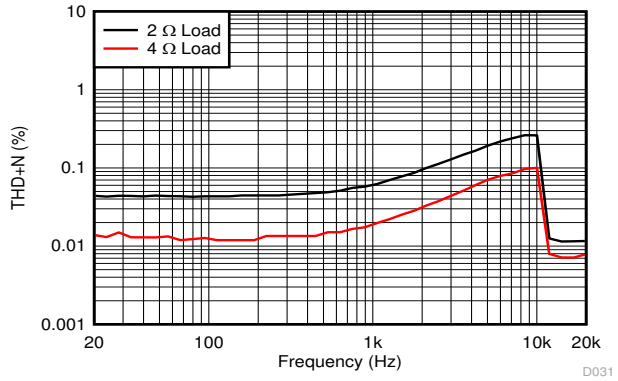


P_O = 1 W f_{SW} = 384 kHz PVDD = 24 V

Figure 7-24. PBTL THD+N vs Frequency

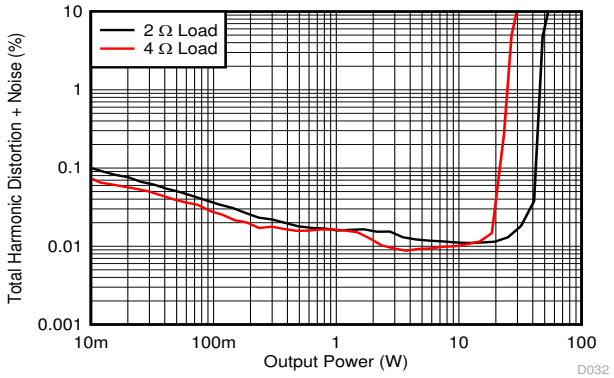
7.6 Typical Characteristics (continued)

T_A = 25 °C, VBAT = PVDD = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, f_s = 48 kHz, AES17 filter, default I^2C settings, see Figure 10-2 and Figure 10-3 (unless otherwise noted)



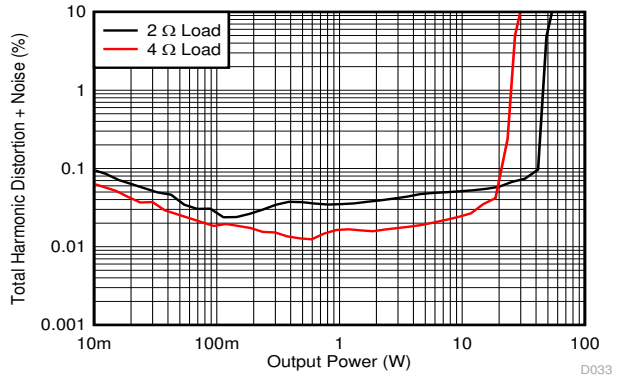
P_O = 1 W f_{SW} = 2.1 MHz PVDD = 24V

Figure 7-25. PBTL THD+N vs Frequency



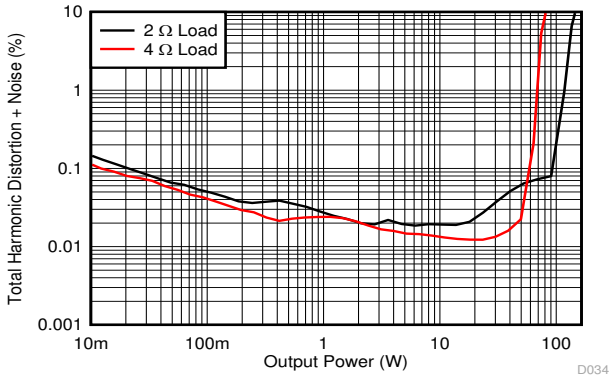
f_{SW} = 384 kHz

Figure 7-26. PBTL THD+N vs Power



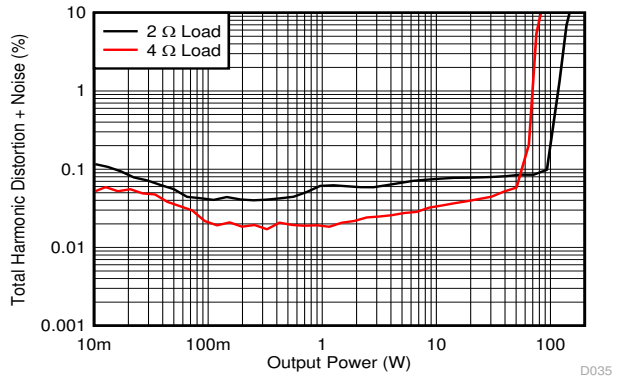
f_{SW} = 2.1 MHz

Figure 7-27. PBTL THD+N vs Power



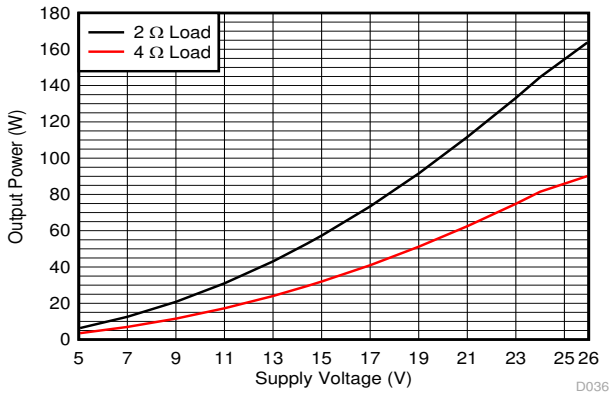
f_{SW} = 384 kHz PVDD = 24 V

Figure 7-28. PBTL THD+N vs Power



f_{SW} = 2.1 MHz PVDD = 24 V

Figure 7-29. PBTL THD+N vs Power

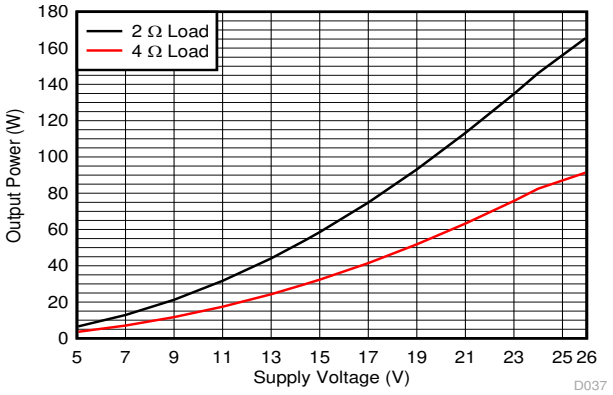


10 % THD f_{SW} = 384 kHz

Figure 7-30. PBTL Output Power vs Voltage

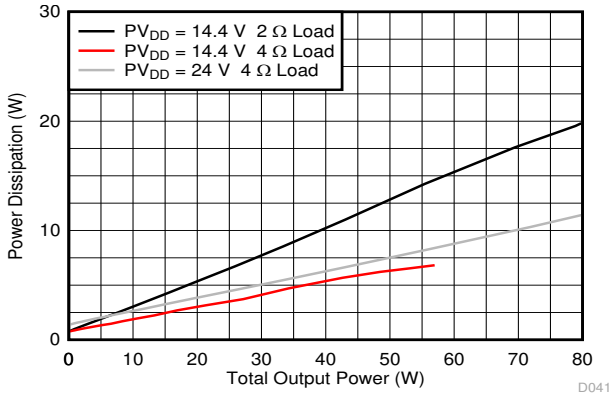
7.6 Typical Characteristics (continued)

T_A = 25 °C, VBAT = PVDD = 14.4 V, VDD = 3.3 V, R_L = 4 Ω, f_{IN} = 1 kHz, f_{SW} = 2.1 MHz, f_s = 48 kHz, AES17 filter, default I^2C settings, see Figure 10-2 and Figure 10-3 (unless otherwise noted)



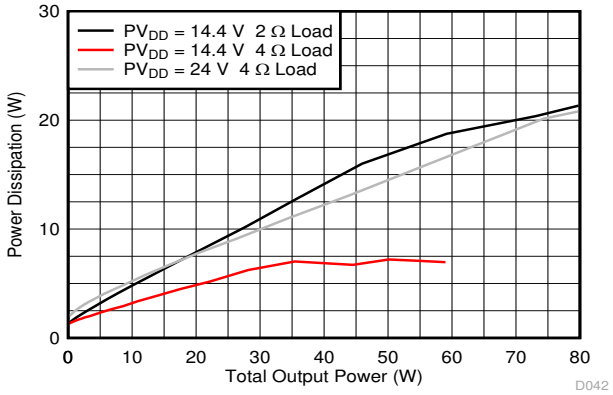
10 % THD f_{SW} = 2.1 MHz

Figure 7-31. PBTL Output Power vs Voltage



f_{SW} = 384 kHz

Figure 7-32. BTL Power Dissipation vs Total Output Power



f_{SW} = 2.1 MHz

Figure 7-33. BTL Power Dissipation vs Total Output Power

8 Parameter Measurement Information

The parameters for the TAS6422E-Q1 device were measured using the circuit in Figure 10-2.

For measurements with 2.1 MHz switching frequency the 3.3 µH inductor from the TAS6422E-Q1 EVM is used.

For measurements with 384 kHz switching frequency a 10 µH inductor was used.

9 Detailed Description

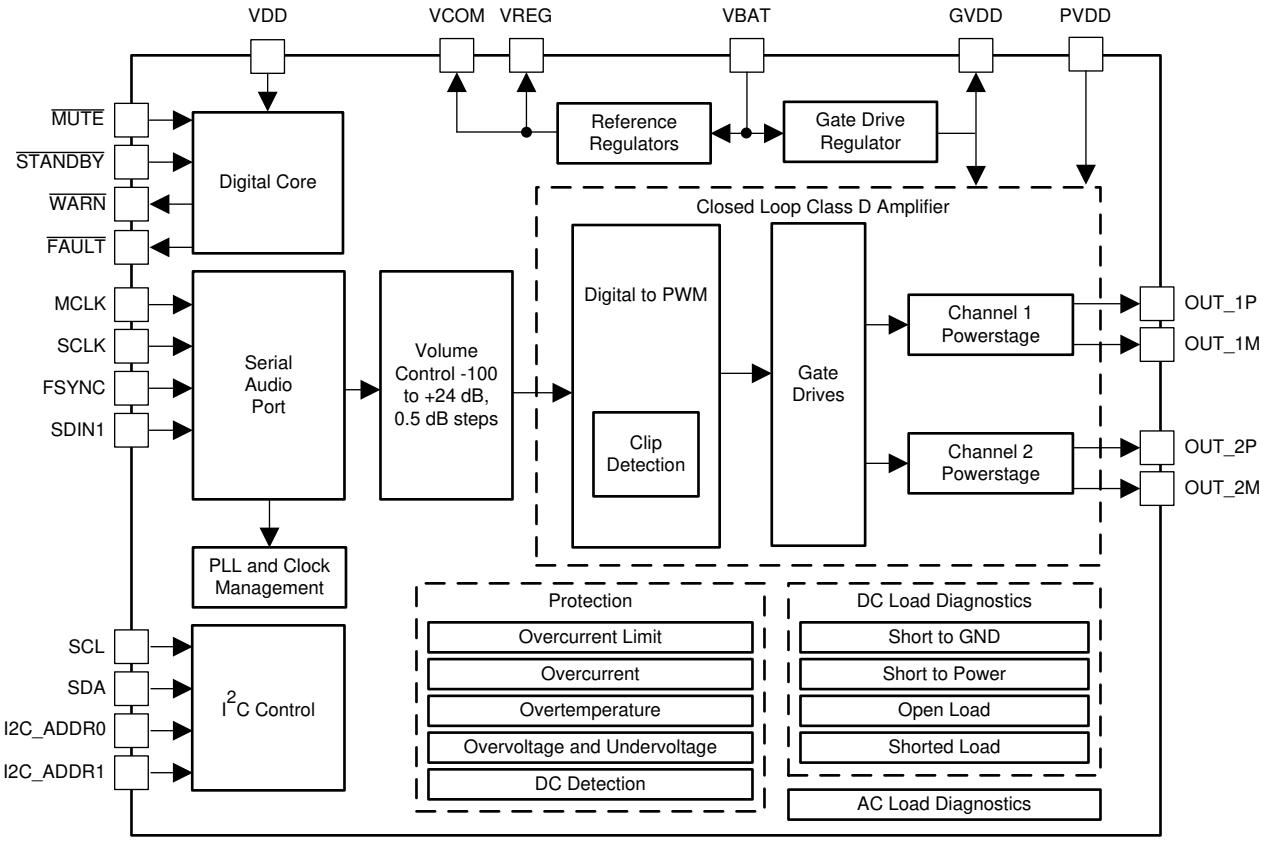
9.1 Overview

The TAS6422E-Q1 is a two-channel digital-input Class-D audio amplifier specifically tailored for use in the automotive industry. The device is designed for vehicle battery operation or boosted voltage systems. This ultra-efficient Class-D technology allows for reduced power consumption, reduced PCB area, and reduced heat. The device realizes an audio sound-system design with smaller size and lower weight than traditional Class-AB solutions.

The core design blocks are as follows:

- Serial audio port
- Clock management
- High-pass filter and volume control
- Pulse width modulator (PWM) with output stage feedback
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- I^2C serial communication bus

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Serial Audio Port

The serial audio port (SAP) receives audio in either I²S, left justified, right justified, or TDM formats.

Settings for the serial audio port are programmed in the *SAP Control Register (address = 0x03) [default = 0x04]*.

Figure 9-1 shows the digital audio data connections for I²S and TDM8 mode for a six channel system.

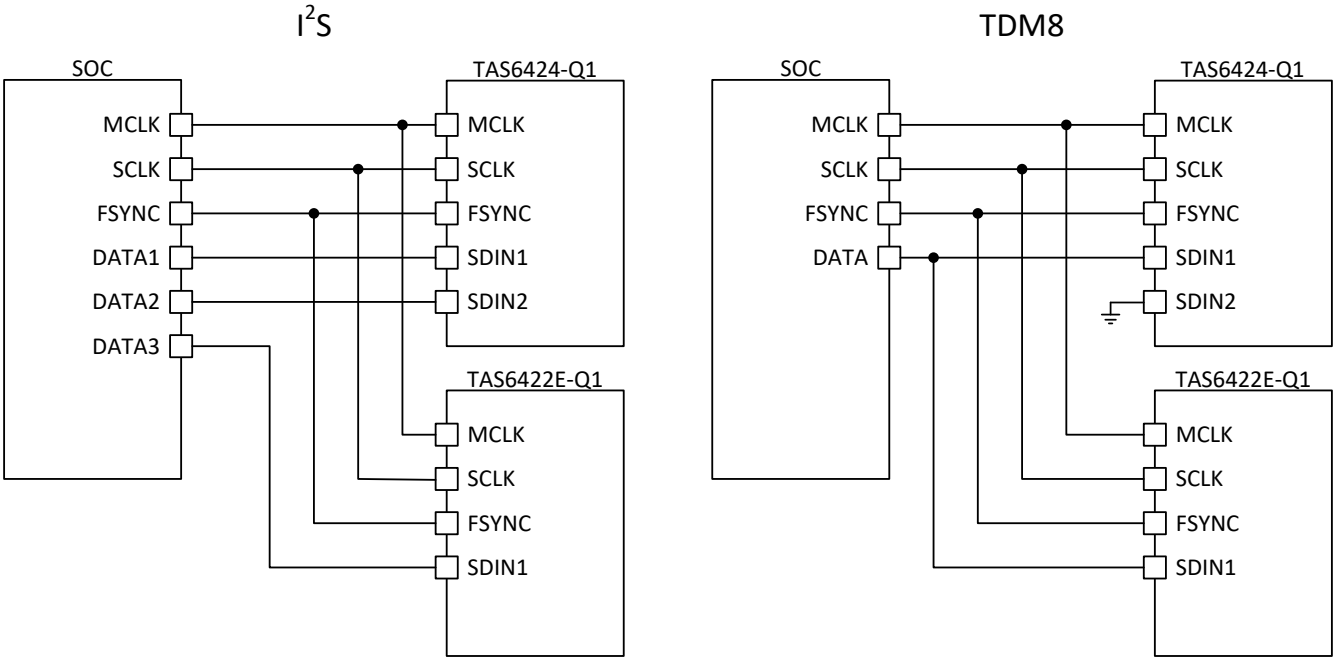


Figure 9-1. Digital-Audio Data Connection

9.3.1.1 I²S Mode

I²S timing uses the FSYNC pin to define when the data being transmitted is for the left channel and when the data is for the right channel. The FSYNC pin is low for the left channel and high for the right channel. The bit clock, SCLK, runs at 32 × f_S or 64 × f_S and is used to clock in the data. A delay of one bit clock occurs from the time the FSYNC signal changes state to the first bit of data on the data lines. The data is presented in 2s-complement form (MSB-first). The data is valid on the rising edge of the bit clock and is used to clock in the data.

9.3.1.2 Left-Justified Timing

Left-justified (LJ) timing also uses the FSYNC pin to define when the data being transmitted is for the left channel and when the data is for the right channel. The FSYNC pin is high for the left channel and low for the right channel. A bit clock running at 32 × f_S or 64 × f_S is used to clock in the data. The first bit of data appears on the data lines at the same time FSYNC toggles. The data is written MSB-first and is valid on the rising edge of the bit clock. Digital words can be 16-bits or 24-bits wide and pad any unused trailing data-bit positions in the left-right (L/R) frame with zeros.

9.3.1.3 Right-Justified Timing

Right-justified (RJ) timing also uses the FSYNC pin to define when the data being transmitted is for the left channel and when the data is for the right channel. The FSYNC pin is high for the left channel and low for the right channel. A bit clock running at 32 × f_S or 64 × f_S is used to clock in the data. The first bit of data appears on the data 8-bit clock periods (for 24-bit data) after the FSYNC pin toggles. In RJ mode the LSB of data is always clocked by the last bit clock before the FSYNC pin transitions. The data is written MSB-first and is valid on the rising edge of bit clock. The device pads the unused leading data-bit positions in the L/R frame with zeros.

9.3.1.4 TDM Mode

TDM mode supports 4 or 8 channels of audio data. The TDM mode is automatically selected when the TDM clocks are present. The device can be configured through I^2C to use different stereo pairs in the TDM data stream. The TDM mode supports 16-bit, 24-bit, and 32-bit input data lengths.

In TDM mode, SCLK must be 128 x f_s or 256 x f_s, depending on the TDM slot size. In TDM mode SCLK and MCLK can be connected together. If SCLK and MCLK are connected together or the frequency of SCLK and MCLK is equal, FSYNC should be minimum 2 MCLK pulses long.

In TDM mode, the SDIN1 pin (pin 15) is used for digital audio data. Table 9-1 lists register settings for the TDM channel selection.

Table 9-1. TDM Channel Selection

REGISTER SETTING		TDM8 CHANNEL SLOT							
0x03 BIT 5	0x03 BIT 3	1	2	3	4	5	6	7	8
0	0	CH1	CH2	—	—	—	—	—	—
1	0	—	—	—	—	CH1	CH2	—	—
0	1	—	—	CH1	CH2	—	—	—	—
1	1	—	—	—	—	—	—	CH1	CH2

If PBTL mode is programmed for channel 1/2 the datasource can be set according to TDM Channel Selection in PBTL Mode.

Table 9-2. TDM Channel Selection in PBTL Mode

REGISTER SETTING			TDM8 CHANNEL SLOT							
0x03 BIT 5	0x03 BIT 3	0x21 BIT 6	1	2	3	4	5	6	7	8
0	0	0	PBTL CH1/2	—	—	—	—	—	—	—
1	0	0	—	—	—	—	PBTL CH1/2	—	—	—
0	0	1	—	PBTL CH1/2	—	—	—	—	—	—
1	0	1	—	—	—	—	—	PBTL CH1/2	—	—
0	1	0	—	—	PBTL CH1/2	—	—	—	—	—
1	1	0	—	—	—	—	—	—	PBTL CH1/2	—
0	1	1	—	—	—	PBTL CH1/2	—	—	—	—
1	1	1	—	—	—	—	—	—	—	PBTL CH1/2

9.3.1.5 Supported Clock Rates

The device supports MCLK rates of 128 × f_S, 256 × f_S, or 512 × f_S.

The device supports SCLK rates of 32 × f_S or 64 × f_S in I^2S, LJ or RJ modes or 128 × f_S, or 256 × f_S in TDM mode.

The device supports FSYNC rates of 44.1 kHz, 48 kHz, or 96 kHz.

The maximum clock frequency is 25 MHz. Therefore, for a 96 kHz FSYNC rate, the maximum MCLK rate is 256 × f_S.

Duty cycle of 50% is required for 128x FSYNC, for 256x and 512x 50% duty cycle is not required.

9.3.1.6 Audio-Clock Error Handling

When any kind of clock error, MCLK-FSYNC or SCLK-FSYNC ratio, or clock halt is detected, the device puts all channels into the Hi-Z state. When all audio clocks are within the expected range, the device automatically returns to the state it was in. See the Electrical Characteristics table for timing requirements.

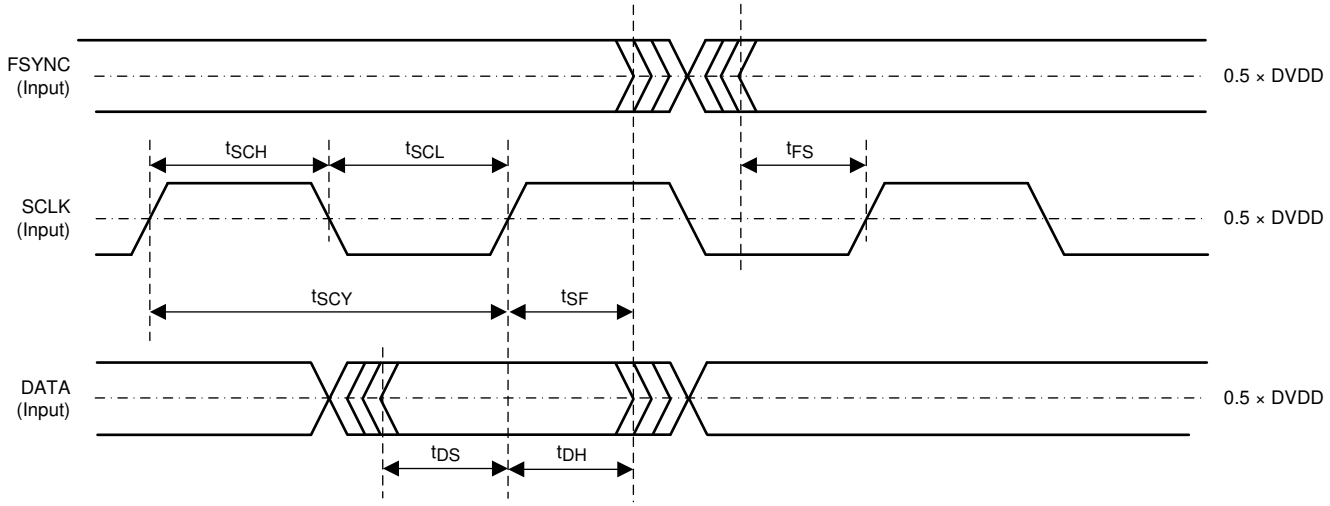


Figure 9-2. Serial Audio Timing

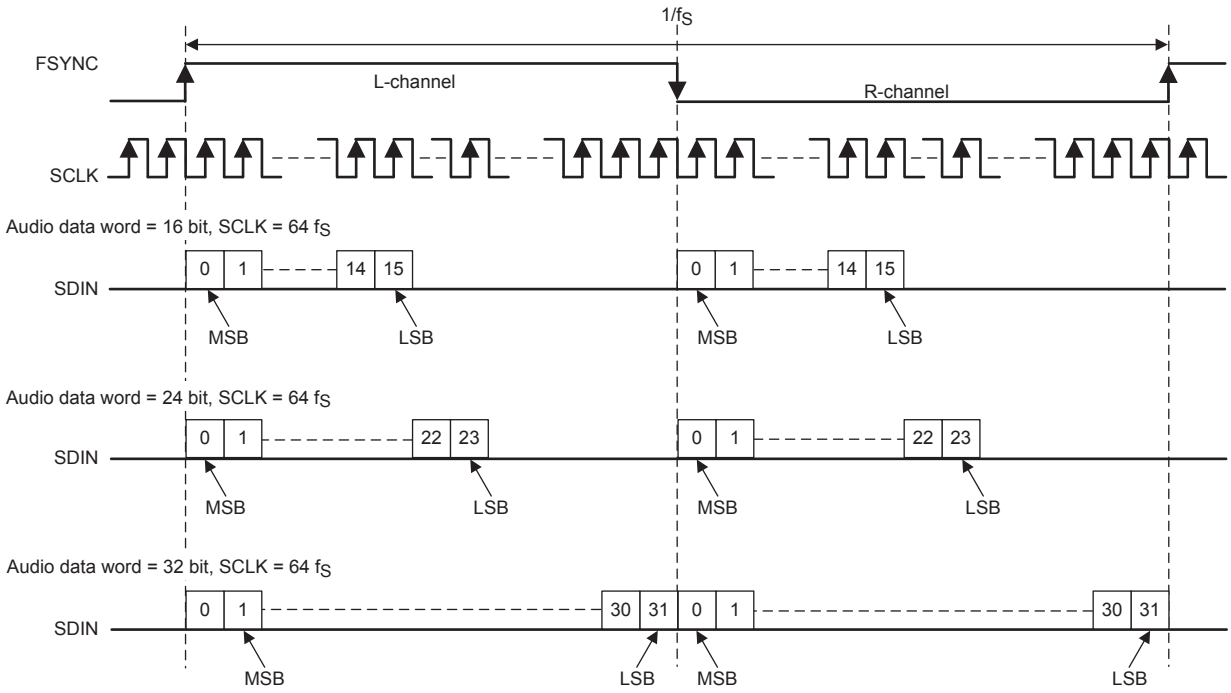


Figure 9-3. Left-Justified Audio Data Format

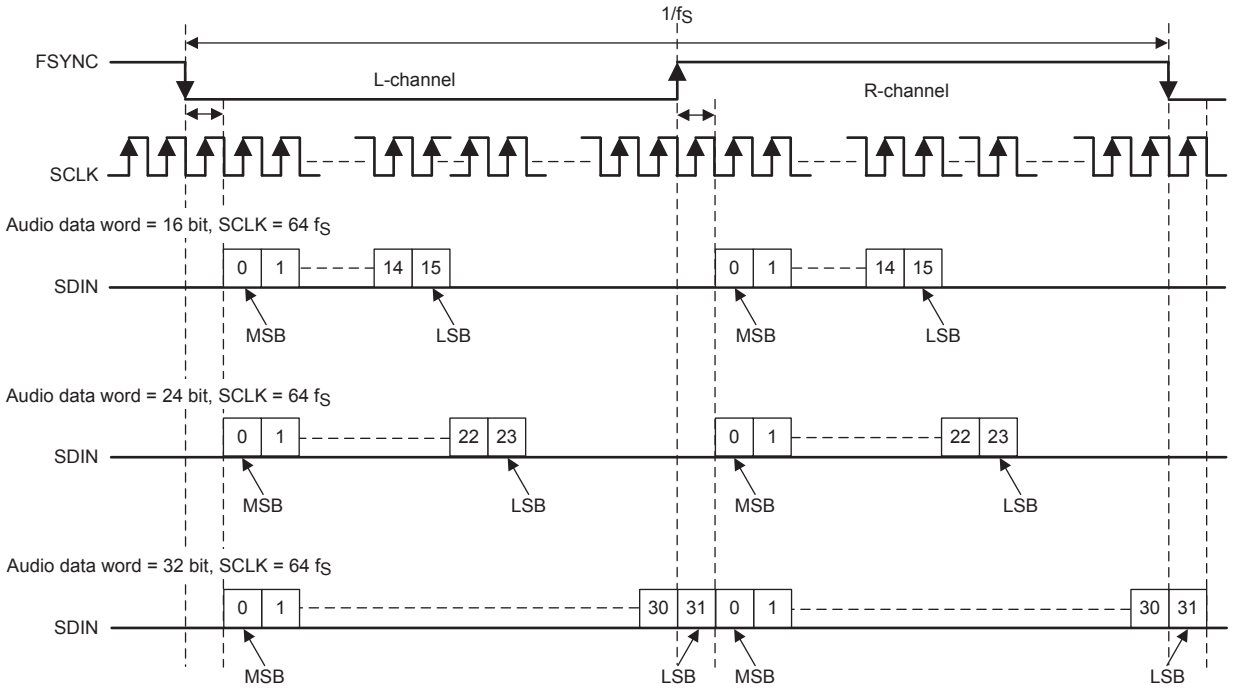
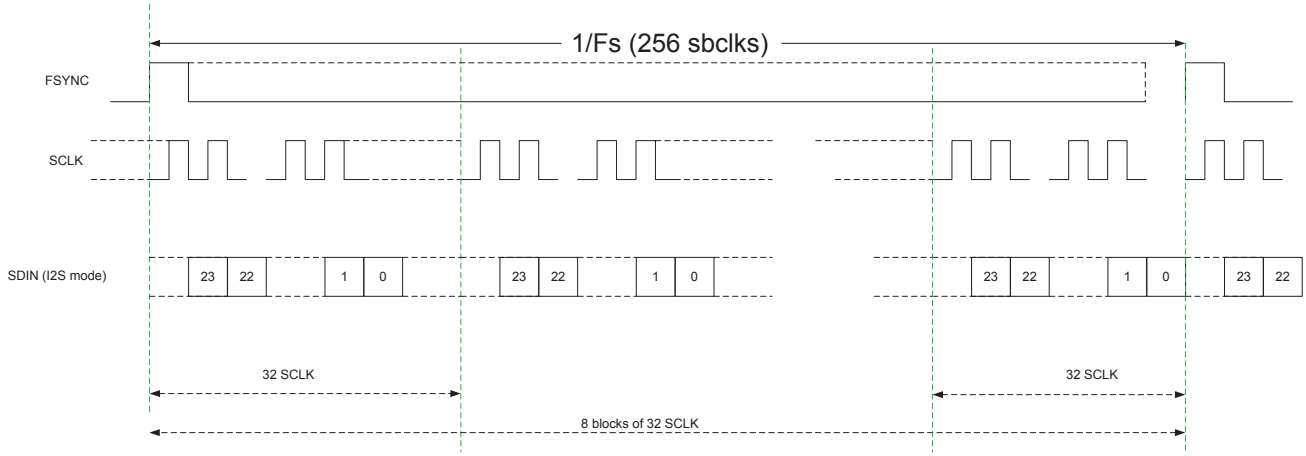


Figure 9-4. I²S Audio Data Format



Audio Data Format: TDM8 mode

Figure 9-5. TDM8 Audio Data Format

9.3.2 DC Blocking

Direct-current (DC) content in the audio signal can damage speakers. The data path has a high-pass filter to remove any DC from the input signal. The corner frequency is selectable from 4 Hz, 8 Hz, or 15 Hz to 30 Hz with bits 0 through 3 in Miscellaneous Control 4 Register (address = 0x26). The default value of –3 dB is approximately 4 Hz for 44.1 kHz or 48 kHz and approximately 8 Hz for 96 kHz sampling rates.

9.3.3 Volume Control and Gain

Each channel has an independent digital-volume control with a range from –100 dB to +24 dB with 0.5-dB steps. The volume control is set through I²C. The gain-ramp rate is programmable through I²C to take one step every 1, 2, 4, or 8 FSYNC cycles.

The peak output-voltage swing is also configurable in the gain control register through I²C. The four gain settings are 7.5 V, 15 V, 21 V, and 29 V. TI recommends selecting the lowest possible for the expected PVDD operation to optimize output noise and dynamic range performance.

9.3.4 High-Frequency Pulse-Width Modulator (PWM)

The PWM converts the PCM input data into a switched signal of varying duty cycle. The PWM modulator is an advanced design with high bandwidth, low noise, low distortion, and excellent stability. The output switching rate is synchronous to the serial audio-clock input and is programmed through I²C to be between 8× and 48× the input-sample rate. The option to switch at high frequency allows the use of smaller and lower cost external filtering components. Table 9-3 lists the switch frequency options for bits 4 through 6 in the Miscellaneous Control 2 Register (address 0x02).

Table 9-3. Output Switch Frequency Option

INPUT SAMPLE RATE	BIT 6:4 SETTINGS					
	000	001	010 to 100	101	110	111
44.1 kHz	352.8 kHz	441 kHz	RESERVED	1.68 MHz	1.94 MHz	2.12 MHz
48 kHz	384 kHz	480 kHz	RESERVED	1.82 MHz	2.11 MHz	Not supported
96 kHz	384 kHz	480 kHz	RESERVED	1.82 MHz	2.11 MHz	Not supported

9.3.5 EMI Management Features

The EMI features are provided to help manage conducted and radiated emissions. Board layout and power supply design will provide the biggest impact on EMI performance, but these features can be used to adjust device operation for fine tuning EMI performance.

9.3.5.1 Spread-Spectrum

Spread-spectrum modulation is a PWM modulation technique that reduces the peaks seen in EMI measurements by varying the output PWM frequency. This feature will vary the output switching frequency by +/- 8%.

To enable spread-spectrum follow the procedure below:

1. Ensure the TAS6422E-Q1 is correctly powered and in Hi-Z mode.
2. While in Hi-Z mode, enable spread-spectrum using I²C by writing "1" to bit 7 of register Spread-Spectrum Control 1 Register (address = 0x77) and setting bit 6-7 of Miscellaneous Control 5 Register (address = 0x28) to "11".
3. The spread-spectrum settings are retained while PVDD and VBAT are applied, but must be enabled again if PVDD or VBAT are removed or invalid.

9.3.5.2 Channel-to-Channel Phase Control

The TAS6422E-Q1 has configurable output PWM phase control to manage conducted and radiated emissions. This feature allows the channel output PWM phase offset, relative to other channels, to be changed..

When the connected output loads have an impedance of 4 Ω or larger, a channel phase offset of 180 degrees, 210 degrees, 225 degrees or 240 degrees can be selected. For loads with an impedance of less than 4 Ω, only the channel phase offsets of 210 degrees, 225 degrees or 240 degrees should be selected and the default value of 180 degree needs to be adjusted.

The phase options available can be found in Miscellaneous Control 2 Register (address = 0x02) [default = 0x62].

9.3.6 Gate Drive

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high-current, full-bridge, power-FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

The gate-driver power-supply voltage, GVDD, is internally generated and a decoupling capacitor is connected at pin 9.

The full H-bridge output stages use only NMOS transistors. Therefore, bootstrap capacitors are required for the proper operation of the high side NMOS transistors. A 1-µF ceramic capacitor of quality X7R or better, rated for at least 16 V, must be connected from each output to the corresponding bootstrap input (see the application circuit diagram in Figure 10-2). The bootstrap capacitors connected between the BST pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high keeping the high-side MOSFETs turned on.

9.3.7 Power FETs

The BTL output for each channel comprises four N-channel 90-mΩ FETs for high efficiency and maximum power transfer to the load. These FETs are designed to handle the fast switching frequency and large voltage transients during load dump.

9.3.8 Load Diagnostics

The device incorporates both DC load diagnostics and AC load diagnostics, which are used to determine the status of the load. The DC diagnostics are turned on by default, but if a fast startup without diagnostics is required, the DC diagnostics can be bypassed through I^2C. The DC diagnostics runs when any channel is directed to leave the Hi-Z state and enter the MUTE or PLAY state. The DC diagnostics can also be enabled manually to run on any or all channels . DC Diagnostics can be started from any operating condition, but if the channel is in PLAY state, then the time to complete the diagnostic is longer because the device must ramp down the audio signal of that channel before transitioning to the Hi-Z state. The DC diagnostics are available as soon as the device supplies are within the recommended operating range. The DC diagnostics do not rely on the audio input clocks to be available to function. DC Diagnostic results are reported for each channel separately through the I^2C registers.

9.3.8.1 DC Load Diagnostics

The DC load diagnostics are used to verify the load is properly connected. The DC diagnostics consists of four tests: short-to-power (S2P), short-to-ground (S2G), open-load (OL), and shorted-load (SL). The S2P and S2G tests trigger if the impedance to GND or a power rail is below that specified in the *Specifications* section. The diagnostic detects a short to vehicle battery, even when the supply is boosted. The SL test has an I^2C-configurable threshold depending on the expected load to be connected. Because the speakers connected to each channel might be different, each channel can be assigned a unique threshold value. The OL test reports if the select channel has a load impedance greater than the limits in the *Specifications* section.

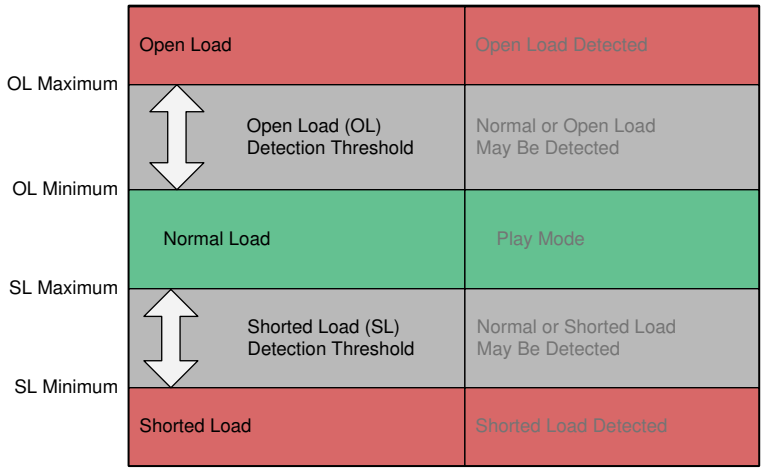


Figure 9-6. DC Load Diagnostic Reporting Thresholds

9.3.8.2 Line Output Diagnostics

The device also includes an optional test to detect a line-output load. A line-output load is a high-impedance load that is above the open-load (OL) threshold such that the DC-load diagnostics report an OL condition. After an OL

condition is detected on a channel, if the line output detection bit is also set, the channel checks if a line-output load is present as well. This test is not pop free, so if an external amplifier is connected it should be muted.

9.3.8.3 AC Load Diagnostics

The AC load diagnostic is used to determine the proper connection of a capacitively-coupled speaker or tweeter when used with a passive crossover. The AC load diagnostic is controlled through I^2C. The AC diagnostics requires an external input signal and reports the approximate load impedance and phase. The selected signal frequency should create current flow through the desired speaker for proper detection. If multiple channels must be tested, the diagnostics should be run in series. The AC load-diagnostic test procedure is as follows.

9.3.8.3.1 Impedance Magnitude Measurement

For load-impedance detection, use the following test procedure:

1. Set the channels to be tested into the Hi-Z state.
2. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to '0'.
3. Apply a full-scale input signal from the DSP for the tested channels with the desired frequency (recommended 10 kHz to 20 kHz).

Note

The device ramps the signal up and down automatically to prevent pops and clicks.

4. Set the device into the AC diagnostic mode (set bit 3 through bit 2 as needed in register 0x15 to '1' for CH1 to CH2. For PBTL mode, test channel 1 for PBTL12)
5. Read back the AC impedance (register 0x17 through register register 0x18).

   When the test is complete the channel reporting register indicates the status change from the AC diagnostic mode to the Hi-Z state. The detected impedance is stored in the appropriate I^2C register.

The hexadecimal register value must be converted to decimal and used to calculate the impedance magnitude using the following equation:

$$Channelx\ Impedance = \frac{Impedance\_CHx \times 2.371 mV}{(Gain)(I\ mA)}\ (Ohms)$$

Figure 9-7. AC Magnitude Calculation

9.3.8.3.2 Impedance Phase Reference Measurement

The first stage to determine the AC phase is to utilize the built-in loopback mode to determine the reference value for the phase measurement. This reference nullifies any phase offset in the device and measure only the phase of the load. This is measured for channels 1. Channel 2 uses the results of channel 1 for the calculations.

For loopback delay detection, use the following test procedure for either BTL mode or PBTL mode:

- BTL mode
  1. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to '1' to enable AC loopback mode.
  2. Apply a 0-dBFS 19 kHz signal and enable AC load diagnostics. CH1 and CH2 reuse the AC sensing loop of CH1 (set bit 3 in register 0x15 to '1').
  3. Read back the 16-bit hexadecimal, AC_LDG_PHASE1 value. Register 0x1B holds the MSB and register 0x1C holds the LSB.
  4. For channel 1/2 set bit 3 in register 0x15 to '0'.
- PBTL mode $\overline{\text{STANDBY}}$
  1. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to '1' to enable AC loopback mode.
  2. Set the PBTL CH12 bits (see register 0x00) to '0' without toggling pin to enter BTL mode only for load diagnostics.
  3. Apply a 0 dBFS 19 kHz signal and enable AC load diagnostics. For PBTL12, enable the AC sensing loop of CH1 (set bit 3 in register 0x15 to '1').

4. Read back the AC_LDG_PHASE1 value. Register 0x1B holds the MSB and register 0x1C holds the LSB.
5. Set the PBTL CH12 bits (see register 0x00) to '1' to go back to PBTL mode for load diagnostics.
6. For PBTL12 set bit 3 in register 0x15 to '0'.

When the test is complete, the channel reporting register indicates the status change from the AC diagnostic mode to the Hi-Z state. The detected impedance is stored in the appropriate I^2C register.

9.3.8.3.3 Impedance Phase Measurement

After performing the phase reference measurements, measure the phase of the speaker load. This is performed in the same manner as the reference measurements, except the loopback is disabled in bit 7 register 0x16. Previously, the phase reference is measured on channel 1. In this test stage all two channels are measured. Measure the channels sequentially as they cannot be measured at the same time.

For loopback delay detection, use the following test procedure for either BTL mode or PBTL mode:

- BTL mode
  1. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to '0' to disable AC loopback mode.
  2. Apply a 0-dBFS 19 kHz signal and enable AC load diagnostics. CH1 and CH2 reuse the AC sensing loop of CH1 (set bit 3 in register 0x15 to '1').
  3. Read back the 16-bit hexadecimal, AC_LDG_PHASE1 value. Register 0x1B holds the MSB and register 0x1C holds the LSB.
  4. Read back the hexadecimal stimulus value, STI. Register 0x1D holds the MSB and register 0x1E holds the LSB.
  5. For channel 1/2 set bit 3 in register 0x15 to '0'.

     When the test is complete, the channel reporting register indicates the status change from the AC diagnostic mode to the Hi-Z state. The detected impedance is stored in the appropriate I^2C register.
- PBTL mode
  1. Set the AC_DIAGS_LOOPBACK bit (bit 7 in register 0x16) to '0' to disable AC loopback mode.
  2. Set the PBTL CH12 bits (see register 0x00) to '0' without toggling $\overline{\text{STANDBY}}$ pin to enter BTL mode only for load diagnostics.
  3. Apply a 0 dBFS 19 kHz signal and enable AC load diagnostics. For PBTL12, enable the AC sensing loop of CH1 (set bit 3 in register 0x15 to '1').
  4. Read back the AC_LDG_PHASE1 value. Register 0x1B holds the MSB and register 0x1C holds the LSB.
  5. Read back the hexadecimal stimulus value, STI. Register 0x1D holds the MSB and register 0x1E holds the LSB.
  6. Set the PBTL CH12 bits (see register 0x00) to '1' to go back to PBTL mode for load diagnostics.
  7. For PBTL12 set bit 3 in register 0x15 to '0'.

The AC phase in degrees is calculated with the following equation:

$$Phase\_CHx = 360(\frac{Phase\_CHx(LBK) - Phase\_CHx(LDM)}{STI\_CHx(LDM)})$$

Figure 9-8. AC Phase Calculation

Where:

- Phase_CHx(LBK) is the reference phase measurement. LBK stands for loopback mode
- Phase_CHx(LDM) is the phase measure of the load. LDM stands for load mode
- STI_CHx(LDM) is the stimulus value

9.3.8.3.4

Table 9-4. AC Impedance Code to Magnitude

SETTING	GAIN AT 19 kHz	I(A)	MEASUREMENT RANGE (Ω)	MAPPING FROM CODE TO MAGNITUDE (Ω/ Code)
Gain = 4, I = 10 mA (recommended)	4.28	0.01	12	0.05832
Gain = 4, I = 19 mA	4.28	0.019	6	0.0307
Gain = 1, I = 10 mA (recommended)	1	0.01	48	0.2496
Gain = 1, I = 19 mA	1	0.019	24	0.1314

9.3.9 Protection and Monitoring

9.3.9.1 Overcurrent Limit (I_{LIMIT})

The overcurrent limit terminates each PWM pulse to limit the output current flow when the current limit (I_{LIMIT}) is exceeded. Power is limited, but operation continues without disruption and prevents undesired shutdown for transient music events. I_{LIMIT} is not reported as a fault condition to either registers or the $\overline{FAULT}$ pin but as warning condition to the $\overline{WARN}$ pin and ILIMIT Status Register (address = 0x25). Each channel is independently monitored and limited. The two programable levels can be set by bit 4 in the Miscellaneous Control 1 register (address 0x01).

9.3.9.2 Overcurrent Shutdown (I_{SD})

If the output load current reaches I_{SD}, such as an output short to GND, then a peak current limit occurs, which shuts down the channel. The time to shutdown the channel varies depending on the severity of the short condition. The affected channel is placed into the Hi-Z state, the fault is reported to the register, and the $\overline{FAULT}$ pin is asserted. The device remains in this state until the CLEAR FAULT bit is set in Miscellaneous Control 3 Register, 0x21 bit 7. After clearing this bit and if the diagnostics are enabled, the device automatically starts diagnostics on the channel and, if no load failure is found, the device restarts. If a load fault is found the device continues to rerun the diagnostics once per second. Because this hiccup mode uses the diagnostics, no high current is created. If the diagnostics are disabled, the device sets the state for that channel to Hi-Z and requires the MCU to take the appropriate action, setting the CLEAR FAULT bit after the fault got removed, in order to return to Play state.

Two programable levels can be set by bit 4 in the Miscellaneous Control 1 register (address 0x01).

9.3.9.3 DC Detect

This circuit detects a DC offset continuously during normal operation at the output of the amplifier. If the DC offset exceeds the threshold, that channel is placed in the Hi-Z state, the fault is reported to the I^2C register, and the $\overline{FAULT}$ pin is asserted. A register bit can be used to mask reporting to the $\overline{FAULT}$ pin if required.

9.3.9.4 Clip Detect

The clip detect is reported on the $\overline{\text{WARN}}$ pin if 100% duty-cycle PWM is reached for a minimum number of PWM cycles set by the Clip Window Register (address = 0x23). The default is 20 PWM cycles. The Clip Detect is latched and can be cleared by I^2C. Masking the clip reporting to the pin is possible through I^2C. If desired, the Clip Detect can be configured to be non-latching through I^2C. In non-latching mode, Clip Detect is reported when the PWM duty cycle reaches 100%, and deasserted once the PWM duty cycle falls below 100%.

9.3.9.5 Global Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD)

Four overtemperature warning levels are available in the device (see the *Register Maps* section for thresholds). When the junction temperature exceeds the warning level, the $\overline{\text{WARN}}$ pin is asserted, unless the mask bit in Pin Control Register (address = 0x14) has been set to disable reporting. The device functions until the OTSD value is reached at which point all channels are placed in the Hi-Z state, and the $\overline{\text{FAULT}}$ pin is asserted. By default, the device remains shut down after the temperature drops to normal levels. This configuration can be changed in bit 3 of the Miscellaneous Control 3 Register (address = 0x21) to auto-recovery: When the junction temperature returns to normal levels, the device automatically recovers and places the channel into the state indicated by the state control register. Note that even in auto-recovery configuration the $\overline{\text{FAULT}}$ pin remains asserted until the CLEAR FAULT bit (bit 7) is set in register 0x21.

9.3.9.6 Channel Overtemperature Warning [OTW(i)] and Shutdown [OTSD(i)]

In addition to the global OTW, each output channel also has an individual overtemperature warning and shutdown. If any channel exceeds the OTW(i) threshold, the warning register bit in Warnings Register (address = 0x13) is set as the $\overline{\text{WARN}}$ pin is asserted, unless the mask bit has been set to disable reporting. If the channel temperature exceeds the OTSD(i) threshold then the channel goes to the Hi-Z state and either remains there or auto-recovers to the state indicated by the state control register when the temperature drops below the OTW(i) threshold, depending on the setting of bit 3 of the Miscellaneous Control 3 Register (address = 0x21).

9.3.9.7 Undervoltage (UV) and Power-On-Reset (POR)

The UV protection detects low voltages on the PVDD and VBAT pins. In the event of an UV condition, the $\overline{\text{FAULT}}$ pin is asserted, and the I^2C register is updated. A POR on the VDD pin causes the I^2C to goes to the high-impedance (Hi-Z) state, and all registers are reset to default values. At power-on or after a POR event, the POR warning bit and $\overline{\text{WARN}}$ pin are asserted.

9.3.9.8 Overvoltage (OV) and Load Dump

The OV protection detects high voltages on the PVDD pin. If the PVDD pin reaches the OV threshold, the $\overline{\text{FAULT}}$ pin is asserted and the I^2C register is updated. The device can withstand 40 V load dump voltage spikes.

9.3.10 Power Supply

The device has three power supply inputs, VDD, PVDD, and VBAT, which are described as follows:

VDD This pin is a 3.3V supply pin that provides power to the low voltage circuitry.

VBAT This pin is a higher voltage supply that can be connected to the vehicle battery or the regulated voltage rail in a boosted system within the recommended limits. For best performance, this rail should be 10 V or higher. See the *Electrical Characteristics* table for the maximum supply voltage. This supply rail is used for higher voltage analog circuits but not the output FETs.

PVDD This pin is a high-voltage supply that can either be connected to the vehicle battery or to another voltage rail in a boosted system. The PVDD pin supplies the power to the output FETs and can be within the recommended operating limits, even if that is below the VBAT supply, to allow for dynamic voltage systems.

Several on-chip regulators are included for generating the voltages necessary for the internal circuitry. The external pins are provided only for bypass capacitors to filter the supply and should not be used to power other circuits.

The device can withstand fortuitous open ground and power conditions within the absolute maximum ratings for the device. Fortuitous open ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs.

9.3.10.1 Vehicle-Battery Power-Supply Sequence

The device can accept any sequence of the VBAT, PVDD and VDD supply.

9.3.10.1.1 Power-Up Sequence

In a typical system, the VBAT and PVDD supplies are both connected to the vehicle battery and power up at the same time. The VDD supply should be applied after the VBAT and PVDD supplies are within the recommended operating range.

9.3.10.1.2 Power-Down Sequence

To power-down the device, first set the $\overline{\text{STANDBY}}$ pin low for at least 15ms before removing PVDD, VBAT or VDD. After 15ms, the power supplies can be removed.

9.3.10.2 Boosted Power-Supply Sequence

In this case, the VBAT and PVDD inputs are not connected to the same supply.

When powering up, apply the VBAT supply first, the VDD supply second, and the PVDD supply last.

When powering down, first set the $\overline{\text{STANDBY}}$ pin low for at least 15ms before removing PVDD, VBAT or VDD. After 15ms, the power supplies can be removed.

9.3.11 Hardware Control Pins

The device has four pins for control and device status: $\overline{\text{FAULT}}$, $\overline{\text{MUTE}}$, $\overline{\text{WARN}}$, and $\overline{\text{STANDBY}}$.

9.3.11.1 $\overline{\text{FAULT}}$

The $\overline{\text{FAULT}}$ pin reports faults and is active low under any of the following conditions:

- Any channel faults (overcurrent or DC detection)
- Overtemperature shutdown
- Overvoltage or undervoltage conditions on the VBAT or PVDD pins
- Clock errors

For all listed faults, the $\overline{\text{FAULT}}$ pin remains asserted after the fault condition is rectified. Deassert the $\overline{\text{FAULT}}$ pin by writing the CLEAR FAULT bit (bit 7) in register 0x21.

The register reports for all fault reports remain asserted until they are cleared by writing the CLEAR FAULT bit (bit 7) in register 0x21.

Register bits are available to mask fault categories from reporting to the $\overline{\text{FAULT}}$ pin. These bits only mask the setting of the pin and do not affect the register reporting or protection of the device. By default all faults are reported to the pin. See the *Register Maps* section for a description of the mask settings.

This pin is an open-drain output with an internal 100 kΩ pullup resistor to VDD.

9.3.11.2 $\overline{\text{WARN}}$

This active-low output pin reports audio clipping, overtemperature warnings,overcurrent limit warnings and POR events.

Clipping is reported if any channel is at the maximum modulation for 20 consecutive PWM clocks (default value) which results in a 10-µs delay to report the onset of clipping. Changing the number of required consecutive PWM clocks in the Clip Window Register (address = 0x23) impacts the report delay time. The Clip Detect Warning bit is sticky in latching mode and can be cleared by the CLEAR FAULT bit (bit 7) in register 0x21.

An overtemperature warning (OTW) is reported if the general temperature or any of the channel temperature warnings are set. The warning temperature can be set through bits 5 and 6 in Miscellaneous Control 1 Register (address = 0x01).

Register bits are available to mask either clipping, OTW or I_{LIMIT} reporting to the pin. These bits only mask the setting of the pin and do not affect the register reporting. By default both clipping, I_{LIMIT} and OTW are reported.

The $\overline{\text{WARN}}$ pin is latched and can be cleared by writing the CLEAR FAULT bit (bit 7) in register 0x21.

This pin is an open-drain output with an internal 100 kΩ pull-up resistor to VDD.

9.3.11.3 $\overline{\text{MUTE}}$

This active-low input pin is used for hardware control of the mute and unmute function for all channels.

This pin has a 100 kΩ internal pull-down resistor.

9.3.11.4 $\overline{\text{STANDBY}}$

When this active-low input pin is asserted, the device goes into shutdown and current draw is limited. This pin can be used to shut down the device rapidly. The outputs are ramped down in less than 5 ms if the device is not already in the Hi-Z state.

This pin has a 100 kΩ internal pull-down resistor.

9.4 Device Functional Modes

9.4.1 Operating Modes and Faults

The operating modes and faults are listed in the following tables.

Table 9-5. Operating Modes

STATE NAME	OUTPUT FETS	OSCILLATOR	I^2C
STANDBY	Hi-Z	Stopped	Active
Hi-Z	Hi-Z	Active	Active
MUTE	Switching at 50%	Active	Active
PLAY	Switching with audio	Active	Active

Table 9-6. Global Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION RESULT
POR	Voltage fault	All	I^2C + $\overline{WARN}$ pin	Standby
VBAT UV		Hi-Z, mute, normal	I^2C + $\overline{FAULT}$ pin	Hi-Z
PVDD UV				
VBAT or PVDD OV				
OTW	Thermal warning	Hi-Z, mute, normal	I^2C + $\overline{WARN}$ pin	None
OTSD	Thermal shutdown	Hi-Z, mute, normal	I^2C + $\overline{FAULT}$ pin	Hi-Z

Table 9-7. Channel Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE
Clipping	Warning	Mute and play	I^2C + $\overline{WARN}$ pin	None
Overcurrent limiting	Protection		I^2C + $\overline{WARN}$ pin	Current limit
Overcurrent fault	Output channel fault		I^2C + $\overline{FAULT}$ pin	Hi-Z
DC detect				

9.5 Programming

9.5.1 I²C Serial Communication Bus

The device communicates with the system processor through the Inter-Integrated Circuit (I²C) serial communication bus as an I²C slave-only device. The processor can poll the device through I²C to determine the operating status, configure settings, or run diagnostics. For a complete list and description of all I²C controls, see the *Register Maps* section.

The device includes two I²C address pins, so up to four devices can be used together in a system with no additional bus switching hardware. The I²C ADDRx pins set the slave address of the device as listed in Table 9-8.

Table 9-8. I²C Addresses

DESCRIPTION	I²C ADDR1	I²C ADDR0	I²C Write	I²C Read
Device 0	0	0	0xD4	0xD5
Device 1	0	1	0xD6	0xD7
Device 2	1	0	0xD8	0xD9
Device 3	1	1	0xDA	0xDB

9.5.2 I²C Bus Protocol

The device has a bidirectional serial-control interface that is compatible with the I²C bus protocol and supports 100 kbps and 400 kbps data transfer rates for random and sequential write and read operations. The TAS6422E-Q1 device is a slave-only device that does not support a multimaster bus environment or wait-state insertion. The control interface is used to program the registers of the device and to read device status.

The I²C bus uses two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Data is transferred on the bus serially, one bit at a time. The address and data are transferred in byte (8-bit) format with the most-significant bit (MSB) transferred first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is HIGH to indicate a start and stop conditions. A HIGH-to-LOW transition on SDA indicates a start, and a LOW-to-HIGH transition indicates a stop. Normal data bit transitions must occur within the low time of the clock period. The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then wait for an acknowledge condition. The device holds SDA LOW during the acknowledge-clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus a R/W bit (1 byte). All compatible devices share the same signals via a bidirectional bus using a wired-AND connection. An external pullup resistor must be used for the SDA and SCL signals to set the HIGH level for the bus. The number of bytes that can be transmitted between start and stop conditions is unlimited. When the last word transfers, the master generates a stop condition to release the bus.

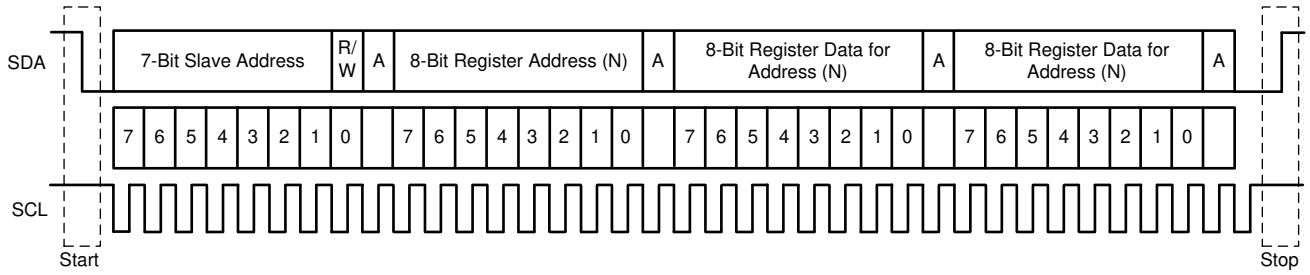


Figure 9-9. Typical I²C Sequence

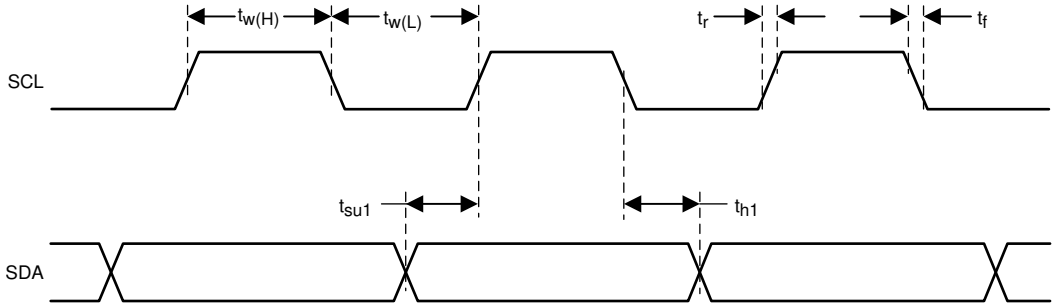


Figure 9-10. SCL and SDA Timing

Use the I²C ADDRx pins to program the device slave address. Read and write data can be transmitted using single-byte or multiple-byte data transfers.

9.5.3 Random Write

As shown in Figure 9-11, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. The R/W bit determines the direction of the data transfer. For a write data transfer, the R/W bit is a 0. After receiving the correct I²C device address and the R/W bit, the device responds with an acknowledge bit. Next, the master transmits the address byte or bytes corresponding to the internal memory address being accessed. After receiving the address byte, the device again responds with an acknowledge bit. Next, the master device transmits the data byte to be written to the memory address being accessed. After receiving the data byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

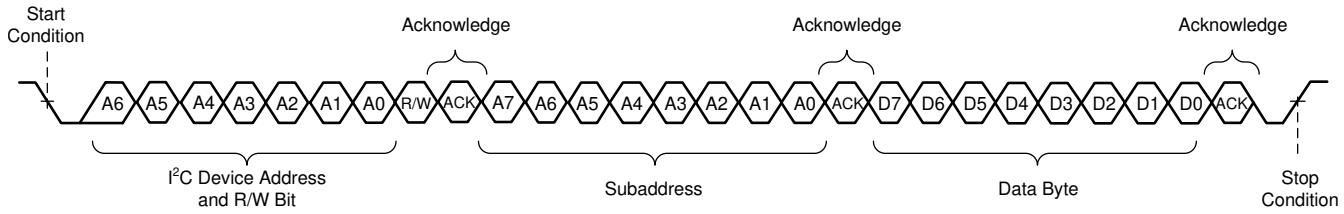


Figure 9-11. Random Write Transfer

9.5.4 Sequential Write

A sequential data-write transfer is identical to a single-byte data-write transfer except that multiple data bytes are transmitted by the master to the device as shown in Figure 9-12. After receiving each data byte, the device responds with an acknowledge bit and the I²C subaddress is automatically incremented by one.

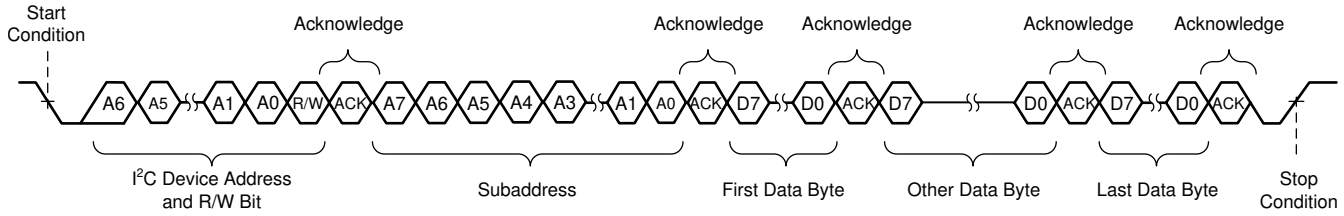


Figure 9-12. Sequential Write Transfer

9.5.5 Random Read

As shown in Figure 9-13, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I²C device address and the R/W bit. For the data-read transfer, both a write followed by a read occur. Initially, a write occurs to transfer the address byte or bytes of the internal memory address to be read. As a result, the R/W bit is a 0. After receiving the address and the R/W bit, the device responds with an acknowledge bit. In addition, after sending the internal memory address byte or bytes, the master device transmits another start condition followed by the address and the R/W bit again. This time the R/W bit is a 1,

indicating a read transfer. After receiving the address and the R/W bit, the device again responds with an acknowledge bit. Next, the device transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data-read transfer.

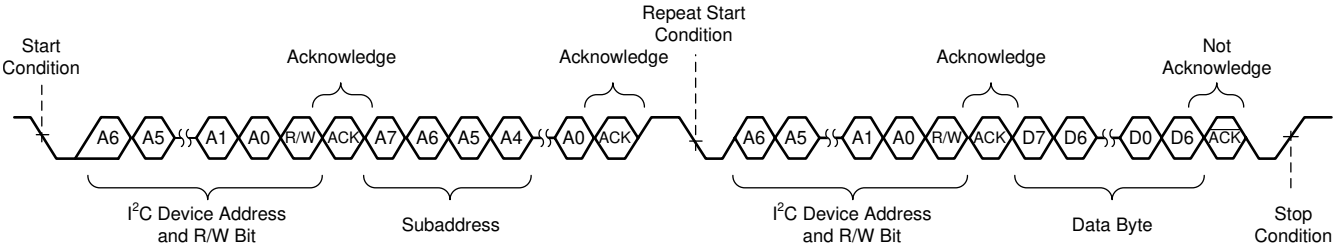


Figure 9-13. Random Read Transfer

9.5.6 Sequential Read

A sequential data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the device to the master device as shown in Figure 9-14. Except for the last data byte, the master device responds with an acknowledge bit after receiving each data byte and automatically increments the I^2C subaddress by one. After receiving the last data byte, the master device transmits a not-acknowledge bit followed by a stop condition to complete the transfer.

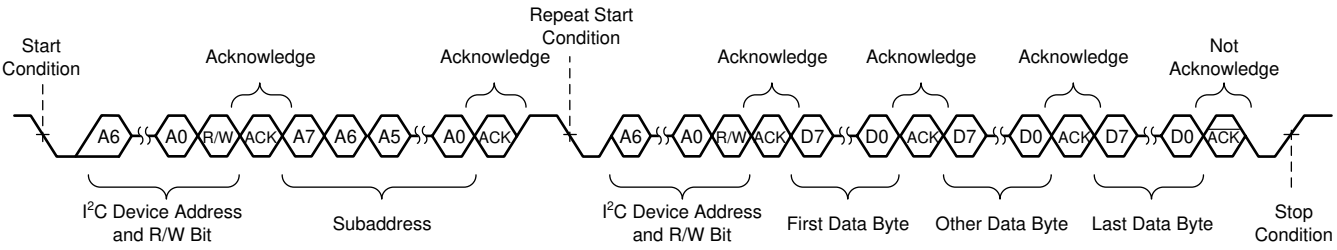


Figure 9-14. Sequential Read Transfer

9.6 Register Maps

Table 9-9. I²C Address Register Definitions

Address	Type	Register Description	Section
0x00	R/W	Mode Control	Go
0x01	R/W	Miscellaneous Control 1	Go
0x02	R/W	Miscellaneous Control 2	Go
0x03	R/W	SAP Control (Serial Audio-Port Control)	Go
0x04	R/W	Channel State Control	Go
0x05	R/W	Channel 1 Volume Control	Go
0x06	R/W	Channel 2 Volume Control	Go
0x07	R	RESERVED	
0x08	R	RESERVED	
0x09	R/W	DC Diagnostic Control 1	Go
0x0A	R/W	DC Diagnostic Control 2	Go
0x0B	R	RESERVED	
0x0C	R	DC Load Diagnostic Report 1 (Channels 1 and 2)	Go
0x0D	R	RESERVED	
0x0E	R	DC Load Diagnostic Report 3-Line Output	Go
0x0F	R	Channel State Reporting	Go
0x10	R	Channel Faults (Overcurrent, DC Detection)	Go
0x11	R	Global Faults 1	Go
0x12	R	Global Faults 2	Go
0x13	R	Warnings	Go
0x14	R/W	Pin Control	Go
0x15	R/W	AC Load Diagnostic Control 1	Go
0x16	R/W	AC Load Diagnostic Control 2	Go
0x17	R	AC Load Diagnostic Report Channel 1	Go
0x18	R	AC Load Diagnostic Report Channel 2	Go
0x19	R	RESERVED	
0x1A	R	RESERVED	
0x1B	R	AC Load Diagnostic Phase Report High	Go
0x1C	R	AC Load Diagnostic Phase Report Low	Go
0x1D	R	AC Load Diagnostic STI Report High	Go
0x1E	R	AC Load Diagnostic STI Report Low	Go
0x1F	R	RESERVED	
0x20	R	RESERVED	
0x21	R/W	Miscellaneous Control 3	Go
0x22	R/W	Clip Control	Go
0x23	R/W	Clip Window	Go
0x24	R/W	Clip Warning	Go
0x25	R/W	ILIMIT Status	Go
0x26	R/W	Miscellaneous Control 4	Go
0x27	R	RESERVED	
0x28	R/W	Miscellaneous Control 5	Go
0x77	R/W	Spread Spectrum Control 1	Go
0x78	R/W	Spread Spectrum Control 2	Go

Table 9-9. I²C Address Register Definitions (continued)

Address	Type	Register Description	Section
0x79	R/W	Spread Spectrum Control 3	Go

9.6.1 Mode Control Register (address = 0x00) [default = 0x00]

The Mode Control register is shown in Figure 9-15 and described in Table 9-10.

Figure 9-15. Mode Control Register

7	6	5	4	3	2	1	0
RESET	RESERVED	RESERVED	PBTL CH12	CH1 LO MODE	CH2 LO MODE	RESERVED	RESERVED
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 9-10. Mode Control Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	R/W	0	**0: Normal operation** 1: Resets the device. Self-clearing, reads back 0.
6	RESERVED	R/W	0	RESERVED
5	RESERVED	R/W	0	RESERVED
4	PBTL CH12	R/W	0	**0: Channels 1 and 2 are in BTL mode** 1: Channels 1 and 2 are in parallel BTL mode
3	CH1 LO MODE	R/W	0	**0: Channel 1 is in normal/speaker mode** 1: Channel 1 is in line output mode
2	CH2 LO MODE	R/W	0	**0: Channel 2 is in normal/speaker mode** 1: Channel 2 is in line output mode
1	RESERVED	R/W	0	RESERVED
0	RESERVED	R/W	0	RESERVED

9.6.2 Miscellaneous Control 1 Register (address = 0x01) [default = 0x32]

The Miscellaneous Control 1 register is shown in Figure 9-16 and described in Table 9-11.

Figure 9-16. Miscellaneous Control 1 Register

7	6	5	4	3	2	1	0
HPF BYPASS	OTW CONTROL		OC CONTROL	VOLUME RATE		GAIN	
R/W-0	R/W-01		R/W-1	R/W-00		R/W-10	

Table 9-11. Misc Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	HPF BYPASS	R/W	0	**0: High pass filter eneabled** 1: High pass filter disabled
6–5	OTW CONTROL	R/W	01	00: Global overtemperature warning set to 140°C **01: Global overtemperature warning set to 130C** 10: Global overtemperature warning set to 120°C 11: Global overtemperature warning set to 110°C
4	OC CONTROL	R/W	1	0: Overcurrent is level 1 **1: Overcurrent is level 2**
3–2	VOLUME RATE	R/W	00	**00: Volume update rate is 1 step / FSYNC** 01: Volume update rate is 1 step / 2 FSYNCs 10: Volume update rate is 1 step / 4 FSYNCs 11: Volume update rate is 1 step / 8 FSYNCs
1–0	GAIN	R/W	10	00: Gain level 1 = 7.5 V peak output voltage 01: Gain Level 2 = 15 V peak output voltage **10: Gain Level 3 = 21 V peak output voltage** 11: Gain Level 4 = 29 V peak output voltage

9.6.3 Miscellaneous Control 2 Register (address = 0x02) [default = 0x62]

The Miscellaneous Control 2 register is shown in Figure 9-17 and described in Table 9-12.

Figure 9-17. Miscellaneous Control 2 Register

7	6	5	4	3	2	1	0
RESERVED	PWM FREQUENCY			RESERVED	SDM_OSR	OUTPUT PHASE	
R/W-0	R/W-110			R/W-0	R/W-0	R/W-10	

Table 9-12. Misc Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	RESERVED
6–4	PWM FREQUENCY	R/W	110	000: 8 × f_S (352.8 kHz / 384 kHz) 001: 10 × f_S (441 kHz / 480 kHz) 010: RESERVED 011: RESERVED 100: RESERVED 101: 38 × f_S (1.68 MHz / 1.82 MHz) **110: 44 × f_S (1.94 MHz / 2.11 MHz)** 111: 48 × f_S (2.12 MHz / not supported)
3	RESERVED	R/W	0	RESERVED
2	SDM_OSR	R/W	0	**0: 64x OSR** 1: 128x OSR
1–0	OUTPUT PHASE	R/W	10	**The channel-to-channel PWM output phase, PHASE_SEL[2:0], is selected with the two LSB bits in this register and the MSB bit from Section 9.6.30.** 000: RESERVED 001: CH1- 0, CH2- 180 **010: CH1- 0, CH2- 180** 011: CH1- 0, CH2- 180 100: RESERVED 101: CH1- 0, CH2- 210 110: CH1- 0, CH2- 225 111: CH1- 0, CH2- 240

9.6.4 SAP Control (Serial Audio-Port Control) Register (address = 0x03) [default = 0x04]

The SAP Control (serial audio-port control) register is shown in Figure 9-18 and described in Table 9-13.

Figure 9-18. SAP Control Register

7	6	5	4	3	2	1	0
INPUT SAMPLING RATE		8 Ch TDM SLOT SELECT	TDM SLOT SIZE	TDM SLOT SELECT 2	INPUT FORMAT		
R/W-00		R/W-0	R/W-0	R/W-0	R/W-100		

Table 9-13. SAP Control Field Descriptions

Bit	Field	Type	Reset	Description
7–6	INPUT SAMPLING RATE	R/W	00	**00: 44.1 kHz** 01: 48 kHz 10: 96 kHz 11: RESERVED
5	8 Ch TDM SLOT SELECT	R/W	0	**0: First four TDM slots** 1: Last four TDM slots
4	TDM SLOT SIZE	R/W	0	**0: TDM slot size is 24-bit or 32-bit** 1: TDM slot size is 16-bit
3	TDM SLOT SELECT 2	R/W	0	See TDM Mode for details. **0: Normal** 1: Swapped
2–0	INPUT FORMAT	R/W	100	000: 24-bit right justified 001: 20-bit right justified 010: 18-bit right justified 011: 16-bit right justified **100: I^2S (16-bit or 24-bit)** 101: Left justified (16-bit or 24-bit) 110: DSP mode (16-bit or 24-bit) 111: RESERVED

9.6.5 Channel State Control Register (address = 0x04) [default = 0x55]

The Channel State Control register is shown in Figure 9-19 and described in Table 9-14.

Figure 9-19. Channel State Control Register

7	6	5	4	3	2	1	0
CH1 STATE CONTROL		CH2 STATE CONTROL		RESERVED		RESERVED	
R/W-01		R/W-01		R/W-01		R/W-01	

Table 9-14. Channel State Control Field Descriptions

Bit	Field	Type	Reset	Description
7–6	CH1 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
5–4	CH2 STATE CONTROL	R/W	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
3–2	RESERVED	R/W	01	RESERVED
1–0	RESERVED	R/W	01	RESERVED

9.6.6 Channel 1 Through 2 Volume Control Registers (address = 0x05–0x06) [default = 0xCF]

The Channel 1 Through 2 Volume Control registers are shown in Figure 9-20 and described in Table 9-15.

Figure 9-20. Channel x Volume Control Register

7	6	5	4	3	2	1	0
CH x VOLUME							
R/W-CF							

Table 9-15. Ch x Volume Control Field Descriptions

Bit	Field	Type	Reset	Description
7–0	CH x VOLUME	R/W	0xCF	8-Bit Volume Control for each channel, register address for Ch1 is 0x05, Ch2 is 0x06, 0.5 dB/step: 0xFF: 24 dB **0xCF: 0 dB** 0x07: –100 dB < 0x07: MUTE

9.6.7 DC Load Diagnostic Control 1 Register (address = 0x09) [default = 0x00]

The DC Diagnostic Control 1 register is shown in Figure 9-21 and described in Table 9-16.

Figure 9-21. DC Load Diagnostic Control 1 Register

7	6	5	4	3	2	1	0
DC LDG ABORT	2x_RAMP	2x_SETTLE	RESERVED			LDG LO ENABLE	LDG BYPASS
R/W-0	R/W-0	R/W-0				R/W-0	R/W-0

Table 9-16. DC Load Diagnostics Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	DC LDG ABORT	R/W	0	**0: Default state, clear after abort** 1: Aborts the load diagnostics in progress
6	2x_RAMP	R/W	0	**0: Normal ramp time** 1: Double ramp time
5	2x_SETTLE	R/W	0	**0: Normal Settle time** 1: Double settling time
4–2	RESERVED	R/W	000	RESERVED
1	LDG LO ENABLE	R/W	0	**0: Line output diagnostics are disabled** 1: Line output diagnostics are enabled
0	LDG BYPASS	R/W	0	**0: Automatic diagnostics when leaving Hi-Z and after channel fault** 1: Diagnostics are not run automatically

9.6.8 DC Load Diagnostic Control 2 Register (address = 0x0A) [default = 0x11]

The DC Diagnostic Control 2 register is shown in Figure 9-22 and described in Table 9-17.

Figure 9-22. DC Load Diagnostic Control 2 Register

7	6	5	4	3	2	1	0
CH1 DC LDG SL				CH2 DC LDG SL			
R/W-0001				R/W-0001			

Table 9-17. DC Load Diagnostics Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7–4	CH1 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω
3–0	CH2 DC LDG SL	R/W	0001	DC load diagnostics shorted-load threshold 0000: 0.5 Ω **0001: 1 Ω** 0010: 1.5 Ω ... 1001: 5 Ω

9.6.9 DC Load Diagnostic Report 1 Register (address = 0x0C) [default = 0x00]

DC Load Diagnostic Report 1 register is shown in Figure 9-23 and described in Table 9-18.

Figure 9-23. DC Load Diagnostic Report 1 Register

7	6	5	4	3	2	1	0
CH1 S2G	CH1 S2P	CH1 OL	CH1 SL	CH2 S2G	CH2 S2P	CH2 OL	CH2 SL
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Table 9-18. DC Load Diagnostics Report 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 S2G	R	0	**0: No short-to-GND detected** 1: Short-To-GND Detected
6	CH1 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
5	CH1 OL	R	0	**0: No open load detected** 1: Open load detected
4	CH1 SL	R	0	**0: No shorted load detected** 1: Shorted load detected
3	CH2 S2G	R	0	**0: No short-to-GND detected** 1: Short-to-GND detected
2	CH2 S2P	R	0	**0: No short-to-power detected** 1: Short-to-power detected
1	CH2 OL	R	0	**0: No open load detected** 1: Open load detected
0	CH2 SL	R	0	**0: No shorted load detected** 1: Shorted load detected

9.6.10 DC Load Diagnostics Report 3 Line Output Register (address = 0x0E) [default = 0x00]

The DC Load Diagnostic Report, Line Output, register is shown in Figure 9-24 and described in Table 9-19.

Figure 9-24. DC Load Diagnostics Report 3 Line Output Register

7	6	5	4	3	2	1	0
RESERVED				CH1 LO LDG	CH2 LO LDG	RESERVED	RESERVED
R-0000				R-0	R-0	R-0	R-0

Table 9-19. DC Load Diagnostics Report 3 Line Output Field Descriptions

Bit	Field	Type	Reset	Description
7–4	RESERVED	R	0000	RESERVED
3	CH1 LO LDG	R	0	**0: No line output detected on channel 1** 1: Line output detected on channel 1
2	CH2 LO LDG	R	0	**0: No line output detected on channel 2** 1: Line output detected on channel 2
1	RESERVED	R	0	RESERVED
0	RESERVED	R	0	RESERVED

9.6.11 Channel State Reporting Register (address = 0x0F) [default = 0x55]

The Channel State Reporting register is shown in Figure 9-25 and described in Table 9-20.

Figure 9-25. Channel State-Reporting Register

7	6	5	4	3	2	1	0
CH1 STATE REPORT		CH2 STATE REPORT		RESERVED		RESERVED	
R-01		R-01		R-01		R-01	

Table 9-20. State-Reporting Field Descriptions

Bit	Field	Type	Reset	Description
7–6	CH1 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
5–4	CH2 STATE REPORT	R	01	00: PLAY **01: Hi-Z** 10: MUTE 11: DC load diagnostics
3–2	RESERVED	R	01	RESERVED
1–0	RESERVED	R	01	RESERVED

9.6.12 Channel Faults (Overcurrent, DC Detection) Register (address = 0x10) [default = 0x00]

The Channel Faults (overcurrent, DC detection) register is shown in Figure 9-26 and described in Table 9-21.

Figure 9-26. Channel Faults Register

7	6	5	4	3	2	1	0
CH1 OC	CH2 OC	RESERVED	RESERVED	CH1 DC	CH2 DC	RESERVED	RESERVED
R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0

Table 9-21. Channel Faults Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1 OC	R	0	**0: No overcurrent fault detected** 1: Overcurrent fault detected
6	CH2 OC	R	0	**0: No overcurrent fault detected** 1: Overcurrent fault detected
5	RESERVED	R	0	RESERVED
4	RESERVED	R	0	RESERVED
3	CH1 DC	R	0	**0: No DC fault detected** 1: DC fault detected
2	CH2 DC	R	0	**0: No DC fault detected** 1: DC fault detected
1	RESERVED	R	0	RESERVED
0	RESERVED	R	0	RESERVED

9.6.13 Global Faults 1 Register (address = 0x11) [default = 0x00]

The Global Faults 1 register is shown in Figure 9-27 and described in Table 9-22.

Figure 9-27. Global Faults 1 Register

7	6	5	4	3	2	1	0
RESERVED			INVALID CLOCK	PVDD OV	VBAT OV	PVDD UV	VBAT UV
			R-0	R-0	R-0	R-0	R-0

Table 9-22. Global Faults 1 Field Descriptions

Bit	Field	Type	Reset	Description
7–5	RESERVED	R	0	RESERVED
4	INVALID CLOCK	R	0	**0: No clock fault detected** 1: Clock fault detected
3	PVDD OV	R	0	**0: No PVDD overvoltage fault detected** 1: PVDD overvoltage fault detected
2	VBAT OV	R	0	**0: No VBAT overvoltage fault detected** 1: VBAT overvoltage fault detected
1	PVDD UV	R	0	**0: No PVDD undervoltage fault detected** 1: PVDD undervoltage fault detected
0	VBAT UV	R	0	**0: No VBAT undervoltage fault detected** 1: VBAT undervoltage fault detected

9.6.14 Global Faults 2 Register (address = 0x12) [default = 0x00]

The Global Faults 2 register is shown in Figure 9-28 and described in Table 9-23.

Figure 9-28. Global Faults 2 Register

7	6	5	4	3	2	1	0
RESERVED			OTSD	CH1 OTSD	CH2 OTSD	RESERVED	RESERVED
R-000			R-0	R-0	R-0	R-0	R-0

Table 9-23. Global Faults 2 Field Descriptions

Bit	Field	Type	Reset	Description
7–5	RESERVED	R	000	RESERVED
4	OTSD	R	0	**0: No global overtemperature shutdown** 1: Global overtemperature shutdown
3	CH1 OTSD	R	0	**0: No overtemperature shutdown on Ch1** 1: Overtemperature shutdown on Ch1
2	CH2 OTSD	R	0	**0: No overtemperature shutdown on Ch2** 1: Overtemperature shutdown on Ch2
1	RESERVED	R	0	RESERVED
0	RESERVED	R	0	RESERVED

9.6.15 Warnings Register (address = 0x13) [default = 0x20]

The Warnings register is shown in Figure 9-29 and described in Table 9-24.

Figure 9-29. Warnings Register

7	6	5	4	3	2	1	0
RESERVED		VDD POR	OTW	OTW CH1	OTW CH2	RESERVED	RESERVED
		R-0	R-0	R-0	R-0	R-0	R-0

Table 9-24. Warnings Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0	RESERVED
5	VDD POR	R	0	0: No VDD POR has occurred **1 VDD POR occurred**
4	OTW	R	0	**0: No global overtemperature warning** 1: Global overtemperature warning
3	OTW CH1	R	0	**0: No overtemperature warning on channel 1** 1: Overtemperature warning on channel 1
2	OTW CH2	R	0	**0: No overtemperature warning on channel 2** 1: Overtemperature warning on channel 2
1	RESERVED	R	0	RESERVED
0	RESERVED	R	0	RESERVED

9.6.16 Pin Control Register (address = 0x14) [default = 0x00]

The Pin Control register is shown in Figure 9-30 and described in Table 9-25.

Figure 9-30. Pin Control Register

7	6	5	4	3	2	1	0
MASK OC	MASK OTSD	MASK UV	MASK OV	MASK DC	RESERVED	MASK CLIP	MASK OTW
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 9-25. Pin Control Field Descriptions

Bit	Field	Type	Reset	Description
7	MASK OC	R/W	0	**0: Report overcurrent faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report overcurrent faults on the $\overline{\text{FAULT}}$ Pin
6	MASK OTSD	R/W	0	**0: Report overtemperature faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report overtemperature faults on the $\overline{\text{FAULT}}$ pin
5	MASK UV	R/W	0	**0: Report undervoltage faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report undervoltage faults on the $\overline{\text{FAULT}}$ pin
4	MASK OV	R/W	0	**0: Report overvoltage faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report overvoltage faults on the $\overline{\text{FAULT}}$ pin
3	MASK DC	R/W	0	**0: Report DC faults on the $\overline{\text{FAULT}}$ pin** 1: Do not report DC faults on the $\overline{\text{FAULT}}$ pin
2	RESERVED	R/W	0	RESERVED
1	MASK CLIP	R/W	0	**0: Report clipping on the $\overline{\text{WARN}}$ pin** 1: Do not report clipping on the $\overline{\text{WARN}}$ pin **0: Report clipping on the configured pin ($\overline{\text{WARN}}$ or $\overline{\text{FAULT}}$)**
0	MASK OTW	R/W	0	**0: Report overtemperature warnings on the $\overline{\text{WARN}}$ pin** 1: Do not report overtemperature warnings on the $\overline{\text{WARN}}$ pin

9.6.17 AC Load Diagnostic Control 1 Register (address = 0x15) [default = 0x00]

The AC Load Diagnostic Control 1 register is shown in Figure 9-31 and described in Table 9-26.

Figure 9-31. AC Load Diagnostic Control 1 Register

7	6	5	4	3	2	1	0
CH1 GAIN	CH2 GAIN	RESERVED	RESERVED	CH1 ENABLE	CH2 ENABLE	RESERVED	RESERVED
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 9-26. AC Load Diagnostic Control 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	CH1, PBTL12: GAIN	R/W	0	**0: Gain 1** 1: Gain 4
6	CH2 GAIN	R/W	0	**0: Gain 1** 1: Gain 4
5	RESERVED	R/W	0	RESERVED
4	RESERVED	R/W	0	RESERVED
3	CH1 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics
2	CH2 ENABLE	R/W	0	**0: AC diagnostics disabled** 1: Enable AC diagnostics
1	RESERVED	R/W	0	RESERVED
0	RESERVED	R/W	0	RESERVED

9.6.18 AC Load Diagnostic Control 2 Register (address = 0x16) [default = 0x00]

The AC Load Diagnostic Control 2 register is shown in Figure 9-32 and described in Table 9-27.

Figure 9-32. AC Load Diagnostic Control 2 Register

7	6	5	4	3	2	1	0
AC_DIAGS_LOOPBACK	RESERVED		AC TIMING	AC CURRENT		RESERVED	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

Table 9-27. AC Load Diagnostic Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	AC_DIAGS_LOOPBACK	R/W	0	**0: Disable AC Diag loopback** 1: Enable AC Diag loopback
6-5	RESERVED	R/W	00	RESERVED
4	AC TIMING	R/W	0	**0: 32 Cycles** 1: 64 Cycles
3-2	AC CURRENT	R/W	00	**00: 10mA** 01: 19 mA 10: RESERVED 11: RESERVED
1-0	RESERVED	R/W	00	RESERVED

9.6.19 AC Load Diagnostic Impedance Report Ch1 through Ch2 Registers (address = 0x17–0x18) [default = 0x00]

The AC Load Diagnostic Report Ch1 through Ch2 registers are shown in Figure 9-33 and described in Table 9-28.

Figure 9-33. AC Load Diagnostic Impedance Report Chx Register

7	6	5	4	3	2	1	0
CHx IMPEDANCE							
R-00000000							

Table 9-28. Chx AC LDG Impedance Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	CH x IMPEDANCE	R	00000000	8-bit AC-load diagnostic report for each channel with a step size of 0.2496 Ω/bit (control by register 0x15 and register 0x16) **0x00: 0 Ω** 0x01: 0.2496 Ω ... 0xFF: 63.65 Ω

9.6.20 AC Load Diagnostic Phase Report High Register (address = 0x1B) [default = 0x00]

The AC Load Diagnostic Phase High value registers are shown in Figure 9-34 and described in Table 9-29.

Figure 9-34. AC Load Diagnostic (LDG) Phase High Report Register

7	6	5	4	3	2	1	0
AC Phase High							
R-00000000							

Table 9-29. AC LDG Phase High Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	AC Phase High	R	00000000	Bit 15:8

9.6.21 AC Load Diagnostic Phase Report Low Register (address = 0x1C) [default = 0x00]

The AC Load Diagnostic Phase Low value registers are shown in Figure 9-35 and described in Table 9-30.

Figure 9-35. AC Load Diagnostic (LDG) Phase Low Report Register

7	6	5	4	3	2	1	0
AC Phase Low							
R-00000000							

Table 9-30. AC LDG Phase Low Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	AC Phase Low	R	00000000	Bit 7:0

9.6.22 AC Load Diagnostic STI Report High Register (address = 0x1D) [default = 0x00]

The AC Load Diagnostic STI High value registers are shown in Figure 9-36 and described in Table 9-31.

Figure 9-36. AC Load Diagnostic (LDG) STI High Report Register

7	6	5	4	3	2	1	0
AC STI High							
R-00000000							

Table 9-31. AC LDG STI High Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	AC STI High	R	00000000	Bit 15:8

9.6.23 AC Load Diagnostic STI Report Low Register (address = 0x1E) [default = 0x00]

The AC Load Diagnostic STI Low value registers are shown in Figure 9-37 and described in Table 9-32.

Figure 9-37. AC Load Diagnostic (LDG) STI Low Report Register

7	6	5	4	3	2	1	0
AC STI Low							
R-00000000							

Table 9-32. Chx AC LDG STI Low Report Field Descriptions

Bit	Field	Type	Reset	Description
7–0	AC STI Low	R	00000000	Bit 7:0

9.6.24 Miscellaneous Control 3 Register (address = 0x21) [default = 0x00]

The Miscellaneous Control 3 register is shown in Figure 9-38 and described in Table 9-33.

Figure 9-38. Miscellaneous Control 3 Register

7	6	5	4	3	2	1	0
CLEAR FAULT	PBTL_CH_SEL	MASK ILIMIT WARNING	RESERVED	OTSD AUTO RECOVERY	RESERVED		
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			

Table 9-33. Misc Control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	CLEAR FAULT	R/W	0	**0: Normal operation** 1: Clear fault
6	PBTL_CH_SEL	R/W	0	**0: PBTL normal signal source** 1: PBTL flip signal source
5	RESERVED	R/W	0	RESERVED
4	RESERVED	R/W	0	RESERVED
3	OTSD AUTO RECOVERY	R/W	0	**0: OTSD is latched** 1: OTSD is autorecovery
2–0	RESERVED		0	RESERVED

9.6.25 Clip Control Register (address = 0x22) [default = 0x01]

The Clip Detect register is shown in and described in Table 9-34. To ensure the Clip Detect Warning is operating according to the expectation, the related bit values in the Section 9.6.26 and Section 9.6.27 must be set accordingly.

Figure 9-39. Clip Control Register

7	6	5	4	3	2	1	0
RESERVED					CLIP_PIN	CLIP_LATCH	CLIPDET_EN
R-00000					R/W-0	R/W-0	R/W-1

Table 9-34. Clip Control Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	00000	RESERVED
2	CLIP_PIN	R/W	0	**0: CH1-2 Clip Detect report to $\overline{\text{WARN}}$ pin** 1: Reserved
1	CLIP_LATCH	R/W	0	**0: Pin latching** 1: Pin non-latching
0	CLIPDET_EN	R/W	1	0: Clip Detect disable **1: Clip Detect Enable**

9.6.26 Clip Window Register (address = 0x23) [default = 0x14]

The Clip Window register is shown in Figure 9-40 and described in Table 9-35. The register value represents the minimum number of 100% duty-cycle PWM cycles in hexadecimal notation before Clip Detect is reported.

Figure 9-40. Clip Window Register

7	6	5	4	3	2	1	0
CLIP_WINDOW_SEL[7:1]							
R/W-00010100							

Table 9-35. Clip Window Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CLIP_WINDOW_SEL[7:1]	R/W	00010100	**00010100: 20-100% duty-cycle PWM cycles before Clip Detect is triggered**

9.6.27 Clip Warning Register (address = 0x24) [default = 0x00]

The Clip Window register is shown in Figure 9-41 and described in Table 9-36.

Figure 9-41. Clip Warning Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	CH2_CLIP	CH1_CLIP
				R-0	R-0	R-0	R-0

Table 9-36. Clip Warning Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED		0	RESERVED
3	RESERVED	R	0	RESERVED
2	RESERVED	R	0	RESERVED
1	CH2_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect
0	CH1_CLIP	R	0	**0: No Clip Detect** 1: Clip Detect

9.6.28 ILIMIT Status Register (address = 0x25) [default = 0x00]

The ILIMIT Status register is shown in Figure 9-42 and described in Table 9-37.

Figure 9-42. ILIMIT Status Register

7	6	5	4	3	2	1	0
RESERVED				RESERVED	RESERVED	CH2_ILIMIT_WARN	CH1_ILIMIT_WARN
				R-0	R-0	R-0	R-0

Table 9-37. ILIMIT Status Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED		0	RESERVED
3	RESERVED	R	0	RESERVED
2	RESERVED	R	0	RESERVED
1	CH2_ILIMIT_WARN	R	0	**0: No ILIMIT** 1: ILIMIT Warning
0	CH1_ILIMIT_WARN	R	0	**0: No ILIMIT** 1: ILIMIT Warning

9.6.29 Miscellaneous Control 4 Register (address = 0x26) [default = 0x40]

The Miscellaneous Control 4 register is shown in and described in Table 9-38.

Figure 9-43. Miscellaneous Control 4 Register

7	6	5	4	3	2	1	0
RESERVED				BCLK_INV	HPF_CORNER[2:0]		
R/W-0100				R/W-0	R/W-000		

Table 9-38. Misc Control 4 Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RESERVED	R/W	0100	RESERVED
3	BCLK_INV	R/W	0	**0: All other MCLK/BCLK frequency / phase use cases** 1: Inverted MCLK/BCLK phase relationship when MCLK/BCLK run at the same frequency
2-0	HPF_CORNER[2:0]	R/W	000	**000: 3.7 Hz** 001: 7.4 Hz 010: 15 Hz 011: 30 Hz 100: 59 Hz 101: 118 Hz 110: 235 Hz 111: 463 Hz

9.6.30 Miscellaneous Control 5 Register (address = 0x28) [default = 0x0A]

The Miscellaneous Control 5 register is shown in and described in Table 9-39.

Figure 9-44. Miscellaneous Control 5 Register

7	6	5	4	3	2	1	0
SS_BW_SEL	SS_DIV2	PHASE_SEL_MSB	RESERVED				
R/W-0	R/W-0	R/W-0	R/W-01010				

Table 9-39. Misc Control 5 Field Descriptions

Bit	Field	Type	Reset	Description
7	SS_BW_SEL	R/W	0	Spread Spectrum Bandwidth Selection. Must be set to "1" when Spread Spectrum is enabled. **0: Spread Spectrum disabled** 1: Spread Spectrum enabled
6	SS_DIV2	R/W	0	Spread Spectrum Post Divider Control. Must be set to "1" when Spread Spectrum is enabled. **0: Spread Spectrum disabled** 1: Spread Spectrum enabled
5	PHASE_SEL_MSB	R/W	0	MSB of PHASE_SEL[2:0]. See Section 9.6.3 for LSB's for phase selection.
4-0	RESERVED	R/W	01010	RESERVED

9.6.31 Spread Spectrum Control 1 Register (address = 0x77) [default = 0x00]

The Miscellaneous Control 5 register is shown in Figure 9-45 and described in Table 9-40.

Figure 9-45. Spread-Spectrum Control Register

7	6	5	4	3	2	1	0
SS_EN	RESERVED						
R/W-0	R/W-0000000						

Table 9-40. Spread-Spectrum Control Field Descriptions

Bit	Field	Type	Reset	Description
7	SS_EN	R/W	0	Spread Spectrum Enable **0: Spread-Spectrum Disabled.** 1: Spread-Spectrum Enabled.
6-0	RESERVED	R/W	0000000	RESERVED

9.6.32 Spread Spectrum Control 2 Register (address = 0x78) [default = 0x3F]

The Spread Spectrum Control 2 register is shown in Figure 9-46 and described in Table 9-41.

Figure 9-46. Spread Spectrum Control 2 Register

7	6	5	4	3	2	1	0
RESERVED	SS_PRE_DIV[6:0]						
R/W-0	R/W-0111111						

Table 9-41. Spread Spectrum Control 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0	RESERVED
6-0	SS_PRE_DIV	R/W	0111111	Pre-divider control for spread spectrum

9.6.33 Spread Spectrum Control 3 Register (address = 0x79) [default = 0x00]

The Spread Spectrum Control 3 register is shown in Figure 9-47 and described in Table 9-42.

Figure 9-47. Spread Spectrum Control 3 Register

7	6	5	4	3	2	1	0
SS_STEP[7:0]							
R/W-00000000							

Table 9-42. Spread Spectrum Control 3 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SS_STEP[7:0]	R/W	00000000	Spread Spectrum frequency step size configuration

10 Application Information Disclaimer

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TAS6422E-Q1 is a two-channel class-D digital-input audio-amplifier design for use in automotive head units and external amplifier modules. The TAS6422E-Q1 incorporates the necessary functionality to perform in demanding OEM applications.

10.1.1 AM-Radio Band Avoidance

AM-radio frequency interference can be avoided by setting the switching frequency of the device above the AM band. The switching frequency options available are 38 f_s, 44 f_s, and 48 f_s. If the switch frequency cannot be set above the AM band, then use the two options of 8 f_s and 10 f_s. These options should be changed to avoid AM active channels.

10.1.2 Parallel BTL Operation (PBTL)

The device can drive more current-paralleling BTL channels on the load side of the LC output filter. For parallel operation, the parallel BTL mode, PBTL, must be used and the paralleled channels must have the same state in the state control register. If the two states are not aligned the device reports a fault condition.

To set the requested channels to PBTL mode the device must be in standby mode for the commands to take effect.

A load diagnostic is supported for PBTL channels. Paralleling on the device side of the LC output filter is not supported.

10.1.3 Demodulation Filter Design

The amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either fully off or fully on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. An LC demodulation filter is used to recover the audio signal. The filter attenuates the high-frequency components of the output signals that are out of the audio band. The design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N requirements, the selection of the inductors used in the output filter should be carefully considered.

10.1.4 Line Driver Applications

In many automotive audio applications, the same head unit must drive either a speaker (with several ohms of impedance) or an external amplifier input (with several kΩ of impedance). The design is capable of supporting both applications and has special line-drive gain and diagnostics. Coupled with the high switching frequency, the device is well suited for this type of application. Set the desired channel in line driver mode through I^2C register 0x00, the externally connected amplifier must have a differential impedance from 600 Ω to 4.7 kΩ for the DC line diagnostic to detect the connected external amplifier. Figure 10-1 shows the recommended external amplifier input configuration.

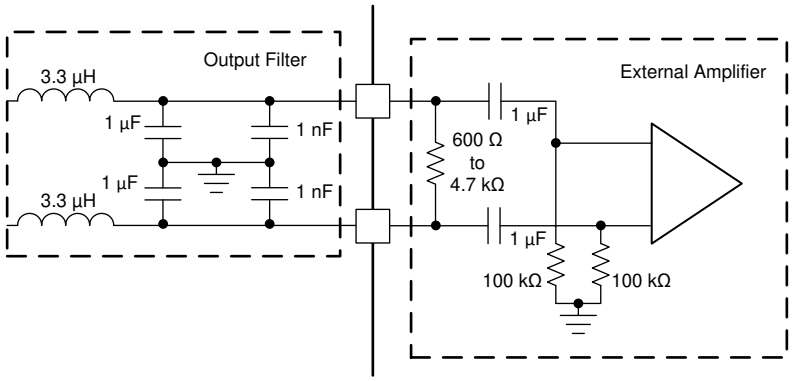


Figure 10-1. External Amplifier Input Configuration for Line Driver

10.2 Typical Applications

10.2.1 BTL Application

Figure 10-2 shows the schematic of a typical 2-channel solution for a head-unit application.

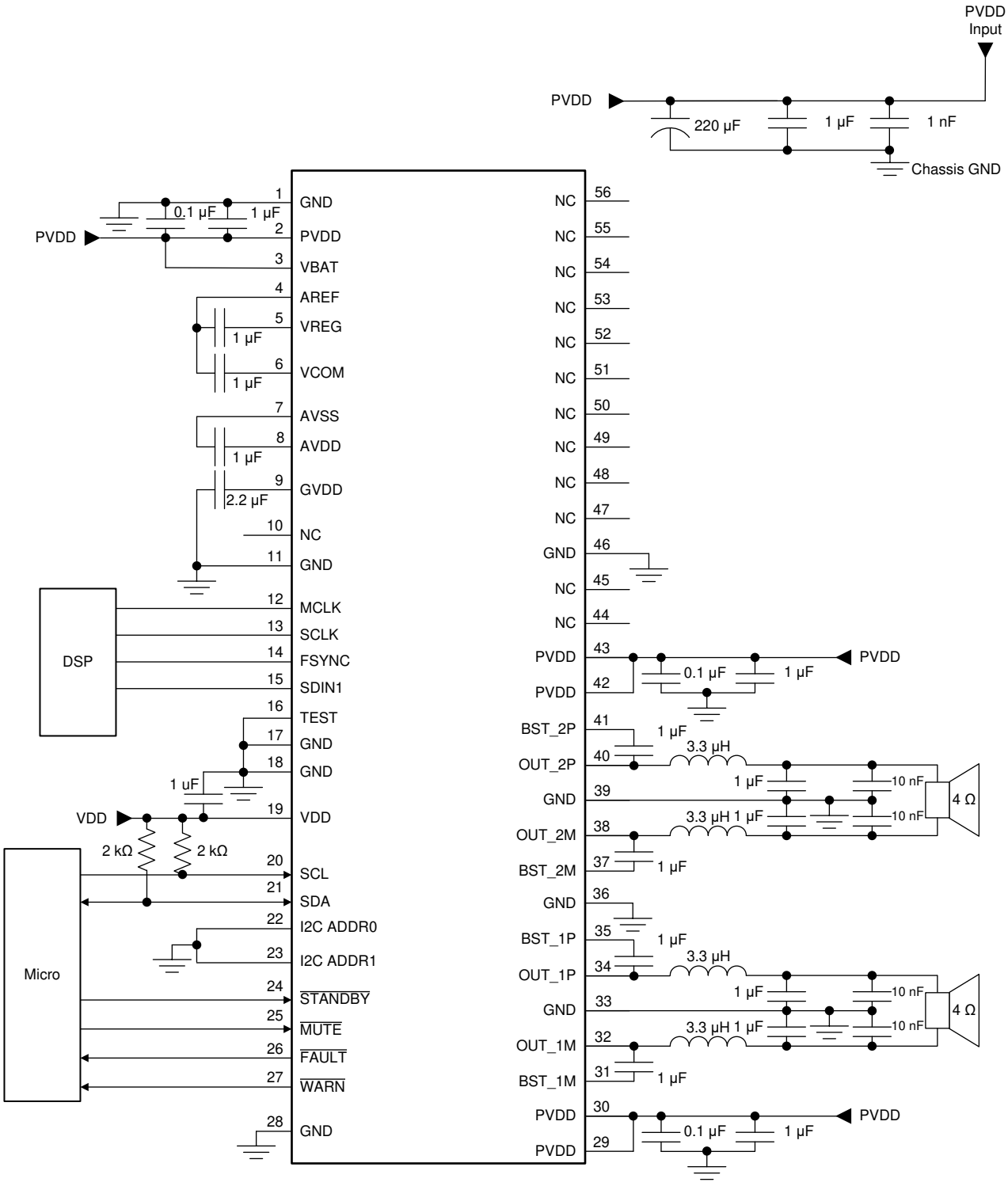


Figure 10-2. Typical 2-Channel BTL Application Schematic

10.2.1.1 Design Requirements

Use the following requirements for this design:

- This head-unit example is focused on the smallest solution size for 1 x 50 W output power into 2 Ω with a battery supply of 14.4 V.
- The switching frequency is set above the AM-band with 44 times the input sample rate of 48 kHz which results in a frequency of 2.11 MHz.
- The selection of a 2.11 MHz switch frequency enables the use of a small output inductor value of 3.3 µH which leads to a very small solution size.

10.2.1.1.1 Communication

All communications to the TAS6422E-Q1 are through the I^2C protocol. A system controller can communicate with the device through the SDA pins and SCL pins. The device is an I^2C slave and requires a master. The device cannot generate an I^2C clock or initiate a transaction. The maximum clock speed accepted by the device is 400 kHz. If multiple TAS6422E-Q1devices are on the same I^2C bus, the I^2C address must be different for each device. Up to four TAS6422E-Q1 devices can be on the same I^2C bus.

The I^2C bus is shared internally.

Note

Complete any internal operations, such as load diagnostics, before reading the registers for the results.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Hardware Design

Use the following procedure for the hardware design:

- Determine the input format. The input format can be either I^2S or TDM mode. The mode determines the correct pin connections and the I^2C register settings.
- Determine the power output that is required into the load. The power requirement determines the required power-supply voltage and current. The output reconstruction-filter components that are required are also driven by the output power.
- With the requirements, adjust the typical application schematic in Figure 10-2 for the input connections.

10.2.1.2.2 Digital Input and the Serial Audio Port

The TAS6422E-Q1 device supports four different digital input formats which are: I^2S, Right Justified, Left Justified, and TDM mode. Depending on the format, the device can support 16, 18, 20, 24, and 32 bit data. The supported frequencies are 96 kHz, 48 kHz, and 44.1 kHz. Please see SAP Control (Serial Audio-Port Control) Register (address = 0x03) for the complete matrix to set up the serial audio port.

Note

Bits 3, 4, and 5 in this register are ignored in all input formats except for TDM. Setting up all the control registers to the system requirements should be done before the device is placed in Mute mode or Play mode. After the registers are setup, use bit 7 in Miscellaneous Control 3 Register (address = 0x21) to clear any faults. Then read the fault registers to make sure no faults are present. When no faults are present, use *SAP Control Register (address = 0x03) [default = 0x04]* to place the device properly into Play mode.

10.2.1.2.3 Bootstrap Capacitors

The bootstrap capacitors provide the gate-drive voltage of the upper N-channel FET. These capacitors must be sized appropriately for the system specification. A special condition can occur where the bootstrap may sag if the capacitor is not sized accordingly. The special condition is just below clipping where the PWM is slightly less than 100% duty cycle with sustained low-frequency signals. Changing the bootstrap capacitor value to 2.2 µF for driving subwoofers that require frequencies below 30 Hz may be necessary.

10.2.1.2.4 Output Reconstruction Filter

The output FETs drive the amplifier outputs in an H-Bridge configuration. These transistors are either fully off or fully on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. The amplifier outputs require a reconstruction filter that comprises a series inductor and a capacitor to ground on each output, generally called an LC filter. The LC filter attenuates the PWM frequency and reduces electromagnetic emissions, allowing the reconstructed audio signal to pass to the speakers. refer to the *Class-D LC Filter Design Application Report*, (SLAA701A) for a detailed description of proper component description and design of the LC filter based upon the specified load and frequency response. The recommended low-pass cutoff frequency of the LC filter is dependent on the selected switching frequency. The low-pass cutoff frequency can be as high as 100 kHz for a PWM frequency of 2.1 MHz. At a PWM frequency of 384 kHz the low-pass cutoff frequency should be less than 40 kHz. Certain specifications must be understood for a proper inductor. The inductance value is given at zero current, but the device has current. Use the inductance versus current curve for the inductor to make sure the inductance does not drop below 1 µH (for f_{SW} = 2.1 MHz) at the maximum current provided by the system design. The DCR of the inductor directly affects the output power of the system design. The lower the DCR, the more power is provided to the speakers. The typical inductor DCR for a 4 Ω system is 40 to 50 mΩ and for a 2 Ω system is 20 to 25 mΩ. Further guidance is provided in the Inductor Selection Guide for 2.1 MHz Class-D Amplifiers.

10.2.2 PBTL Application

Figure 10-3 shows a schematic of a typical 1-channel solution for a head unit or external amplifier application where high power into 2 Ω is required.

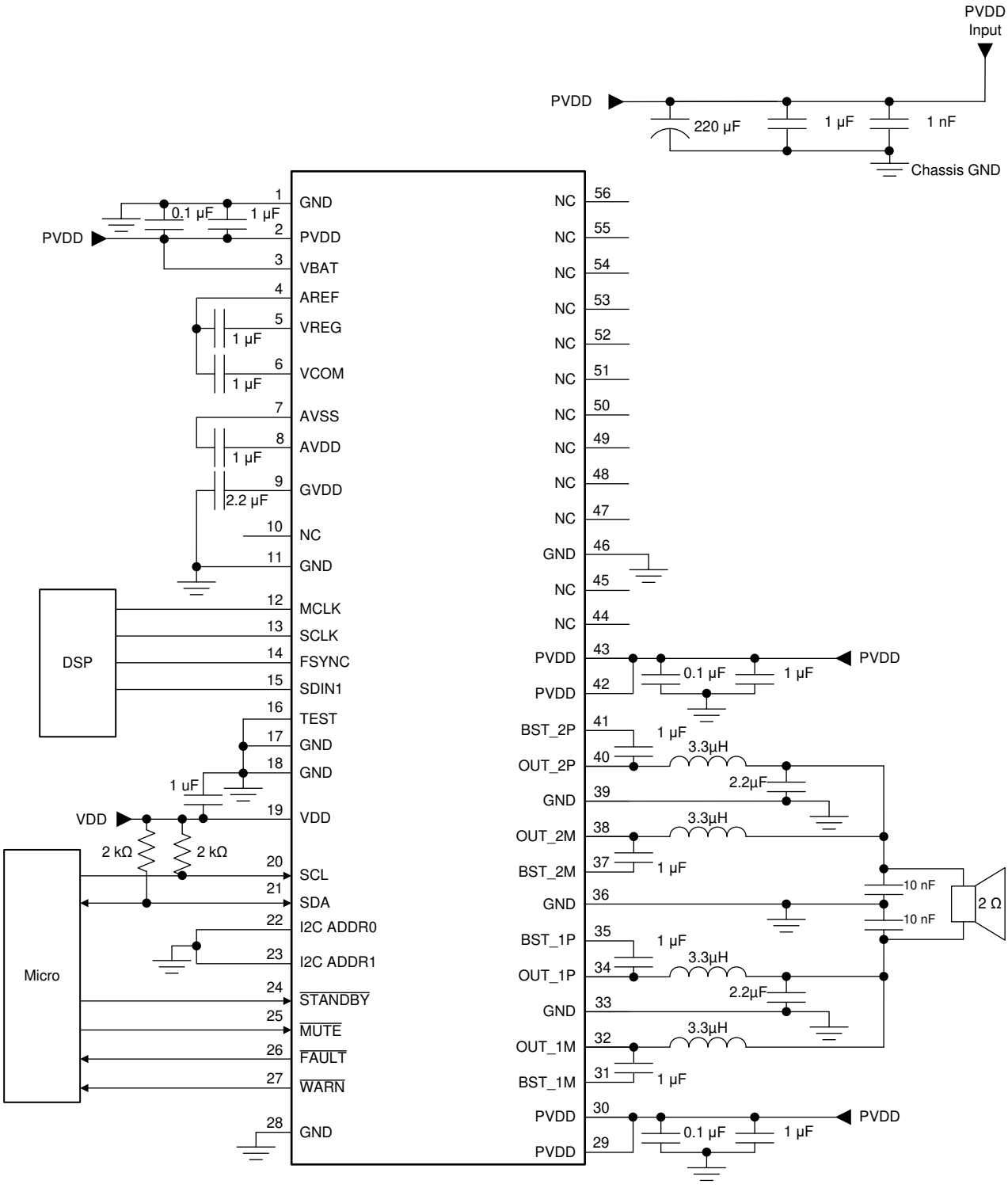


Figure 10-3. Typical 1-Channel PBTL Application Schematic

To operate in PBTL mode the output stage must be paralleled according to the schematic in Figure 10-3.

10.2.2.1 Design Requirements

Use the following requirements for this design:

- This head-unit example is focused on the smallest solution size for 1 x 50 W output power into 2 Ω with a battery supply of 14.4 V.
- The switching frequency is set above the AM-band with 44 times the input sample rate of 48 kHz which results in a frequency of 2.11 MHz.
- The selection of a 2.11 MHz switch frequency enables the use of a small output inductor value of 3.3 µH which leads to a very small solution size.

10.2.2.2 Detailed Design Procedure

As a starting point, refer to the section for the BTL application. PBTL mode requires schematic changes in the output stage as shown in Figure 10-3. The other required changes include setting up the I^2C registers correctly (see SAP Control Field Descriptions) and selecting which frame or channel to use on each output. Bit 6 in Miscellaneous Control 3 Register (address = 0x21) controls the frame selection.

11 Power Supply Recommendations

The TAS6422E-Q1 requires three power supplies. The PVDD supply is the high-current supply in the recommended supply range. The VBAT supply is lower current supply that must be in the recommended supply range. The PVDD and VBAT pins can be connected to the same supply if the recommended supply range for VBAT is maintained. The VDD supply is the 3.3 V_{dc} logic supply and must be maintained in the tolerance as shown in the *Recommended Operating Conditions* table.

For best device performance and to avoid unexpected device behavior follow the recommendations in the *Vehicle-Battery Power-Supply Sequence* section.

12 Layout

12.1 Layout Guidelines

The pinout of the TAS6422E-Q1 was selected to provide flowthrough layout with all high-power connections on the right side, and all low-power signals and supply decoupling on the left side.

Figure 12-1 shows the area for the components in the application example (see the *Typical Applications* *Typical Applications* section).

The TAS6422E-Q1 EVM uses a four-layer PCB. The copper thickness was selected as 70 µm to optimize power loss.

The small value of the output filter provides a small size and, in this case, the low height of the inductor enables double-sided mounting.

The EVM PCB shown in Figure 12-1 is the basis for the layout guidelines.

12.1.1 Electrical Connection of Thermal pad and Heat Sink

For the DKQ package, the heat sink connected to the thermal pad of the device should be connected to GND. The heat slug must not be connected to any other electrical node.

12.1.2 EMI Considerations

Automotive-level EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design. The design has minimal parasitic inductances because of the short leads on the package which reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase. The design also incorporates circuitry that optimizes output transitions that cause EMI.

For optimizing the EMI a solid ground layer plane is recommended, for a PCB design that fulfills the CISPR25 level 5 requirements, see the TAS6422E-Q1 EVM layout.

12.1.3 General Guidelines

The EVM layout is optimized for low noise and EMC performance.

The TAS6422E-Q1 has an exposed thermal pad that is up, away from the PCB. The layout must consider an external heat sink.

Refer to Figure 12-1 for the following guidelines:

- A ground plane, *A*, on the same side as the device pins helps reduce EMI by providing a very-low loop impedance for the high-frequency switching current.
- The decoupling capacitors on PVDD, *B*, are very close to the device with the ground return close to the ground pins.
- The ground connections for the capacitors in the LC filter, *C*, have a direct path back to the device and also the ground return for each channel is the shared. This direct path allows for improved common mode EMI rejection.
- The traces from the output pins to the inductors, *D*, should have the shortest trace possible to allow for the smallest loop of large switching currents.
- Heat-sink mounting screws, *E*, should be close to the device to keep the loop short from the package to ground.
- Many vias, *F*, stitching together the ground planes can create a shield to isolate the amplifier and power supply.

12.2 Layout Example

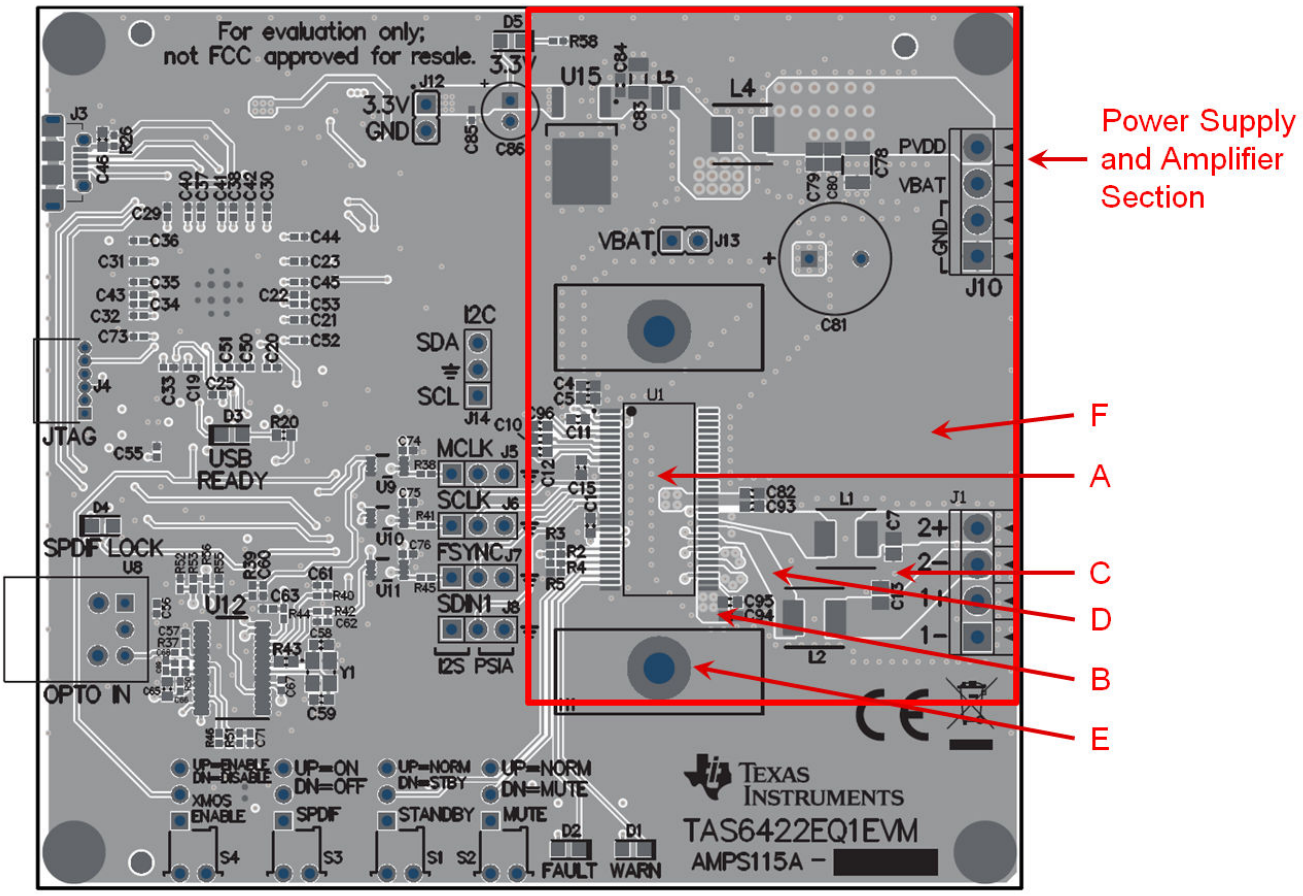


Figure 12-1. EVM Layout

12.3 Thermal Considerations

The thermally enhanced PowerPAD package has an exposed pad up for connection to a heat sink. The output power of any amplifier is determined by the thermal performance of the amplifier as well as limitations placed on it by the system, such as the ambient operating temperature. The heat sink absorbs heat from the TAS6422E-Q1 and transfers it to the air. With proper thermal management this process can reach equilibrium and heat can be continually transferred from the device. Heat sinks can be smaller than that of classic linear amplifier design because of the excellent efficiency of class-D amplifiers. This device is intended for use with a heat sink, therefore, $R_{\theta JC}$ is used as the thermal resistance from junction to the exposed metal package. This resistance dominates the thermal management, so other thermal transfers is not considered. The thermal resistance of $R_{\theta JA}$ (junction to ambient) is required to determine the full thermal solution. The thermal resistance is comprised of the following components:

- $R_{\theta JC}$ of the TAS6422E-Q1
- Thermal resistance of the thermal interface material
- Thermal resistance of the heat sink

The thermal resistance of the thermal interface material can be determined from the manufacturer's value for the area thermal resistance (expressed in °Cmm^2/W) and the area of the exposed metal package. For example, a typical, white, thermal grease with a 0.0254 mm (0.001 inch) thick layer is approximately 4.52°C mm^2/W. The TAS6422E-Q1 in the DKQ package has an exposed area of 47.6 mm^2. By dividing the area thermal resistance by the exposed metal area determines the thermal resistance for the thermal grease. The thermal resistance of the thermal grease is 0.094°C/W

Table 12-1 lists the modeling parameters for one device on a heat sink. The junction temperature is assumed to be 115°C while delivering and average power of 10 watts per channel into a 4 Ω load. The thermal-grease example previously described is used for the thermal interface material. Use Equation 1 to design the thermal system.

$$R_{\theta JA} = R_{\theta JC} + \text{thermal interface resistance} + \text{heat sink resistance} \quad (1)$$

Table 12-1. Thermal Modeling

Description	Value
Ambient Temperature	25°C
Average Power to load	20W (2 x 10W)
Power dissipation	4W (2 x 2W)
Junction Temperature	115°C
ΔT inside package	3.2°C (0.8°C/W × 4W)
ΔT through thermal interface material	0.38°C (0.094°C/W × 4W)
Required heat sink thermal resistance	21.6°C/W ([115°C – 25°C – 3.2°C – 0.38°C] / 4W)
System thermal resistance to ambient $R_{\theta JA}$	22.49°C/W (0.8°C/W + 0.094°C/W + 21.6°C/W)

13 Device and Documentation Support

13.1 Documentation Support

13.2 Related Documentation

For related documentation see the following:

- *PurePath™ Console 3* Graphical Development Suite
- TAS6422E-Q1 EVM User's Guide (SLOU541)

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

PurePath™ is a trademark of Texas Instruments.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS6422EQDKQRQ1	ACTIVE	HSSOP	DKQ	56	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS 6422E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

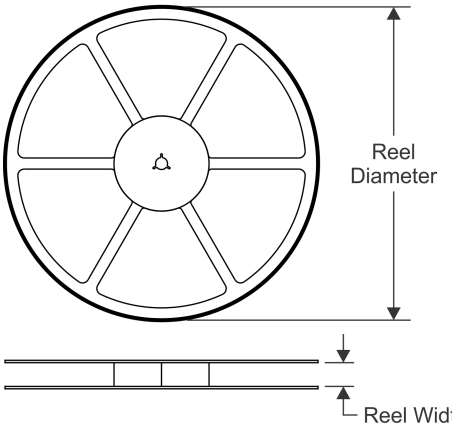
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

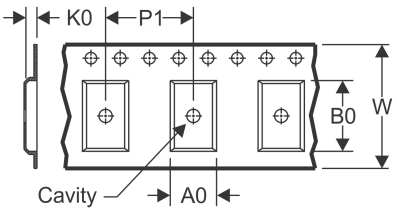
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

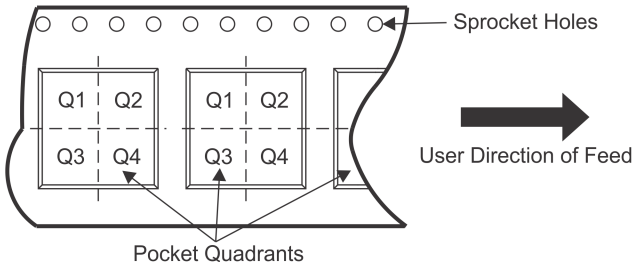


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

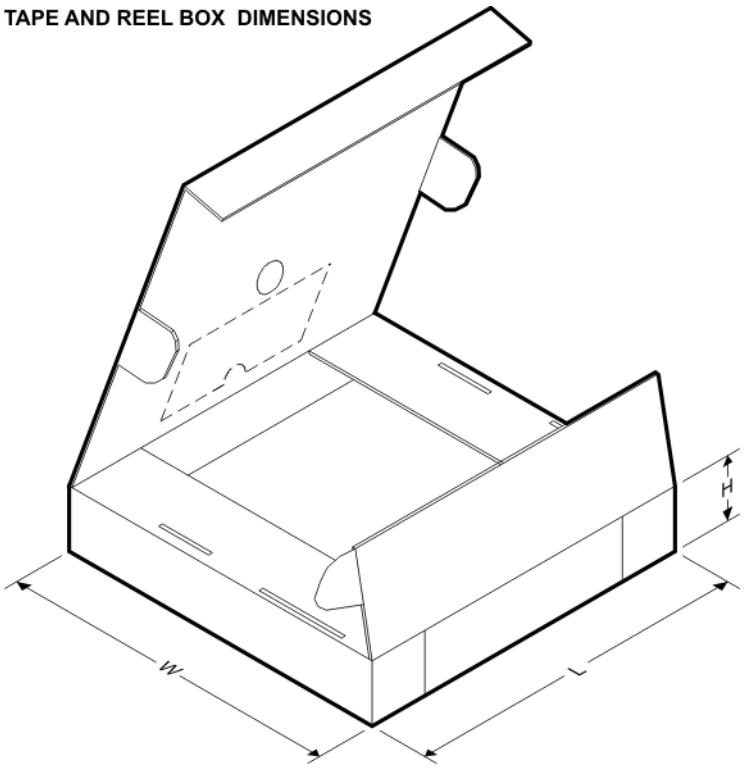
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS6422EQDKQRQ1	HSSOP	DKQ	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

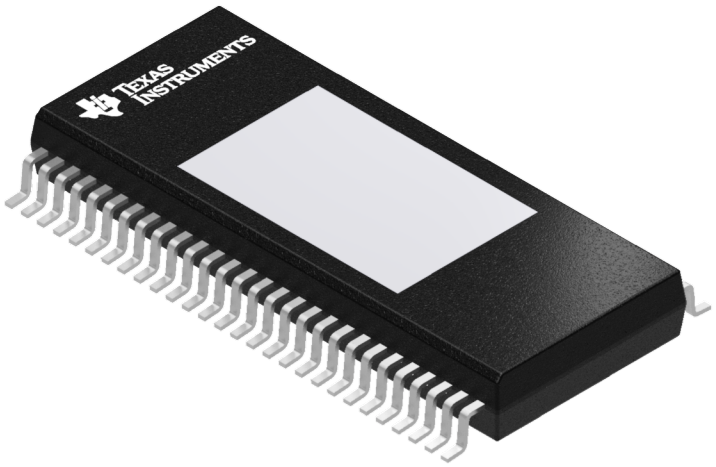


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS6422EQDKQRQ1	HSSOP	DKQ	56	1000	367.0	367.0	55.0

DKQ 56 PowerPAD™ SSOP - 2.34 mm max height

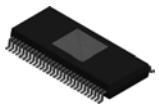
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

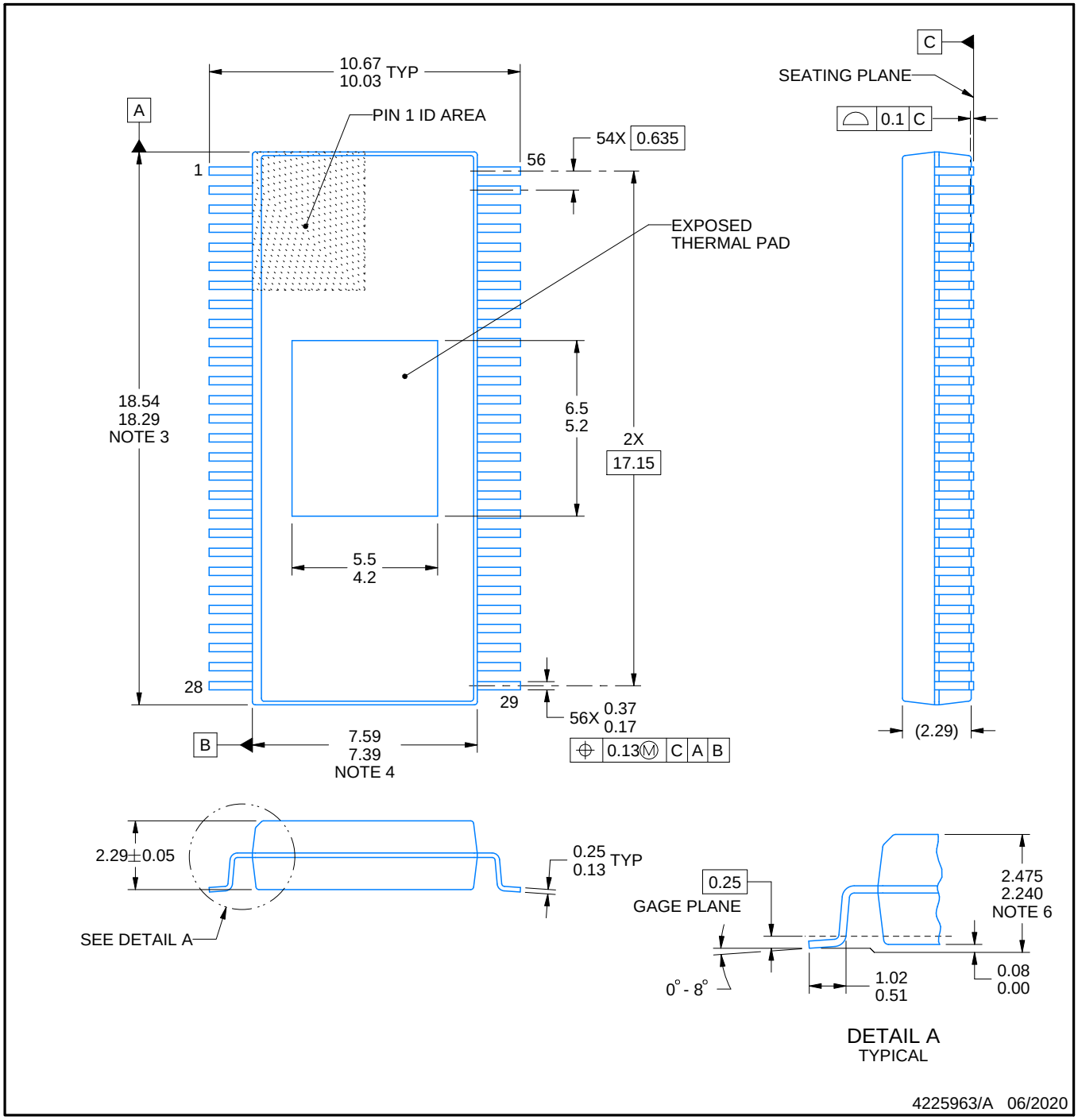
PACKAGE OUTLINE

DKQ0056C



PowerPAD™ HSSOP - 2.475 mm max height

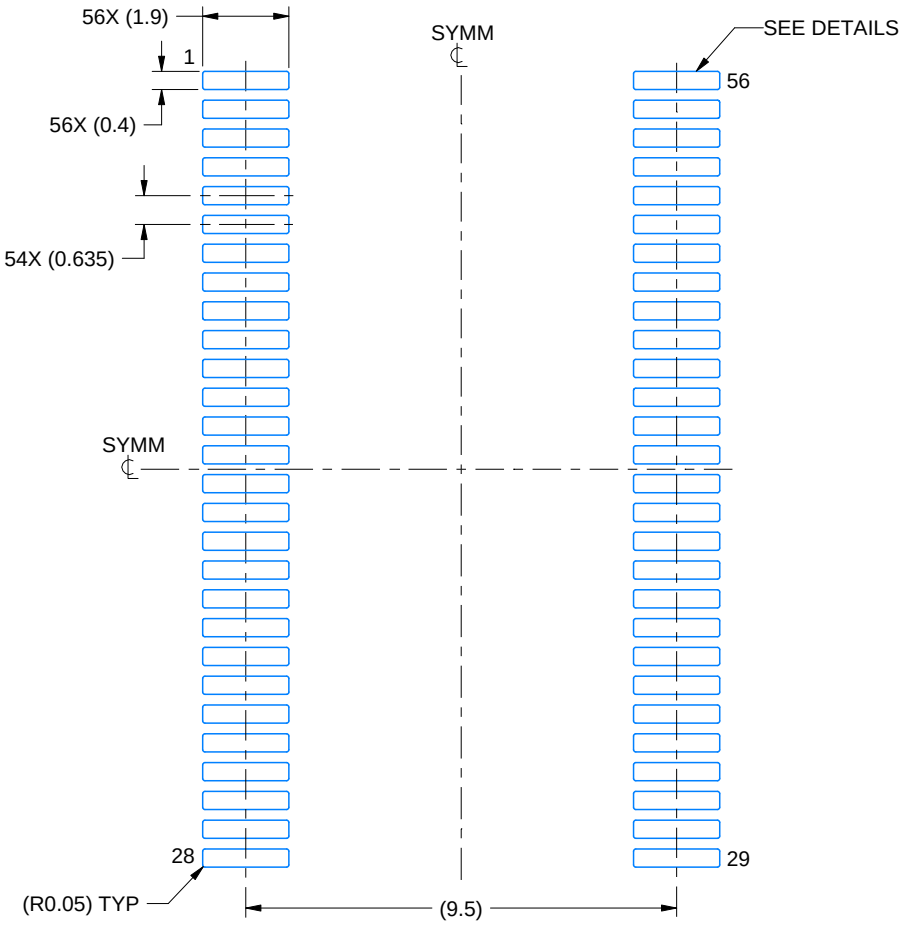
PLASTIC SMALL OUTLINE



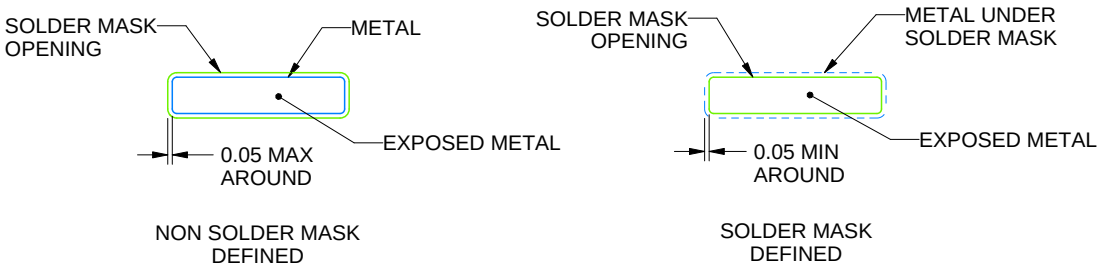
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. For clamped heatsink design, refer to overall package height above the seating plane as 2.325 +/- 0.075 and molded body thickness dimension.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS
NOT TO SCALE

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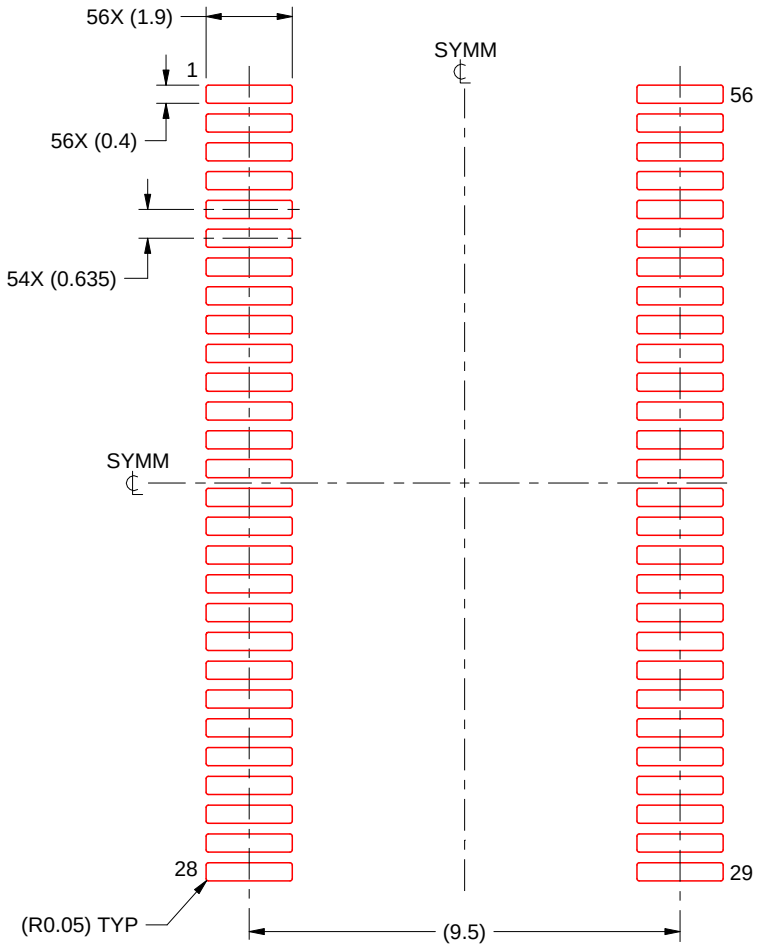
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE:6X

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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