



# CUSTOMER ADVISORY

## ADV2217

### Intel® Agilex™ Device Update

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#### Description:

Intel® is notifying customers of an important update to the Intel® Agilex™ devices.

Table 1

Problem Statement	Resolution
<ul style="list-style-type: none"><li>• Due to a problem in the Intel® Quartus® Prime Pro Edition Software version 21.1 and later, dedicated HPS output pins may be incorrectly mapped to pin locations during the Fitter stage.</li><li>• This may cause a mismatch between the pin locations defined in the HPS IP parameter GUI in Platform Designer and the pinout file generated during compilation, and unexpected behavior at runtime.</li></ul>	<p><b>Link to KDB:</b> <a href="#">Why do I see unexpected behavior on dedicated HPS IOs for my Intel® Agilex™ SoC FPGA design, and incorrect pin locations in the pinout report?</a></p> <ul style="list-style-type: none"><li>• Add pin location assignments to the HPS output pins in the .qsf file according to the HPS IP parameter GUI in Platform Designer OR</li><li>• Use the Assignment Editor in Intel® Quartus® Prime Pro Software to force the Fitter to place HPS outputs in designated pin locations.</li></ul> <p>This problem is scheduled to be fixed in a future release of the Intel® Quartus® Prime Pro Software.</p>

## Recommended Actions:

Customers are requested to review the changes and determine the impact on their designs. Refer to the relevant KDB link in Table 1.

For questions or support, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:

<https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html>

## Products Affected:

All Intel Agilex devices.

The list of affected part numbers (OPNs) can be downloaded in Excel form:

<https://www.intel.com/content/dam/support/us/en/programmable/support-resources/bulk-container/pdfs/literature/pcn/pcn2217-opn-list.xlsx>

## Contact:

For more information, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:

<https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html>

## Customer Notifications Subscription:

If you would like to receive customer notifications by email, please follow the instructions in [ADV 2209](#)

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*Intel references J-STD-046 guidelines for PCN.*

*In accordance with J-STD-046, this change is deemed acceptable to the customer if no acknowledgement is received within 30 days from date of notification.*

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## Revision History

Date	Rev	Description
7/15/2022	1.0.0	Initial Release

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