

Click [here](#) for the 3D model.

### Dimensions

Footprint	5634
L	5.59mm +/-0.38mm
W	3.43mm +/-0.38mm
H	1.78mm +/-0.38mm
S	0.76mm +0.25/-0.13mm
F	3.3mm +/-0.13mm
K	1.02mm MIN
P	0.51mm MIN

### Packaging Specifications

Packaging	T&R, 178mm
Packaging Quantity	500

### General Information

Series	T497 HRA
Dielectric	MnO <sub>2</sub> Tantalum
Style	SMD Chip
Description	SMD, MnO <sub>2</sub> , Molded, High Reliability, Medical
Features	High Reliability, Medical
RoHS	No
Prop 65	<b>⚠ WARNING:</b> Cancer and reproductive harm - <a href="http://www.p65warnings.ca.gov">http://www.p65warnings.ca.gov</a> .
SCIP Number	1dd2e1b8-26dd-4d52-927c-6f9d519011aa
Termination	Solder Coated
Qualifications	CWR09/19/29 Style
AEC-Q200	No
Component Weight	173.63 mg
Notes	Note: When solder coated terminations are required, add an additional 0.38mm (0.015inch) to the tolerances for "L", "W", "H", "K", "F" and "S".
MSL	1

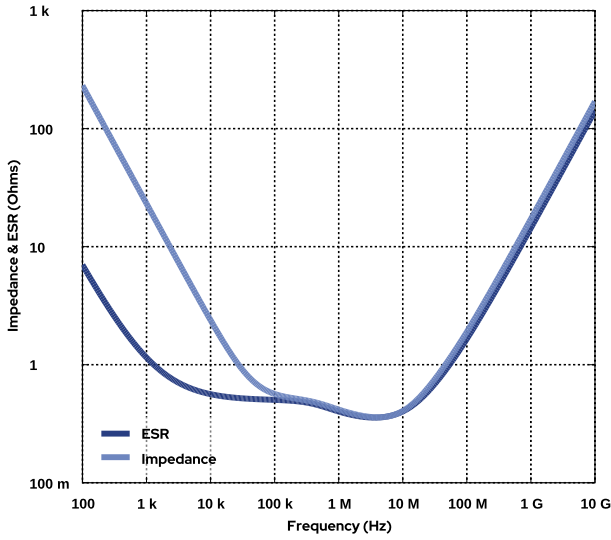
### Specifications

Capacitance	6.8 uF
Capacitance Tolerance	10%
Voltage DC	25 VDC (85C), 16.75 VDC (125C)
Temperature Range	-55/+125°C
Rated Temperature	85°C
Humidity	85C, 85% RH, 1000 Hours, No Load
Dissipation Factor	6% 120Hz 25C
Failure Rate	N/A
Resistance	3 Ohms (100kHz 25C)
Ripple Current	183 mA (rms, 100kHz 25C)
Leakage Current	1.7 uA (5min 25°C)
Testing and Reliability	Standard Testing Only

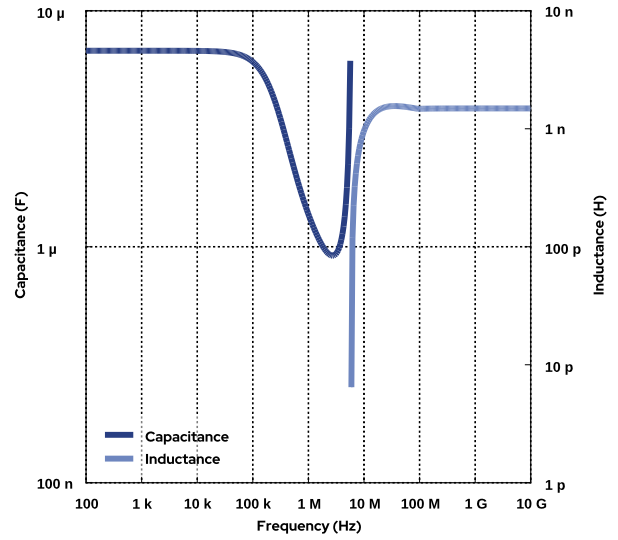
## Simulations

For the complete simulation environment please visit [K-SIM](#).

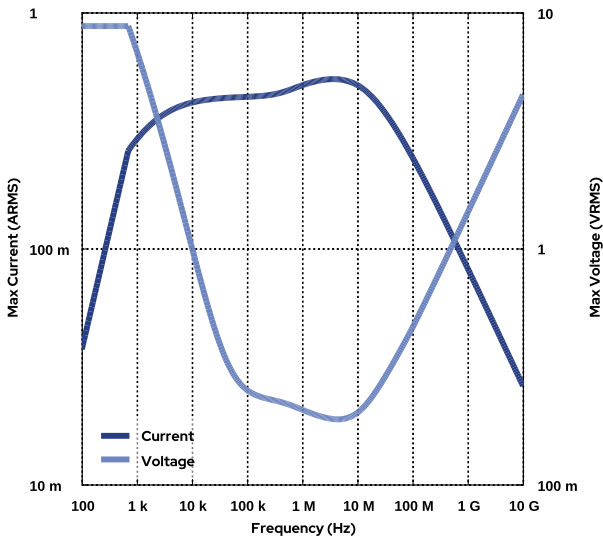
**Impedance and ESR**



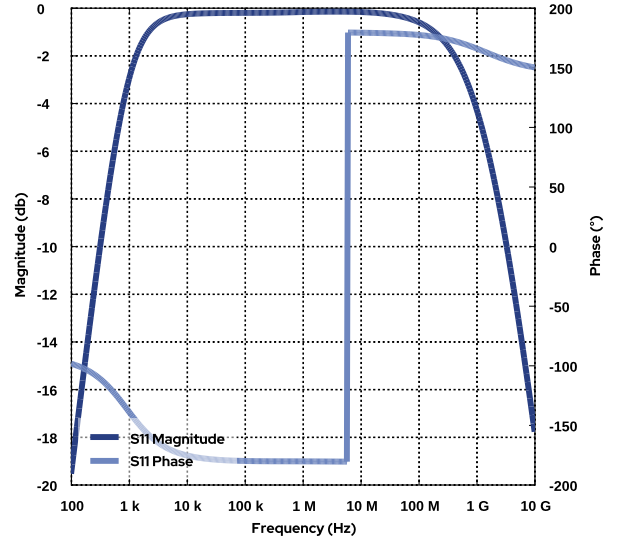
**Capacitance and Inductance**

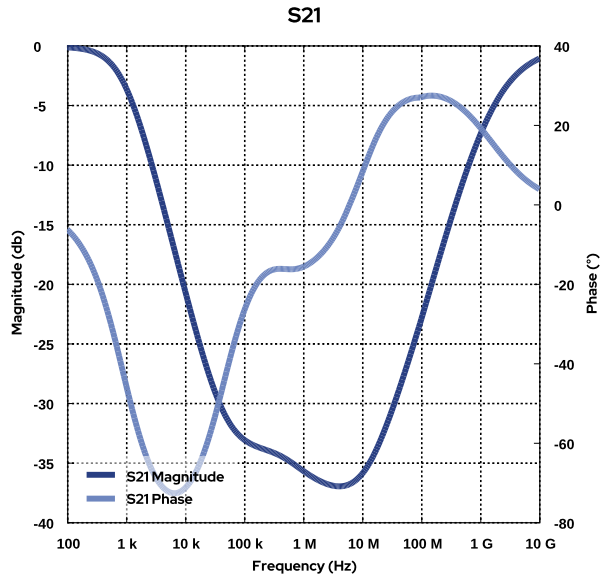


**Current and Voltage**



**S11**





**These are simulations.**

This is not a specification!

The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

The responses shown do not represent a specified or implied maximum capability of the device for all applications.

- The ESR used for ripple "Ripple Current/Voltage vs. Frequency" plots is the ESR at ambient temperature.
- The ESR in the "Temperature Rise vs. Ripple Current" plots is adjusted to each incremental temperature rise before the power and ripple current is calculated.
- The effects shown herein are based on measured data from a multiple part sample of the parts in question.
- Ripple capability of this device will be factored by thermal resistance (Rth) created by circuit traces (addi affects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.
- The peak voltages generated in the "Temperature Rise vs. Combined Ripple Currents" plot are calculated for each frequency and are not combined with voltages generated at any other harmonics.
- Please consult with the catalog or field applications engineer for maximum capability of the device in specific applications.

All product information and data (collectively, the "Information") are subject to change without notice.

KEMET K-SIM is designed to simulate behavior of components with respect to frequency, ambient temperature, and DC bias levels. The responses shown represent the typical response for each part type. Specific responses may vary, depending on manufacturing variation effects of all parameters involved, including the specified tolerances applied to capacitance and unspecified variations of ESR, ESL, and leakage resistance.

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If you have any questions please contact K-SIM.