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U_DDR3-RAM
DDR3-RAM.SchDoc

U_Ethernet
Ethernet.SchDoc

U_USB-PHY
USB-PHY.SchDoc

U_SOC
SOC.SchDoc

U_CPLD
CPLD.SchDoc

U_POWER2
POWER2.SchDoc

U_HyperFlash_RAM
HyperFlash_RAM.SchDoc

U_Clock
Clock.SchDoc

U_eMMC
eMMC.SchDoc

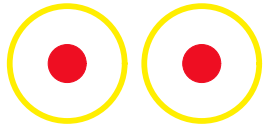
U_Connectors
Connectors.SchDoc

U_POWER
POWER.SchDoc

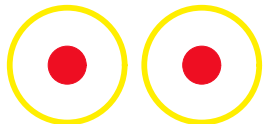
LOGO1

TE Logo PRINT Layer

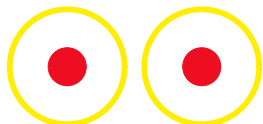
LOGO PRINT



PM1 PM2




PM3 PM4



PM5 PM6

Serial
Serial
Serialnumber 6,3 x 6.3mm

		Title: TE0782 - Overview	
		A4	Number: TE0782 TE0782-02-100-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: TE0782.SchDoc		Page1 of 31	

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A

A

B

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C

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A

A

U_HSMC_CONN_J1
HSMC_CONN_J1.SchDoc



U_HSMC_CONN_J2
HSMC_CONN_J2.SchDoc



U_HSMC_CONN_J3
HSMC_CONN_J3.SchDoc



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		Title: TE0782 - Connectors	
		A4	Number: TE0782 TE0782-02-100-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: Connectors.SchDoc		Page2 of 31	

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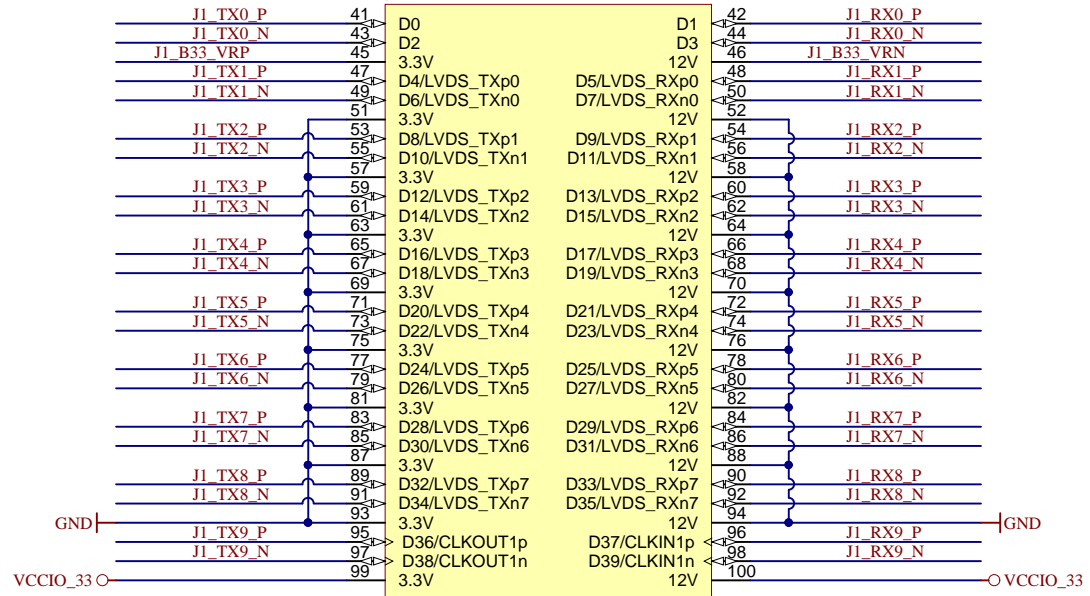
C

C

D

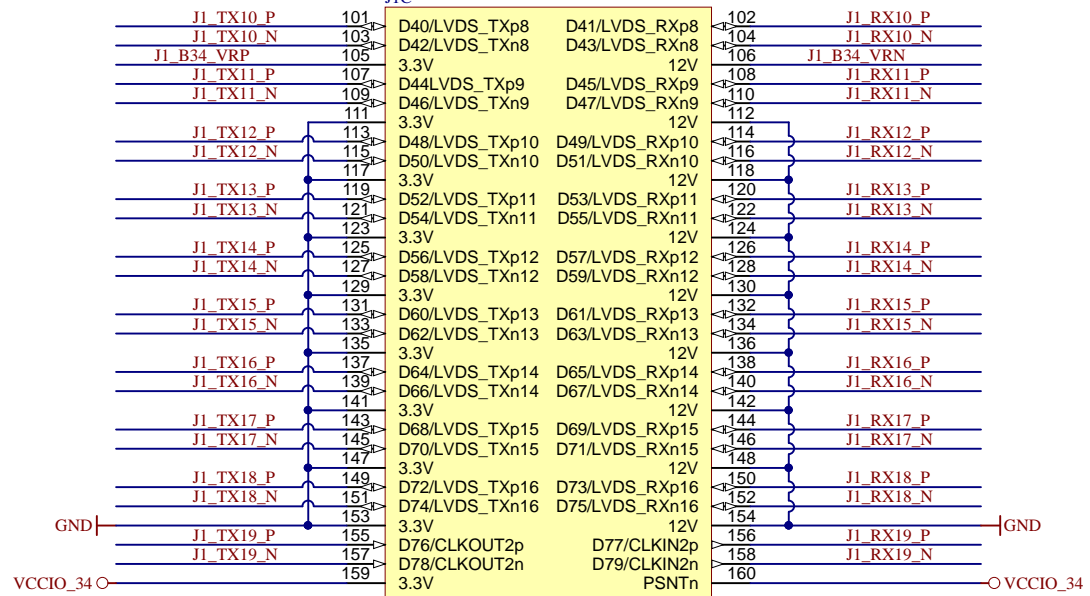
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J1B



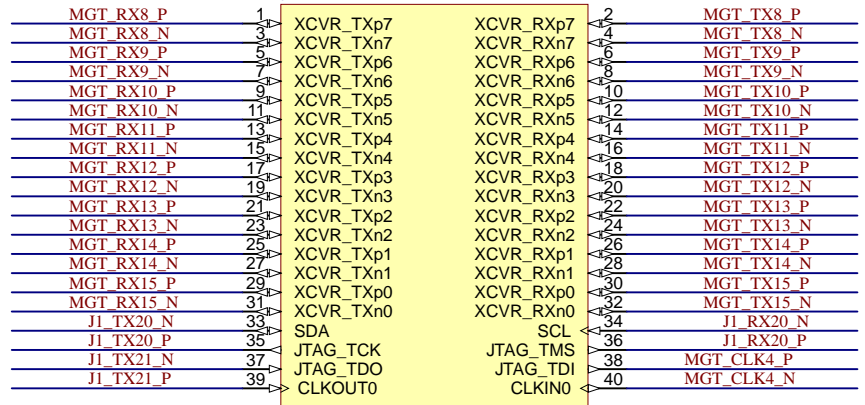
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J1C



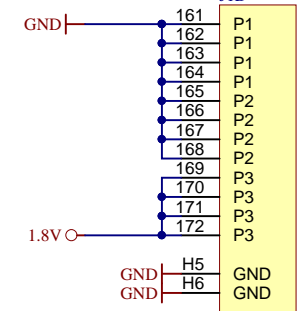
ASP-122952-01

J1A



ASP-122952-01

J1D



ASP-122952-01



Title: TE0782 - HSMC_Connector_J1		
A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page3 of 31
Filename: HSMC_CONN_J1.SchDoc		

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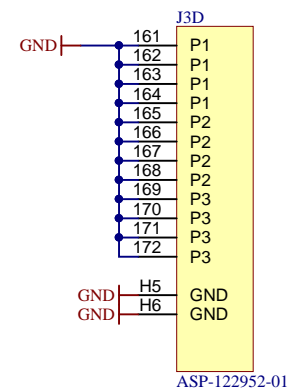
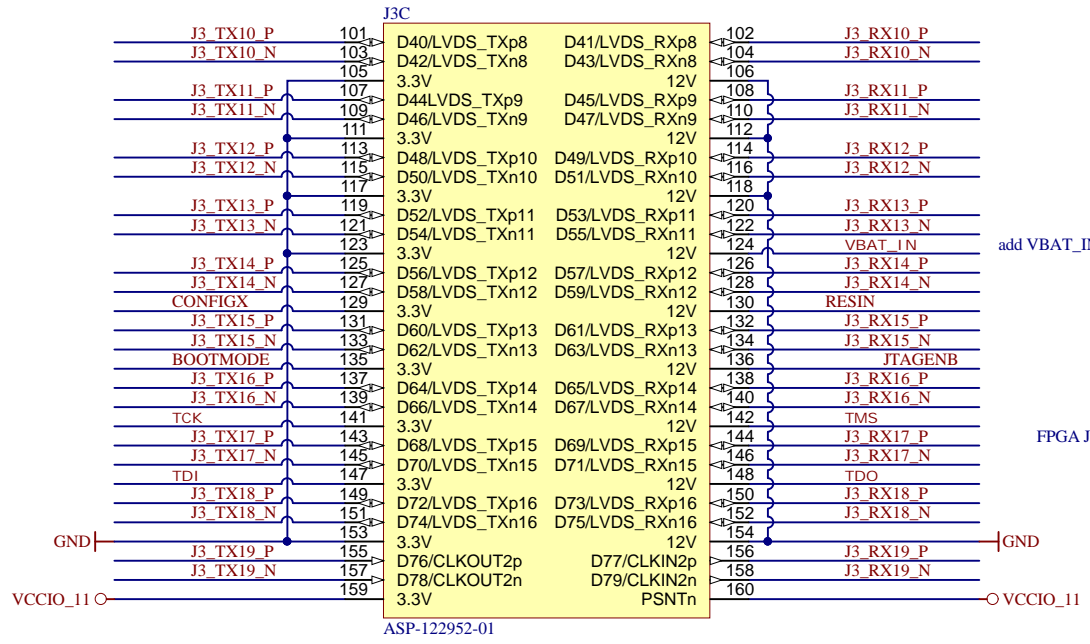
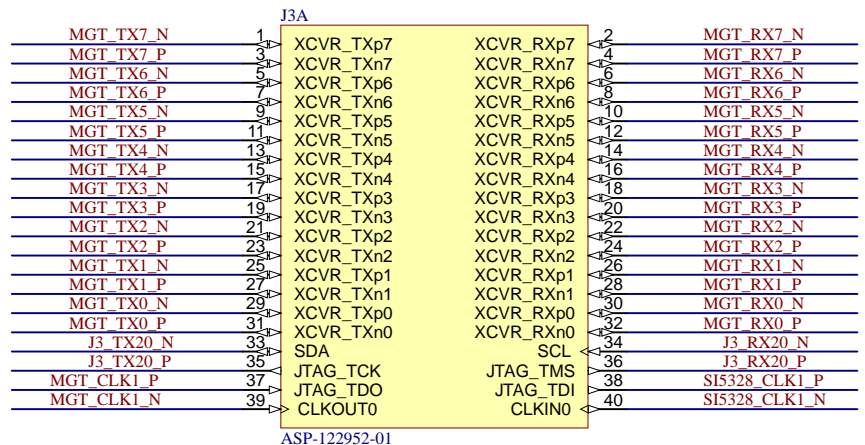
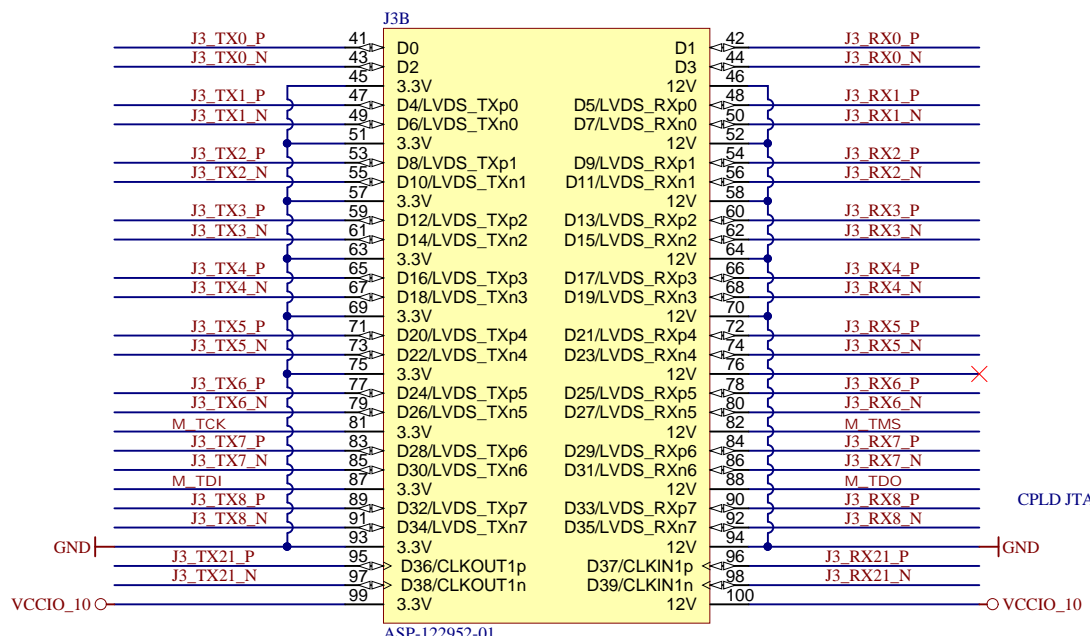
B

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Title: TE0782 - HSMC_Connector_J3		
A4	Number: TE0782 TE0782-02-100-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page4 of 31
Filename: HSMC_CONN_J3.SchDoc		

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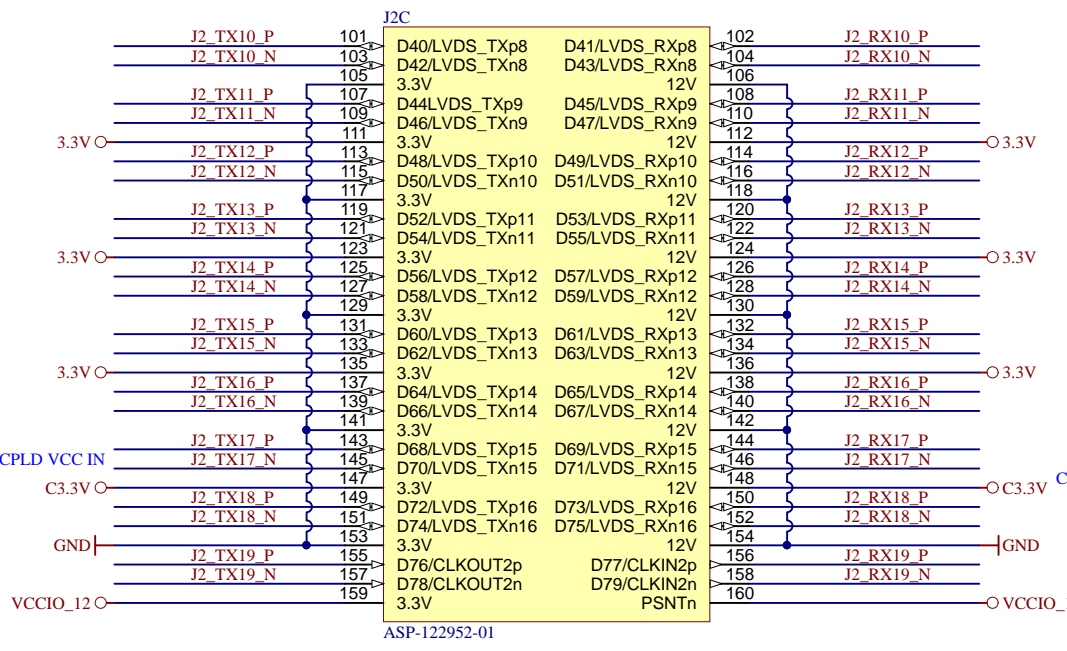
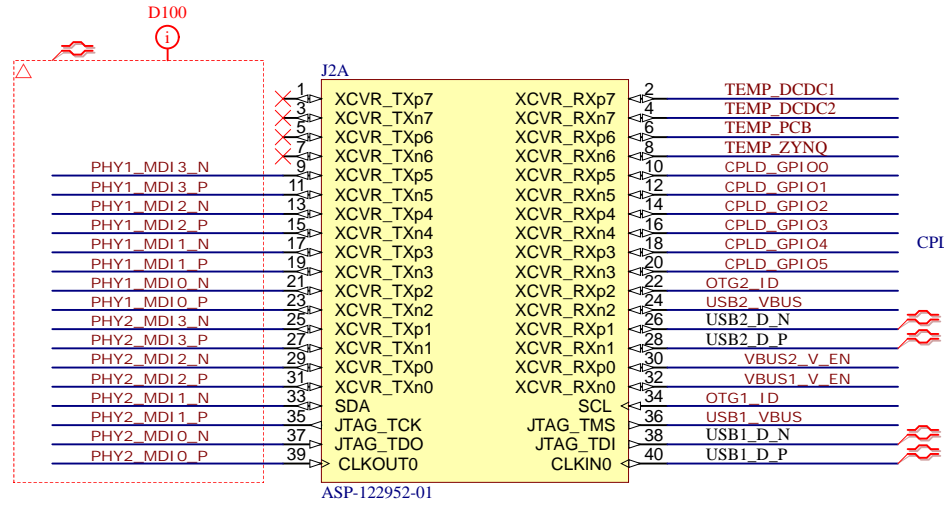
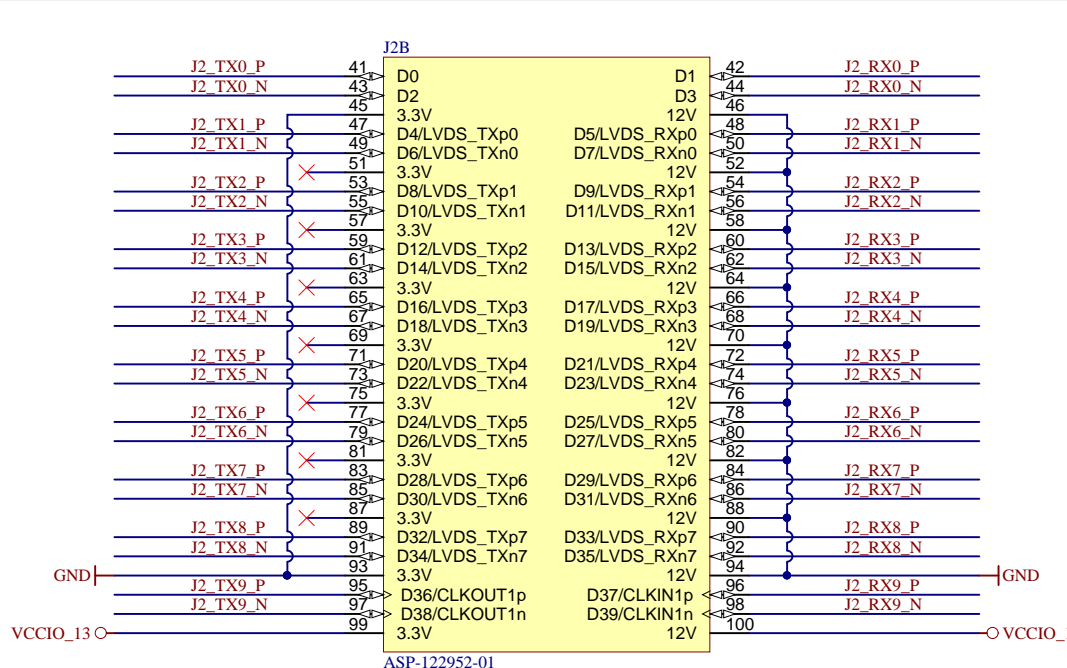
D

A

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Title: TE0782 - HSMC_Connector_J2		
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 5 of 31
Filename: HSMC_CONN_J2.SchDoc		

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A

A

U_PS-DDR
PS-DDR.SchDoc



U_B9
B9.SchDoc



U_MIO-BANKS
MIO-BANKS.SchDoc



U_B10
B10.SchDoc



U_HP-BANKS
HP-BANKS.SchDoc



U_B11
B11.SchDoc



B

B

U_FPGA-MGT
FPGA-MGT.SchDoc



U_B12
B12.SchDoc



U_FPGA-CFG
FPGA-CFG.SchDoc



U_B13
B13.SchDoc



C

C

U_FPGA-PWR
FPGA-PWR.SchDoc



D

D



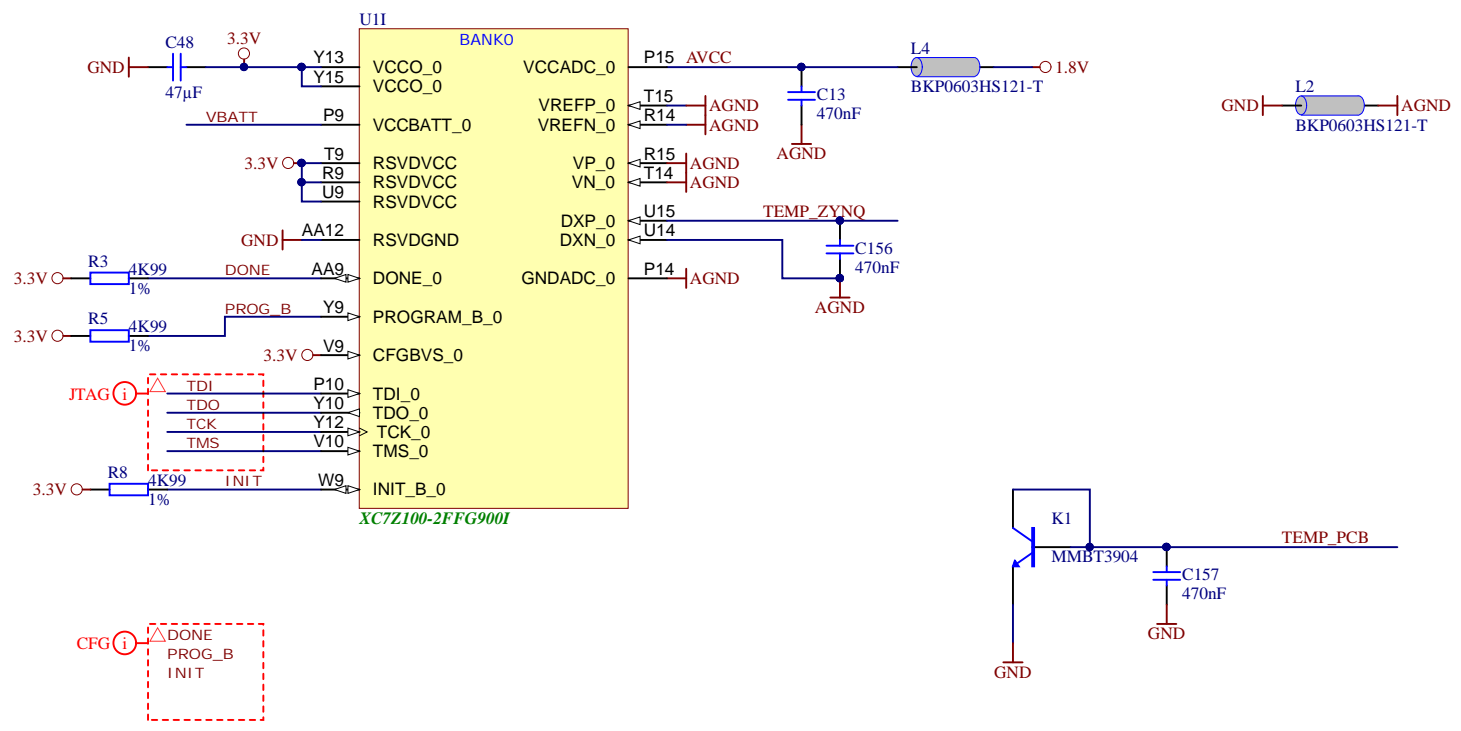
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 6 of 31
Filename: SOC.SchDoc		

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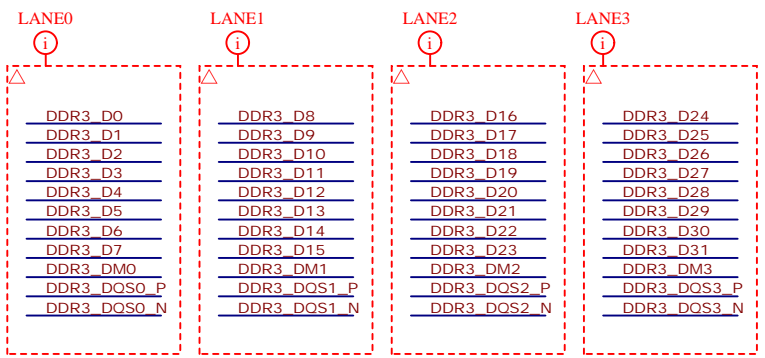
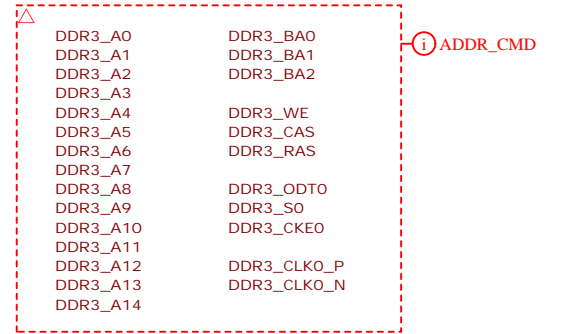
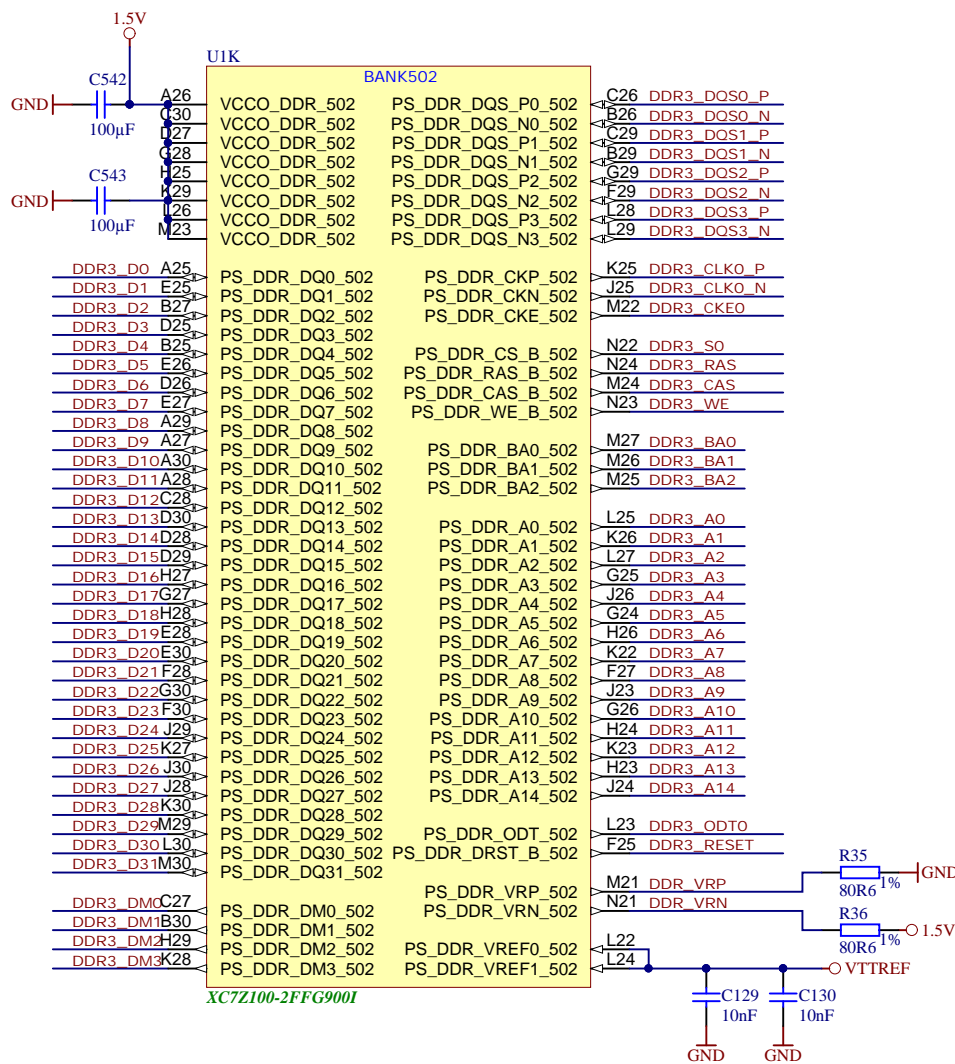
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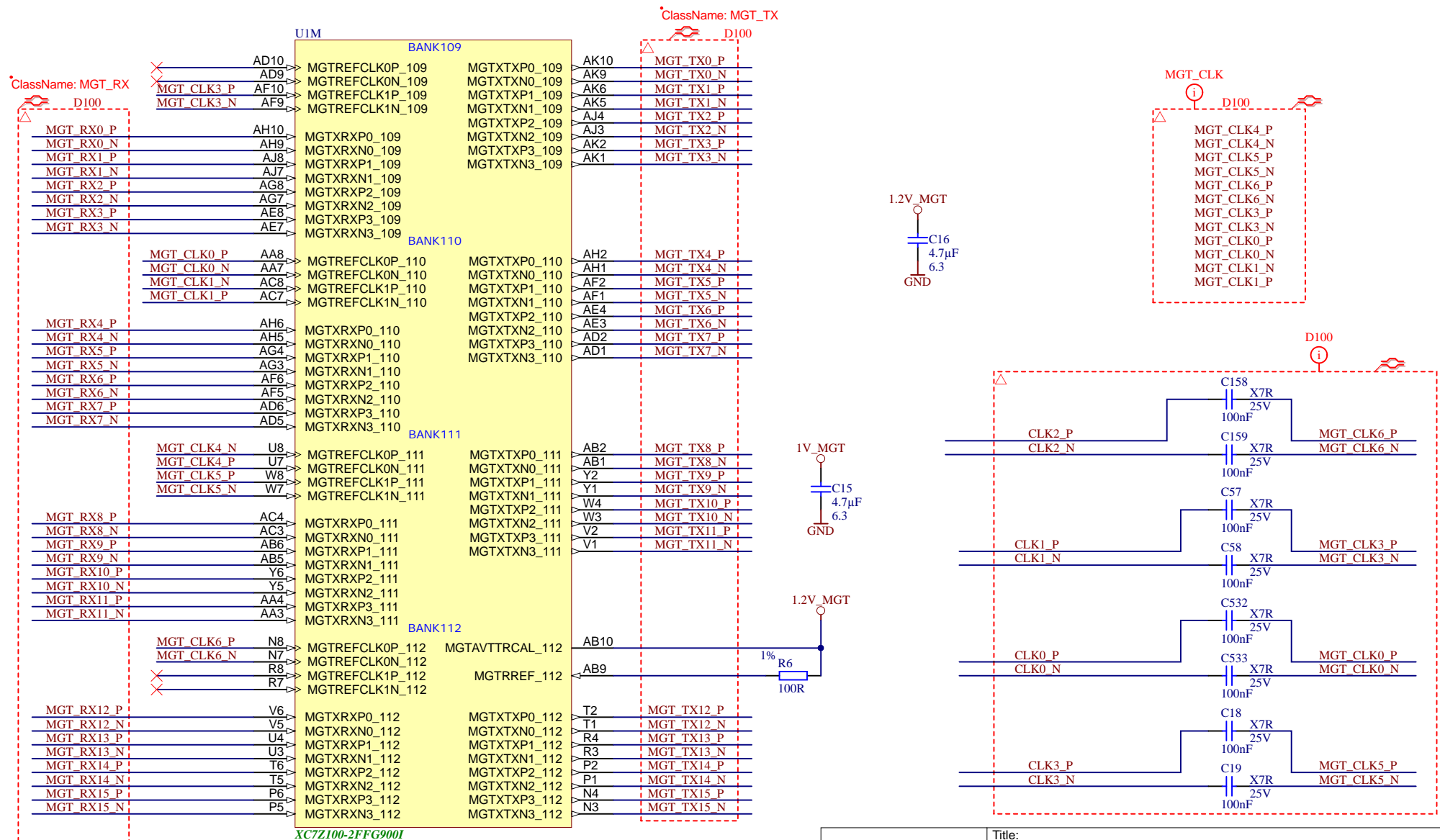
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Title: TE0782 - FPGA Configuration		
A4	Nummer: TE0782 TE0782-02-100-2I	Rev. 02
Datum: 2015-05-27	Zeichner: Trenz Electronic GmbH	Blatt 7 von 31
Filename: FPGA-CFG.SchDoc		



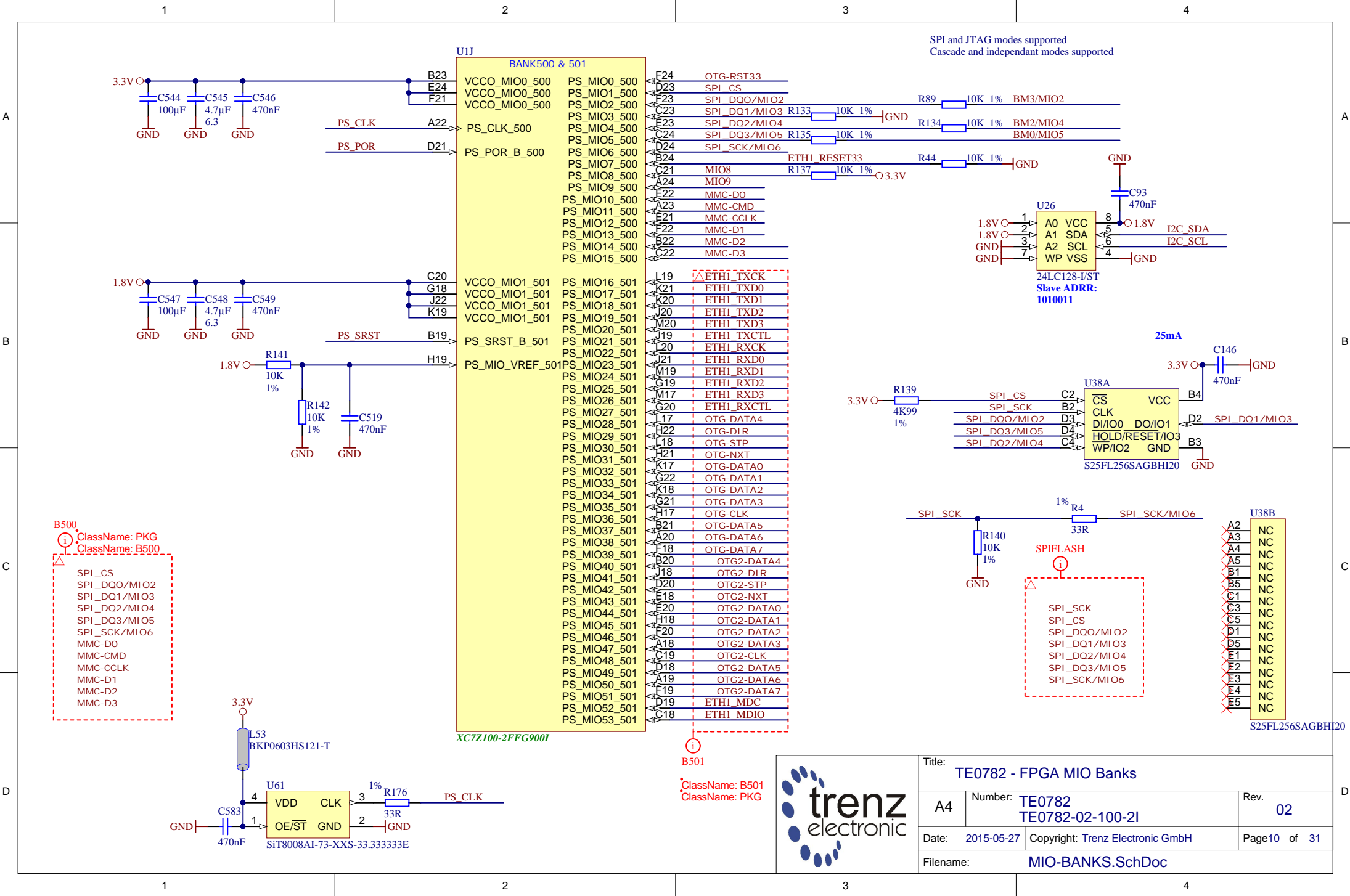
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		A4	Number: TE0782 TE0782-02-100-21
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: PS-DDR.SchDoc		Page 8 of 31	



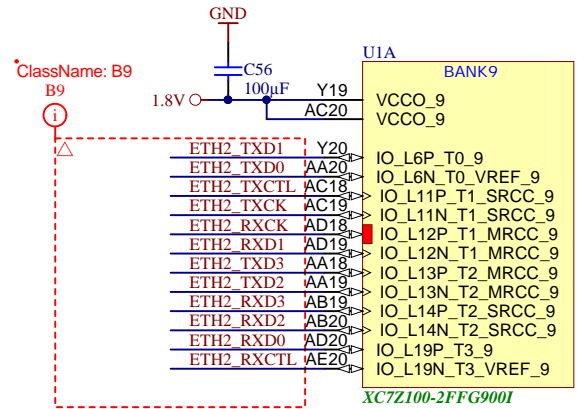
XC7Z100-2FFG9001




Title: TE0782 - FPGA MGT		
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page9 of 31
Filename: FPGA-MGT.SchDoc		



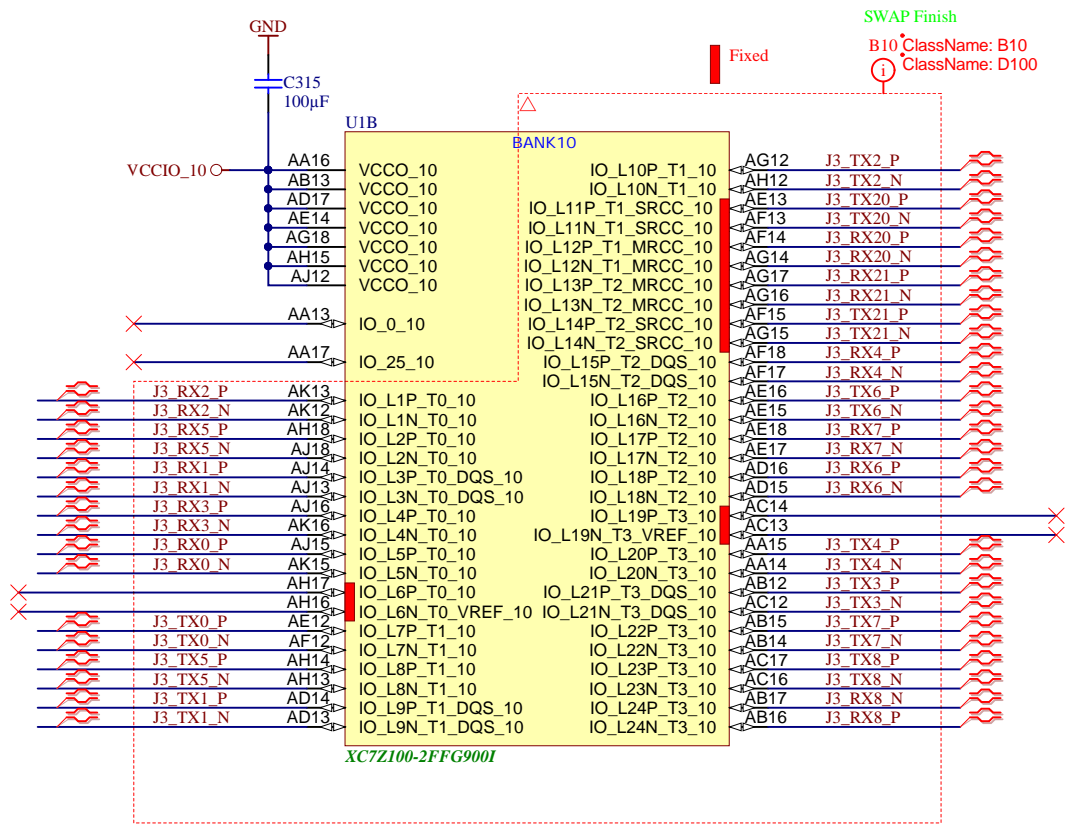
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A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 10 of 31
Filename: MIO-BANKS.SchDoc		



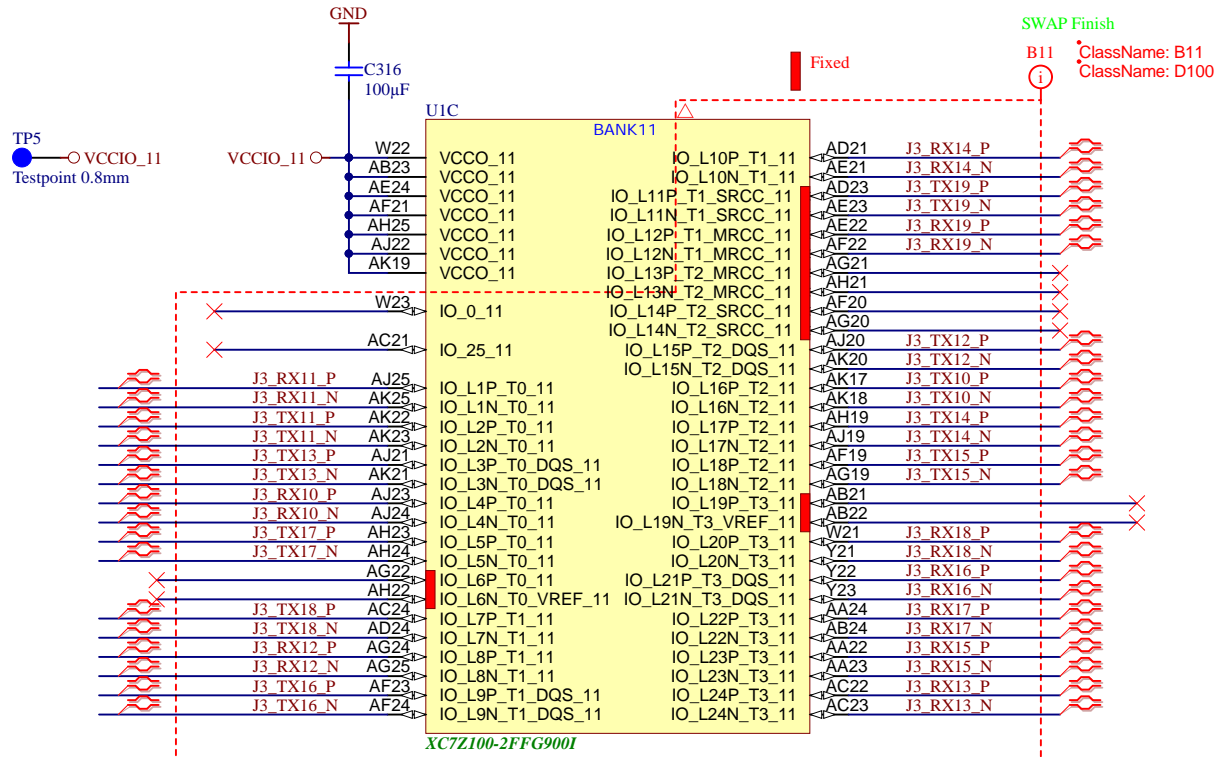
RXCK Fix to MRCCL
Fixed

			Title: TE0782 - FPGA B9		
			A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 11 of 31	
Filename: B9.SchDoc					


TP4
 ● VCCIO_10
 ○ Testpoint 0.8mm

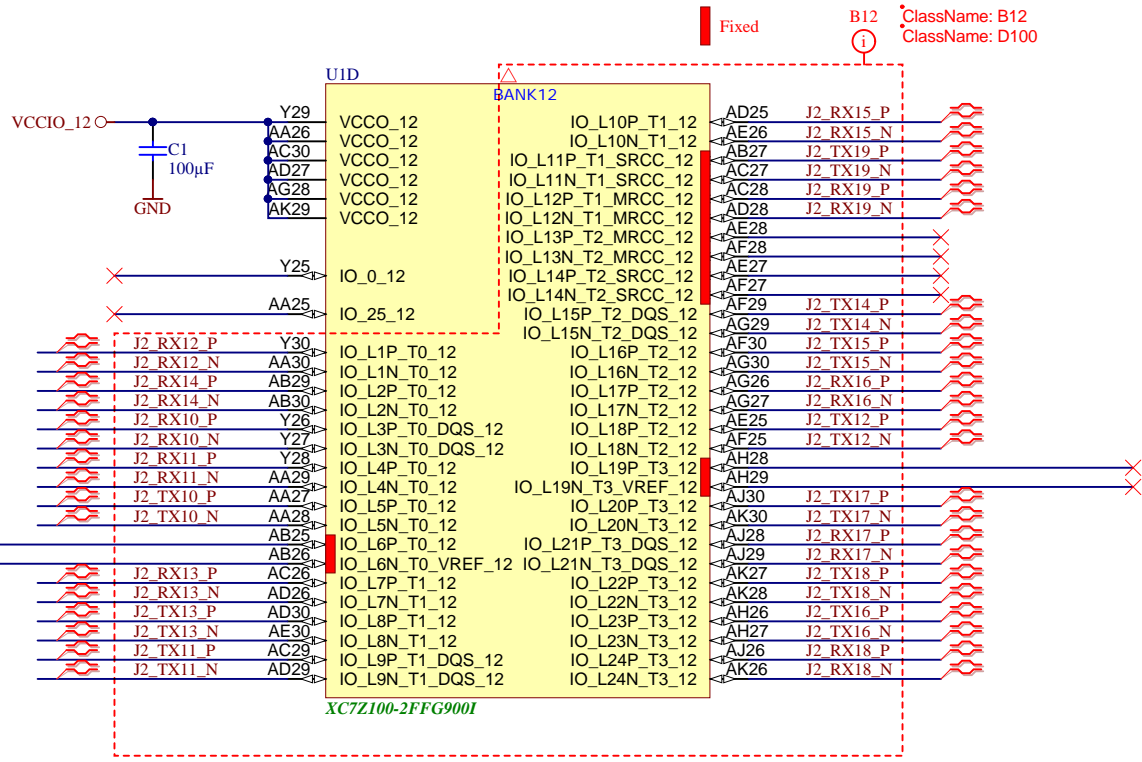


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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 12 of 31
Filename: B10.SchDoc		



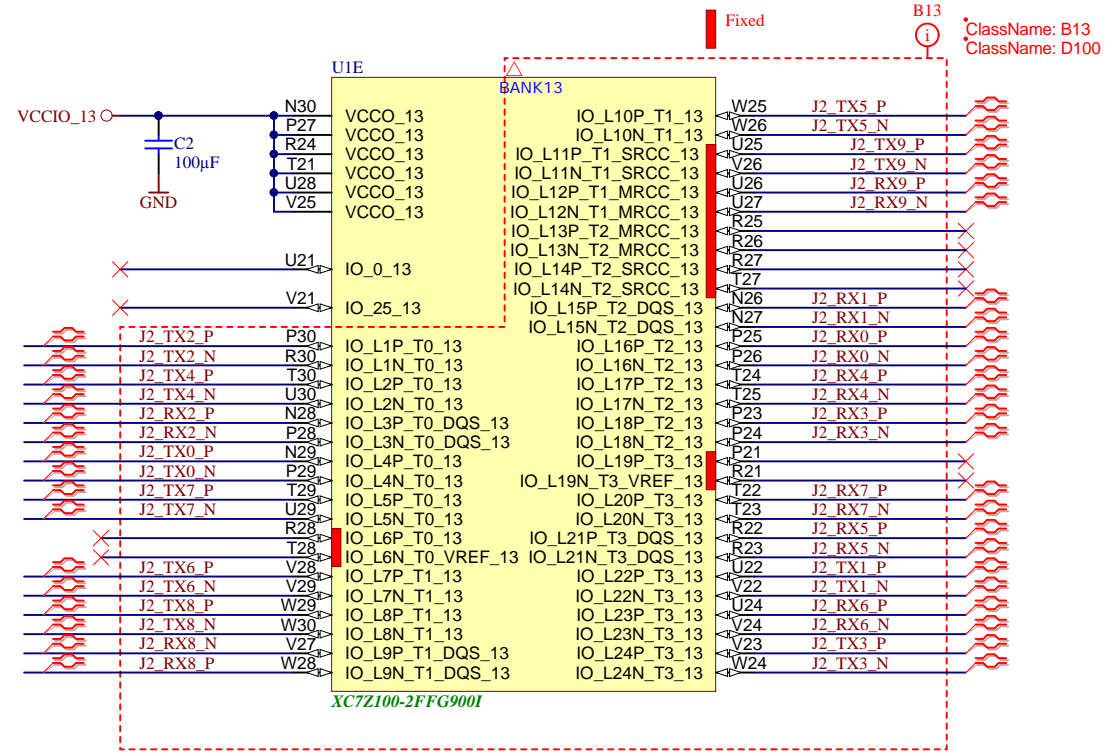
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	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page13 of 31
	Filename: B11.SchDoc		


TP1
 VCCIO_12
 Testpoint 0.8mm



Title: TE0782 - FPGA B12		
A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 14 of 31
Filename: B12.SchDoc		

TP2
 ● ○ VCCIO_13
 Testpoint 0.8mm



		Title: TE0782 - FPGA B13	
		A4	Number: TE0782 TE0782-02-100-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: B13.SchDoc		Page 15 of 31	

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U_B33
B33.SchDoc



U_B34
B34.SchDoc



U_B35
B35.SchDoc



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Title: TES0782 - FPGA HP Banks		
A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 16 of 31
Filename: HP-BANKS.SchDoc		

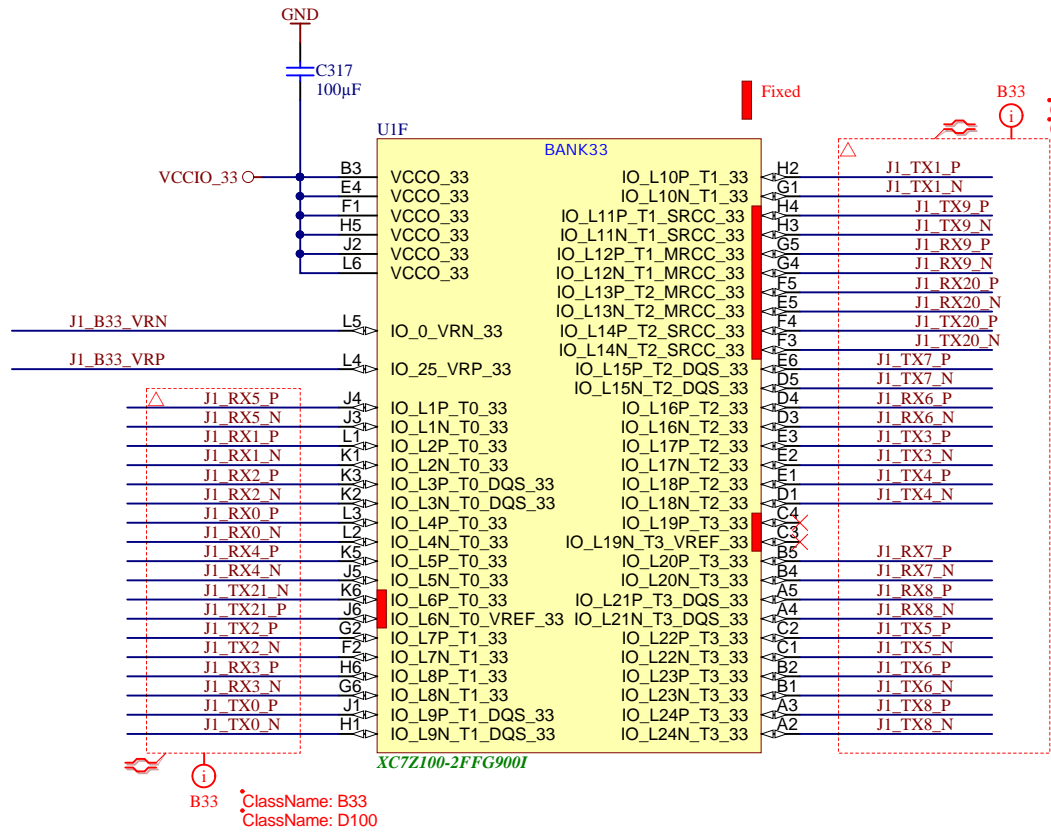
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TP6
 VCCIO_33
 Testpoint 0.8mm




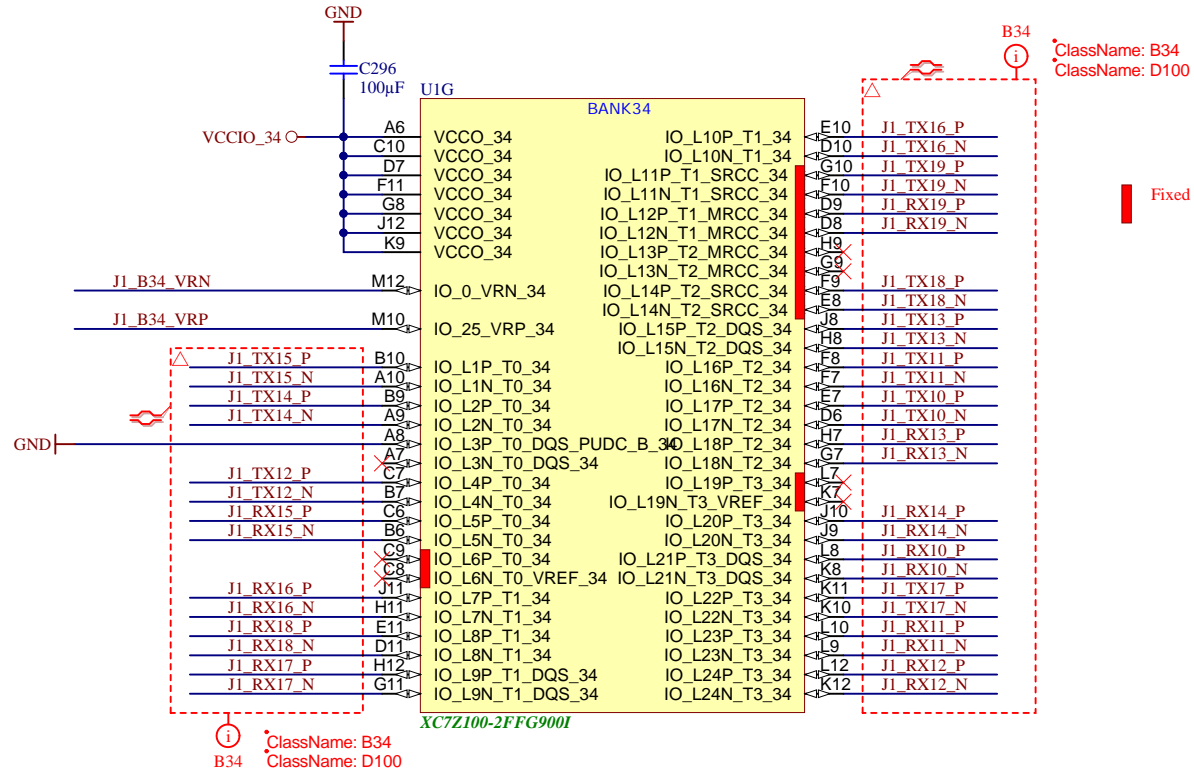
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 ClassName: D100

B33
 ClassName: B33
 ClassName: D100

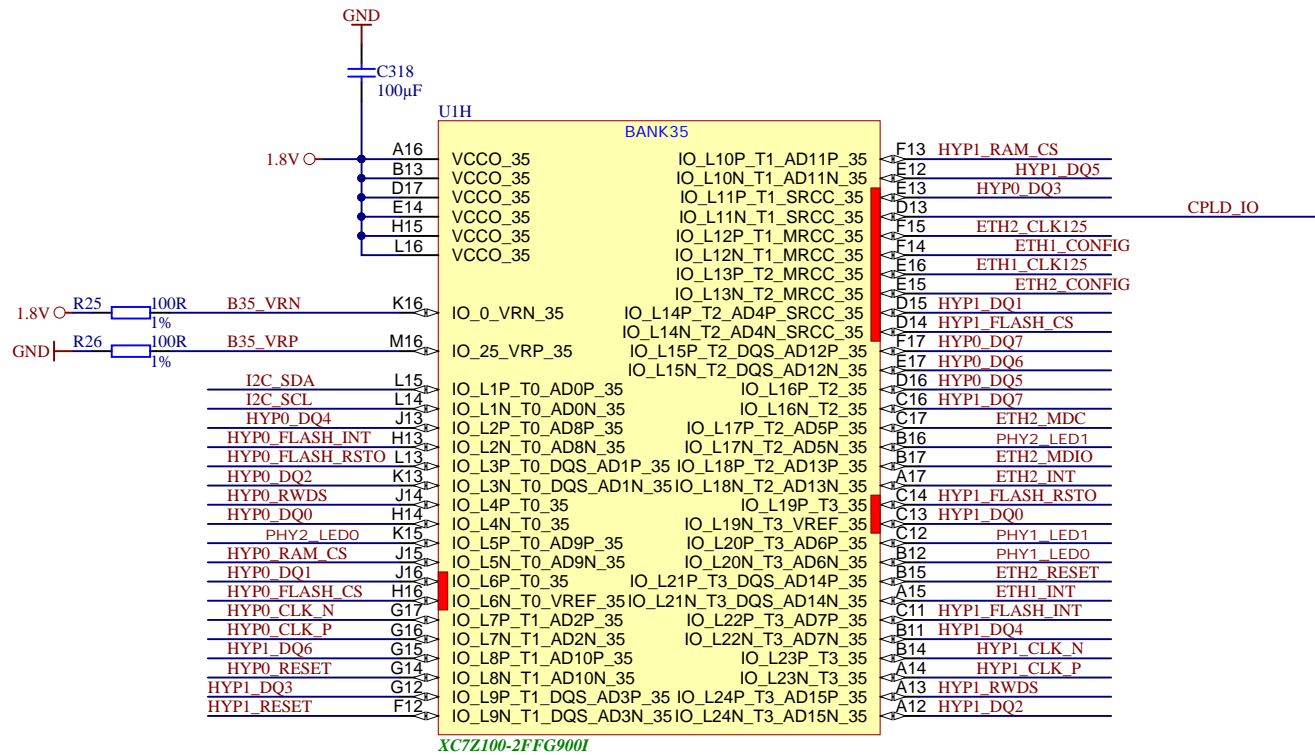


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A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 17 of 31
Filename: B33.SchDoc		

TP3
 VCCIO_34
 Testpoint 0.8mm



Title: TE0782 - FPGA B34		
A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page18 of 31
Filename: B34.SchDoc		

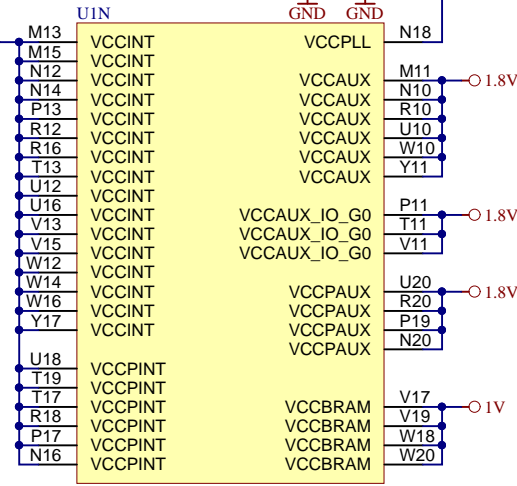
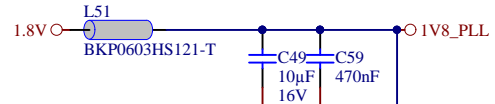
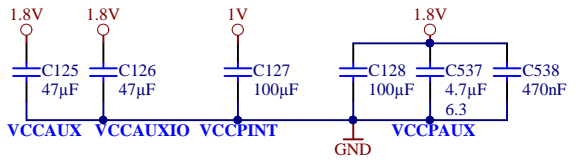
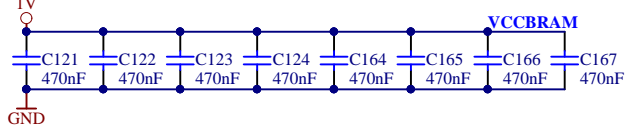
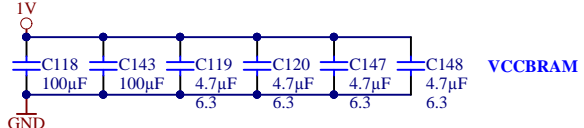
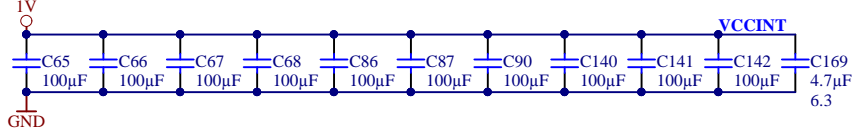
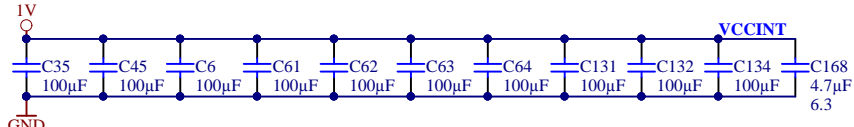


XC7Z100-2FFG9001

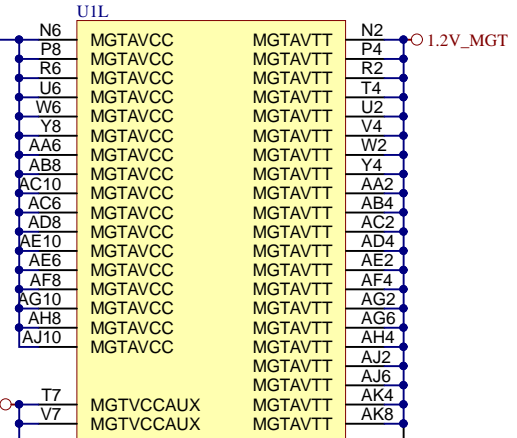


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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 19 of 31
Filename: B35.SchDoc		

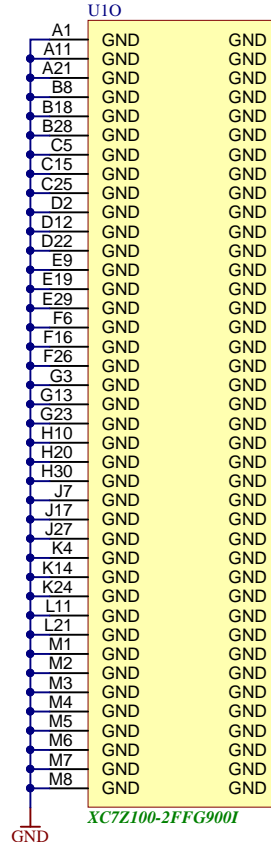
Capacitors suitable for XC7Z100



XC7Z100-2FFG900I

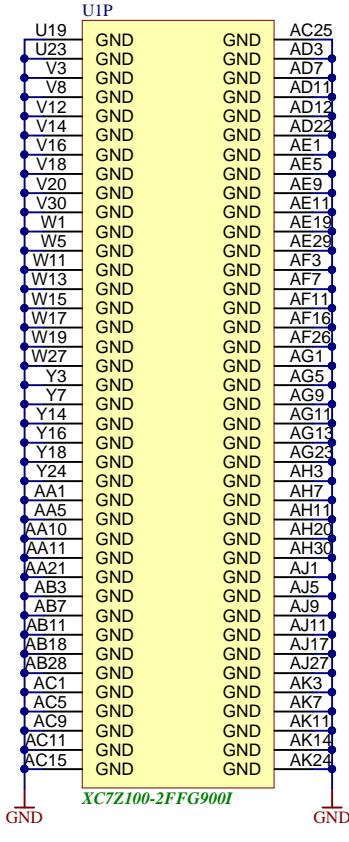


XC7Z100-2FFG900I



U10

XC7Z100-2FFG900I

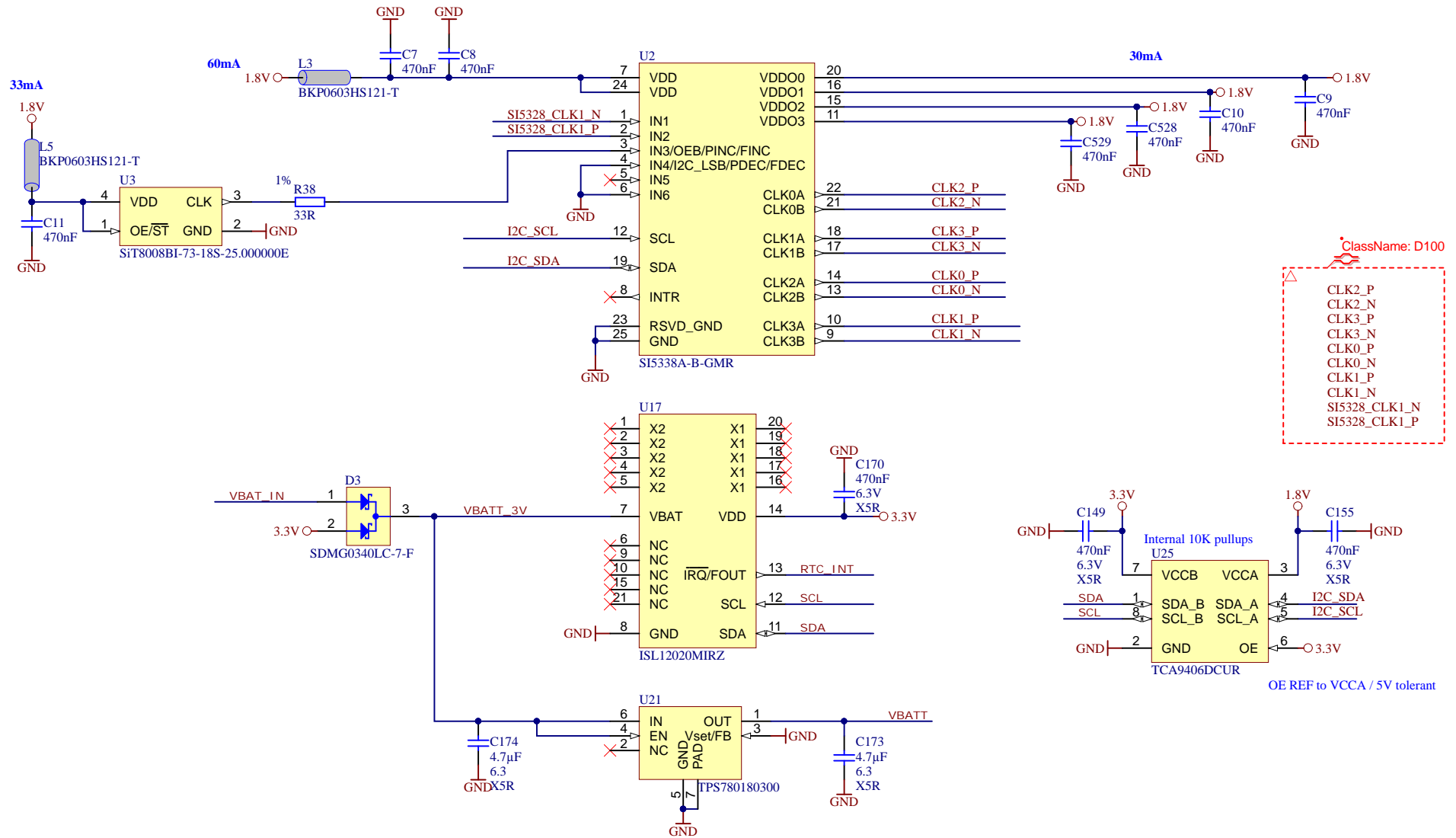


UIP

XC7Z100-2FFG900I



Title: TE0782 - ZYNQ POWER		
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Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page20 of 31
Filename: FPGA-PWR.SchDoc		



ClassName: D100

CLK2_P
 CLK2_N
 CLK3_P
 CLK3_N
 CLK0_P
 CLK0_N
 CLK1_P
 CLK1_N
 SI5328_CLK1_N
 SI5328_CLK1_P

OE REF to VCCA / 5V tolerant



Title: TE0782 - Clock		
A4	Number: TE0782 TE0782-02-100-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 21 of 31
Filename: Clock.SchDoc		

A

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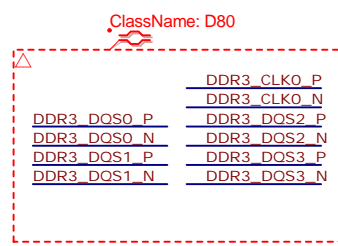
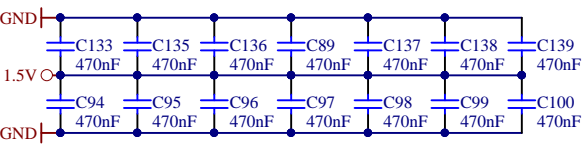
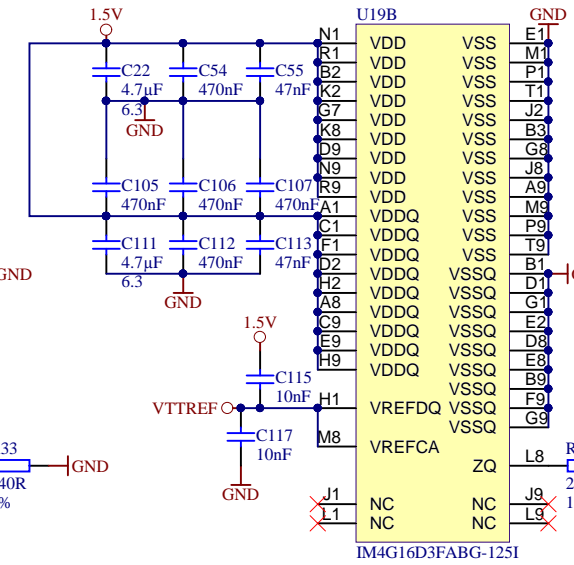
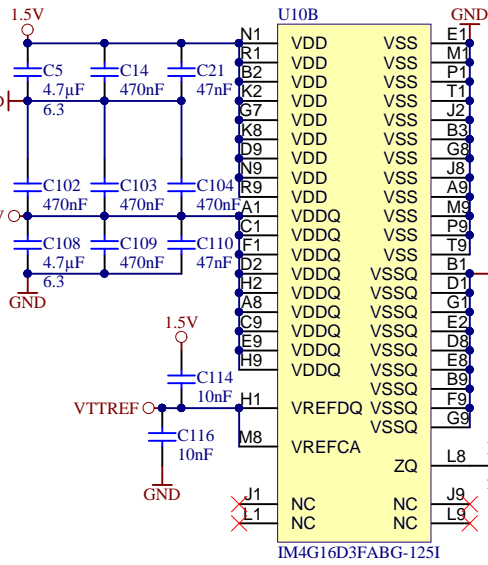
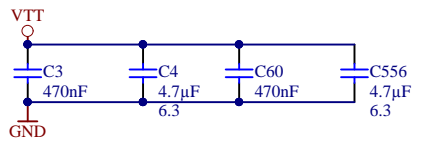
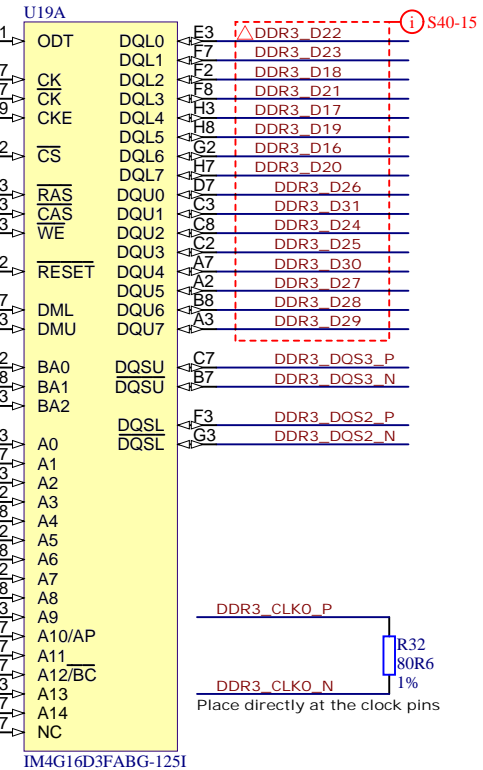
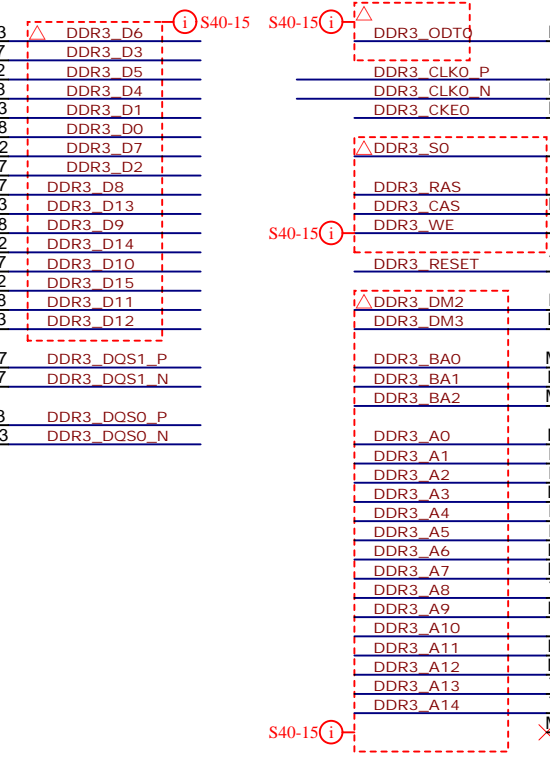
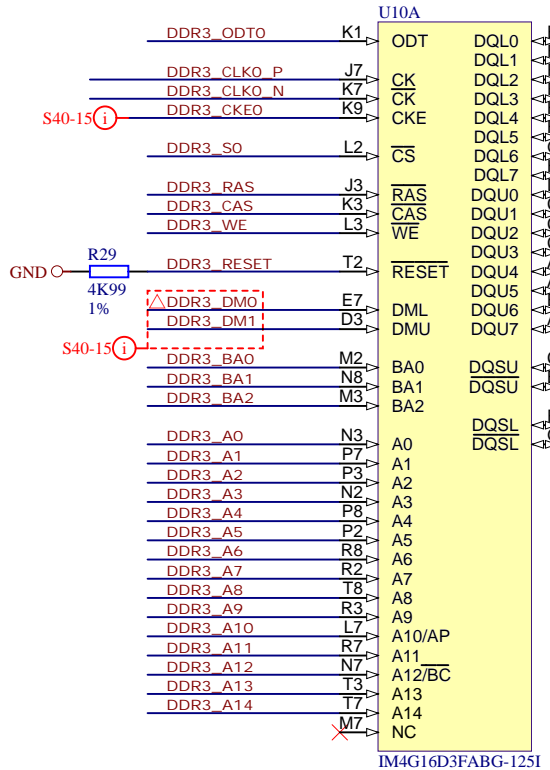
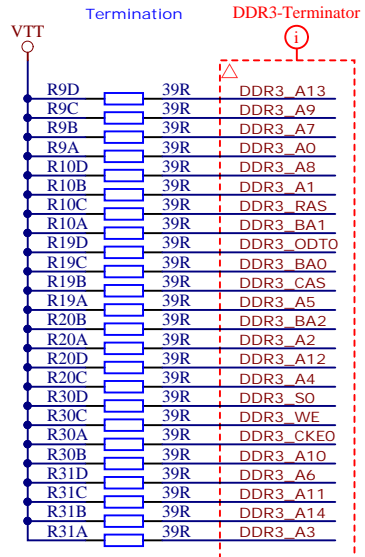
B

C

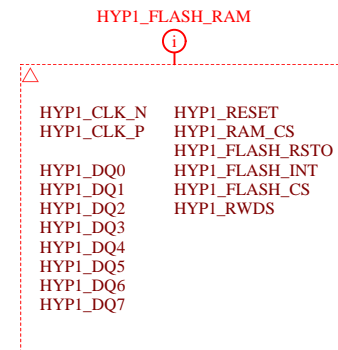
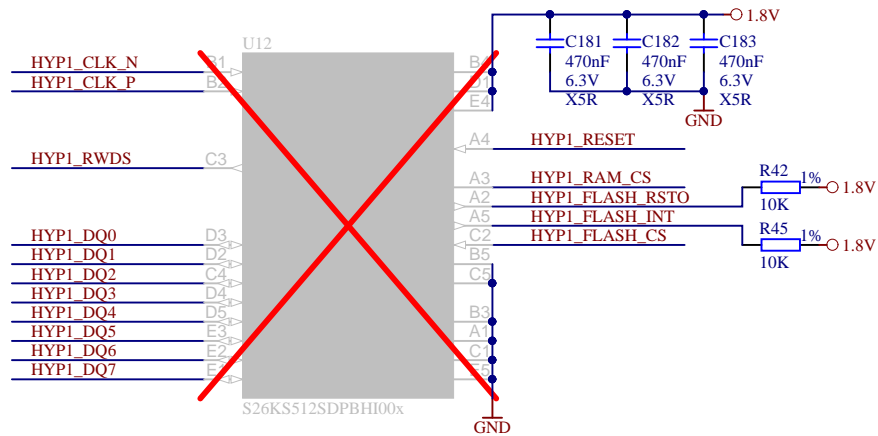
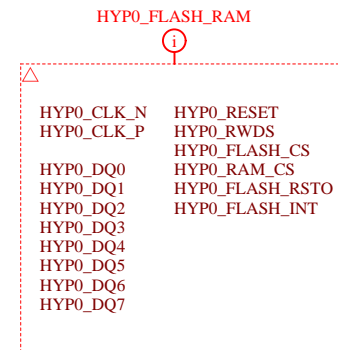
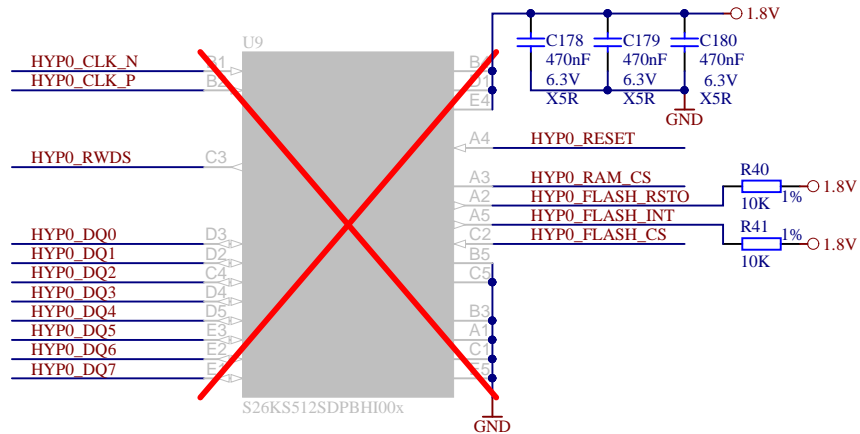
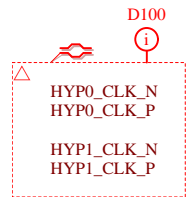
C

D

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Title: TE0782 - DDR3 RAM		
A4	Number: TE0782 TE0782-02-100-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 22 of 31
Filename: DDR3-RAM.SchDoc		



	Title: TE0782 - HyperFlash_RAM		
	A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
	Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 23 of 31
	Filename: HyperFlash_RAM.SchDoc		

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A

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B

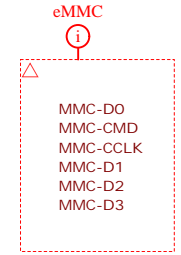
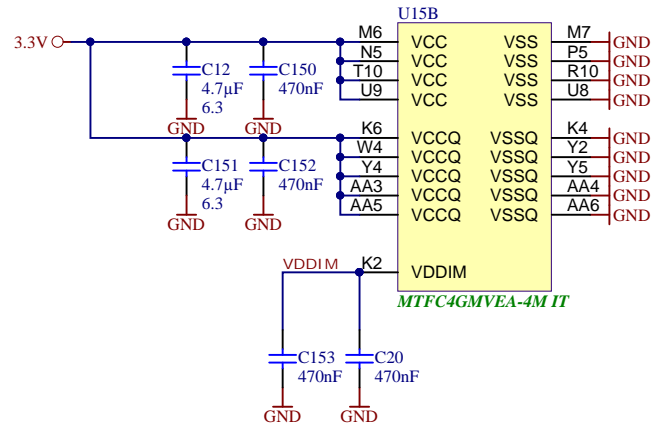
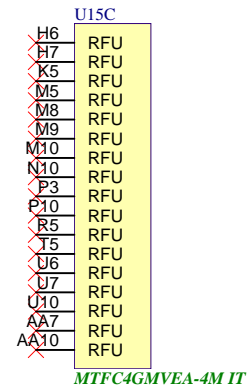
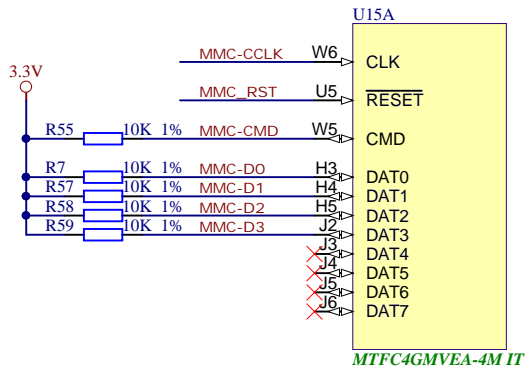
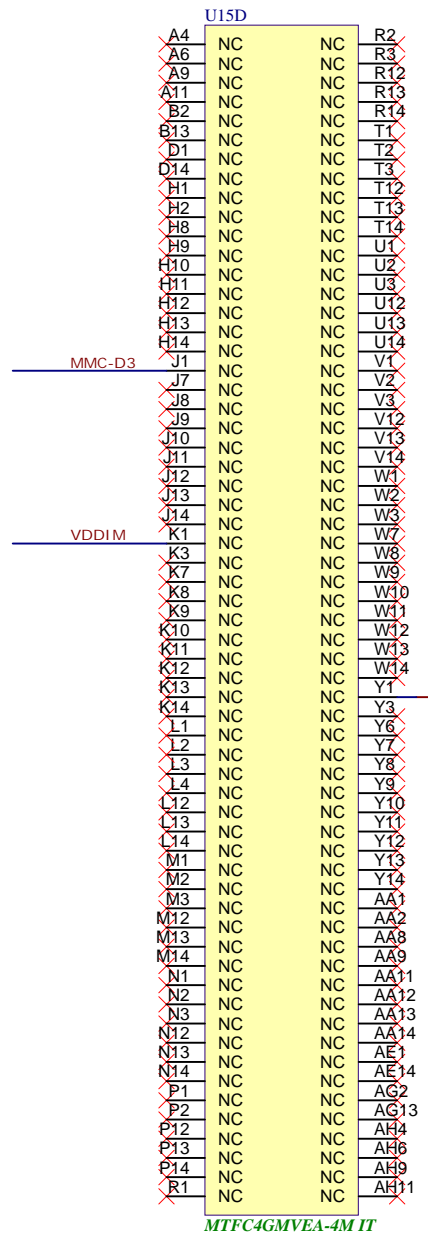
B

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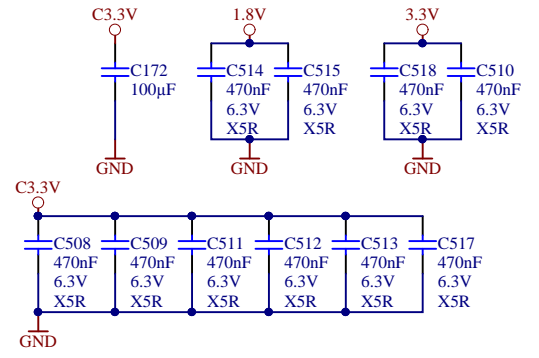
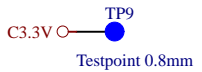
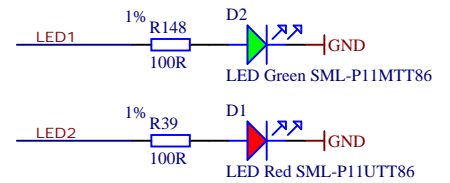
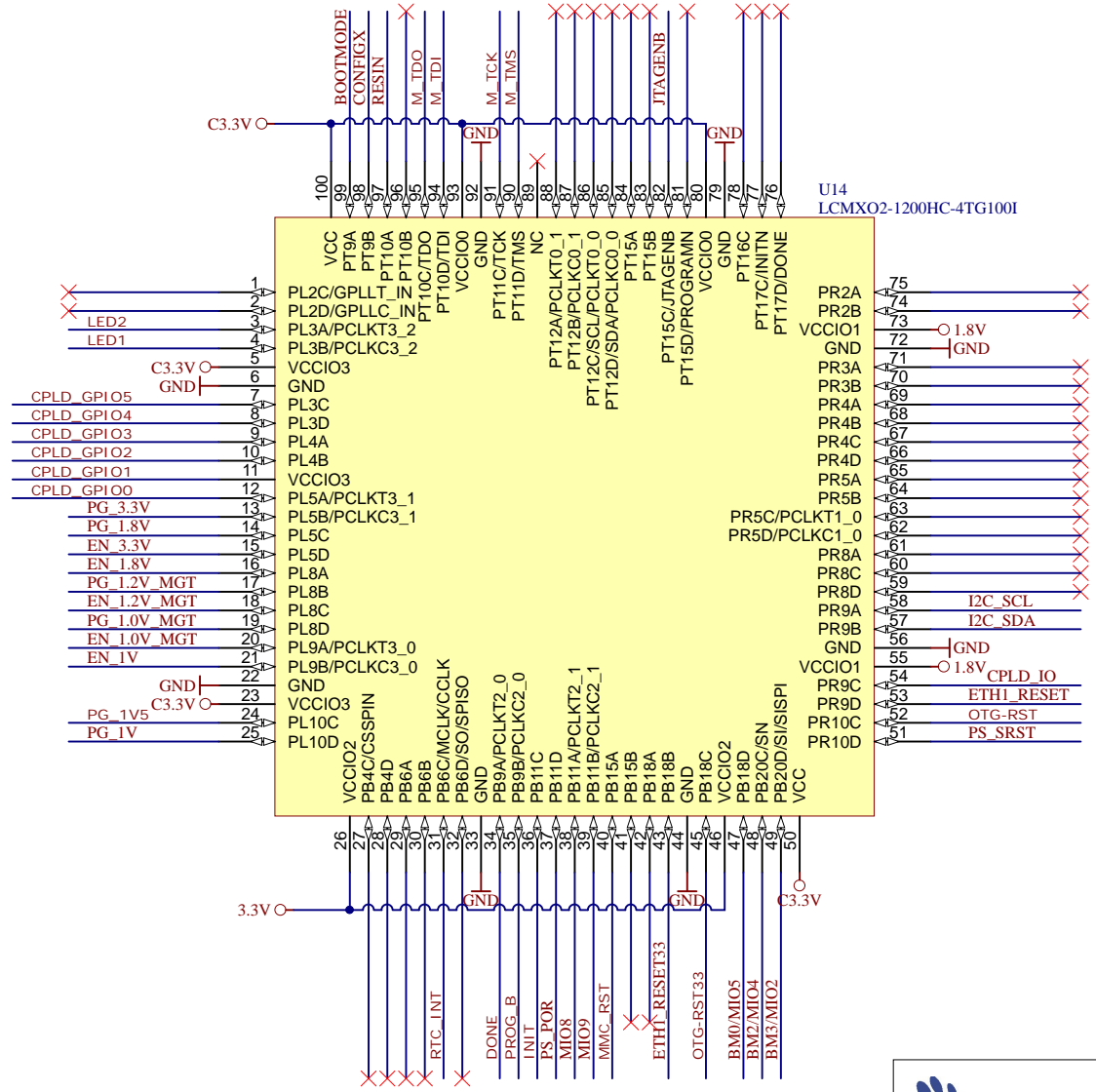
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A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page24 of 31
Filename: eMMC.SchDoc		

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2

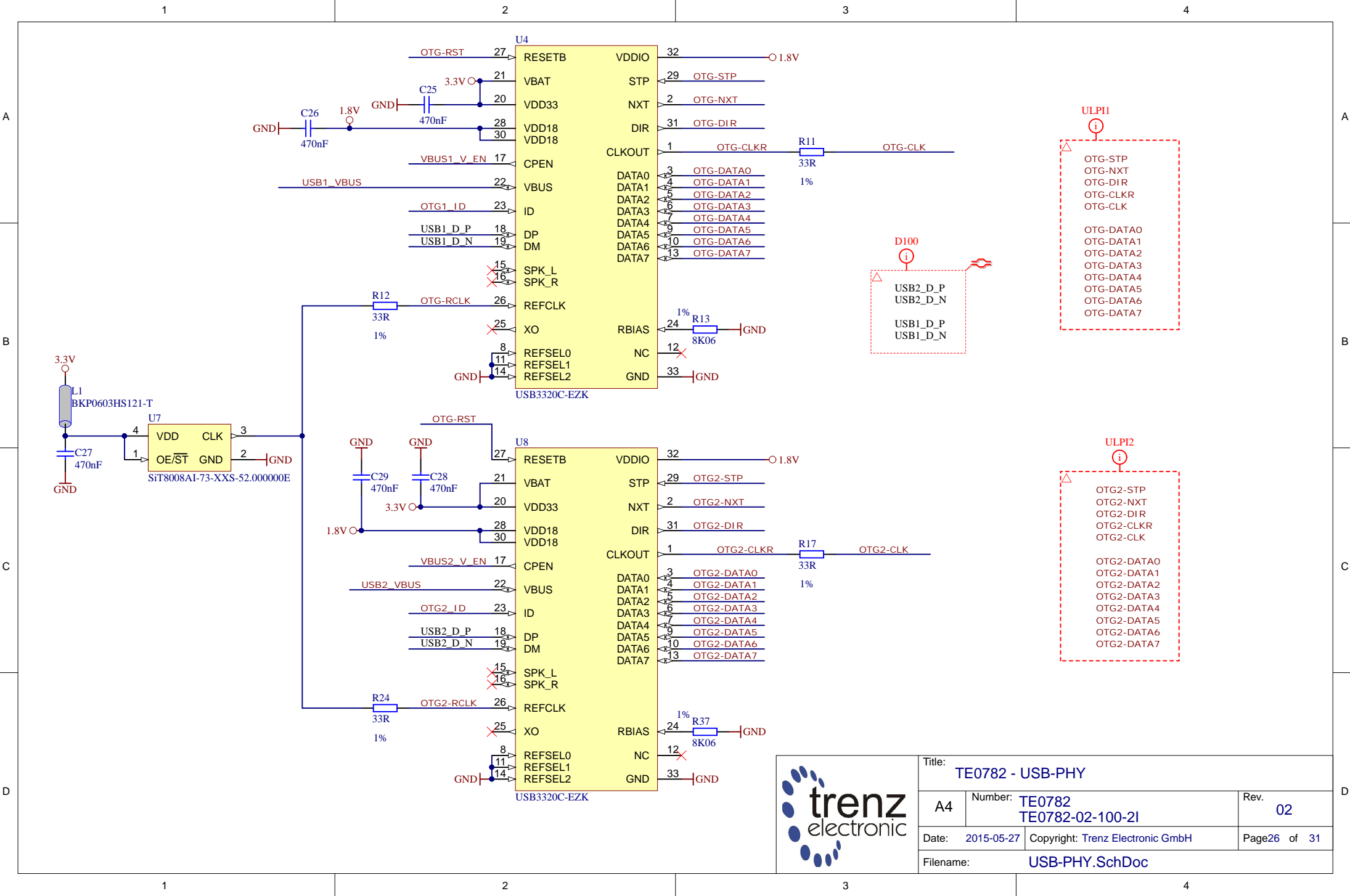
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4



Title: TE0782 - CPLD		
A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 25 of 31
Filename: CPLD.SchDoc		





			Title: TE0782 - USB-PHY	
			A4	Number: TE0782 TE0782-02-100-21
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page 26 of 31
Filename: USB-PHY.SchDoc				

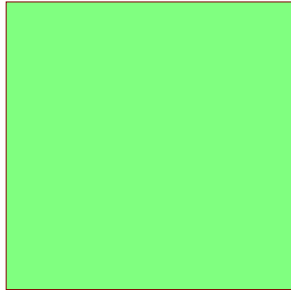
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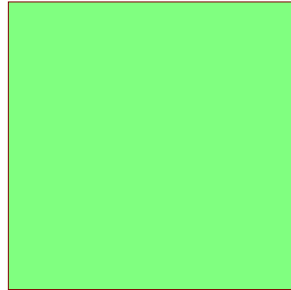
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U_ETH1
ETH1.SchDoc



U_ETH2
ETH2.SchDoc



A

A

B


B

C

C

D

D

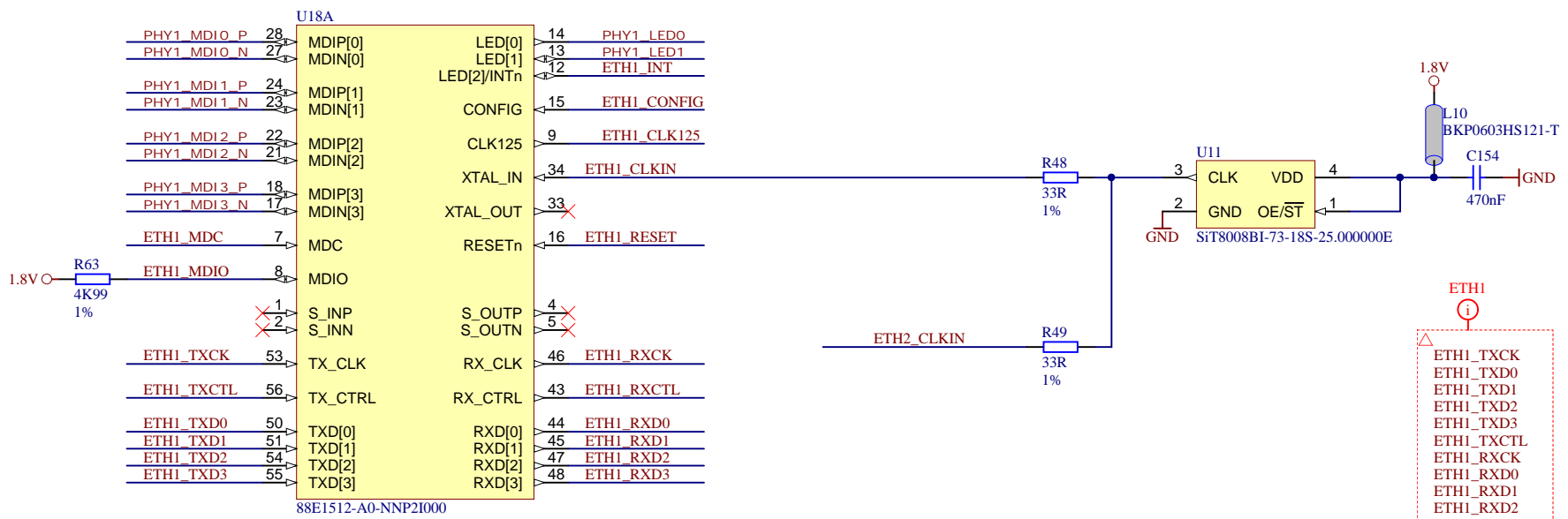
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		A4	Number: TE0782 TE0782-02-100-2I
Date: 2015-05-27		Copyright: Trenz Electronic GmbH	
Filename: Ethernet.SchDoc		Page 27 of 31	

1

2

3

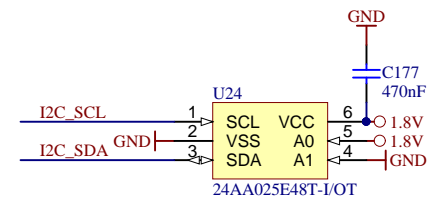
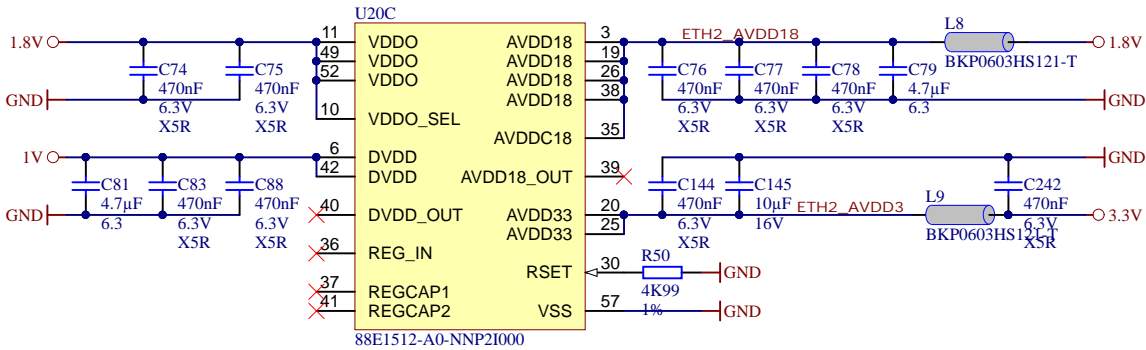
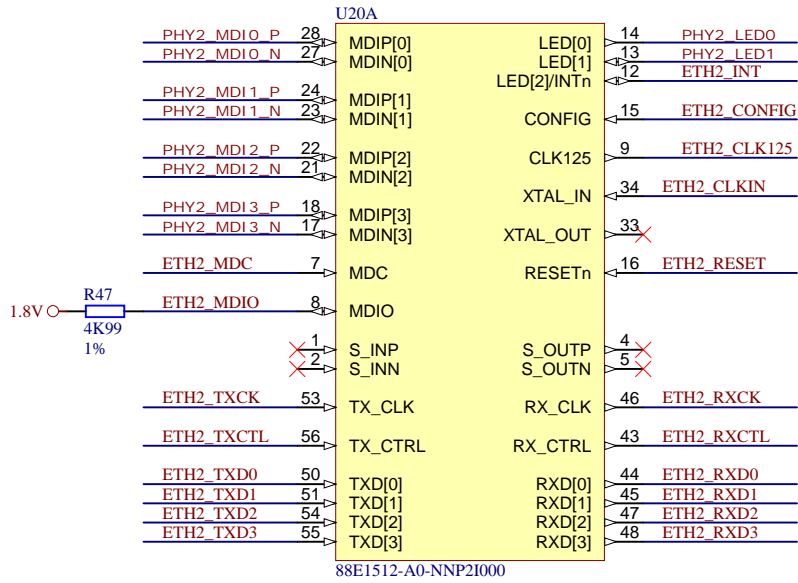
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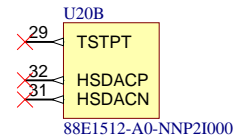
- ETH1**
- ETH1_TXCK
 - ETH1_TXD0
 - ETH1_TXD1
 - ETH1_TXD2
 - ETH1_TXD3
 - ETH1_TXCTL
 - ETH1_RXCK
 - ETH1_RXD0
 - ETH1_RXD1
 - ETH1_RXD2
 - ETH1_RXD3
 - ETH1_RXCTL
 - ETH1_MDC
 - ETH1_MDIO
- PHY1_LED0
PHY1_LED1
ETH1_INT
ETH1_CONFIG
ETH1_CLK125
ETH1_RESET



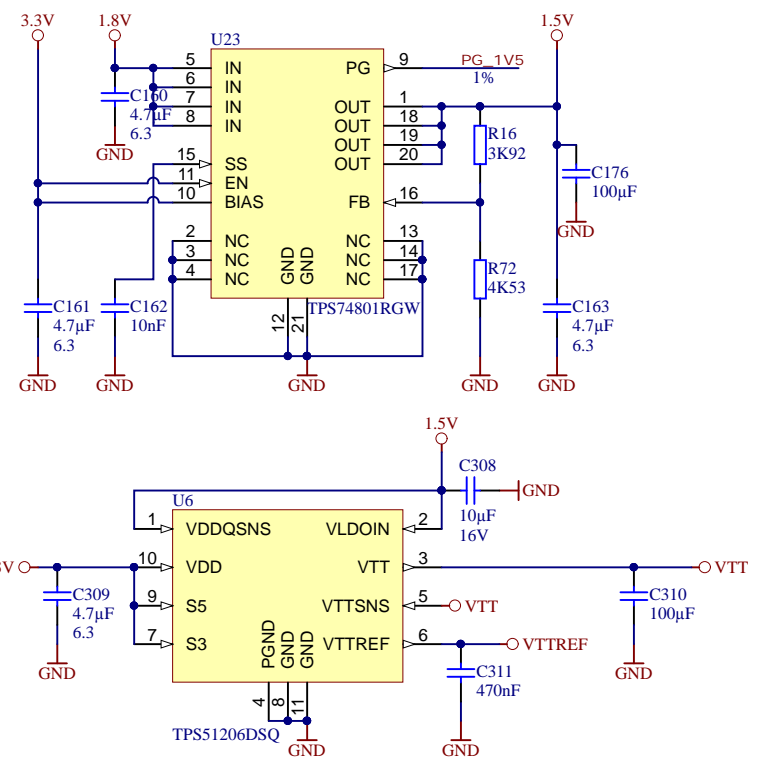
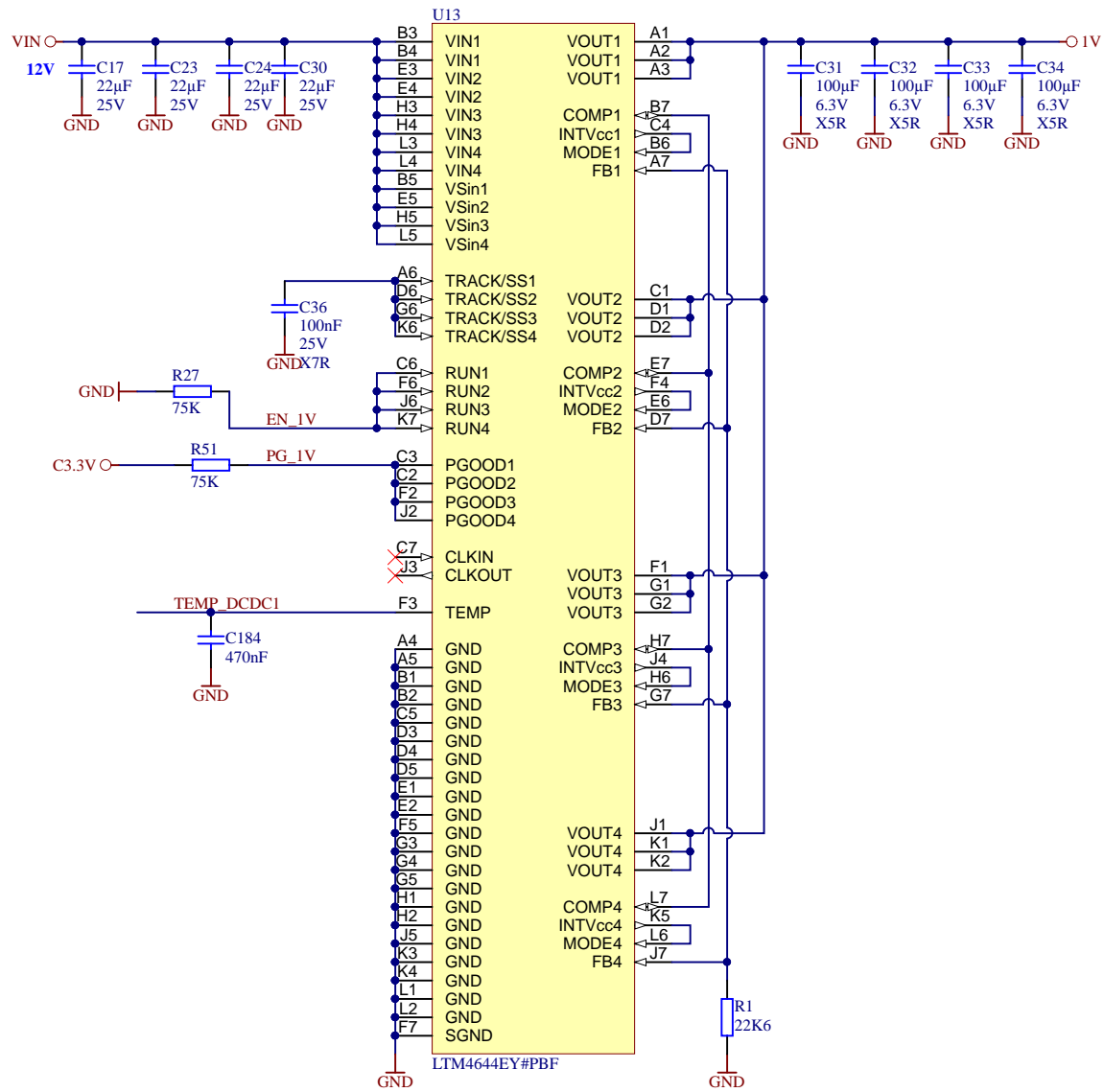
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A4	Number: TE0782 TE0782-02-100-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 28 of 31
Filename: ETH1.SchDoc		




Slave ADDR:
1010001

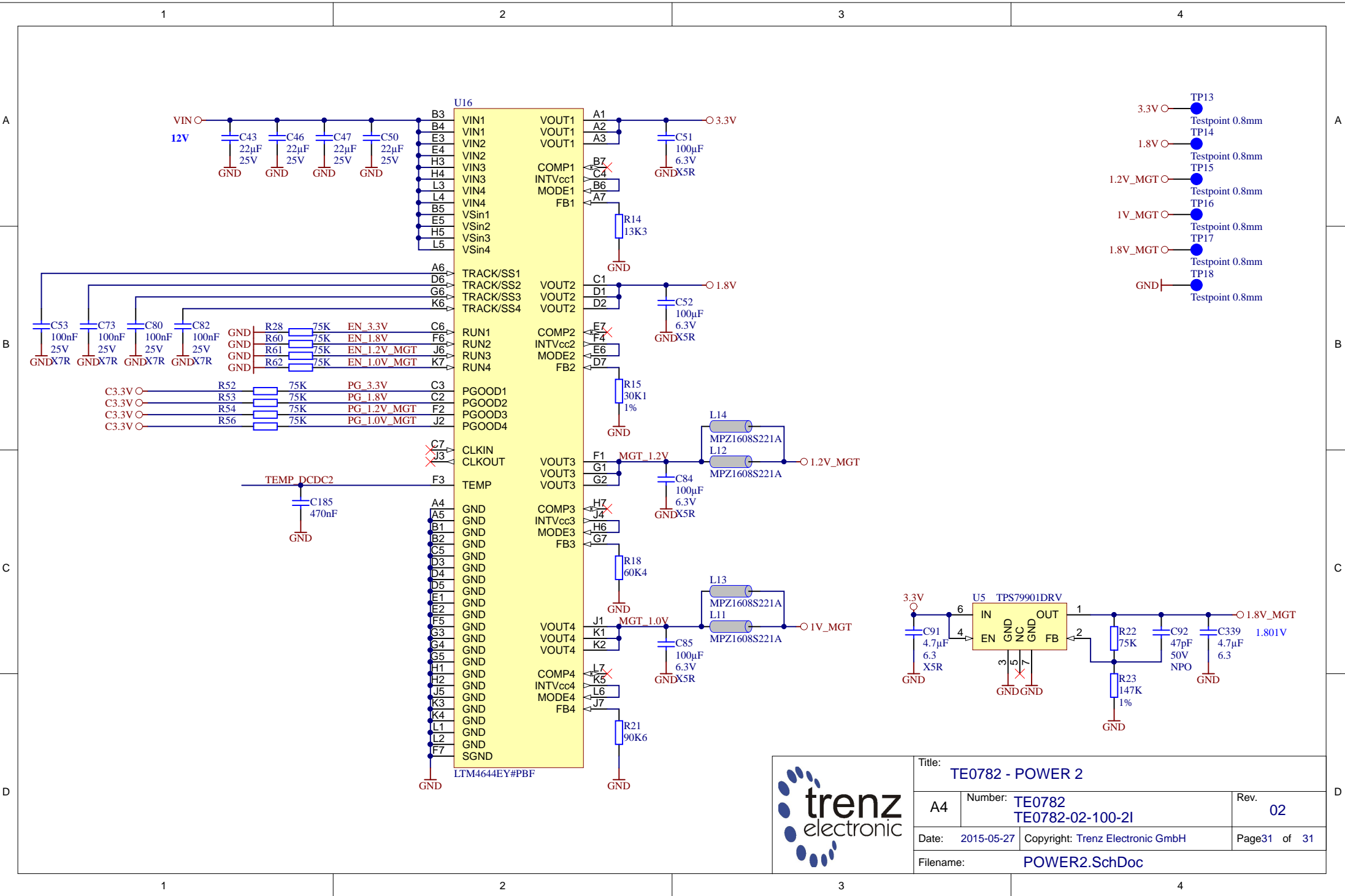


Title: TE0782 - ETH_PHY2		
A4	Number: TE0782 TE0782-02-100-21	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 29 of 31
Filename: ETH2.SchDoc		



- TP7 1V ○ ● Testpoint 0.8mm
- TP8 GND ○ ● Testpoint 0.8mm
- TP10 1.5V ○ ● Testpoint 0.8mm
- TP11 VTT ○ ● Testpoint 0.8mm
- TP12 VTTREF ○ ● Testpoint 0.8mm

			Title: TE0782 - POWER	
			A4	Number: TE0782 TE0782-02-100-21
Date: 2015-05-27		Copyright: Trenz Electronic GmbH		Page30 of 31
Filename: POWER.SchDoc				



- 3.3V ○ TP13 Testpoint 0.8mm
- 1.8V ○ TP14 Testpoint 0.8mm
- 1.2V_MGT ○ TP15 Testpoint 0.8mm
- 1V_MGT ○ TP16 Testpoint 0.8mm
- 1.8V_MGT ○ TP17 Testpoint 0.8mm
- GND ○ TP18 Testpoint 0.8mm



Title: TE0782 - POWER 2		
A4	Number: TE0782 TE0782-02-100-2I	Rev. 02
Date: 2015-05-27	Copyright: Trenz Electronic GmbH	Page 31 of 31
Filename: POWER2.SchDoc		