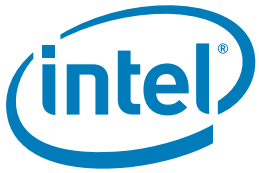


Intel® Celeron™ P4000 and U3000 Mobile Processor Series

External Design Specification — Volume One

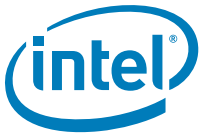
This is volume 1 of 2. Refer to Document 416057 for Volume 2

Rev 1.5

March 2010

Intel Confidential

Document Number: 442690



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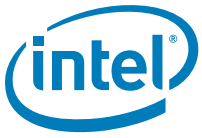

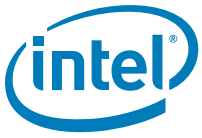

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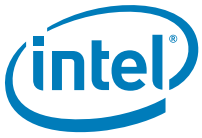
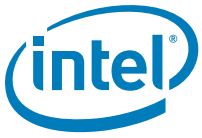


Revision History

Document Number	Revision Number	Description	Revision Date
442690	1.5	• Initial release	Feburary 2010



Revision Number Descriptions		
Revision	**Associated Life Cycle Milestone**	**Release Information**
0.5	Design Win Phase	Required Release
0.6–0.7	When Needed	Project Dependent
0.7	Simulations Complete	Required Release
0.8–0.9	When Needed	Project Dependent
1.0	First Silicon Samples	Required Release
1.1–1.4	When Needed	Project Dependent
1.5	Qualification Silicon Samples	Project Dependent
1.6–1.9	When Needed	Project Dependent
NDA - 2.0 Public - XXXXXX-001	First SKU Launch	Required Release Product Launch
2.1 and up	When Needed	Project Dependent

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1 Features Summary

1.1 Introduction

The External Design Specification (EDS) provides DC and AC electrical specifications, signal integrity, differential signaling specifications, pinout and signal definitions, interface functional descriptions, thermal specifications, and additional feature information pertinent to the implementation and operation of the processor on its respective platform.

Intel® Celeron™ P4000 and U3000 mobile processor series is the next generation of 64-bit, multi-core mobile processor built on 32-nanometer process technology. Throughout this document, Intel® Celeron™ P4000 and U3000 mobile processor series may be referred to as simply the processor. Based on the low-power/high-performance Nehalem micro-architecture, the processor is designed for a two-chip platform as opposed to the traditional three-chip platforms (processor, GMCH, and ICH). The two-chip platform consists of a processor and the Platform Controller Hub (PCH) and enables higher performance, lower cost, easier validation, and improved x-y footprint. The PCH may also be referred to as Mobile Intel® 5 Series Chipset (formerly Ibex Peak-M). Intel® Celeron™ P4000 and U3000 mobile processor series is designed for the Calpella platform and is offered in an rPGA988A or a BGA1288 package.

Included in this family of processors is Intel® HD graphics and memory controller die on the same package as the processor core die. This two-chip solution of a processor core die with an integrated graphics and memory controller die is known as a multi-chip package (MCP) processor.

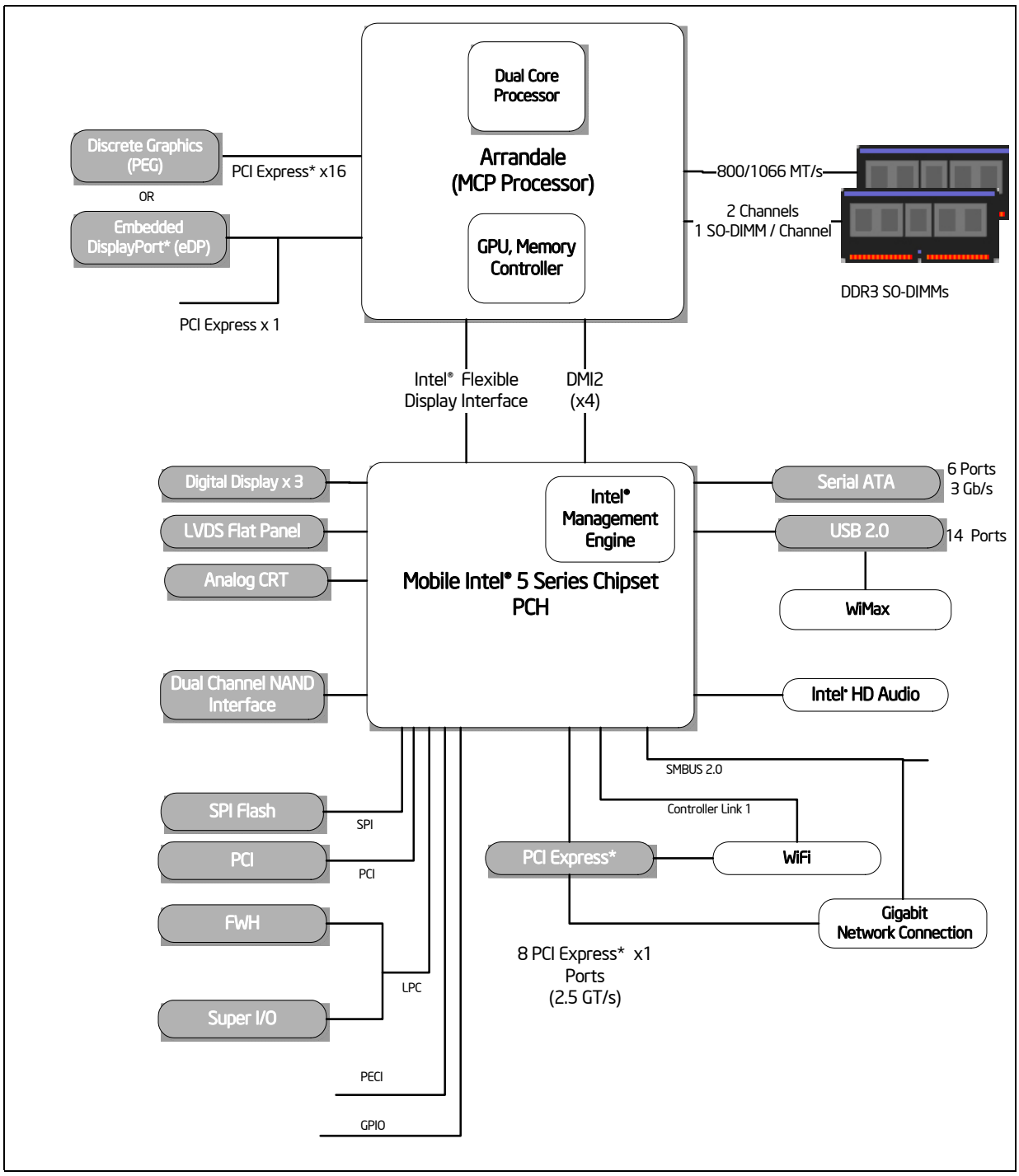
Note: Throughout this document, Intel® Celeron™ P4000 and U3000 mobile processor series may be referred to as simply the processor.

Throughout this document, Intel® HD graphics may be referred to as simply the integrated graphics.

Integrated graphics and memory controller die is built on 45-nanometer process technology

Intel® Celeron™ P4000 and U3000 mobile processor series is not vPro eligible

Figure 1. Intel® Celeron™ P4000 and U3000 mobile processor series on the Calpella Platform



1.2 Processor Feature Details

- Two execution cores
- A 32-KB instruction and 32-KB data first-level cache (L1) for each core
- A 256-KB shared instruction/data second-level cache (L2) for each core
- Up to 2-MB shared instruction/data third-level cache (L3), shared among all cores

1.2.1 Supported Technologies

- Intel® Virtualization Technology (Intel® VT-x)
- Intel® 64 architecture
- Execute Disable Bit
- Processor Context Identifier(PCID)

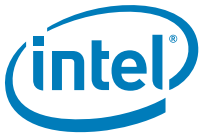
Note: Please refer to the Intel® Celeron™ P4000 and U3000 mobile processor series Specification Update for feature support details

For more information on AESNI, PCLMULQDQ instructions and Processor Context Identifier, please refer to the Intel Software Developer's Manual

1.3 Interfaces

1.3.1 System Memory Support

- One or two channels of DDR3 memory with a maximum of one SO-DIMM per channel
- Single- and dual-channel memory organization modes
- Data burst length of eight for all memory organization modes
- Memory DDR3 data transfer rates of 800 MT/s (SV, ULV) and 1066 MT/s (SV)
- 64-bit wide channels
- DDR3 I/O Voltage of 1.5 V
- Non-ECC, unbuffered DDR3 SO-DIMMs only
- Theoretical maximum memory bandwidth of:
  - 12.8 GB/s in dual-channel mode assuming DDR3 800 MT/s
  - 17.1 GB/s in dual-channel mode assuming DDR3 1066 MT/s
- 1-Gb, and 2-Gb DDR3 DRAM technologies are supported for x8 and x16 devices.
- Using 2-Gb device technologies, the largest memory capacity possible is 8 GB, assuming dual-channel mode with two x8, double-sided, un-buffered, non-ECC, SO-DIMM memory configuration.
- Up to 32 simultaneous open pages, 16 per channel (assuming 4 Ranks of 8 Bank Devices)



- Memory organizations:
  - — Single-channel modes
  - — Dual-channel modes - Intel® Flex Memory Technology:
    Dual-channel symmetric (Interleaved)
    Dual-channel asymmetric
- Command launch modes of 1n/2n
- Partial Writes to memory using Data Mask (DM) signals
- On-Die Termination (ODT)
- Intel® Fast Memory Access (Intel® FMA):
  - — Just-in-Time Command Scheduling
  - — Command Overlap
  - — Out-of-Order Scheduling

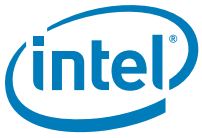
1.3.2 PCI Express*

- The Processor PCI Express* ports are fully compliant to the *PCI Express Base Specification Revision 2.0*.
  - — One 16-lane PCI Express* port intended for graphics attach.
  - — Two 8-lane PCI Express* ports intended for graphics attach.
    PCI Express Port 0 is mapped to PCI Device 1 (PEG 0).
    PCI Express Port 1 is mapped to PCI Device 6 (PEG 1).
- Gen1 (2.5 GT/s) PCI Express* frequency is supported.
- Gen1 Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. This also does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 4 GB/s in each direction simultaneously, for an aggregate of 8 GB/s when x16 Gen 1.
- Hierarchical PCI-compliant configuration mechanism for downstream devices.
- Traditional PCI style traffic (asynchronous snooped, PCI ordering).
- PCI Express extended configuration space. The first 256 bytes of configuration space aliases directly to the PCI compatibility configuration space. The remaining portion of the fixed 4-KB block of memory-mapped space above that (starting at 100h) is known as “extended configuration space”.
- PCI Express Enhanced Access Mechanism. Accessing the device configuration space in a flat memory mapped fashion.
- Automatic discovery, negotiation, and training of link out of reset.
- Traditional AGP style traffic (asynchronous non-snooped, PCI-X Relaxed ordering).
- Peer segment destination posted write traffic (no peer-to-peer read traffic) in Virtual Channel 0:
  - — DMI -> PCI Express Port 0
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros).
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are non-zero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.

- Re-issues configuration cycles that have been previously completed with the Configuration Retry status.
- PCI Express reference clock is 100-MHz differential clock buffered out of system clock generator.
- Power Management Event (PME) functions.
- Static lane numbering reversal
  - Does not support dynamic lane reversal, as defined (optional) by the *PCI Express Base Specification.*
  - PCI Express 1x16 configuration
    Normal (1x16): PEG_RX[15:0]; PEG_TX[15:0]
    Reversal (1x16): PEG_RX[0:15]; PEG_TX[0:15]
- Supports Half Swing "low-power/low-voltage" mode.
- Message Signaled Interrupt (MSI and MSI-X) messages
- PEG Lanes shared with Embedded DisplayPort* (see eDP, Section 1.3.6).
- Polarity inversion

1.3.3 Direct Media Interface (DMI)

- Compliant to Direct Media Interface second generation (DMI2).
- Four lanes in each direction.
- 2.5 GT/s point-to-point DMI interface to PCH is supported.
- Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a real bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface. Does not account for packet overhead and link maintenance.
- Maximum theoretical bandwidth on interface of 1 GB/s in each direction simultaneously, for an aggregate of 2 GB/s when DMI x4.
- Shares 100-MHz PCI Express reference clock.
- 64-bit downstream address format, but the processor never generates an address above 64 GB (Bits 63:36 will always be zeros).
- 64-bit upstream address format, but the processor responds to upstream read transactions to addresses above 64 GB (addresses where any of Bits 63:36 are nonzero) with an Unsupported Request response. Upstream write transactions to addresses above 64 GB will be dropped.
- Supports the following traffic types to or from the PCH:
  - DMI -> PCI Express Port 0 write traffic
  - DMI -> DRAM
  - DMI -> processor core (Virtual Legacy Wires (VLWs), Resetwarn, or MSIs only)
  - Processor core -> DMI
- APIC and MSI interrupt messaging support:
  - Message Signaled Interrupt (MSI and MSI-X) messages
- Downstream SMI, SCI and SERR error indication.
- Legacy support for ISA regime protocol (PHOLD/PHOLDA) required for parallel port DMA, floppy drive, and LPC bus masters.
- DC coupling – no capacitors between the processor and the PCH.
- Polarity inversion.



- PCH end-to-end lane reversal across the link.
- Supports Half Swing "low-power/low-voltage."

1.3.4 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (the processor) and a PECI master (the PCH).

1.3.5 Intel® HD Graphics Controller

- The integrated graphics controller contains a refresh of the fifth generation graphics core
- Intel® Dynamic Video Memory Technology (Intel® DVMT) support
- Intel® Graphics Performance Modulation Technology (Intel® GPMT)
- Intel® Smart 2D Display Technology (Intel® S2DDT)
- Intel® Clear Video Technology
  - MPEG2 Hardware Acceleration
  - WMV9/VC1 Hardware Acceleration
  - AVC Hardware Acceleration
  - ProcAmp
  - Advanced Pixel Adaptive De-interlacing
  - Sharpness Enhancement
  - De-noise Filter
  - High Quality Scaling
  - Film Mode Detection (3:2 pull-down) and Correction
  - Intel® TV Wizard
- 12 EUs
- Dedicated analog and digital display ports are supported through the Intel 5 Series Chipset PCH

1.3.6 Embedded DisplayPort* (eDP*)

- Shared with PCI Express Graphics port
- Shared on upper four logical lanes, after any lane reversal
- eDP[3:0] map to PEG[12:15] (non-reversed)
- eDP[3:0] map to PEG[3:0] (reversed)
- Concurrent eDP and PEG x1 support

1.3.7 Intel® Flexible Display Interface (Intel® FDI)

- Carries display traffic from the integrated graphics controller in the processor to the legacy display connectors in the PCH.
- Based on DisplayPort standard.
- Two independent links - one for each display pipe.
- Four unidirectional downstream differential transmitter pairs:
  - Scalable down to 3X, 2X, or 1X based on actual display bandwidth requirements
  - Fixed frequency 2.7 GT/s data rate
- Two sideband signals for Display synchronization:
  - FDI_FSYNC and FDI_LSYNC (Frame and Line Synchronization)
- One Interrupt signal used for various interrupts from the PCH:
  - FDI_INT signal shared by both Intel FDI Links
- PCH supports end-to-end lane reversal across both links.

1.4 Power Management Support

1.4.1 Processor Core

- Full support of ACPI C-states as implemented by the following processor C-states:
  - Ultra low voltage supports C0, C1, C1E, C3, C6
  - Standard voltage supports C0, C1, C1E, C3
- Enhanced Intel SpeedStep® Technology

1.4.2 System

- S0, S3, S4, S5

1.4.3 Memory Controller

- Conditional self-refresh (Intel® Rapid Memory Power Management (Intel® RMPM))
- Dynamic power-down

1.4.4 PCI Express*

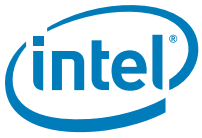
- L0s and L1 ASPM power management capability

1.4.5 DMI

- L0s and L1 ASPM power management capability

1.4.6 Integrated Graphics Controller

- Intel Smart 2D Display Technology (Intel S2DDT)
- Intel® Display Power Saving Technology (Intel® DPST)
- Graphics Render C-State (RC6)



1.5 Thermal Management Support

- Digital Thermal Sensor
- Adaptive Thermal Monitor
- THERMTRIP# and PROCHOT# support
- On-Demand Mode
- Open and Closed Loop Throttling
- Memory Thermal Throttling
- External Thermal Sensor (TS-on-DIMM and TS-on-Board)
- Render Thermal Throttling
- Fan speed control with DTS

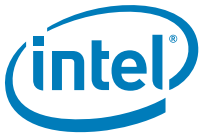
1.6 Package

- The Intel® Celeron™ P4000 and U3000 mobile processor series is available on two packages:
  - A 37.5 x 37.5 mm rPGA package (rPGA988A) (Standard Voltage only)
  - A 34 x 28 mm BGA package (BGA1288) (Ultra Low Voltage only)

1.7 Terminology

Term	Description
BLT	Block Level Transfer
CRT	Cathode Ray Tube
DDR3	Third-generation Double Data Rate SDRAM memory technology
DP	DisplayPort*
DMA	Direct Memory Access
DMI	Direct Media Interface
DTS	Digital Thermal Sensor
ECC	Error Correction Code
eDP*	Embedded DisplayPort*
Intel® DPST	Intel® Display Power Saving Technology
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to laptops.
Execute Disable Bit	The Execute Disable bit allows memory to be marked as executable or non-executable, when combined with a supporting operating system. If code attempts to run in non-executable memory the processor raises an error to the operating system. This feature can prevent some classes of viruses or worms that exploit buffer overrun vulnerabilities and can thus help improve the overall security of the system. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for more detailed information.
(G)MCH	Legacy component - Graphics Memory Controller Hub

Term	Description
GPU	Graphics Processing Unit
ICH	The legacy I/O Controller Hub component that contains the main PCI interface, LPC interface, USB2, Serial ATA, and other I/O functions. It communicates with the legacy (G)MCH over a proprietary interconnect called DMI.
IMC	Integrated Memory Controller
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture
Intel® FDI	Intel® Flexible Display Interface
Intel® TXT	Intel® Trusted Execution Technology
Intel® VT-d	Intel® Virtualization Technology (Intel® VT) for Directed I/O. Intel VT-d is a hardware assist, under system software (Virtual Machine Manager or OS) control, for enabling I/O device virtualization. Intel VT-d also brings robust security by providing protection from errant DMAs by using DMA remapping, a key feature of Intel VT-d.
Intel® Virtualization Technology	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.
ITPM	Integrated Trusted Platform Module
IOV	I/O Virtualization
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling. A high speed, low power data transmission standard used for display connections to LCD panels.
MCP	Multi-Chip Package.
NCTF	Non-Critical to Function. NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.
Nehalem	Intel’s 45-nm processor design, follow-on to the 45-nm Penryn design.
PCH	Platform Controller Hub. The new, 2009 chipset with centralized platform capabilities including the main I/O interfaces along with display connectivity, audio features, power management, manageability, security and storage features. The PCH may also be referred to using the name (Mobile) Intel® 5 Series Chipset
PECI	Platform Environment Control Interface.
PEG	PCI Express* Graphics. External Graphics using PCI Express Architecture. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications.
Processor	The 64-bit, single-core or multi-core component (package).
Processor Core	The term “processor core” refers to Si die itself which can contain multiple execution cores. Each execution core has an instruction cache, data cache, and 256-KB L2 cache. All execution cores share the L3 cache.
Rank	A unit of DRAM corresponding four to eight devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.



Term	Description
Storage Conditions	A non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
TAC	Thermal Averaging Constant.
TDP	Thermal Design Power.
V_{CC}	Processor core power supply.
V_{SS}	Processor ground.
V_{AXG}	Graphics core power supply.
V_{TT}	L3 shared cache, memory controller, and processor I/O power rail.
V_{DDQ}	DDR3 power rail.
VLD	Variable Length Decoding.
x1	Refers to a Link or Port with one Physical Lane.
x4	Refers to a Link or Port with four Physical Lanes.
x8	Refers to a Link or Port with eight Physical Lanes.
x16	Refers to a Link or Port with sixteen Physical Lanes.

1.8 Related Documents

Refer to the following documents for additional information.

Table 1. Processor Documents

Document	Document Number/ Location
[Calpella] Platform, for Arrandale, Clarksfield and Mobile Intel® 5 Series Chipset – Design Guide	398905
RS - Calpella Small Form Factor (SFF) Platform Design Guide	407364
[Calpella] Platform Power Sequence - Product Specification	393353
[Calpella Platform] Thermal Mechanical Design Guide	386682
Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification	414591
RS - Nehalem Processor Family BIOS Writer's Guide (BWG)	1
RS - Platform Environment Control Interface (PECI) Specification	1
[Calpella] Platform, Arrandale and Clarksfield Processor Testability – Boundary Scan Description Language (BSDL) File	410630
RS - Clarkdale/Arrandale Integrated Memory Controller (IMC) BIOS Specification	1

NOTE:
1. Contact your Intel representative for the latest revision of this item.

Table 2. PCH Documents

Document	Document Number / Location
Intel® 5 Series Express Chipset and Intel® 3400 Series Chipset Platform Controller Hub (PCH) – External Design Specification (EDS)	401376
Intel® 5 Series Express Chipset and Intel® 3400 Series Chipset Platform Controller Hub (PCH) – Thermal Mechanical Specifications & Design Guidelines	407051

Table 3. Public Specifications

Document	Document Number / Location
Advanced Configuration and Power Interface Specification 3.0	http://www.acpi.info/
PCI Local Bus Specification 3.0	http://www.pcisig.com/specifications
PCI Express Base Specification 2.0	http://www.pcisig.com
DDR3 SDRAM Specification	http://www.jedec.org
DisplayPort Specification	http://www.vesa.org
Intel® 64 and IA-32 Architectures Software Developer's Manuals	http://www.intel.com/products/processor/manuals/index.htm
Volume 1: Basic Architecture	253665
Volume 2A: Instruction Set Reference, A-M	253666
Volume 2B: Instruction Set Reference, N-Z	253667
Volume 3A: System Programming Guide	253668
Volume 3B: System Programming Guide	253669

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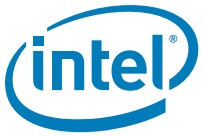


2 Interfaces

This chapter describes the interfaces supported by the processor.

2.1 System Memory Interface

2.1.1 System Memory Technology Supported

The Integrated Memory Controller (IMC) supports DDR3 protocols with two, independent, 64-bit wide channels each accessing one SO-DIMM. It supports a maximum of one, unbuffered non-ECC DDR3 SO-DIMM per-channel thus allowing up to two device ranks per-channel.

DDR3 Data Transfer Rates:

- 800 MT/s (PC3-6400), and 1066 MT/s (PC3-8500)

- DDR3 SO-DIMM Modules:
  - Raw Card A – double-sided x16 unbuffered non-ECC
  - Raw Card B – single-sided x8 unbuffered non-ECC
  - Raw Card C – single-sided x16 unbuffered non-ECC
  - Raw Card D – double-sided x8 (stacked) unbuffered non-ECC
  - Raw Card F – double-sided x8 (planar) unbuffered non-ECC
- DDR3 DRAM Device Technology:
  - Standard 1-Gb, and 2-Gb technologies and addressing are supported for x16 and x8 devices. There is no support for memory modules with different technologies or capacities on opposite sides of the same memory module. If one side of a memory module is populated, the other side is either identical or empty.

Table 4. Supported SO-DIMM Module Configurations[1]

Raw Card Version	DIMM Capacity	DRAM Device Technology	DRAM Organization	# of DRAM Devices	# of Physical Device Ranks	# of Row / Col Address Bits	# of Banks Inside DRAM	Page Size
A	1 GB	1 Gb	64 M x 16	8	2	13/10	8	8K
A	2 GB	2 Gb	128 M x 16	8	2	14/10	8	8K
B	1 GB	1 Gb	128 M x 8	8	1	14/10	8	8K
B	2 GB	2 Gb	256 M x 8	8	1	15/10	8	8K
C	512 MB	1 Gb	64 M x 16	4	1	13/10	8	8K
C	1 GB	2 Gb	128 M x 16	4	1	14/10	8	8K
D[2]	4 GB	2 Gb	256 M x 8	16	2	15/10	8	8K
F	2 GB	1 Gb	128 M x 8	16	2	14/10	8	8K
F	4 GB	2 Gb	256 M x 8	16	2	15/10	8	8K

NOTES:
1. System memory configurations are based on availability and are subject to change.
2. Only Raw Card D SO-DIMMS at 1066 MT/s are supported.

2.1.2 System Memory Timing Support

The IMC supports the following DDR3 Speed Bin, CAS Write Latency (CWL), and command signal mode timings on the main memory interface:

- tCL = CAS Latency
- tRCD = Activate Command to READ or WRITE Command delay
- tRP = PRECHARGE Command Period
- CWL = CAS Write Latency
- Command Signal modes = 1n indicates a new command may be issued every clock and 2n indicates a new command may be issued every 2 clocks. Command launch mode programming depends on the transfer rate and memory configuration.

Table 5. DDR3 System Memory Timing Support

Transfer Rate (MT/s)	tCL (tCK)	tRCD (tCK)	tRP (tCK)	CWL (tCK)	CMD Mode	Notes
800	6	6	6	5	1n	1
1066	7	7	7	6	1n	1
	8	8	8			

NOTES:
1. System memory timing support is based on availability and is subject to change.

2.1.3 System Memory Organization Modes

The IMC supports two memory organization modes, single-channel and dual-channel. Depending upon how the SO-DIMM Modules are populated in each memory channel, a number of different configurations can exist.

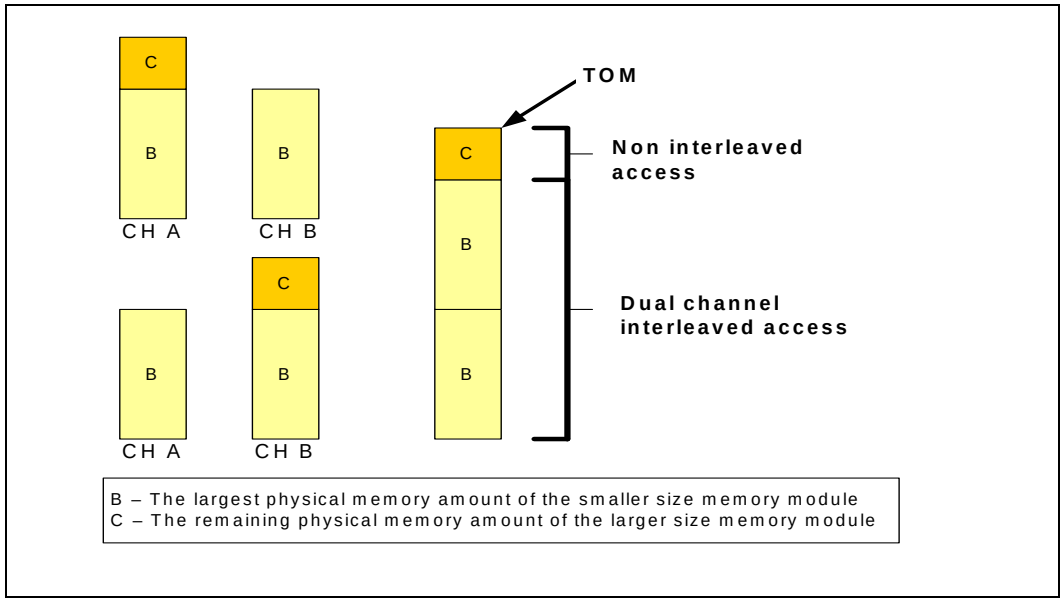
2.1.3.1 Single-Channel Mode

In this mode, all memory cycles are directed to a single-channel. Single-channel mode is used when either Channel A or Channel B SO-DIMM connectors are populated in any order, but not both.

2.1.3.2 Dual-Channel Mode - Intel® Flex Memory Technology Mode

The IMC supports Intel Flex Memory Technology Mode. This mode combines the advantages of the Dual-Channel Symmetric (Interleaved) and Dual-Channel Asymmetric Modes. Memory is divided into a symmetric and a asymmetric zone. The symmetric zone starts at the lowest address in each channel and is contiguous until the asymmetric zone begins or until the top address of the channel with the smaller capacity is reached. In this mode, the system runs with one zone of dual-channel mode and one zone of single-channel mode, simultaneously, across the whole memory array.

Figure 2. Intel Flex Memory Technology Operation



2.1.3.2.1 Dual-Channel Symmetric Mode

Dual-Channel Symmetric mode, also known as interleaved mode, provides maximum performance on real world applications. Addresses are ping-ponged between the channels after each cache line (64-byte boundary). If there are two requests, and the second request is to an address on the opposite channel from the first, that request can be sent before data from the first request has returned. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are ensured to be on opposite channels. Use Dual-Channel Symmetric mode when both Channel A and Channel B SO-DIMM connectors are populated in any order, with the total amount of memory in each channel being the same.

When both channels are populated with the same memory capacity and the boundary between the dual channel zone and the single channel zone is the top of memory, IMC operates completely in Dual-Channel Symmetric mode.

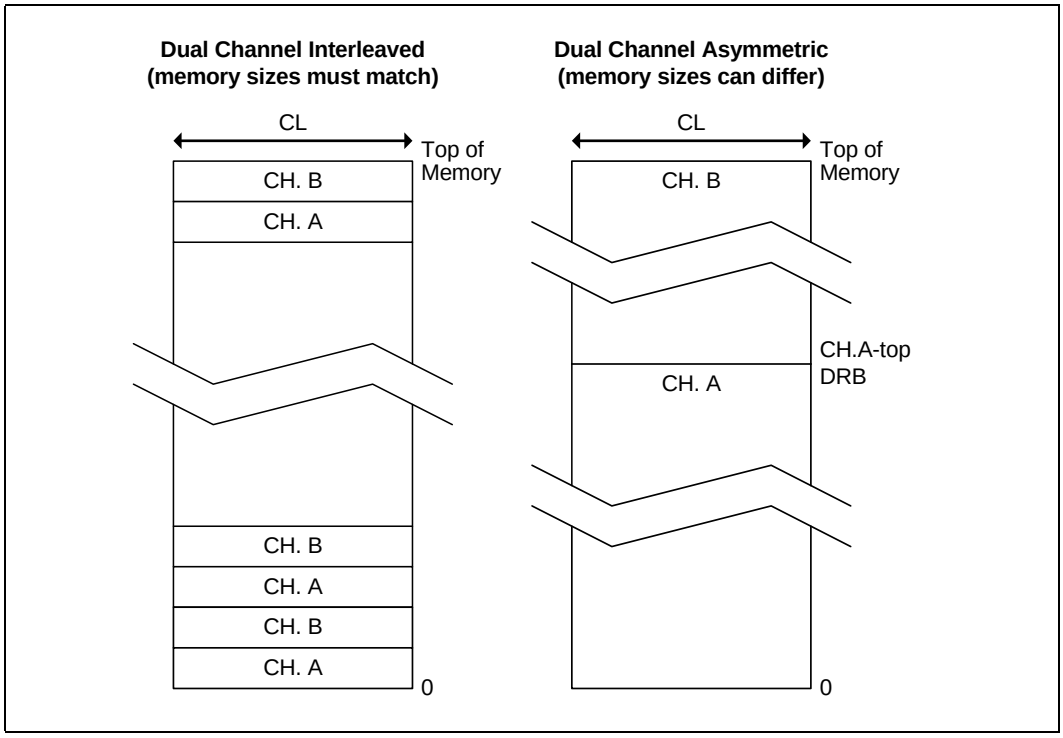
Note: The DRAM device technology and width may vary from one channel to the other.

2.1.3.2.2 Dual-Channel Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start at the bottom of Channel A and stay there until the end of the highest rank in Channel A, and then addresses continue from the bottom of Channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth is limited to a single channel.

This mode is used when Intel Flex Memory Technology is disabled and both Channel A and Channel B SO-DIMM connectors are populated in any order with the total amount of memory in each channel being different.

Figure 3. Dual-Channel Symmetric (Interleaved) and Dual-Channel Asymmetric Modes



2.1.4 Rules for Populating Memory Slots

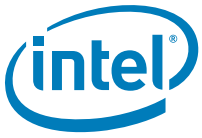
In all modes, the frequency of system memory is the lowest frequency of all memory modules placed in the system, as determined through the SPD registers on the memory modules. The system memory controller supports only one SO-DIMM connector per channel. For dual-channel modes both channels must have an SO-DIMM connector populated. For single-channel mode, only a single-channel can have an SO-DIMM connector populated.

2.1.5 Technology Enhancements of Intel® Fast Memory Access (Intel® FMA)

The following sections describe the Just-in-Time Scheduling, Command Overlap, and Out-of-Order Scheduling Intel FMA technology enhancements.

2.1.5.1 Just-in-Time Command Scheduling

The memory controller has an advanced command scheduler where all pending requests are examined simultaneously to determine the most efficient request to be issued next. The most efficient request is picked from all pending requests and issued to system memory Just-in-Time to make optimal use of Command Overlapping. Thus, instead of having all memory access requests go individually through an arbitration mechanism forcing requests to be executed one at a time, they can be started without interfering with the current request allowing for concurrent issuing of requests. This allows for optimized bandwidth and reduced latency while maintaining appropriate command spacing to meet system memory protocol.



2.1.5.2 Command Overlap

Command Overlap allows the insertion of the DRAM commands between the Activate, Precharge, and Read/Write commands normally used, as long as the inserted commands do not affect the currently executing command. Multiple commands can be issued in an overlapping manner, increasing the efficiency of system memory protocol.

2.1.5.3 Out-of-Order Scheduling

While leveraging the Just-in-Time Scheduling and Command Overlap enhancements, the IMC continuously monitors pending requests to system memory for the best use of bandwidth and reduction of latency. If there are multiple requests to the same open page, these requests would be launched in a back to back manner to make optimum use of the open memory page. This ability to reorder requests on the fly allows the IMC to further reduce latency and increase bandwidth efficiency.

2.1.6 DRAM Clock Generation

Every supported SO-DIMM has two differential clock pairs. There are total of four clock pairs driven directly by the processor to two SO-DIMMs.

2.1.7 System Memory Pre-Charge Power Down Support Details

The IMC supports and enables slow exit DDR3 DRAM Device pre-charge power down DLL control. During a pre-charge power down, a slow exit is where the DRAM device DLL is disabled after entering pre-charge power down for potential power savings.

2.2 PCI Express Interface

This section describes the PCI Express interface capabilities of the processor. See the *PCI Express Base Specification* for details of PCI Express.

The processor has one PCI Express controller that can support one external x16 PCI Express Graphics Device or two external x8 PCI Express Graphics Devices. The primary PCI Express Graphics port is referred to as PEG 0 and the secondary PCI Express Graphics port is referred to as PEG 1.

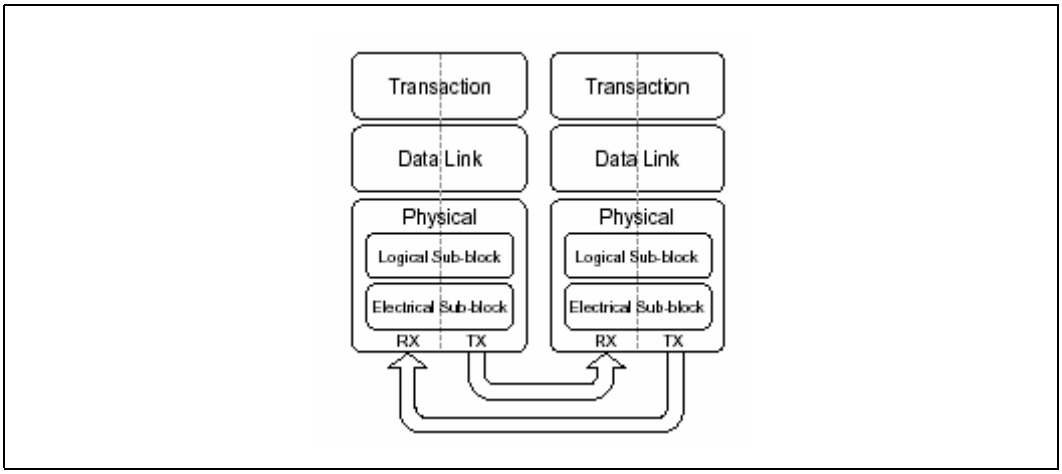
2.2.1 PCI Express Architecture

Compatibility with the PCI addressing model is maintained to ensure that all existing applications and drivers operate unchanged.

The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial recovered clock speed of 1.25 GHz results in 2.5 Gb/s/direction which provides a 250 MB/s communications channel in each direction (500 MB/s total). That is close to twice the data rate of classic PCI. The fact that 8b/10b encoding is used accounts for the 250 MB/s where quick calculations would imply 300 MB/s.

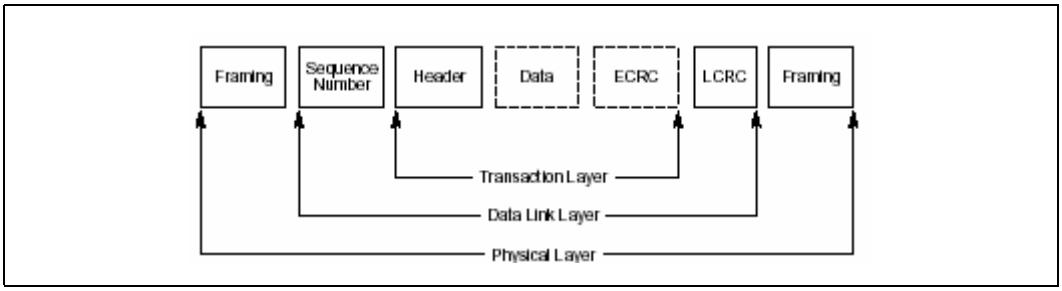
The PCI Express architecture is specified in three layers: Transaction Layer, Data Link Layer, and Physical Layer. The partitioning in the component is not necessarily along these same boundaries. Refer to Figure 4 for the PCI Express Layering Diagram.

Figure 4. PCI Express Layering Diagram



PCI Express uses packets to communicate information between components. Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side, the reverse process occurs and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device.

Figure 5. Packet Flow through the Layers



2.2.1.1 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

2.2.1.2 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

The transmission side of the Data Link Layer accepts TLPs assembled by the Transaction Layer, calculates and applies data protection code and TLP sequence number, and submits them to Physical Layer for transmission across the Link. The

receiving Data Link Layer is responsible for checking the integrity of received TLPs and for submitting them to the Transaction Layer for further processing. On detection of TLP error(s), this layer is responsible for requesting retransmission of TLPs until information is correctly received, or the Link is determined to have failed. The Data Link Layer also generates and consumes packets which are used for Link management functions.

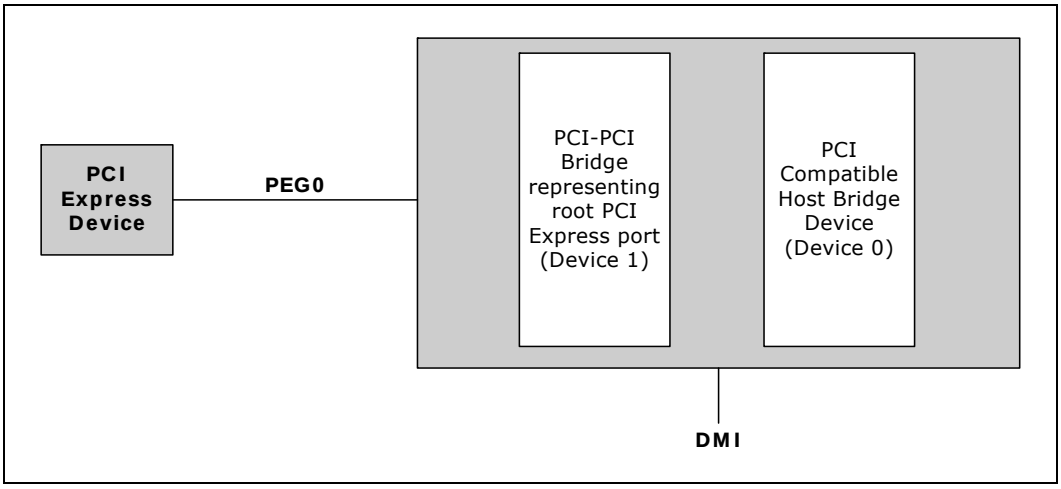
2.2.1.3 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry. It also includes logical functions related to interface initialization and maintenance. The Physical Layer exchanges data with the Data Link Layer in an implementation-specific format, and is responsible for converting this to an appropriate serialized format and transmitting it across the PCI Express Link at a frequency and width compatible with the remote device.

2.2.2 PCI Express Configuration Mechanism

The PCI Express (external graphics) link is mapped through a PCI-to-PCI bridge structure.

Figure 6. PCI Express Related Register Structures in the Processor



PCI Express extends the configuration space to 4096 bytes per-device/function, as compared to 256 bytes allowed by the *Conventional PCI Specification*. PCI Express configuration space is divided into a PCI-compatible region (which consists of the first 256 bytes of a logical device's configuration space) and an extended PCI Express region (which consists of the remaining configuration space). The PCI-compatible region can be accessed using either the mechanisms defined in the PCI specification or using the enhanced PCI Express configuration access mechanism described in the *PCI Express Enhanced Configuration Mechanism* section.

The PCI Express Host Bridge is required to translate the memory-mapped PCI Express configuration space accesses from the host processor to PCI Express configuration cycles. To maintain compatibility with PCI configuration addressing mechanisms, it is recommended that system software access the enhanced configuration space using 32-bit operations (32-bit aligned) only. See the *PCI Express Base Specification* for details of both the PCI-compatible and PCI Express Enhanced configuration mechanisms and transaction rules.

2.2.3 PCI Express* Ports and Bifurcation

The external graphics attach (PEG) on the processor is a single, 16-lane (x16) port that can be:

- configured at narrower widths
- bifucated into two x8 PCI Express ports that may train to narrower widths

The PEG port is being designed to be compliant with the *PCI Express Base Specification, Revision 2.0.*

2.2.3.1 PCI Express Bifurcated Mode

When bifurcated, the signals which had previously been assigned to Lanes 15:8 of the single x16 Primary port are reassigned to lanes 7:0 of the x8 Secondary Port. This assignment applies whether the lane numbering is reversed or not. PCI Express Port 0 is mapped to PCI Device 1 and PCI Express Port 1 is mapped to PCI Device 6.

2.2.3.2 Static Lane Numbering Reversal

Does not support dynamic lane reversal, as defined (optional) by the *PCI Express Base Specification.*

PCI Express 1x16 configuration:

- Normal (1x16): PEG_RX[15:0]; PEG_TX[15:0]
- Reversal (1x16): PEG_RX[0:15]; PEG_TX[0:15]

PCI Express 2x8 configration

- Normal (Port 0): PEG_RX[7:0]; PEG_TX[7:0]
- Normal (Port 1): PEG_RX[15:8]; PEG_TX[15:8]
- Reversal (Port 0): PEG_RX[8:15]; PEG_TX[8:15]
- Reversal (Port 1): PEG_RX[0:7]; PEG_TX[0:7]

2.3 DMI

DMI connects the processor and the PCH chip-to-chip. DMI2 is supported. The DMI is similar to a four-lane PCI Express supporting up to 1 GB/s of bandwidth in each direction.

Note: Only DMI x4 configuration is supported.

2.3.1 DMI Error Flow

DMI can only generate SERR in response to errors, never SCI, SMI, MSI, PCI INT, or GPE. Any DMI related SERR activity is associated with Device 0.

2.3.2 Processor/PCH Compatibility Assumptions

The processor is compatible with the PCH and is not compatible with any previous (G)MCH or ICH products.

2.3.3 DMI Link Down

The DMI link going down is a fatal, unrecoverable error. If the DMI data link goes to data link down, after the link was up, then the DMI link hangs the system by not allowing the link to retrain to prevent data corruption. This is controlled by the PCH.

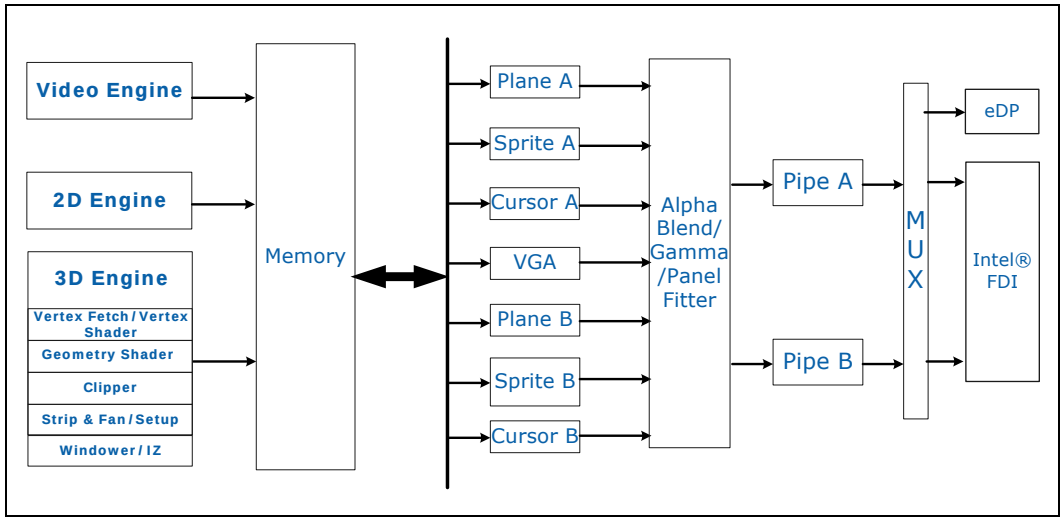
Downstream transactions that had been successfully transmitted across the link prior to the link going down may be processed as normal. No completions from downstream, non-posted transactions are returned upstream over the DMI link after a link down event.

2.4 Intel® HD Graphics Controller

This section details the 2D, 3D and video pipeline and their respective capabilities.

The integrated graphics is powered by a refresh of the fifth generation graphics core and supports twelve, fully-programmable execution cores. Full-precision, floating-point operations are supported to enhance the visual experience of compute-intensive applications.The integrated graphics controller contains several types of components; the graphics engines, planes, pipes, port and the Intel FDI. The integrated graphics has a 3D/2D Instruction Processing unit to control the 3D and 2D engines respectively. The integrated graphics controller's 3D and 2D engines are fed with data through the IMC. The outputs of the graphics engine are surfaces sent to memory, which are then retrieved and processed by the planes. The surfaces are then blended in the pipes and the display timings are transitioned from display core clock to the pixel (dot) clock.

Figure 7. Integrated Graphics Controller Unit Block Diagram



2.4.1 3D and Video Engines for Graphics Processing

The 3D graphics pipeline architecture simultaneously operates on different primitives or on different portions of the same primitive. All the cores are fully programmable, increasing the versatility of the 3D Engine. The Gen 5.75 3D engine provides the following performance and power-management enhancements:

- Execution units (EUs) increased to 12 from the previous 10 EUsin Gen 5.0.
- Includes Hierarchal-Z
- Includes video quality enhancements

2.4.1.1 3D Engine Execution Units

- Support 12 EUs. The EUs perform 128-bit wide execution per clock.
- Support SIMD8 instructions for vertex processing and SIMD16 instructions for pixel processing.

2.4.1.2 3D Pipeline

2.4.1.2.1 Vertex Fetch (VF) Stage

The VF stage executes 3DPRIMITIVE commands. Some enhancements have been included to better support legacy D3D APIs as well as SGI OpenGL*.

2.4.1.2.2 Vertex Shader (VS) Stage

The VS stage performs shading of vertices output by the VF function. The VS unit produces an output vertex reference for every input vertex reference received from the VF unit, in the order received.

2.4.1.2.3 Geometry Shader (GS) Stage

The GS stage receives inputs from the VS stage. Compiled application-provided GS programs, specifying an algorithm to convert the vertices of an input object into some output primitives. For example, a GS shader may convert lines of a line strip into polygons representing a corresponding segment of a blade of grass centered on the line. Or it could use adjacency information to detect silhouette edges of triangles and output polygons extruding out from the edges.

2.4.1.2.4 Clip Stage

The Clip stage performs general processing on incoming 3D objects. However, it also includes specialized logic to perform a Clip Test function on incoming objects. The Clip Test optimizes generalized 3D Clipping. The Clip unit examines the position of incoming vertices, and accepts/rejects 3D objects based on its Clip algorithm.

2.4.1.2.5 Strips and Fans (SF) Stage

The SF stage performs setup operations required to rasterize 3D objects. The outputs from the SF stage to the Windower stage contain implementation-specific information required for the rasterization of objects and also supports clipping of primitives to some extent.

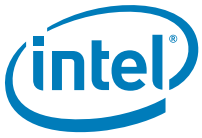
2.4.1.2.6 Windower/IZ (WIZ) Stage

The WIZ unit performs an early depth test, which removes failing pixels and eliminates unnecessary processing overhead.

The Windower uses the parameters provided by the SF unit in the object-specific rasterization algorithms. The WIZ unit rasterizes objects into the corresponding set of pixels. The Windower is also capable of performing dithering, whereby the illusion of a higher resolution when using low-bpp channels in color buffers is possible. Color dithering diffuses the sharp color bands seen on smooth-shaded objects.

2.4.1.3 Video Engine

The Video Engine handles the non-3D (media/video) applications. It includes support for VLD and MPEG2 decode in hardware.



2.4.1.4 2D Engine

The 2D Engine contains BLT (Block Level Transfer) functionality and an extensive set of 2D instructions. To take advantage of the 3D during engine's functionality, some BLT functions make use of the 3D renderer.

2.4.1.4.1 Integrated Graphics VGA Registers

The 2D registers consists of original VGA registers and others to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

2.4.1.4.2 Logical 128-Bit Fixed BLT and 256 Fill Engine

This BLT engine accelerates the GUI of Microsoft Windows* operating systems. The 128-bit BLT engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data alignment
- To perform logical operations (raster ops)

The rectangular block of data does not change, as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern is always 8 x 8 pixels wide and may be 8, 16, or 32 bits per pixel.

The BLT engine expands monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the BLT engine specifies which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (source, pattern, and destination) defined by Microsoft, including transparent BLT.

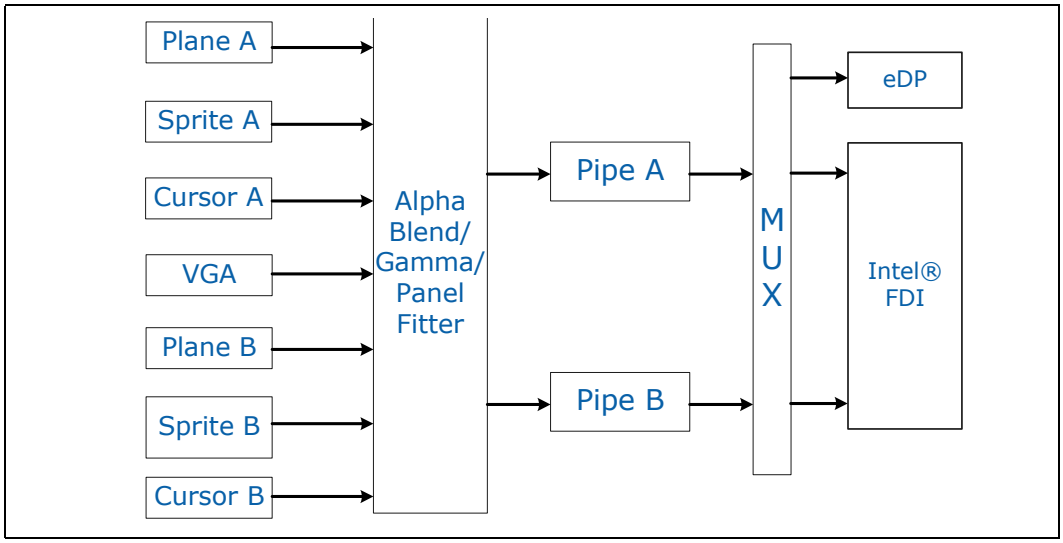
The BLT engine has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The BLT engine can perform hardware clipping during BLTs.

2.4.2 Integrated Graphics Display Pipes

The integrated graphics controller display pipe can be broken down into three components:

- Display Planes
- Display Pipes
- Embedded DisplayPort and Intel FDI

Figure 8. Processor Display Block Diagram



2.4.2.1 Display Planes

A display plane is a single displayed surface in memory and contains one image (desktop, cursor, overlay). It is the portion of the display HW logic that defines the format and location of a rectangular region of memory that can be displayed on display output device and delivers that data to a display pipe. This is clocked by the Core Display Clock.

2.4.2.1.1 Planes A and B

Planes A and B are the main display planes and are associated with Pipes A and B respectively. The two display pipes are independent, allowing for support of two independent display streams. They are both double-buffered, which minimizes latency and improves visual quality.

2.4.2.1.2 Sprite A and B

Sprite A and Sprite B are planes optimized for video decode, and are associated with Planes A and B respectively. Sprite A and B are also double-buffered.

2.4.2.1.3 Cursors A and B

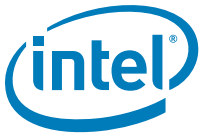
Cursors A and B are small, fixed-sized planes dedicated for mouse cursor acceleration, and are associated with Planes A and B respectively. These planes support resolutions up to 256 x 256 each.

2.4.2.1.4 VGA

Used for boot, safe mode, legacy games, etc. Can be changed by an application without OS/driver notification, due to legacy requirements.

2.4.2.2 Display Pipes

The display pipe blends and synchronizes pixel data received from one or more display planes and adds the timing of the display output device upon which the image is displayed. This is clocked by the Display Reference clock inputs.



The display pipes A and B operate independently of each other at the rate of 1 pixel per clock. They can attach to any of the display ports. Each pipe sends display data to the PCH over the Intel Flexible Display Interface (Intel FDI).

2.4.2.3 Display Ports

The display ports consist of output logic and pins that transmit the display data to the associated encoding logic and send the data to the display device (i.e., LVDS, HDMI, DVI, SDVO, etc.). All display interfaces connecting external displays are now repartitioned and driven from the PCH with the exception of the eDP DisplayPort. Refer to the Calpella Platform Design Guide and the PCH EDS for more details on DisplayPort support on the Calpella platform.

2.4.2.4 Embedded DisplayPort (eDP)

The DisplayPort abbreviated as DP (different than the generic term display port) specification is a VESA standard. DisplayPort consolidates internal and external connection methods to reduce device complexity, support cross industry applications, and provide performance scalability. The integrated graphics supports an embedded DisplayPort (eDP) interface for display devices that are integrated into the system (e.g., laptop LCD panel). All other display interfaces connecting to the LVDS or external panels are driven from the PCH.

The eDP interface is physically shared with a subset of the PCIe interface. Specifically, eDP[3:0] map to Logical Lanes PEG[12:15] of the PCIe interface. Mapping for reversed case is: eDP[3:0] maps to PEG[3:0], ex: eDP[0]=PEG[15] in non reversed case. In reversed case: eDP[0] = PEG[0].

Table 6. eDP/PEG Ball Mapping

eDP Signal	PEG Signal	Lane Reversal
eDP_AUX	PEG_RX[13]	PEG_RX[2]
eDP_AUX#	PEG_RX#[13]	PEG_RX#[2]
eDP_HPD#	PEG_RX[12]	PEG_RX[3]
eDP_TX[0]	PEG_TX[15]	PEG_TX[0]
eDP_TX#[0]	PEG_TX#[15]	PEG_TX#[0]
eDP_TX[1]	PEG_TX[14]	PEG_TX[1]
eDP_TX#[1]	PEG_TX#[14]	PEG_TX#[1]
eDP_TX[2]	PEG_TX[13]	PEG_TX[2]
eDP_TX#[2]	PEG_TX#[13]	PEG_TX#[2]
eDP_TX[3]	PEG_TX[12]	PEG_TX[3]
eDP_TX#[3]	PEG_TX#[12]	PEG_TX#[3]

When eDP is enabled, the lower logical lanes are still available for standard PCIe devices, using the PEG 0 controller. PEG 0 is limited to x1. The board manufacture chooses whether to use eDP and whether to use lane numbering reversal.

The eDP interface supports link-speeds of 1.62 Gbps and 2.7 Gbps on 1, 2 or 4 data lanes. The eDP and PCI Express x1 may be supported concurrently. eDP interface may support -0.5% SSC and non-SSC clock settings.

2.4.3 Intel Flexible Display Interface

The Intel Flexible Display Interface (Intel FDI) is a proprietary link for carrying display traffic from the integrated graphics controller to the PCH display I/O's. Intel FDI supports two independent channels; one for pipe A and one for pipe B.

- Each channel has four transmit (Tx) differential pairs used for transporting pixel and framing data from the display engine.
- Each channel has one single-ended LineSync and one FrameSync input (1-V CMOS signaling).
- One display interrupt line input (1-V CMOS signaling).
- Intel FDI may dynamically scalable down to 2X or 1X based on actual display bandwidth requirements.
- Common 100-MHz reference clock is sent to both processor and PCH.
- Each channel transports at a rate of 2.7 Gbps.
- PCH supports end-to-end lane reversal across both channels (no reversal support required)

2.5 Platform Environment Control Interface (PECI)

The PECI is a one-wire interface that provides a communication channel between a PECI client (processor) and a PECI master, usually the PCH. The processor implements a PECI interface to:

- Allow communication of processor thermal and other information to the PECI master.
- Read averaged Digital Thermal Sensor (DTS) values for fan speed control.

2.6 Interface Clocking

2.6.1 Internal Clocking Requirements

Table 7. Processor Reference Clocks

Reference Input Clocks	Input Frequency	Associated PLL
BCLK/BCLK#	133 MHz	Processor/Memory/Graphics
PEG_CLK/PEG_CLK#	100 MHz	PCI Express*/DMI/Intel® FDI
DPLL_REF_SSCLK/DPLL_REF_SSCLK#	120 MHz	Embedded DisplayPort* (eDP)

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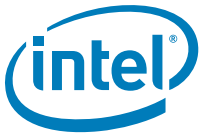


3 Technologies

3.1 Intel® Virtualization Technology (Intel® VT)

Intel Virtualization Technology (Intel VT) is the technology that makes a single system appear as multiple independent systems to software. This allows multiple, independent operating systems to be running simultaneously on a single system. Intel VT comprises technology components to support virtualization of platforms based on Intel architecture microprocessors and chipsets. Intel Virtualization Technology (Intel VT-x) added hardware support in the processor to improve the virtualization performance and robustness. Intel Virtualization Technology for Directed I/O (Intel VT-d) adds chipset hardware implementation to support and improve I/O virtualization performance and robustness.

Intel VT-x specifications and functional descriptions are included in the *Intel® 64 and IA-32 Architectures Software Developer's Manual, Volume 3B* and is available at http://www.intel.com/products/processor/manuals/index.htm.

The Intel VT-d spec and other Intel VT documents can be referenced at http://www.intel.com/technology/virtualization/index.htm.

3.1.1 Intel® VT-x Objectives

Intel VT-x provides hardware acceleration for virtualization of IA platforms. Virtual Machine Monitor (VMM) can use Intel VT-x features to provide improved reliable virtualized platform. By using Intel VT-x, a VMM is:

- **Robust:** VMMs no longer need to use para-virtualization or binary translation. This means that they will be able to run off-the-shelf operating systems and applications without any special steps.
- **Enhanced:** Intel VT enables VMMs to run 64-bit guest operating systems on IA x86 processors.
- **More reliable:** Due to the hardware support, VMMs can now be smaller, less complex, and more efficient. This improves reliability and availability and reduces the potential for software conflicts.
- **More secure:** The use of hardware transitions in the VMM strengthens the isolation of VMs and further prevents corruption of one VM from affecting others on the same system.

3.1.2 Intel VT-x Features

The processor core supports the following, new, Intel VT-x features:

- Extended Page Tables (EPT)
  - Hardware-assisted page table virtualization.
  - Eliminates VM exits from guest OS to the VMM for shadow page-table maintenance.
- Virtual Processor IDs (VPID)
  - Ability to assign a VM ID to tag processor core hardware structures (e.g., TLBs).
  - Avoids flushes on VM transitions to give a lower-cost VM transition time and an overall reduction in virtualization overhead.
- Guest Preemption Timer
  - Mechanism for a VMM to preempt the execution of a guest OS after an amount of time specified by the VMM. The VMM sets a timer value before entering a guest.
  - The feature aids VMM developers in flexibility and Quality of Service (QoS) guarantees.
- Descriptor-Table Exiting
  - Descriptor-table exiting allows a VMM to protect a guest OS from internal (malicious software based) attack by preventing relocation of key system data structures like IDT (interrupt descriptor table), GDT (global descriptor table), LDT (local descriptor table), and TSS (task segment selector).
  - A VMM using this feature can intercept (by a VM exit) attempts to relocate these data structures and prevent them from being tampered by malicious software.

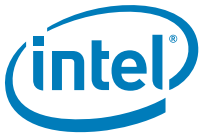
3.2 Intel® Graphics Dynamic Frequency

3.2.1 Intel Graphics Dynamic Frequency

Graphics render frequency are selected by the Intel graphics driver dynamically based on graphics workload demand as permitted by Intel Turbo Boost Technology Driver. Intel Turbo Boost Technology Driver can optimize both processor and integrated graphics performance through Intelligent Power Sharing. The processor core die and the integrated graphics and memory controller core die have an individual TDP limit. If one component is not consuming enough thermal power to reach its TDP, the other component can increase its TDP limit and take advantage of the unused thermal power headroom. For the integrated graphics, this could mean an increase in the render core frequency (above its rated frequency) and increased graphics performance.

Processor Utilization of Intel Graphics Dynamic Frequency require the following

- Graphics driver
- Intel Turbo Boost Technology Driver



Enabling Intel Graphics Dynamic Frequency will maximize the performance of the processor core and the GPU within its specified power levels. Compared with previous generation products, Intel Graphics Dynamic Frequency will increase the ratio of application power to TDP. Thus, thermal solutions and platform cooling that are designed to less than thermal design guidance might experience thermal and performance issues since more applications will tend to run at the maximum power limit for significant periods of time. For more details, refer to Chapter 5, “Thermal Management”.

§

4 Power Management

This chapter provides information on the following power management topics:

- ACPI States
- Processor Core
- Integrated Memory Controller (IMC)
- PCI Express
- Direct Media Interface (DMI)
- Integrated Graphics Controller

4.1 ACPI States Supported

The ACPI states supported by the processor are described in this section.

4.1.1 System States

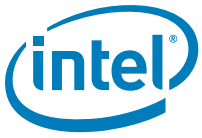
Table 8. System States

State	Description
G0/S0	Full On
G1/S3-Cold	Suspend-to-RAM (STR). Context saved to memory (S3-Hot is not supported by the processor).
G1/S4	Suspend-to-Disk (STD). All power lost (except wakeup on PCH).
G2/S5	Soft off. All power lost (except wakeup on PCH). Total reboot.
G3	Mechanical off. All power (AC and battery) removed from system.

4.1.2 Processor Core/Package Idle States

Table 9. Processor Core/Package State Support

State	Description
C0	Active mode, processor executing code.
C1	AutoHALT state.
C1E	AutoHALT state with lowest frequency and voltage operating point.
C3	Execution cores in C3 flush their L1 instruction cache, L1 data cache, and L2 cache to the L3 shared cache. Clocks are shut off to each core.
C6	Execution cores in this state save their architectural state before removing core voltage.



4.1.3 Integrated Memory Controller States

Table 10. Integrated Memory Controller States

State	Description
Power up	CKE asserted. Active mode.
Pre-charge Power down	CKE deasserted (not self-refresh) with all banks closed.
Active Power down	CKE deasserted (not self-refresh) with minimum one bank active.
Self-Refresh	CKE deasserted using device self-refresh.

4.1.4 PCIe Link States

Table 11. PCIe Link States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.

4.1.5 DMI States

Table 12. DMI States

State	Description
L0	Full on – Active transfer state.
L0s	First Active Power Management low power state – Low exit latency.
L1	Lowest Active Power Management - Longer exit latency.
L3	Lowest power state (power-off) – Longest exit latency.

4.1.6 Integrated Graphics Controller States

Table 13. Integrated Graphics Controller States

State	Description
D0	Full on, display active.
D3 Cold	Power-off.

4.1.7 Interface State Combinations

Table 14. G, S and C State Combinations

Global (G) State	Sleep (S) State	Processor Core (C) State	Processor State	System Clocks	Description
G0	S0	C0	Full On	On	Full On
G0	S0	C1/C1E	Auto-Halt	On	Auto-Halt
G0	S0	C3	Deep Sleep	On	Deep Sleep
G0	S0	C6	Deep Power Down	On	Deep Power Down
G1	S3	Power off		Off, except RTC	Suspend to RAM
G1	S4	Power off		Off, except RTC	Suspend to Disk
G2	S5	Power off		Off, except RTC	Soft Off
G3	NA	Power off		Power off	Hard off

Table 15. D, S, and C State Combination

Graphics Adapter (D) State	Sleep (S) State	Package (C) State	Description
D0	S0	C0	Full On, Displaying
D0	S0	C1/C1E	Auto-Halt, Displaying
D0	S0	C3	Deep sleep, Displaying
D0	S0	C6	Deep Power Down, Displaying
D3	S0	Any	Not displaying
D3	S3	N/A	Not displaying, Graphics Core is powered off
D3	S4	N/A	Not displaying, suspend to disk

4.2 Processor Core Power Management

While executing code, Enhanced Intel SpeedStep Technology optimizes the processor's frequency and core voltage based on workload. Each frequency and voltage operating point is defined by ACPI as a P-state. When the processor is not executing code, it is idle. A low-power idle state is defined by ACPI as a C-state. In general, lower power C-states have longer entry and exit latencies.

4.2.1 Enhanced Intel SpeedStep® Technology

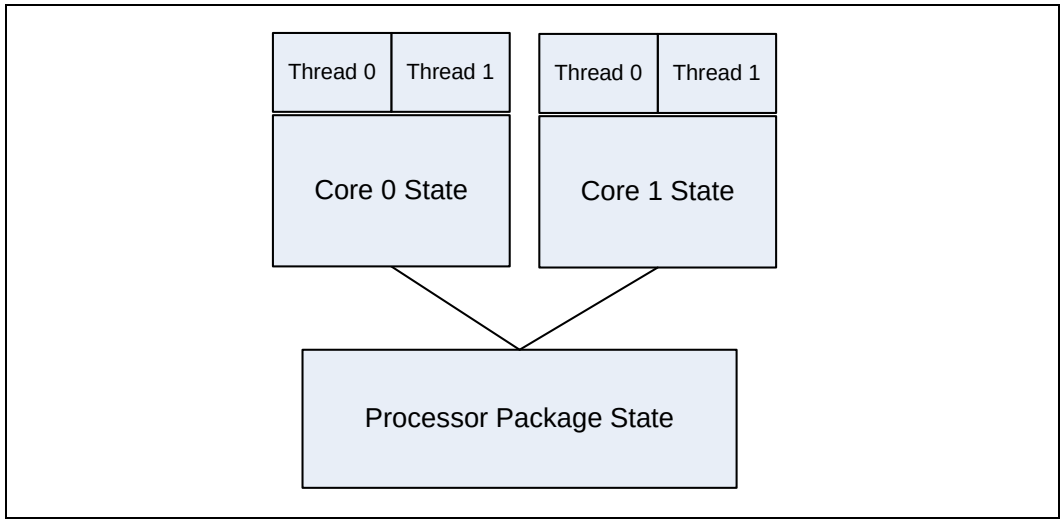
The following are the key features of Enhanced Intel SpeedStep Technology:

- Multiple frequency and voltage points for optimal performance and power efficiency. These operating points are known as P-states.
- Frequency selection is software controlled by writing to processor MSRs. The voltage is optimized based on the selected frequency and the number of active processor cores.
  - If the target frequency is higher than the current frequency, V_{CC} is ramped up in steps to an optimized voltage. This voltage is signaled by the VID[6:0] pins to the voltage regulator. Once the voltage is established, the PLL locks on to the target frequency.
  - If the target frequency is lower than the current frequency, the PLL locks to the target frequency, then transitions to a lower voltage by signaling the target voltage on the VID[6:0] pins.
  - All active processor cores share the same frequency and voltage. In a multi-core processor, the highest frequency P-state requested amongst all active cores is selected.
  - Software-requested transitions are accepted at any time. If a previous transition is in progress, the new transition is deferred until the previous transition is completed.
- The processor controls voltage ramp rates internally to ensure glitch-free transitions.
- Because there is low transition latency between P-states, a significant number of transitions per-second are possible.

4.2.2 Low-Power Idle States

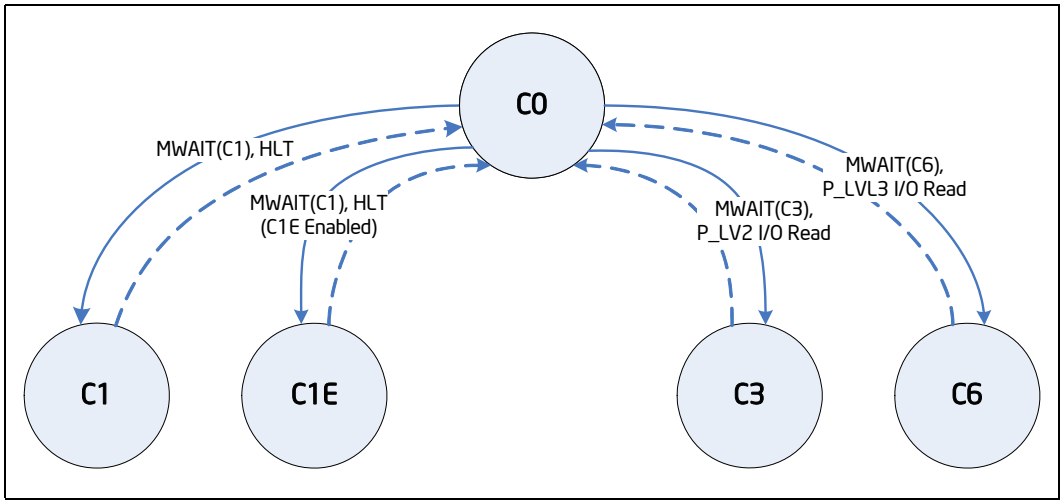
When the processor is idle, low-power idle states (C-states) are used to save power. More power savings actions are taken for numerically higher C-states. However, higher C-states have longer exit and entry latencies. Resolution of C-states occur at the thread, processor core, and processor package level. Thread-level C-states are available if Intel Hyper-Threading Technology is enabled.

Figure 9. Idle Power Management Breakdown of the Processor Cores



Entry and exit of the C-States at the thread and core level are shown in Figure 10.

Figure 10. Thread and Core C-State Entry and Exit



While individual threads can request low power C-states, power saving actions only take place once the core C-state is resolved. Core C-states are automatically resolved by the processor. For thread and core C-states, a transition to and from C0 is required before entering any other C-state.

Table 16. Coordination of Thread Power States at the Core Level

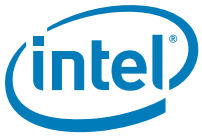
Processor Core C-State		Thread 1			
		C0	C1	C3	C6
Thread 0	C0	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

NOTE: If enabled, the core C-state will be C1E if all actives cores have also resolved a core C1 state or higher

4.2.3 Requesting Low-Power Idle States

The primary software interfaces for requesting low power idle states are through the MWAIT instruction with sub-state hints and the HLT instruction (for C1 and C1E). However, software may make C-state requests using the legacy method of I/O reads from the ACPI-defined processor clock control registers, referred to as P_LVLx. This method of requesting C-states provides legacy support for operating systems that initiate C-state transitions via I/O reads.

For legacy operating systems, P_LVLx I/O reads are converted within the processor to the equivalent MWAIT C-state request. Therefore, P_LVLx reads do not directly result in I/O reads to the system. The feature, known as I/O MWAIT redirection, must be enabled in the BIOS. To enable it, refer to the *RS-Nehalem Processor Family BIOS Writer's Guide (BWG)*.



Note: The P_LVLx I/O Monitor address needs to be set up before using the P_LVLx I/O read interface. Each P-LVLx is mapped to the supported MWAIT(Cx) instruction as follows.

Table 17. P_LVLx to MWAIT Conversion

P_LVLx	MWAIT(Cx)	Notes
P_LVL2	MWAIT(C3)	The P_LVL2 base address is defined in the PMG_IO_CAPTURE MSR, described in the *RS - Nehalem Processor Family BWG*.
P_LVL3	MWAIT(C6)	C6. No sub-states allowed.

The BIOS can write to the C-state range field of the PMG_IO_CAPTURE MSR to restrict the range of I/O addresses that are trapped and emulate MWAIT like functionality. Any P_LVLx reads outside of this range does not cause an I/O redirection to MWAIT(Cx) like request. They fall through like a normal I/O instruction.

Note: When P_LVLx I/O instructions are used, MWAIT substates cannot be defined. The MWAIT substate is always zero if I/O MWAIT redirection is used. By default, P_LVLx I/O redirections enable the MWAIT 'break on EFLAGS.IF' feature which triggers a wakeup on an interrupt even if interrupts are masked by EFLAGS.IF.

4.2.4 Core C-states

The following are general rules for all core C-states, unless specified otherwise:

- A core C-State is determined by the lowest numerical thread state (e.g., Thread 0 requests C1E while Thread 1 requests C3, resulting in a core C1E state). See Table 14.
- A core transitions to C0 state when:
  - An interrupt occurs
  - There is an access to the monitored address if the state was entered via an MWAIT instruction
- For core C1/C1E, and core C3, an interrupt directed toward a single thread wakes only that thread. However, since both threads are no longer at the same core C-state, the core resolves to C0.
- For core C6, an interrupt coming into either thread wakes both threads into C0 state.
- Any interrupt coming into the processor package may wake any core.

4.2.4.1 Core C0 State

The normal operating state of a core where code is being executed.

4.2.4.2 Core C1/C1E State

C1/C1E is a low power state entered when all threads within a core execute a HLT or MWAIT(C1/C1E) instruction.

A System Management Interrupt (SMI) handler returns execution to either Normal state or the C1/C1E state. See the *Intel® 64 and IA-32 Architecture Software Developer's Manual, Volume 3A/3B: System Programmer's Guide for more information.*

While a core is in C1/C1E state, it processes bus snoops and snoops from other threads. For more information on C1E, see "Package C1/C1E".

4.2.4.3 Core C3 State

Individual threads of a core can enter the C3 state by initiating a P_LVL2 I/O read to the P_BLK or an MWAIT(C3) instruction. A core in C3 state flushes the contents of its L1 instruction cache, L1 data cache, and L2 cache to the shared L3 cache, while maintaining its architectural state. All core clocks are stopped at this point. Because the core's caches are flushed, the processor does not wake any core that is in the C3 state when either a snoop is detected or when another core accesses cacheable memory.

4.2.4.4 Core C6 State

Individual threads of a core can enter the C6 state by initiating a P_LVL3 I/O read or an MWAIT(C6) instruction. Before entering core C6, the core will save its architectural state to a dedicated SRAM.Once complete, a core will have its voltage reduced to zero volts. During exit, the core is powered on and its architectural state is restored.

4.2.4.5 C-State Auto-Demotion

In general, deeper C-states such as C6 have long latencies and have higher energy entry/exit costs. The resulting performance and energy penalties become significant when the entry/exit frequency of a deeper C-state is high. Therefore incorrect or inefficient usage of deeper C-states have a negative impact on battery life. In order to increase residency and improve battery life in deeper C-states, the processor supports C-state auto-demotion.

There are two C-State auto-demotion options:

- C6 to C3
- C6/C3 To C1

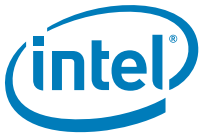
The decision to demote a core from C6 to C3 or C3/C6 to C1 is based on each core's immediate residency history. Upon each core C6 request, the core C-state is demoted to C3 or C1 until a sufficient amount of residency has been established. At that point, a core is allowed to go into C3/C6. Each option can be run concurrently or individually.

This feature is disabled by default. BIOS must enable it in the PMG_CST_CONFIG_CONTROL register. The auto-demotion policy is also configured by this register. See the *RS- Nehalem Processor Family BIOS Writer's Guide* for more details.

4.2.5 Package C-States

The processor supports C0, C1/C1E, C3, and C6 package idle power states. The following is a summary of the general rules for package C-state entry. These apply to all package C-states unless specified otherwise:

- A package C-state request is determined by the lowest numerical core C-state amongst all cores.
- A package C-state is automatically resolved by the processor depending on the core idle power states and the status of the platform components.
  - Each core can be at a lower idle power state than the package if the platform does not grant the processor permission to enter a requested package C-state.
  - The platform may allow additional power savings to be realized in the processor. "Conditional Self-Refresh" on page 50
- For package C-states, the processor is not required to enter C0 before entering any other C-state.



The processor exits a package C-state when a break event is detected. Depending on the type of break event, the processor does the following:

- If a core break event is received, the target core is activated and the break event message is forwarded to the target core.
  - If the break event is not masked, the target core enters the core C0 state and the processor enters package C0.
  - If the break event is masked, the processor attempts to re-enter its previous package state.
- If the break event was due to a memory access or snoop request.
  - But the platform did not request to keep the processor in a higher package C-state, the package returns to its previous C-state.
  - And the platform requests a higher power C-state, the memory access or snoop request is serviced and the package remains in the higher power C-state.

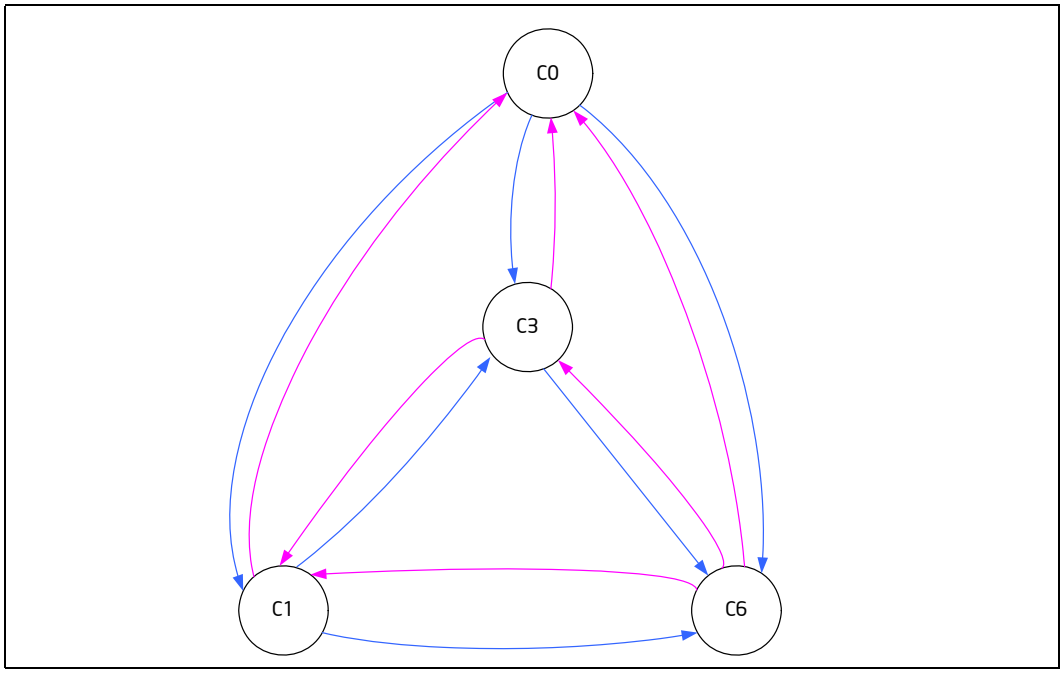
Table 18 shows package C-state resolution for a dual-core processor. Figure 11 summarizes package C-state transitions.

Table 18. Coordination of Core Power States at the Package Level

Package C-State		Core 1			
		C0	**C1**	**C3**	**C6**
Core 0	**C0**	C0	C0	C0	C0
	C1	C0	C1[1]	C1[1]	C1[1]
	C3	C0	C1[1]	C3	C3
	C6	C0	C1[1]	C3	C6

NOTE:
1. If enabled, the package C-state will be C1E if all actives cores have resolved a core C1 state or higher.

Figure 11. Package C-State Entry and Exit



4.2.5.1 Package C0

The normal operating state for the processor. The processor remains in the normal state when at least one of its cores is in the C0 or C1 state or when the platform has not granted permission to the processor to go into a low power state. Individual cores may be in lower power idle states while the package is in C0.

4.2.5.2 Package C1/C1E

No additional power reduction actions are taken in the package C1 state. However, if the C1E sub-state is enabled, the processor automatically transitions to the lowest supported core clock frequency, followed by a reduction in voltage.

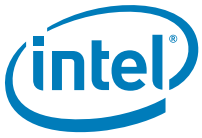
The package enters the C1 low power state when:

- At least one core is in the C1 state.
- The other cores are in a C1 or lower power state.

The package enters the C1E state when:

- All cores have directly requested C1E via MWAIT(C1) with a C1E sub-state hint.
- All cores are in a power state lower that C1/C1E but the package low power state is limited to C1/C1E via the PMG_CST_CONFIG_CONTROL MSR.
- All cores have requested C1 using HLT or MWAIT(C1) and C1E auto-promotion is enabled in IA32_MISC_ENABLES.

No notification to the system occurs upon entry to C1/C1E.



4.2.5.3 Package C3 State

A processor enters the package C3 low power state when:

- At least one core is in the C3 state.
- The other cores are in a C3 or lower power state, and the processor has been granted permission by the platform.
- The platform has not granted a request to a package C6 state but has allowed a package C6 state.

In package C3-state, the L3 shared cache is snoopable.

4.2.5.4 Package C6 State

A processor enters the package C6 low power state when:

- At least one core is in the C6 state.
- The other cores are in a C6 or lower power state, and the processor has been granted permission by the platform.

In package C6 state, all cores have saved their architectural state and have had their core voltages reduced to zero volts. The L3 shared cache is still powered and snoopable in this state. The processor remains in package C6 state as long as any part of the L3 cache is active.

4.2.5.5 Power Status Indicator (PSI#) and DPRSLPVR#

PSI# and DPRSLPVR# are signals used to optimize VR efficiency over a wide power range depending on amount of activity within the processor core. The PSI# signal is utilized by the processor core to:

- Improve intermediate and light load efficiency of the voltage regulator when the processor is active (P-states).
- Optimize voltage regulator efficiency in very low power states. Assertion of DPRSLPVR# indicates that the processor core is in a C6 low power state.

The VR efficiency gains result in overall platform power savings and extended battery life. For more details, refer to the platform design guide and *Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification*

4.3 IMC Power Management

The main memory is power managed during normal operation and in low-power ACPI Cx states.

4.3.1 Disabling Unused System Memory Outputs

Any system memory (SM) interface signal that goes to a memory module connector in which it is not connected to any actual memory devices (such as SO-DIMM connector is unpopulated, or is single-sided) is tri-stated. The benefits of disabling unused SM signals are:

- Reduced power consumption.
- Reduced possible overshoot/undershoot signal quality issues seen by the processor I/O buffer receivers caused by reflections from potentially un-terminated transmission lines.

When a given rank is not populated, the corresponding chip select and CKE signals are not driven.

At reset, all rows must be assumed to be populated, until it can be proven that they are not populated. This is due to the fact that when CKE is tristated with an SO-DIMM present, the SO-DIMM is not guaranteed to maintain data integrity.

4.3.2 DRAM Power Management and Initialization

The processor implements extensive support for power management on the SDRAM interface. There are four SDRAM operations associated with the Clock Enable (CKE) signals, which the SDRAM controller supports. The processor drives four CKE pins to perform these operations.

4.3.2.1 Initialization Role of CKE

During power-up, CKE is the only input to the SDRAM that has its level is recognized (other than the DDR3 reset pin) once power is applied. It must be driven LOW by the DDR controller to make sure the SDRAM components float DQ and DQS during power-up. CKE signals remain LOW (while any reset is active) until the BIOS writes to a configuration register. Using this method, CKE is guaranteed to remain inactive for much longer than the specified 200 micro-seconds after power and clocks to SDRAM devices are stable.

4.3.2.2 Conditional Self-Refresh

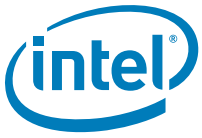
The processor conditionally places memory into self-refresh in the package C3 and C6 low-power states.

When entering the Suspend-to-RAM (STR) state, the processor core flushes pending cycles and then enters all SDRAM ranks into self refresh. In STR, the CKE signals remain LOW so the SDRAM devices perform self-refresh.

The target behavior is to enter self-refresh for the package C3 and C6 states as long as there are no memory requests to service. The target usage is shown in Table 19.

Table 19. Targeted Memory State Conditions

Mode	Memory State with Internal Graphics	Memory State with External Graphics
C0, C1, C1E	Dynamic memory rank power down based on idle conditions.	Dynamic memory rank power down based on idle conditions.
C3, C6	If the internal graphics engine is idle and there are no pending display requests when in single display mode, then enter self-refresh. Otherwise use dynamic memory rank power down based on idle conditions.	If there are no memory requests, then enter self-refresh. Otherwise use dynamic memory rank power down based on idle conditions.
S3	Self-Refresh Mode.	Self-Refresh Mode.
S4	Memory power down (contents lost).	Memory power down (contents lost)



4.3.2.3 Dynamic Power Down Operation

Dynamic power-down of memory is employed during normal operation. Based on idle conditions, a given memory rank may be powered down. The IMC implements aggressive CKE control to dynamically put the DRAM devices in a power down state. The processor core controller can be configured to put the devices in *active power down* (CKE deassertion with open pages) or *precharge power down* (CKE deassertion with all pages closed). Precharge power down provides greater power savings but has a bigger performance impact, since all pages will first be closed before putting the devices in power down mode.

If dynamic power-down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

4.3.2.4 DRAM I/O Power Management

Unused signals should be disabled to save power and reduce electromagnetic interference. This includes all signals associated with an unused memory channel. Clocks can be controlled on a per SO-DIMM basis. Exceptions are made for per SO-DIMM control signals such as CS#, CKE, and ODT for unpopulated SO-DIMM slots.

The I/O buffer for an unused signal should be tri-stated (output driver disabled), the input receiver (differential sense-amp) should be disabled, and any DLL circuitry related ONLY to unused signals should be disabled. The input path must be gated to prevent spurious results due to noise on the unused signals (typically handled automatically when input receiver is disabled).

4.4 PCIe Power Management

- Active power management support using L0s, and L1 states.
- All inputs and outputs disabled in L2/L3 Ready state.

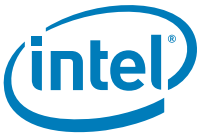
4.5 DMI Power Management

Active power management support using L0s/L1 state.

4.6 Integrated Graphics Power Management

4.6.1 Intel® Display Power Saving Technology 5.0 (Intel® DPST 5.0)

Intel DPST maintains visual experience by managing display image brightness and contrast while adaptively dimming the backlight. As a result, the display backlight power can be reduced by up to 25% depending on Intel DPST settings and system use. Intel DPST 5.0 provides enhanced image quality over the previous version of Intel DPST.



4.6.2 Graphics Render C-State

Render C-State (RC6) is a technique designed to optimize the average power to the graphics render engine during times of idleness of the render engine. RC6 is entered when the graphics render engine, blitter engine and the video engine have no workload being currently worked on and no outstanding graphics memory transactions. When the render engine idleness condition is met: The graphics VR will lower the graphics voltage rail (V_{AXG}) into a lower voltage state (0.3 V).The render frequency clock will shut down.

4.6.3 Graphics Performance Modulation Technology

Graphics Performance Modulation Technology (GPMT) is a method for optimizing the power efficiency in the graphics render engine while continuing to render 3D objects during battery operation. The GPMT feature will dynamically switch the render frequency based on the render workload, on power policy, skew, and environmental conditions.

4.6.4 Intel® Smart 2D Display Technology (Intel® S2DDT)

Intel S2DDT reduces display refresh memory traffic by reducing memory reads required for display refresh. Power consumption is reduced by less accesses to the IMC.

Intel S2DDT is most effective with:

- Display images well suited to compression, such as text windows, slide shows, etc. Poor examples are 3D games.
- Static screens such as screens with significant portions of the background showing 2D applications, CPU benchmarks, etc., or conditions when the CPU is idle. Poor examples are full-screen 3D games and benchmarks that flip the display image at or near display refresh rates.

4.7 Thermal Power Management

- See Section 5, “Thermal Management” on page 53 for all graphics thermal power management-related features.

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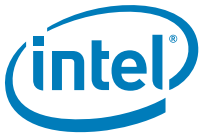


5 Thermal Management

A multi-chip package (MCP) processor requires a thermal solution to maintain temperatures of the processor core and graphics/memory core within operating limits. A complete thermal solution provides both the component-level and the system-level thermal management. To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed so that the processor:

- Remains below the maximum junction temperature ($T_{j,Max}$) specification at the maximum thermal design power (TDP).
- Conforms to system constraints, such as system acoustics, system skin-temperatures, and exhaust-temperature requirements.

Caution: Thermal specifications given in this chapter are on the component and package level and apply specifically to the processor. Operating the processor outside the specified limits may result in permanent damage to the processor and potentially other components in the system.

5.1 Thermal Design Power and Junction Temperature

The TDP of an MCP processor is the expected maximum power from each of its components (processor core and integrated graphics and memory controller) while running realistic, worst case applications (TDP applications). TDP is not the absolute worst case power of each component. It could, for example, be exceeded under a synthetic worst case condition or under short power spikes. In production, a range of power is to be expected from the components due to the natural variation in the manufacturing process. The thermal solution, at a minimum, needs to ensure that the junction temperatures of both components do not exceed the maximum junction temperature ($T_{j,max}$) limit while running TDP applications.

5.1.1 Intel Graphics Dynamic Frequency

Typical workloads are not intensive enough to push both the processor core and the integrated graphics and memory controller towards their TDP limit simultaneously. As such, the opportunity exists to share thermal power between the components and boost the performance of either the processor core or integrated graphics and memory controller on demand. This intelligent power sharing capability is implemented by Intel Turbo Boost Technology Driver on these processors. When enabled, the processor core or the integrated graphics and memory controller can increase its thermal power consumption above its own component TDP limit. However, the sum of component thermal powers adhere to the specified MCP thermal power limit.

On this processor, Intel Graphics Dynamic Frequency is implemented via a combination of Intel silicon capabilities, graphics driver and the Intel Turbo Boost Technology driver. If Intel provides Intel Graphics Dynamic Frequency support for the target operating system that is shipped with the customer’s platform and Intel Graphics Dynamic Frequency is enabled, the Intel Turbo Boost Technology driver and graphics driver must be installed and operating to keep the product operating within specification limits.

Caution: The TURBO_POWER_CURRENT_LIMIT MSR is exclusively reserved for Intel Turbo Technology Driver use. Under no circumstances should this value be altered from the

default register value after reset of the processor. Altering this MSR value may result in unpredictable behavior.

5.1.2 Intel Graphics Dynamic Frequency Thermal Design Considerations and Specifications

When designing a thermal solution for Graphics Dynamic frequency enabled processor:

- Both component TDPs as well as extreme thermal power levels for the processor core and integrated graphics and memory controller must be considered.
- Note that the processor can consume close to its maximum thermal power limit more frequently, and for prolonged periods of time.
- One must ensure that the component $T_{j,max}$ limits are not exceeded when either component is operating at its extreme thermal power limit.

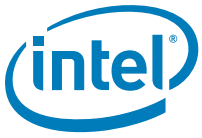
There are two "extreme" design points:

- The processor core operating at maximum thermal power level (which is greater than its component TDP) and the integrated graphics and memory controller operating at its minimum thermal power.
- The integrated graphics operates at its maximum thermal power level, while the processor core consumes the remaining thermal power budget.

In both cases, the combined component thermal power will not exceed the total MCP package power limit. The design approach accommodating two extreme power levels is referred to as a "two-point" design. For more details on two-point design, refer to the *Calpella Platform Thermal and Mechanical Design Guide*.

The following notes apply to Table 25, Table 28, and Table 29.

Note	Definition
1	The component TDPs given are not the maximum power the components can generate. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained periods of time.
2	A range of power is to be expected among the components due to the natural variation in the manufacturing process. Nevertheless, the individual component powers are not to exceed the component TDPs specified.
3	Concurrent package power refers to the actual power consumed by the package while TDP applications are running simultaneously by the processor core and the integrated graphics controller. An example of this could be the processor core running a Prime95* application, and the integrated graphics core running a Star Wars: Jedi Knight* menu simultaneously.
4	The thermal solution needs to ensure that the temperatures of both components do not exceed the maximum junction temperature ($T_{j,max}$) limit, as measured by the DTS and the critical temperature bit. Please refer to processor Specification Update for Tjmax value per sku.
5	Processor core and integrated graphics and memory controller junction temperatures are monitored by their respective DTS. A DTS outputs a temperature relative to the maximum supported junction temperature. The error associated with DTS measurements will not exceed ±5°C within the operating range.
6	The power supply to the processor core and the integrated graphics /Memory core should be designed as per Intel's guidelines in the *Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification*



Note	Definition
7	Processor core currents is monitored by IMON VR feedback (ISENSE) and calculated using a moving average method. Error associated with power monitoring will depend upon individual VR design. Refer to the *Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification* for more details.
8	A thermal solution for an power sharing enabled system needs to ensure that the Tj limit is not exceeded while operating under the two extreme power conditions between the processor core and the integrated graphics and memory controller components. For more details on two-point design, refer to the *Calpella Platform Thermal and Mechanical Design Guide*.
9	Projected range in advance of the measured product data. Measured values will be available after silicon characterization.
10	For power sharing designs it is recommended to establish the full cooling capability within 10°C of the $T_{j,max}$ specifications. Some processors may have a different Tj max value, please refer to the processor Specification Update for details.
11	In rare occasions the specified maximum power limits may be violated when the package is not at a thermally constrained environment
12	Tj, min =0 deg
13	While running intensive graphical and computational workloads simultaneously the concurrent package power may exceed specified limits in exceptional occasions. Nevertheless, the individual component powers are not to exceed the component TDPs specified.

Table 20. Intel® Celeron™ P4000 mobile processor series Dual-Core SV Thermal Power Specifications

		TDP[1,2,6,7]			Frequency		Power Sharing Design Points[8]			$T_{j,max}$[4,5,10,12]	
Processor number	State	CPU Core(W)	Int. Gfx & Memeory Controller(w)	Pkg Concurrent Power(w)[3]	CPU Core(GHz)	Int. Gfx(MHz)	CPU Core Extreme (W)[6,7,11]	Int. Gfx Extreme (W)[6,7]	MCP Thermal Power Limit (W)	CPU Core(ºC)	Int. Gfx & Memory Controller(ºC)
P4500	HFM	25	12.5	35	1.86	500 up to 667	Proc: 29 Int Gfx: 6	Proc: 15 Int Gfx: 20	35	90	85
	LFM	20	12.5	32.5	933 MHz	N/A	N/A	N/A	N/A		

Table 21. Intel® Celeron™ U3000 mobile processor series Dual-Core ULV Thermal Power Specifications

		TDP[1,2,6,7]			Frequency		Power Sharing Design Points[8]			$T_{j,max}$[4,5,10,12]	
Processor number	State	CPU Core(W)	Int. Gfx & Memeory Controller(w)	Pkg Concurrent Power(w)[3,13]	CPU Core(GHz)	Int. Gfx(MHz)	CPU Core Extreme (W)[6,7]	Int. Gfx Extreme (W)[6,7]	MCP Thermal Power Limit (W)	CPU Core(ºC)	Int. Gfx & Memory Controller(ºC)
U3400	HFM	10.5	8.5	18	1.06	166 up to 500	Proc: 10.5 Int. Gfx: 4	Proc: 7 Int Gfx: 11	18	105	100
	LFM	9	8.5	17.5	667 MHz	N/A	N/A	N/A	N/A		

5.1.3 Idle Power Specifications

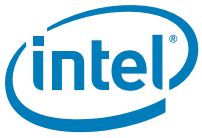
The idle power specifications in Table 22, Table 34, and Table 23 are not 100% tested. These power specifications are determined by the characterization of the processor currents at higher temperatures and extrapolating the values for the junction temperature indicated.

Table 22. 35W Standard Voltage(SV) Processor Idle Power

Symbol	Parameter	Min	Typ	Max	T_j
P_{C1E}	Idle power in the Package C1e state	-	-	16 W	50ºC
P_{C3}	Idle power in the Package C3 state	-	-	7.5 W	35ºC

Table 23. 18W Ultra Low Voltage(ULV) Processor Idle Power

Symbol	Parameter	Min	Typ	Max	T_j
P_{C1E}	Idle power in the Package C1e state	-	-	12 W	50ºC
P_{C3}	Idle power in the Package C3 state	-	-	5.0 W	35ºC
P_{C6}	Idle power in the Package C6 state	-	-	2.6 W	35ºC



5.1.4 Intelligent Power Sharing Control Overview

Based upon knowledge of the processor core and integrated graphics and memory controller thermal power, performance state, and temperature, power sharing control does the following:

- Utilizes and internal graphics controller dynamic frequency performance states to achieve their highest performance within the rated thermal power envelope. Intel Dynamic Frequency enabled processors will offer a range of upside performance capability beyond their rated or guaranteed frequency.
- Controls the processor core and internal graphics controller Intel Turbo Boost performance states to ensure that overall MCP thermal power consumption does not exceed the specified MCP thermal power limit.
- Limits MCP component usage to ensure that each of the components' $T_{j,max}$ value is not exceeded.

It is possible that the thermal influence between the MCP components could potentially cause a component to reach its $T_{j,max}$, invoking undesirable component hardware auto-throttling. It is expected that when running the TDP workload, power sharing control may limit the entire range of component turbo capabilities (effectively, disabling them).

The principal component of the power sharing control architecture is the policy manager within the Intel Turbo Boost Technology driver which:

- Communicates with the graphics software driver to limit, or increase, internal graphics thermal power.
- Communicates with the processor core via the PCH to processor core PECI interface to limit, or increase, processor core thermal power.

The Intel Turbo Boost Technology policy manager will set a thermal power limit to which the graphics driver and processor core will adjust their turbo Technology performance dynamically, to stay within the limit.

Note: The processor PECI pin must be connected to the PCH PECI pin in order for graphics dynamic frequency to properly function.

5.1.5 Component Power Measurement/Estimation Error

The processor input pin (ISENSE) informs the processor core of how much amperage the processor core is consuming. This information is provided by the processor core VR. The process will calculate its current power based upon the ISENSE input information and current voltage state. The internal graphics and memory controller power is estimated by the GFX driver using PMON.

Any error in power estimation or measurement may limit or completely eliminate the performance benefit of Intel Turbo Boost Technology. When a power limit is reached, Power sharing control will adaptively remove Intel Turbo Boost Technology states to remain with the MCP thermal power limit. Power sharing control assumes the power error is always accurate so if the ISENSE input reports power greater than the actual power, control mechanisms will lower performance before the actual TDP power limit is reached. Intelligent Power sharing will provide better overall Intel Turbo Boost Technology performance with increasing VR current sense accuracy. Designers and system manufacturers should study trade-offs on VR component accuracy characteristics, such as inductors, to find the best balance of cost vs. performance for their system price and performance targets.

5.2 Thermal Management Features

This section will cover thermal management features for the processor.

5.2.1 Processor Core Thermal Features

Occasionally the processor core will operate in conditions that exceed its maximum allowable operating temperature. This can be due to internal overheating or due to overheating in the entire system. In order to protect itself and the system from thermal failure, the processor core is capable of reducing its power consumption and thereby its temperature until it is back within normal operating limits via the Adaptive Thermal Monitor.

The Adaptive Thermal Monitor can be activated when any core temperature, monitored by a digital thermal sensor (DTS), exceeds its maximum junction temperature ($T_{j,Max}$) and asserts PROCHOT#. The assertion of PROCHOT# activates the thermal control circuit (TCC). The TCC will remain active as long as any core exceeds its temperature limit. Therefore, the Adaptive Thermal Monitor will continue to reduce the processor core power consumption until the TCC is de-activated.

Caution: The Adaptive Thermal Monitor must be enabled for the processor to remain within specification.

5.2.1.1 Adaptive Thermal Monitor

The purpose of the Adaptive Thermal Monitor is to reduce processor core power consumption and temperature until it operates at or below its maximum operating temperature. Processor core power reduction is achieved by:

- Adjusting the operating frequency (via the core ratio multiplier) and input voltage (via the VID signals).
- Modulating (starting and stopping) the internal processor core clocks (duty cycle).

The Adaptive Thermal Monitor dynamically selects the appropriate method. BIOS is not required to select a specific method as with previous-generation processors supporting Intel® Thermal Monitor 1 (TM1) or Intel® Thermal Monitor 2 (TM2). The temperature at which the Adaptive Thermal Monitor activates the Thermal Control Circuit is not user configurable but is software visible in the IA32_TEMPERATURE_TARGET (0x1A2) MSR, Bits 23:16. The Adaptive Thermal Monitor does not require any additional hardware, software drivers, or interrupt handling routines. Note that the Adaptive Thermal Monitor is not intended as a mechanism to maintain processor TDP. The system design should provide a thermal solution that can maintain TDP within its intended usage range.

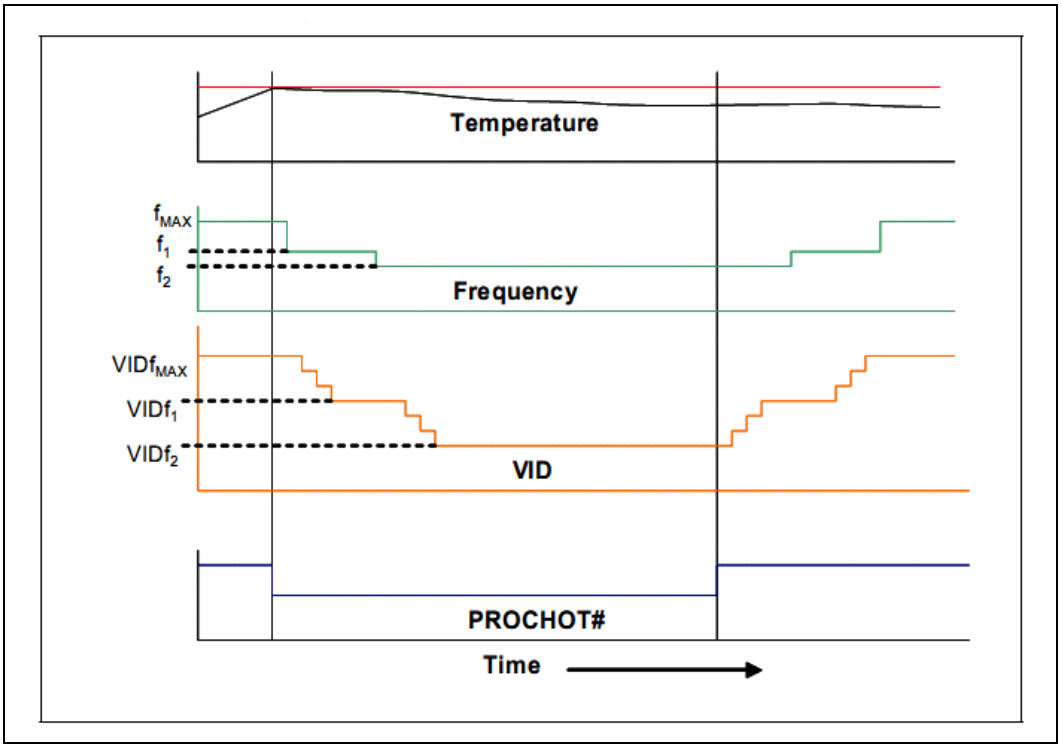
5.2.1.1.1 Frequency/VID Control

Upon TCC activation, the processor core attempts to dynamically reduce processor core power by lowering the frequency and voltage operating point. The operating points are automatically calculated by the processor core itself and do not require the BIOS to program them as with previous generations of Intel processors. The processor core will scale the operating points such that:

- The voltage will be optimized according to the temperature, the core bus ratio, and number of cores in deep C-states.
- The core power and temperature are reduced while minimizing performance degradation.

A small amount of hysteresis has been included to prevent an excessive amount of operating point transitions when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature and the hysteresis timer has expired, the operating frequency and voltage transition back to the normal system operating point. This is illustrated in Figure 12.

Figure 12. Frequency and Voltage Ordering



Once a target frequency/bus ratio is resolved, the processor core will transition to the new target automatically.

- On an upward operating point transition, the voltage transition precedes the frequency transition.
- On a downward transition, the frequency transition precedes the voltage transition.

When transitioning to a target core operating voltage, a new VID code to the voltage regulator is issued. The voltage regulator must support dynamic VID steps to support this method.

During the voltage change:

- It will be necessary to transition through multiple VID steps to reach the target operating voltage.
- Each step is 12.5 mV for Intel MVP-6.5 compliant VRs.
- The processor continues to execute instructions. However, the processor will halt instruction execution for frequency transitions.

If a processor load-based Enhanced Intel SpeedStep Technology/P-state transition (through MSR write) is initiated while the Adaptive Thermal Monitor is active, there are two possible outcomes:

- If the P-state target frequency is higher than the processor core optimized target frequency, the p-state transition will be deferred until the thermal event has been completed.
- If the P-state target frequency is lower than the processor core optimized target frequency, the processor will transition to the P-state operating point.

5.2.1.1.2 Clock Modulation

If the frequency/voltage changes are unable to end an Adaptive Thermal Monitor event, the Adaptive Thermal Monitor will utilize clock modulation. Clock modulation is done by alternately turning the clocks off and on at a duty cycle (ratio between clock "on" time and total time) specific to the processor. The duty cycle is factory configured to 37.5% on and 62.5% off and cannot be modified. The period of the duty cycle is configured to 32 microseconds when the TCC is active. Cycle times are independent of processor frequency. A small amount of hysteresis has been included to prevent excessive clock modulation when the processor temperature is near its maximum operating temperature. Once the temperature has dropped below the maximum operating temperature, and the hysteresis timer has expired, the TCC goes inactive and clock modulation ceases. Clock modulation is automatically engaged as part of the TCC activation when the frequency/VID targets are at their minimum settings. Processor performance will be decreased by the same amount as the duty cycle when clock modulation is active. Snooping and interrupt processing are performed in the normal manner while the TCC is active.

5.2.1.2 Digital Thermal Sensor

Each processor execution core has an on-die Digital Thermal Sensor (DTS) which detects the core's instantaneous temperature. The DTS is the preferred method of monitoring processor die temperature because

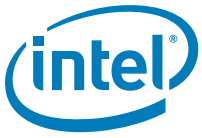
- It is located near the hottest portions of the die.
- It can accurately track the die temperature and ensure that the Adaptive Thermal Monitor is not excessively activated.

Temperature values from the DTS can be retrieved through

- A software interface via processor Model Specific Register (MSR).
- A processor hardware interface as described in "Platform Environment Control Interface (PECI)" on page 66.

Note: When temperature is retrieved by processor MSR, it is the instantaneous temperature of the given core. When temperature is retrieved via PECI, it is the average temperature of each execution core's DTS over a programmable window (default window of 256 ms.) Intel recommends using the PECI output reading for fan speed or other platform thermal control.

Code execution is halted in C1-C6. Therefore temperature cannot be read via the processor MSR without bringing a core back into C0. However, temperature can still be monitored through PECI in lower C-states.



Unlike traditional thermal devices, the DTS outputs a temperature relative to the maximum supported operating temperature of the processor ($T_{j,max}$). It is the responsibility of software to convert the relative temperature to an absolute temperature. The absolute reference temperature is readable in an MSR. The temperature returned by the DTS is an implied negative integer indicating the relative offset from $T_{j,max}$. The DTS does not report temperatures greater than $T_{j,max}$. Refer to the *RS - Nehalem Processor Family BIOS Writer's Guide (BWG)* for specific register details.

The DTS-relative temperature readout directly impacts the Adaptive Thermal Monitor trigger point. When a DTS indicates that the maximum processor core temperature has been reached (a reading of 0x0 on any core), the TCC will activate and indicate a Adaptive Thermal Monitor event.

Changes to the temperature can be detected via two programmable thresholds located in the processor thermal MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

5.2.1.3 PROCHOT# Signal

PROCHOT# (processor hot) is asserted when the processor core temperature has reached its maximum operating temperature ($T_{j,max}$). This will activate the TCC and signal a thermal event which is then resolved by the Adaptive Thermal Monitor. See Figure 12 (above) for a timing diagram of the PROCHOT# signal assertion relative to the Adaptive Thermal Response. Only a single PROCHOT# pin exists at a package level of the processor. When any core arrives at the TCC activation point, the PROCHOT# signal will be driven by the processor core. PROCHOT# assertion policies are independent of Adaptive Thermal Monitor enabling.

Note: Bus snooping and interrupt latching are active while the TCC is active.

5.2.1.3.1 Bi-Directional PROCHOT#

By default, the PROCHOT# signal is defined as an output only. However, the signal may be configured as bi-directional. When configured as a bi-directional signal, PROCHOT# can be used for thermally protecting other platform components should they overheat as well. When PROCHOT# is signaled externally:

- The processor core will immediately reduce processor power to the minimum voltage and frequency supported. This is contrary to the internally-generated Adaptive Thermal Monitor response.
- Clock modulation is not activated.

The TCC will remain active until the system deasserts PROCHOT#. The processor can be configured to generate an interrupt upon assertion and deassertion of the PROCHOT# signal. Refer to the *RS - Nehalem Processor Family BIOS Writer's Guide (BWG)* for specific register and programming details. Refer to the *Calpella Design Guide* and *Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification – Rev. 1.1* for details on implementing the bi-directional PROCHOT# feature.

5.2.1.3.2 Voltage Regulator Protection

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target thermal design current (I_{TDC}) instead of maximum current. Systems should still provide proper

cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. Overall, the system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP.

5.2.1.3.3 Thermal Solution Design and PROCHOT# Behavior

With a properly designed and characterized thermal solution, it is anticipated that PROCHOT# will only be asserted for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be so minor that it would be immeasurable.

However, an under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may:

- Cause a noticeable performance loss
- Result in prolonged operation at or above the specified maximum junction temperature and affect the long-term reliability of the processor
- May be incapable of cooling the processor even when the TCC is active continuously (in extreme situations)

Refer to the *Calpella Platform Thermal and Mechanical Design Guide* for information on implementing the bi-directional PROCHOT# feature and designing a compliant thermal solution.

5.2.1.3.4 Low-Power States and PROCHOT# Behavior

If the processor enters a low-power package idle state such as C3 or C6 with PROCHOT# asserted, PROCHOT# will remain asserted until:

- The processor exits the low-power state
- The processor junction temperature drops below the thermal trip point

Note that the PECI interface is fully operational during all C-states and it is expected that the platform continues to manage processor core thermals even during idle states by regularly polling for thermal data over PECI.

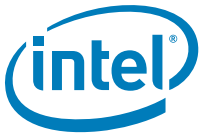
5.2.1.4 On-Demand Mode

The processor provides an auxiliary mechanism that allows system software to force the processor to reduce its power consumption via clock modulation. This mechanism is referred to as “On-Demand” mode and is distinct from Adaptive Thermal Monitor and bi-directional PROCHOT#. platforms must not rely on software usage of this mechanism to limit the processor temperature. On-Demand Mode can be done via processor MSR or chipset I/O emulation.

On-Demand Mode may be used in conjunction with the Adaptive Thermal Monitor. However, if the system software tries to enable On-Demand mode at the same time the TCC is engaged, the factory configured duty cycle of the TCC will override the duty cycle selected by the On-Demand mode. If the I/O based and MSR-based On-Demand modes are in conflict, the duty cycle selected by the I/O emulation-based On-Demand mode will take precedence over the MSR-based On-Demand Mode. For more details, refer to the *RS-Nehalem Processor BIOS Writer's Guide.*

5.2.1.4.1 MSR Based On-Demand Mode

If Bit 4 of the IA32_CLOCK_MODULATION MSR is set to a 1, the processor will immediately reduce its power consumption via modulation of the internal core clock, independent of the processor temperature. The duty cycle of the clock modulation is programmable via Bits 3:1 of the same IA32_CLOCK_MODULATION MSR. In this mode,



the duty cycle can be programmed from 12.5% on/87.5% off to 87.5% on/12.5% off in 12.5% increments. Thermal throttling using this method will modulate each processor core's clock independently.

5.2.1.4.2 I/O Emulation-Based On-Demand Mode

I/O emulation-based clock modulation provides legacy support for operating system software that initiates clock modulation through I/O writes to ACPI defined processor clock control registers on the chipset (PROC_CNT). Thermal throttling using this method will modulate all processor cores simultaneously. For more details, refer to the *RS-Nehalem Processor BIOS Writer's Guide.*

5.2.1.5 THERMTRIP# Signal

Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached an elevated temperature that risks physical damage to the processor. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles.

5.2.1.6 Critical Temperature Detection

Critical Temperature detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shutdown before the THERMTRIP# is activated. If the processor's Adaptive Thermal Monitor is triggered and the temperature remains high, a critical temperature status and sticky bit are latched in the thermal status MSR register and also generates a thermal interrupt if enabled. The assertion of critical temperature bit indicates that processor can no longer be assumed to be working reliably.For more details on the interrupt mechanism, refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* or *RS - Nehalem Processor BIOS Writer's Guide.*

5.2.2 Integrated Graphics and Memory Controller Thermal Features

The integrated graphics and memory controller provides the following features for monitoring the integrated graphics and memory controller temperature and triggering thermal management:

- One internal digital thermal sensor
- Hooks for an external thermal sensor mechanism which can either be TS-on-DIMM or TS-on-Board

The integrated graphics and memory controller has implemented several silicon level thermal management features that can lower both integrated graphics and memory controller and DDR3 power during periods of high activity. As a result, these features can help control temperature and help prevent thermally induced component failures. These features include:

- Bandwidth throttling triggered by memory loading
- Bandwidth throttling triggered by integrated graphics and memory controller heating
- THERMTRIP# support
- Render Thermal Throttling

5.2.2.1 Internal Digital Thermal Sensor

The integrated graphics and memory controller incorporates one on-die digital thermal sensor for thermal management. The thermal sensor may be programmed to cause hardware throttling and/or software interrupts. Hardware throttling includes render thermal throttling and main memory programmable throttling thresholds. Sensor trip points may also be programmed to generate various interrupts including SCI, SMI, INTR, and SERR. The internal thermal sensor reports six trip points: Aux0, Aux1, Aux2, Aux3, Hot, and Catastrophic trip points in order of increasing temperature.

5.2.2.1.1 Aux0, Aux1, Aux2, Aux3 Temperature Trip Points

These trip points may be set dynamically if desired and provides a configurable interrupt mechanism to allow software to respond when a trip is crossed in either direction. These auxiliary temperature trip points do not automatically cause any hardware throttling but may be used by software to trigger interrupts.

5.2.2.1.2 Hot Temperature Trip Point

This trip point is set at the temperature at which the integrated graphics and memory controller must start throttling. It may optionally enable integrated graphics and memory controller throttling when the temperature is exceeded. This trip point may provide an interrupt to ACPI (or other software) when it is crossed in either direction. Software could optionally set this as an interrupt when the temperature exceeds this level setting.

5.2.2.1.3 Catastrophic Trip Point

This trip point is set at the temperature at which the integrated graphics and memory controller must be shut down immediately without any software support. This trip point may be programmed to generate an interrupt, enable throttling, or immediately shut down the system (via Halt or via THERMTRIP# assertion). Crossing a trip point in either direction may generate several types of interrupts.

5.2.2.1.4 Recommended Programming for Available Trip Points

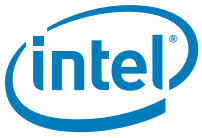
See the integrated graphics and memory controller BIOS Specification for recommended Trip Point programming. Aux Trip Points (0, 1, 2, 3) should be programmed for software and firmware control via interrupts. HOT Trip Point should be set to throttle integrated graphics and memory controller to avoid $T_{j,max}$ of 100°C. Catastrophic Trip Point should be set to halt operation to avoid maximum Tj of 130°C.

Note: Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register that can be programmed to select the type of interrupt to be generated. Crossing a trip point is implemented as edge detection on each trip point to generate the interrupts. Either edge (i.e., crossing the trip point in either direction) generates the interrupt.

5.2.2.1.5 Thermal Sensor Accuracy ($T_{accuracy}$)

The error associated with DTS measurement will not exceed ±5°C within the operating range. Integrated graphics and memory controller may not operate above $T_{j,max}$ spec. This value is based on product characterization and is not guaranteed by manufacturing test.

Software has the ability to program the T_{cat}, T_{hot}, and T_{aux} trip points, but these trip points should be selected with consideration for the thermal sensor accuracy and the quality of the platform thermal solution. Overly conservative (unnecessarily low)



temperature settings may unnecessarily degrade performance due to frequent throttling, while overly aggressive (dangerously high) temperature settings may fail to protect the part against permanent thermal damage.

5.2.2.1.6 Hysteresis Operation

Hysteresis provides a small amount of positive feedback to the thermal sensor circuit to prevent a trip point from flipping back and forth rapidly when the temperature is right at the trip point. The digital hysteresis offset is programmable via processor registers.

5.2.2.2 Memory Thermal Throttling Options

The integrated graphics and memory controller has two, independent mechanisms that cause system memory throttling:

TDP Controller: The TDP Controller is the main mechanism for limiting MCH power by limiting memory bandwidth. Utilized as a thermal throttling mechanism, this feature is triggered by the Hot temperature trip point of the Graphics and Memory Controller digital thermal sensor (DTS) and initiates duty cycle throttling to delay memory transactions and thereby reducing MCH power. Power reduction is memory configuration and application dependant but duty cycle throttling intervals can be customized for maximum throttling efficiency. The TDP Controller can also be used as a bandwidth limiter using programmable memory read/write bandwidth thresholds. Intel sets the default thresholds that will not restrict bandwidth and performance for most applications but these thresholds can be modified to reduce MCH power regardless of DTS temperature.

Note: The TDP controller can be used as a closed loop thermal throttling (CLTT) mechanism or an open loop thermal throttling (OLTT) mechanism, although CLTT is recommended.

- DRAM Thermal Management: Ensures that the DRAM chips are operating within thermal limits. The integrated graphics and memory controller can control the amount of integrated graphics and memory controller-initiated bandwidth per rank to a programmable limit via a weighted input averaging filter.

5.2.2.3 External Thermal Sensor Interface Overview

The integrated graphics and memory controller supports two inputs for external thermal sensor notifications, based on which it can regulate memory accesses.

Note: The thermal sensors should be capable of measuring the ambient temperature only and should be able to assert PM_EXT_TS#[0] and/or PM_EXT_TS#[1] if the pre-programmed thermal limits/conditions are met or exceeded.

An external thermal sensor with a serial interface may be placed next to a SO-DIMM (or any other appropriate platform location), or a remote Thermal Diode may be placed next to the SO-DIMM (or any other appropriate platform location) and connected to the external Thermal Sensor.

Additional external thermal sensor's outputs, for multiple sensors, can be wire-OR'd together allow signaling from multiple sensors that are physically located separately. Software can, if necessary, distinguish which SO-DIMM(s) is the source of the overtemp through the serial interface. However, since the SO-DIMM's is located on the same Memory Bus Data lines, any integrated graphics and memory controller-based read throttle will apply equally.

Thermal sensors can either be directly routed to the integrated graphics and memory controller PM_EXT_TS#[0] and PM_EXT_TS#[1] pins or indirectly routed to integrated graphics and memory controller by invoking an Embedded Controller (EC) connected in between the thermal sensor and integrated graphics and memory controller pins. Both

routing methods are applicable for both thermal sensors placed on the motherboard (TS-on-Board) and/or thermal sensors located on the memory modules (TS-on-DIMM). Please refer to the *Calpella Platform Design Guide* for further details.

5.2.2.4 THERMTRIP# Operation

The integrated graphics and memory controller can assert THERMTRIP# (Thermal Trip) to indicates that its junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the integrated graphics and memory controller will shut off its internal clocks (thus halting program execution) in an attempt to reduce the core junction temperature. Once activated, THERMTRIP# remains latched until RSTIN# is asserted.

5.2.2.5 Render Thermal Throttling

Render Thermal Throttling of the integrated graphics and memory controller allows for the reduction the render core engine frequency and voltage, thus reducing internal graphics controller power and integrated graphics and memory controller thermals. Performance is degraded, but the platform thermal burden is relieved.

Render Thermal Throttling using several frequency/voltage operating points that can be used to throttle the render core. If the temperature of the integrated graphics and memory controller internal DTS exceeds the Hot-trip point, the integrated graphics will switch to a lower frequency/voltage operating point. After a timeout, the DTS is rechecked, and if the DTS temperature is still greater than the designed hysteresis, the integrated graphics will continue to switch to lower frequency/voltage operating points. Once the DTS reports a temperature below the hysteresis value, the render clock frequency and voltage will be restored to its pre-thermal event state.

Caution: The Render Thermal Throttling must be enabled for the product to remain within specification.

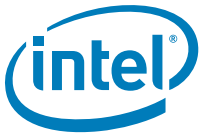
5.2.3 Platform Environment Control Interface (PECI)

The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices. The processor implements a PECI interface to allow communication of processor thermal information to other devices on the platform. The processor provides a digital thermal sensor (DTS) for fan speed control. The DTS is calibrated at the factory to provide a digital representation of relative processor temperature. Averaged DTS values are read via the PECI interface.

The PECI physical layer is a self-clocked one-wire bus that begins each bit with a driven, rising edge from an idle level near zero volts. The duration of the signal driven high depends on whether the bit value is a Logic 0 or Logic 1. PECI also includes variable data transfer rate established with every message. The single wire interface provides low board routing overhead for the multiple load connections in the congested routing area near the processor and chipset components. Bus speed, error checking, and low protocol overhead provides adequate link bandwidth and reliability to transfer critical device operating conditions and configuration information.

5.2.3.1 Fan Speed Control with Digital Thermal Sensor

Digital Thermal Sensor based fan speed control (T_{FAN}) is a recommended feature to achieve optimal thermal performance. At the T_{FAN} temperature, Intel recommends full cooling capability well before the DTS reading reaches $T_{j,max}$. An example of this would be $T_{FAN} = T_{j,max}$ - 10ºC.



5.2.3.2 Processor Thermal Data Sample Rate and Filtering

The processor digital thermal sensor (DTS) provides an improved capability to monitor device hot spots, which inherently leads to more varying temperature readings over short time intervals. To reduce the sample rate requirements on PECI and improve thermal data stability vs. time the processor DTS implements an averaging algorithm that filters the incoming data. This filter is expressed mathematically as:

PECI(t) = PECI(t-1)+1/(2^^X)*[Temp - PECI(t-1)]

where:

- PECI(t) is the new averaged temperature
- PECI(t-1) is the previous averaged temperature
- Temp is the raw temperature data from the DTS
- X is the Thermal Averaging Constant (TAC)

The Thermal Averaging Constant is a BIOS configurable value that determines the time in milliseconds over which the DTS temperature values are averaged (the default time is 256 ms). Short averaging times will make the averaged temperature values respond more quickly to DTS changes. Long averaging times will result in better overall thermal smoothing but also incur a larger time lag between fast DTS temperature changes and the value read via PECI.

Within the processor, the DTS converts an analog signal into a digital value representing the temperature relative to PROCHOT# circuit activation. The conversions are in integers with each single number change corresponding to approximately 1°C. DTS values reported via the internal processor MSR will be in whole integers.

As a result of the PECI averaging function described above, DTS values reported over PECI will include a 6-bit fractional value. Under typical operating conditions, where the temperature is close to PROCHOT#, the fractional values may not be of interest. But when the temperature approaches zero, the fractional values can be used to detect the activation of the PROCHOT# circuit. An averaged temperature value between 0 and 1 can only occur if the PROCHOT# circuit has been activated during the averaging window. As PROCHOT# circuit activation time increases, the fractional value will approach zero. Fan control circuits can detect this situation and take appropriate action as determined by the system designers. Of course, fan control chips can also monitor the PROCHOT# pin to detect PROCHOT# circuit activation via a dedicated input pin on the package.

§

6 Signal Description

This chapter describes the processor signals. They are arranged in functional groups according to their associated interface or category. The following notations are used to describe the signal type:

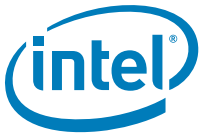
Notations	Signal Type
I	Input Pin
O	Output Pin
I/O	Bi-directional Input/Output Pin

The signal description also includes the type of buffer used for the particular signal:

Table 24. Signal Description Buffer Types

Signal	Description
PCI Express*	PCI Express interface signals. These signals are compatible with PCI Express 2.0 Signalling Environment AC Specifications and are AC coupled. The buffers are not 3.3-V tolerant. Refer to the PCIe specification.
FDI	Intel Flexible Display interface signals. These signals are compatible with PCI Express 2.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3-V tolerant.
DMI	Direct Media Interface signals. These signals are compatible with PCI Express 2.0 Signaling Environment AC Specifications, but are DC coupled. The buffers are not 3.3-V tolerant.
CMOS	CMOS buffers. 1.1-V tolerant
DDR3	DDR3 buffers: 1.5-V tolerant
A	Analog reference or output. May be used as a threshold voltage or for buffer compensation
GTL	Gunning Transceiver Logic signaling technology
Ref	Voltage reference signal
Asynchronous[1]	Signal has no timing relationship with any reference clock.

NOTES:
1. Qualifier for a buffer type.



6.1 System Memory Interface

Table 25. Memory Channel A (Sheet 1 of 2)

Signal Name	Description	Direction / Buffer Type
SA_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SA_WE#	**Write Enable Control Signal:** Used with SA_RAS# and SA_CAS# (along with SA_CS#) to define the SDRAM Commands.	O DDR3
SA_RAS#	**RAS Control Signal:** Used with SA_CAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_CAS#	**CAS Control Signal:** Used with SA_RAS# and SA_WE# (along with SA_CS#) to define the SRAM Commands.	O DDR3
SA_DM[7:0]	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM[7:0] for every data byte lane.	O DDR3
SA_DQS[7:0]	**Data Strobes:** SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS#[7:0] during read and write transactions	I/O DDR3
SA_DQS#[7:0]	**Data Strobe Complements:** These are the complementary strobe signals.	I/O DDR3
SA_DQ[63:0]	**Data Bus:** Channel A data signal interface to the SDRAM data bus.	I/O DDR3
SA_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SA_CK[1:0]	**SDRAM Differential Clock:** Channel A SDRAM Differential clock signal pair. The crossing of the positive edge of SA_CK and the negative edge of its complement SA_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SA_CK#[1:0]	**SDRAM Inverted Differential Clock:** Channel A SDRAM Differential clock signal-pair complement.	O DDR3

Table 25. Memory Channel A (Sheet 2 of 2)

Signal Name	Description	Direction / Buffer Type
SA_CKE[1:0]	**Clock Enable:** (1 per rank) Used to: - Initialize the SDRAMs during power-up - Power-down SDRAM ranks - Place all SDRAM ranks into and out of self-refresh during STR	O DDR3
SA_CS#[1:0]	**Chip Select:** (1 per rank) Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SA_ODT[1:0]	**On Die Termination:** Active Termination Control.	O DDR3

Table 26. Memory Channel B (Sheet 1 of 2)

Signal Name	Description	Direction / Buffer Type
SB_BS[2:0]	**Bank Select:** These signals define which banks are selected within each SDRAM rank.	O DDR3
SB_WE#	**Write Enable Control Signal:** Used with SB_RAS# and SB_CAS# (along with SB_CS#) to define the SDRAM Commands.	O DDR3
SB_RAS#	**RAS Control Signal:** Used with SB_CAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_CAS#	**CAS Control Signal:** Used with SB_RAS# and SB_WE# (along with SB_CS#) to define the SRAM Commands.	O DDR3
SB_DM[7:0]	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane.	O DDR3
SB_DM[7:0]	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane.	O DDR3
SB_DQS[7:0]	**Data Strobes:** SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS#[7:0] during read and write transactions.	I/O DDR3

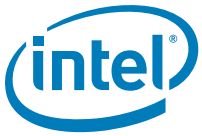


Table 26. Memory Channel B (Sheet 2 of 2)

Signal Name	Description	Direction / Buffer Type
SB_DQS#[7:0]	**Data Strobe Complements:** These are the complementary strobe signals.	I/O DDR3
SB_DQ[63:0]	**Data Bus:** Channel B data signal interface to the SDRAM data bus.	I/O DDR3
SB_MA[15:0]	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM.	O DDR3
SB_CK[1:0]	**SDRAM Differential Clock:** Channel B SDRAM Differential clock signal pair. The crossing of the positive edge of SB_CK and the negative edge of its complement SB_CK# are used to sample the command and control signals on the SDRAM.	O DDR3
SB_CK#[1:0]	**SDRAM Inverted Differential Clock:** Channel B SDRAM Differential clock signal-pair complement.	O DDR3
SB_CKE[1:0]	**Clock Enable:** (1 per rank) Used to: - Initialize the SDRAMs during power-up. - Power-down SDRAM ranks. - Place all SDRAM ranks into and out of self-refresh during STR.	O DDR3
SB_CS#[1:0]	**Chip Select:** (1 per rank) Used to select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank.	O DDR3
SB_ODT[1:0]	**On Die Termination:** Active Termination Control.	O DDR3

6.2 Memory Reference and Compensation

Table 27. Memory Reference and Compensation

Signal Name	Description	Direction / Buffer Type
SM_RCOMP[2:0]	**System Memory Impedance Compensation:** Refer to the Calpella Platform Design Guide for implementation.	I A
SA_DIMM_VREFDQ SB_DIMM_VREFDQ	**Memory Channel A/B DIMM Voltage Reference:** Refer to the Calpella Platform Design Guide.	O A

6.3 Reset and Miscellaneous Signals

Table 28. Reset and Miscellaneous Signals (Sheet 1 of 2)

Signal Name	Description	Direction / Buffer Type
SM_DRAMRST#	**DDR3 DRAM Reset:** Reset signal from processor to DRAM devices. One for all channels or SO-DIMMs.	O DDR3
PM_EXT_TS#[0] PM_EXT_TS#[1]	**External Thermal Sensor Input:** If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling.	I CMOS
COMP0	Impedance compensation must be terminated on the system board using a precision resistor.	I A
COMP1	Impedance compensation must be terminated on the system board using a precision resistor.	I A
COMP2	Impedance compensation must be terminated on the system board using a precision resistor.	I A
COMP3	Impedance compensation must be terminated on the system board using a precision resistor.	I A
PM_SYNC	**Power Management Sync:** A sideband signal to communicate power management status from the platform to the processor.	I CMOS
RESET_OBS#	This signal is an indication of the processor being reset.	O Asynchronous CMOS
RSTIN#	**Reset In:** When asserted this signal will asynchronously reset the processor logic. This signal is connected to the PLTRST# output of the PCH.	I CMOS

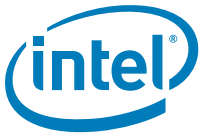


Table 28. Reset and Miscellaneous Signals (Sheet 2 of 2)

Signal Name	Description	Direction / Buffer Type
CFG[17:0]	**Configuration Signals:** The CFG signals have a default value of '1' if not terminated on the board. Refer to the Calpella Platform Design Guide for pull-down recommendations when a logic low is desired. **CFG[2:0]** - Reserved configuration pins. Test points may be placed on these pins on a common motherboard design. **CFG[3]** – PCI Express* Static Lane Numbering Reversal. Lane Reversal will be applied across all 16 Lanes. • 1: No lane reversal • 0: Reversal **CFG[4]** - Embedded DisplayPort Detection: This is used to detect the presence of a device on the Embedded DisplayPort. **CFG[17:5]** - Reserved configuration pins. **Note:** Hardware straps are sampled on the asserting edge of VCCPWRGOOD_0 and VCCPWRGOOD_1 and latched inside the processor.	I CMOS
BPM#[7:0]	**Breakpoint and Performance Monitor Signals:** Outputs from the processor that indicate the status of breakpoints and programmable counters used for monitoring processor performance.	I/O GTL
DBR#	**Debug Reset:** Used only in systems where no debug port is implemented on the system board. DBR# is used by a debug port interposer so that an in-target probe can drive system reset. This signal only routes through the package and does not connect to the the processor silicon itself.	O
PRDY#	**PRDY#**: A processor output used by debug tools to determine processor debug readiness.	O Asynchronous GTL
PREQ#	**PREQ#:** Used by debug tools to request debug operation of the processor.	I Asynchronous GTL
RSVD RSVD_TP RSVD_NCTF	**RESERVED.** All signals that are RSVD and RSVD_NCTF must be left unconnected on the board. However, Intel recommends that all RSVD_TP signals have via test points.	No Connect Test Point Non-Critical to Function

6.4 PCI Express Graphics Interface Signals

Table 29. PCI Express Graphics Interface Signals

Signal Name	Description	Direction / Buffer Type
PEG_RX[15:0] PEG_RX#[15:0]	**PCI Express Graphics Receive Differential Pair**	I PCI Express
PEG_TX[15:0] PEG_TX#[15:0]	**PCI Express Graphics Transmit Differential Pair**	O PCI Express
PEG_ICOMPI	PCI Express Graphics Input Current Compensation	I A
PEG_ICOMPO	PCI Express Graphics Output Current Compensation	I A
PEG_RCOMPO	PCI Express Graphics Resistance Compensation	I A
PEG_RBIAS	PCI Express Resistor Bias Control	I A

6.5 Embedded DisplayPort (eDP)

Table 30. Embedded Display Port Signals (Sheet 1 of 2)

Signal Name	Description	Direction / Buffer Type
eDP_TX[3:0] eDP_TX#[3:0]	**Embedded DisplayPort Transmit Differential Pair:** Nominally, eDP_TX[3:0] is multiplexed with PEG_TX[12:15] and eDP_TX#[3:0] is multiplexed with PEG_TX#[12:15]. When reversed, eDP_TX[3:0] is multiplexed with PEG_TX[3:0] and eDP_TX#[3:0] is multiplexed with PEG_TX#[3:0]	O PCI Express
eDP_AUX eDP_AUX#	**Embedded DisplayPort Auxiliary Differential Pair:** Nominally, eDP_AUX is multiplexed with PEG_RX[13] and eDP_AUX# is multiplexed with PEG_RX#[13]. When reversed, eDP_AUX is multiplexed with PEG_RX[2] and eDP_AUX# is multiplexed with PEG_RX#[2]	I/O PCI Express
eDP_HPD#	**Embedded DisplayPort Hot Plug Detect:** Nominally, eDP_HPD# is multiplexed with PEG_RX[12]. When reversed, eDP_HPD# is multiplexed with PEG_RX[3]	I PCI Express
eDP_ICOMPI	**Embedded DisplayPort Input Current Compensation:** Multiplexed with PEG_ICOMPI	I A

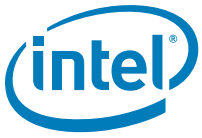


Table 30. Embedded Display Port Signals (Sheet 2 of 2)

Signal Name	Description	Direction / Buffer Type
eDP_ICOMPO	**Embedded DisplayPort Output Current and Resistance Compensation:** Multiplexed with PEG_ICOMPO	I A
eDP_RCOMPO	**Embedded DisplayPort Resistance Compensation:** Multiplexed with PEG_RCOMPO	I A
eDP_RBIAS	**Embedded DisplayPort Resistor Bias Control:** Multiplexed with PEG_RBIAS	I A

6.6 Intel Flexible Display Interface Signals

Table 31. Intel® Flexible Display Interface

Signal Name	Description	Direction / Buffer Type
FDI_TX[3:0] FDI_TX#[3:0]	**Intel® Flexible Display Interface Transmit Differential Pair - Pipe A**	O FDI
FDI_FSYNC[0]	Intel® Flexible Display Interface Frame Sync - Pipe A	I CMOS
FDI_LSYNC[0]	Intel® Flexible Display Interface Line Sync - Pipe A	I CMOS
FDI_TX[7:4] FDI_TX#[7:4]	**Intel® Flexible Display Interface Transmit Differential Pair - Pipe B**	O FDI
FDI_FSYNC[1]	Intel® Flexible Display Interface Frame Sync - Pipe B	I CMOS
FDI_LSYNC[1]	Intel® Flexible Display Interface Line Sync - Pipe B	I CMOS
FDI_INT	Intel® Flexible Display Interface Hot Plug Interrupt	I CMOS

6.7 DMI

Table 32. DMI - Processor to PCH Serial Interface

Signal Name	Description	Direction / Buffer Type
DMI_RX[3:0] DMI_RX#[3:0]	**DMI Input from PCH:** Direct Media Interface receive differential pair.	I DMI
DMI_TX[3:0] DMI_TX#[3:0]	**DMI Output to PCH:** Direct Media Interface transmit differential pair.	O DMI

6.8 PLL Signals

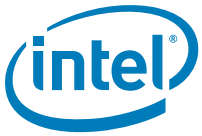
Table 33. PLL Signals

Signal Name	Description	Direction / Buffer Type
BCLK BCLK#	Differential bus clock input to the processor	I Diff Clk
BCLK_ITP BCLK_ITP#	Buffered differential bus clock pair to ITP	O Diff Clk
PEG_CLK PEG_CLK#	**Differential PCI Express Based Graphics / DMI Clock In:** These pins receive a 100-MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express. This also is the reference clock for Intel® FDI.	I Diff Clk
DPLL_REF_SSCLK DPLL_REF_SSCLK#	**Embedded Display Port PLL Differential Clock In:** With or without SSC -120 MHz.	I Diff Clk

6.9 TAP Signals

Table 34. TAP Signals

Signal Name	Description	Direction / Buffer Type
TCK	**TCK (Test Clock):** Provides the clock input for the processor Test Bus (also known as the Test Access Port).	I CMOS
TDI	**TDI (Test Data In):** Transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.	I CMOS
TDO	Test Data Output	O CMOS
TDI_M	**Test Data In for the GPU / Memory core:** Tie TDI_M and TDO_M together on the motherboard	I CMOS
TDO_M	**Test Data Output from the processor core:** Tie TDO_M and TDI_M together on the motherboard.	O CMOS
TMS	**TMS (Test Mode Select):** A JTAG specification support signal used by debug tools.	I CMOS
TRST#	TRST# (Test Reset) Boundary-Scan test reset pin	I CMOS
TAPPWRGOOD	Power good for ITP	O Asynchronous CMOS



6.10 Error and Thermal Protection

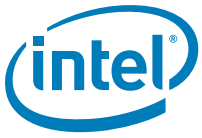
Table 35. Error and Thermal Protection

Signal Name	Description	Direction / Buffer Type
CATERR#	**Catastrophic Error:** This signal indicates that the system has experienced a catastrophic error and cannot continue to operate. The processor will set this for non-recoverable machine check errors or other unrecoverable internal errors. External agents are allowed to assert this pin which will cause the processor to take a machine check exception.	I/O GTL
PECI	**PECI (Platform Environment Control Interface):** A serial sideband interface to the processor, it is used primarily for thermal, power, and error management. Details regarding the PECI electrical specifications, protocols, and functions can be found in the RS - Platform Environment Control Interface (PECI) Specification, Revision 2.0.	I/O Asynchronous
PROCHOT#	**Processor Hot:** PROCHOT# goes active when the processor temperature monitoring sensor(s) detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. This signal can also be driven to the processor to activate the TCC.	I/O Asynchronous GTL
THERMTRIP#	**Thermal Trip:** The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when the junction temperature exceeds approximately 130°C. This is signaled to the system by the THERMTRIP# pin. Refer to the appropriate platform design guide for termination requirements.	O Asynchronous GTL

6.11 Power Sequencing

Table 36. Power Sequencing

Signal Name	Description	Direction / Buffer Type
VCCPWRGOOD_0 VCCPWRGOOD_1	**VCCPWRGOOD_0 and VCCPWRGOOD_1 (Power Good) Processor Input:** The processor requires these signals to be a clean indication that: -VCC, VCCPLL, and VTT supplies are stable and within their specifications -BCLK is stable and has been running for a minimum number of cycles. Both signals must then transition monotonically to a high state. VCCPWRGOOD_0 and VCCPWRGOOD_1 can be driven inactive at any time, but BCLK and power must again be stable before a subsequent rising edge of these signals. VCCPWRGOOD_0 and VCCPWRGOOD_1 should be tied together and connected to the PROCPWRGD output signal of the PCH.	I Asynchronous CMOS
SM_DRAMPWROK	**SM_DRAMPWROK Processor Input**: Connects to PCH DRAMPWROK.	I Asynchronous CMOS
VTTPWRGOOD	**VTTPWRGOOD Processor Input:** The processor requires this input signal to be a clean indication that the VTT power supply is stable and within specifications. Clean implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. Note it is not valid for VTTPWRGOOD to be deasserted while VCCPWRGOOD_0 and VCCPWRGOOD_1 is asserted.	I Asynchronous CMOS
SKTOCC#(rPGA988A only) PROC_DETECT (BGA only)	**SKTOCC# (Socket Occupied) / PROC_DETECT (Processor Detect):** pulled to ground on the processor package. There is no connection to the processor silicon for this signal. System board designers may use this signal to determine if the processor is present.	



6.12 Processor Power Signals

Table 37. Processor Power Signals (Sheet 1 of 3)

Signal Name	Description	Direction / Buffer Type
VCC	Processor core power rail.	Ref
VTT (VTT0 and VTT1)	Processor I/O power rail (1.05 V). VTT0 and VTT1 should share the same VR	Ref
VDDQ	DDR3 power rail (1.5 V)	Ref
VCCPLL	Power rail for filters and PLLs (1.8 V)	Ref
ISENSE	Current Sense from an Intel® MVP6.5 Compliant Regulator to the processor core.	I A
PROC_DPRSLPVR	Processor output signal to Intel MVP-6.5 controller to indicate that the processor is in the package C6 state.	O CMOS
PSI#	**Processor Power Status Indicator:** This signal is asserted when the processor core current consumption is less than 15 A. Assertion of this signal is an indication that the VR controller does not currently need to provide ICC above 15 A. The VR controller can use this information to move to a more efficient operating point. This signal will de-assert at least 3.3 µs before the current consumption will exceed 15 A. The minimum PSI# assertion and de-assertion time is 1 BCLK. Refer to the *Intel® MVP-6.5 Mobile Processor and Mobile Chipset Voltage Regulator Specification* for more details on the PSI# Signal	O Asynchronous CMOS

Table 37. Processor Power Signals (Sheet 2 of 3)

Signal Name	Description	Direction / Buffer Type
VID[6] VID[5:3]/CSC[2:0] VID[2:0]/MSID[2:0]	**VID[6:0] (Voltage ID) Pins:** Used to support automatic selection of power supply voltages (VCC). These are CMOS signals that are driven by the processor. **CSC[2:0]/VID[5:3]** - Current Sense Configuration bits, for ISENSE gain setting. See I-MVP6.5 Mobile Processor and Mobile Chipset Voltage Regulator Specification for more information. This value is latched on the rising edge of VTTPWRGOOD. **MSID[2:0]/VID[2:0]-** Market Segment Identification is used to indicate the maximum platform capability to the processor. A processor will only boot if the MSID[2:0] pins are strapped to the appropriate setting (or higher) on the platform (see **"Market Segment Selection Truth Table for MSID[2:0]" on page 89** for MSID encodings). MSID is used to help protect the platform by preventing a higher power processor from booting in a platform designed for lower power processors. Refer to the appropriate platform design guide for implementation details. MSID[2:0] are latched on the rising edge of VTTPWRGOOD. **NOTE:** VID[5:3] and VID[2:0] are bi-directional. As an input, they are CSC[2:0] and MSID[2:0] respectively.	O CMOS
VTT_SELECT	The VTT_SELECT signal is used to select the correct VTT voltage level for the processor. Refer to the Platform Design Guide for implementation details.	O CMOS
VCC_SENSE VSS_SENSE	Voltage Feedback Signals to an Intel MVP-6.5 Compliant VR: Use VCC_SENSE to sense voltage and VSS_SENSE to sense ground near the silicon with little noise.	O A
VTT_SENSE VSS_SENSE_VTT	Isolated low impedance connection to the processor VTT voltage and ground. They can be used to sense or measure voltage near the silicon.	O A
VAXG	Graphics core power rail.	Ref
VAXG_SENSE VSSAXG_SENSE	VAXG_SENSE and VSSAXG_SENSE provide an isolated, low impedance connection to the VAXG voltage and ground. They can be used to sense or measure voltage near the silicon.	O A
GFX_VID[6:0]	GFX_VID[6:0] (Voltage ID) pins are used to support automatic selection of nominal voltages (VAXG). These are CMOS signals that are driven by the processor.	O CMOS

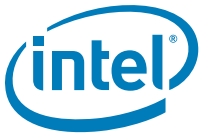


Table 37. Processor Power Signals (Sheet 3 of 3)

Signal Name	Description	Direction / Buffer Type
GFX_VR_EN	GPU output signal to Intel MVP6.5 compliant VR. This signal is used as an on/off control to enable/disable the GPU VR.	O CMOS
GFX_DPRSLPVR	GPU output signal to Intel MVP6.5 compliant VR. When asserted this signal indicates that the GPU is in render suspend mode. This signal is also used to control render suspend state exit slew rate.	O CMOS
GFX_IMON	Current Sense from an Intel MVP6.5 Compliant Regulator to the GPU.	I A
VDDQ_CK	Filtered power for VDDQ (BGA Only)	Ref
VTT0_DDR	Filtered power for VTT0 (BGA Only)	Ref
VCAP0 VCAP1 VCAP2	Processor Connection to On-board decoupling capacitors (BGA only)	PWR

6.13 Ground and NCTF

Table 38. Ground and NCTF

Signal Name	Description	Direction / Buffer Type
VSS	Processor ground node	GND
VSS_NCTF	**Non-Critical to Function:** The pins are for package mechanical reliability.	
DC_TEST_xx#	**Daisy Chain Test** - These pins are for solder joint reliability and are non-critical to function. See *[Calpella] Platform, for Arrandale, Clarksfield and Mobile Intel® 5 Series Chipset – Design Guide* for more details on implementation. (BGA only)	NC

6.14 Processor Internal Pull Up / Pull Down

Table 39. Processor Internal Pull Up / Pull Down

Signal Name	Pull Up / Pull Down	Rail	Value
SM_DRAMPWROK	Pull Down	VSS	10 - 20 kΩ
VCCPWRGOOD_0 VCCPWRGOOD_1	Pull Down	VSS	10 - 20 kΩ
VTTPWRGOOD	Pull Down	VSS	10 - 20 kΩ
BPM#[7:0]	Pull Up	VTT	44 - 55 kΩ
TCK	Pull Up	VTT	44 - 55 kΩ
TDI	Pull Up	VTT	44 - 55 kΩ

Table 39. Processor Internal Pull Up/Pull Down

Signal Name	Pull Up/Pull Down	Rail	Value
TMS	Pull Up	VTT	44 - 55 kΩ
TRST#	Pull Up	VTT	1 - 5 kΩ
TDI_M	Pull Up	VTT	44 - 55 kΩ
PREQ#	Pull Up	VTT	44 - 55 kΩ
CFG[17:0]	Pull Up	VTT	5 - 14 kΩ

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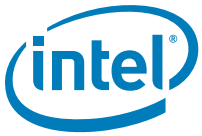


7 Electrical Specifications

7.1 Power and Ground Pins

The processor has V_{CC}, V_{TT}, V_{DDQ}, V_{CCPLL}, V_{AXG} and V_{SS} (ground) inputs for on-chip power distribution. All power pins must be connected to their respective processor power planes, while all V_{SS} pins must be connected to the system ground plane. Use of multiple power and ground planes is recommended to reduce I*R drop. The V_{CC} pins must be supplied with the voltage determined by the processor **V**oltage **ID**entification (VID) signals. Likewise, the V_{AXG} pins must also be supplied with the voltage determined by the GFX_VID signals. Table 40 specifies the voltage level for the various VIDs. The voltage levels are the same for both the processor VIDs and GFX_VIDs.

7.2 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large current swings between low- and full-power states. To keep voltages within specification, output decoupling must be properly designed.

Caution: Design the board to ensure that the voltage provided to the processor remains within the specifications listed in Table 40. Failure to do so can result in timing violations or reduced lifetime of the processor. For further information and design guidelines, refer to the *Calpella Platform Design Guide* and the *RS - Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification*

7.2.1 Voltage Rail Decoupling

The voltage regulator solution must:

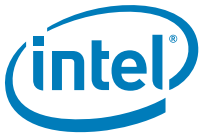
- provide sufficient decoupling to compensate for large current swings generated during different power mode transitions.
- provide low parasitic resistance from the regulator to the socket.
- meet voltage and current specifications as defined in Table 40.

For further information regarding power delivery, decoupling, and layout guidelines refer to the *Calpella Platform Design Guide* and the *Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification*

7.3 Processor Clocking (BCLK, BCLK#)

The processor utilizes a differential clock to generate the processor core(s) operating frequency, memory controller frequency, and other internal clocks. The processor core frequency is determined by multiplying the processor core ratio by 133 MHz. Clock multiplying within the processor is provided by an internal phase locked loop (PLL), which requires a constant frequency input, with exceptions for Spread Spectrum Clocking (SSC).

The processor's maximum core frequency is configured during power-on reset by using its manufacturing default value. This value is the highest core multiplier at which the processor can operate.



7.3.1 PLL Power Supply

An on-die PLL filter solution is implemented on the processor. Refer to Table 40 for DC specifications and to the *Calpella Platform Design Guide* for decoupling and routing guidelines.

7.4 Voltage Identification (VID)

The processor uses seven voltage identification pins, VID[6:0], to support automatic selection of the processor power supply voltages. VID pins for the processor are CMOS outputs driven by the processor VID circuitry. A dedicated graphics voltage regulator is required to deliver voltage to the integrated graphics controller. Like the processor core, the integrated graphics controller will use seven voltage identification pins, GFX_VID[6:0], to set the nominal operating voltage GFX_VID pins for the graphics core are CMOS outputs driven by the graphics core VID circuitry. Table 40 specifies the voltage level for VID[6:0] and GFX_VID[6:0]; 0 refers to a low-voltage level. For more details about VR design and how to satisfy processor power supply requirements, please refer to the *Intel® Mobile Voltage Positioning (Intel® MVP). 6.5 Mobile Processor and Chipset Voltage Regulation – Product Specification*

VID signals are CMOS push/pull drivers. Refer to Table 49 for the DC specifications for these signals. The VID codes will change due to temperature, frequency, and/or power mode load changes in order to minimize the power of the part. A voltage range is provided in Table 40. The specifications are set so that one voltage regulator can operate with all supported frequencies.

Individual processor VID values may be set during manufacturing so that two devices at the same core frequency may have different default VID settings. This is shown in the VID range values in Table 40. The processor provides the ability to operate while transitioning to an adjacent VID and its associated processor core voltage (V_{CC}). This will represent a DC shift in the loadline.

Note: A low-to-high or high-to-low voltage state change will result in as many VID transitions as necessary to reach the target core voltage. Transitions above the maximum or below the minimum specified VID are not permitted. One VID transition occurs in 2.5 µs.

The VR utilized must be capable of regulating its output to the value defined by the new VID values issued. DC specifications for dynamic VID transitions are included in Table 40, while AC specifications are included in Table 65. See the *Intel® MVP6.5 Mobile Processor and Mobile Chipset Voltage Regulation Specification* for further details.

Several of the VID signals (VID[5:3]/CSC[2:0] and VID[2:0]/MSID[2:0]) serve a dual purpose and are sampled during reset. Refer to the signal description table in Chapter 6 for more information. Refer to the *[Calpella] Platform, for Arrandale, Clarksfield and Mobile Intel® 5 Series Chipset – Design Guide* and the *Intel® MVP6.5 Mobile Processor and Mobile Chipset Voltage Regulation Specification* for additional implementation details.

Table 40. Voltage Identification Definition (Sheet 1 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375

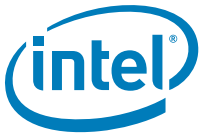


Table 40. Voltage Identification Definition (Sheet 2 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500

Table 40. Voltage Identification Definition (Sheet 3 of 3)

VID6	VID5	VID4	VID3	VID2	VID1	VID0	V_{CC} (V)
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
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1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

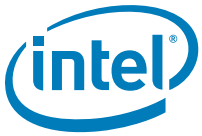


Table 41. Market Segment Selection Truth Table for MSID[2:0]

MSID[2]	MSID[1]	MSID[0]	Description[1,2]	Notes
0	0	0	Reserved	
0	0	1	Reserved	
0	1	0	Reserved	
0	1	1	Reserved	
1	0	0	Standard Voltage (SV) 35-W Supported	3
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

NOTES:
1. MSID[2:0] signals are provided to indicate the maximum platform capability to the processor.
2. MSID is used on rPGA988A platforms only.
3. Processors specified for use with a -1.9 mΩ

7.5 Reserved or Unused Signals

The following are the general types of reserved (RSVD) signals and connection guidelines:

- RSVD - these signals should not be connected
- RSVD_TP - these signals should be routed to a test point
- RSVD_NCTF - these signals are non-critical to function and may be left un-connected

Arbitrary connection of these signals to V_{CC}, V_{TT}, V_{DDQ}, V_{CCPLL}, V_{AXG}, V_{SS}, or to any other signal (including each other) may result in component malfunction or incompatibility with future processors. See Chapter 8 for a pin listing of the processor and the location of all reserved signals.

For reliable operation, always connect unused inputs or bi-directional signals to an appropriate signal level. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs maybe left unconnected; however, this may interfere with some Test Access Port (TAP) functions, complicate debug probing, and prevent boundary scan testing. A resistor must be used when tying bi-directional signals to power or ground. When tying any signal to power or ground, a resistor will also allow for system testability. Resistor values should be within ±20% of the impedance of the baseboard trace, unless otherwise noted in the appropriate platform design guidelines. For details see Table 49.

7.6 Signal Groups

Signals are grouped by buffer type and similar characteristics as listed in Table 42. The buffer type indicates which signaling technology and specifications apply to the signals. All the differential signals, and selected DDR3 and Control Sideband signals have On-Die Termination (ODT) resistors. There are some signals that do not have ODT and need to be terminated on the board.

Table 42. Signal Groups[1] (Sheet 1 of 3)

Signal Group	Alpha Group	Type	Signals
System Reference Clock			
Differential	(a)	CMOS Input	BCLK, BCLK# PEG_CLK, PEG_CLK# DPLL_REF_SSCLK, DPLL_REF_SSCLK#
Differential	(b)	CMOS Output	BCLK_ITP, BCLK_ITP#
DDR3 Reference Clocks[2]			
Differential	(c)	DDR3 Output	SA_CK[1:0], SA_CK#[1:0] SB_CK[1:0], SB_CK#[1:0]
DDR3 Command Signals[2]			
Single Ended	(d)	DDR3 Output	SA_RAS#, SB_RAS#, SA_CAS#, SB_CAS# SA_WE#, SB_WE# SA_MA[15:0], SB_MA[15:0] SA_BS[2:0], SB_BS[2:0] SA_DM[7:0], SB_DM[7:0] SM_DRAMRST# SA_CS#[1:0], SB_CS#[1:0] SA_ODT[1:0], SB_ODT[1:0] SA_CKE[1:0], SB_CKE[1:0]
DDR3 Data Signals[2]			
Single ended	(e)	DDR3 Bi-directional	SA_DQ[63:0], SB_DQ[63:0]
Differential	(f)	DDR3 Bi-directional	SA_DQS[7:0], SA_DQS#[7:0] SB_DQS[7:0], SB_DQS#[7:0]
TAP (ITP/XDP)			
Single Ended	(g)	CMOS Input	TCK, TMS, TRST#
Single Ended	(ga)	CMOS Input	TDI,TDI_M
Single Ended	(h)	CMOS Open-Drain Output	TDO, TDO_M
Single Ended	(i)	Asynchronous CMOS Output	TAPPWRGOOD

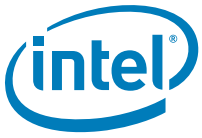


Table 42. Signal Groups[1] (Sheet 2 of 3)

Signal Group	Alpha Group	Type	Signals
Control Sideband			
Single Ended	(ja)	Asynchronous CMOS Input	$V_{CCPWRGOOD\_0}$, $V_{CCPWRGOOD\_1}$, $V_{TTPWRGOOD}$
Single Ended	(jb)	Asynchronous CMOS Input	SM_DRAMPWROK
Single Ended	(k)	Asynchronous CMOS Output	RESET_OBS#
Single Ended	(l)	Asynchronous GTL Output	PRDY#, THERMTRIP#
Single Ended	(m)	Asynchronous GTL Input	PREQ#
Single Ended	(n)	GTL Bi-directional	CATERR#, BPM#[7:0]
Single Ended	(o)	Asynchronous Bi-directional	PECI
Single Ended	(p)	Asynchronous GTL Bi-directional	PROCHOT#
Single Ended	(qa)	CMOS Input	PM_SYNC, PM_EXT_TS#[0], PM_EXT_TS#[1], CFG[17:0]
Single Ended	(qb)	CMOS Input	RSTIN#
Single Ended	(r)	CMOS Output	PROC_DPRSLPVR VID[6] V_{TT_SELECT}
Single Ended	(s)	CMOS Bi-directional	VID[5:3]/CSC[2:0] VID[2:0]/MSID[2:0]
Single Ended	(t)	Analog Input	COMP0, COMP1, COMP2, COMP3, SM_RCOMP[2:0], I_{SENSE}
Single Ended	(ta)	Analog Output	SA_DIMM_VREFDQ[5], SB_DIMM_VREFDQ[5]
Power/Ground/Other			
Single Ended	(u)	Power	V_{CC}, V_{TT0}, V_{TT1}, V_{CCPLL}, V_{DDQ}, V_{AXG}, V_{TT0_DDR}[3], V_{DDQ_CK}[3]
	(v)	Ground	V_{SS}, V_{SS_NCTF}, DC_TEST_xx#[3]
	(w)	No Connect /Test Point	RSVD, RSVD_TP, RSVD_NCTF
	(x)	Asynchronous CMOS Output	PSI#
	(y)	Sense Points	V_{CC_SENSE}, V_{SS_SENSE}, V_{TT_SENSE}, $V_{SS\_SENSE\_VTT}$, V_{AXG_SENSE}, V_{SSAXG_SENSE}
	(z)	Other	SKTOCC#, DBR#, PROC_DETECT[3], VCAP0[3], VCAP[3], VCAP2[3]

Table 42. Signal Groups[1] (Sheet 3 of 3)

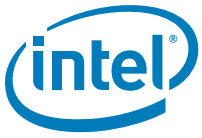
Signal Group	Alpha Group	Type	Signals
Integrated Graphics			
Single Ended	(aa)	Analog Input	GFX_IMON
Single Ended	(ab)	CMOS Output	GFX_VID[6:0], GFX_VR_EN, GFX_DPRSLPVR
PCI Express* Graphics			
Differential	(ac)	PCI Express Input	PEG_RX[15:0], PEG_RX#[15:0]
Differential	(ad)	PCI Express Output	PEG_TX[15:0], PEG_TX#[15:0]
Single Ended	(ae)	Analog Input	PEG_ICOMP0, PEG_ICOMPI, PEG_RCOMP0, PEG_RBIAS
DMI			
Differential	(af)	DMI Input	DMI_RX[3:0], DMI_RX#[3:0]
Differential	(ag)	DMI Output	DMI_TX[3:0], DMI_TX#[3:0]
Intel® FDI			
Single Ended	(ah)	CMOS Input	FDI_FSYNC[1:0], FDI_LSYNC[1:0], FDI_INT
Differential	(ai)	Analog Output	FDI_TX[7:0], FDI_TX#[7:0]

NOTES:
1. Refer to Chapter 6 for signal description details.
2. SA and SB refer to DDR3 Channel A and DDR3 Channel B.
3. These signals are only applicable for the ARD BGA package
4. These signals are only applicable for the rPGA988A package.
5. These signals are not applicable for Arrandale processors and should be left as no connects on platforms using only Arrandale processors.

All Control Sideband Asynchronous signals are required to be asserted/deasserted for at least eight BCLKs in order for the processor to recognize the proper signal state. See Section 7.10 and Section 7.12 for the DC and AC specifications.

7.7 Test Access Port (TAP) Connection

Due to the voltage levels supported by other components in the Test Access Port (TAP) logic, Intel recommends the processor be first in the TAP chain, followed by any other components within the system. Please refer to the *Arrandale and Clarksfield Processor Testability Information – Boundary Scan Description Language (BSDL) File* for more details. A translation buffer should be used to connect to the rest of the chain unless one of the other components is capable of accepting an input of the appropriate voltage. Two copies of each signal may be required with each driving a different voltage level.



7.8 Absolute Maximum and Minimum Ratings

Table 43 specifies absolute maximum and minimum ratings. At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits (but within the absolute maximum and minimum ratings) the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time it will either not function or its reliability will be severely degraded when returned to conditions within the functional operating condition limits.

Although the processor contains protective circuitry to resist damage from Electro-Static Discharge (ESD), precautions should always be taken to avoid high static voltages or electric fields.

Table 43. Processor Absolute Minimum and Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{CC}	Processor Core voltage with respect to V_{SS}	-0.3	1.40	V	1, 2, 3
V_{TT}	Voltage for the memory controller and Shared Cache with respect to V_{SS}	-0.3	1.40	V	1, 2
V_{DDQ}	Processor I/O supply voltage for DDR3 with respect to V_{SS}	-0.3	1.80	V	1, 2
V_{CCPLL}	Processor PLL voltage with respect to V_{SS}	-0.3	1.98	V	1, 2
V_{AXG}	Graphics voltage with respect to V_{SS} SV LV ULV	 -0.3 -0.3 -0.3	 1.55 1.55 1.55	 V V V	 1, 2, 3, 4 1, 2, 3, 4 1, 2, 3, 4

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Overshoot and undershoot voltage guidelines for input, output, and I/O signals are outlined in Section . Excessive overshoot or undershoot on any signal will likely result in permanent damage to the processor.
3. V_{CC} and V_{AXG} are VID based rails.

7.9 Storage Conditions Specifications

Environmental storage condition limits define the temperature and relative humidity to which the device is exposed to while being stored in a moisture barrier bag. The specified storage conditions are for component level prior to board attach.

Table 44 specifies absolute maximum and minimum storage temperature limits which represent the maximum or minimum device condition beyond which damage, latent or otherwise, may occur. The table also specifies sustained storage temperature, relative humidity, and time-duration limits. these limits specify the maximum or minimum device storage conditions for a sustained period of time. At conditions outside sustained limits, but within absolute maximum and minimum ratings, quality and reliability may be affected.

Table 44. Storage Condition Ratings

Symbol	Parameter	Min	Max	Notes
$T_{absolute\ storage}$	The non-operating device storage temperature. Damage (latent or otherwise) may occur when exceeded for any length of time.	-25°C	125°C	1, 2, 3, 4
$T_{sustained\ storage}$	The ambient storage temperature (in shipping media) for a sustained period of time)	-5°C	40°C	5, 6
$RH_{sustained\ storage}$	The maximum device storage relative humidity for a sustained period of time.	60% @ 24°C		6, 7
Time $_{sustained\ storage}$	A prolonged or extended period of time; typically associated with customer shelf life.	0 Months	6 Months	7

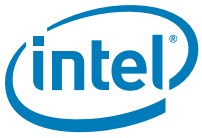
NOTES:
1. Refers to a component device that is not assembled in a board or socket and is not electrically connected to a voltage reference or I/O signal.
2. Specified temperatures are not to exceed values based on data collected. Exceptions for surface mount reflow are specified by the applicable JEDEC standard. Non-adherence may affect processor reliability.
3. $T_{absolute\ storage}$ applies to the unassembled component only and does not apply to the shipping media, moisture barrier bags, or desiccant.
4. Component product device storage temperature qualification methods may follow JESD22-A119 (low temp) and JESD22-A103 (high temp) standards when applicable for volatile memory.
5. Intel® branded products are specified and certified to meet the following temperature and humidity limits that are given as an example only (Non-Operating Temperature Limit: -40°C to 70°C and Humidity: 50% to 90%, non-condensing with a maximum wet bulb of 28°C.) Post board attach storage temperature limits are not specified for non-Intel branded boards.
6. The JEDEC J-JSTD-020 moisture level rating and associated handling practices apply to all moisture sensitive devices removed from the moisture barrier bag.
7. Nominal temperature and humidity conditions and durations are given and tested within the constraints imposed by $T_{sustained\ storage}$ and customer shelf life in applicable Intel boxes and bags.

7.10 DC Specifications

The processor DC specifications in this section are defined at the processor pins, unless noted otherwise. See Chapter 8 for the processor pin listings and Chapter 6 for signal definitions.

The DC specifications for the DDR3 signals are listed in Table 48 Control Sideband and Test Access Port (TAP) are listed in Table 49.

Table 55 lists the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.



7.10.1 Voltage and Current Specifications

Table 45. Arrandale Processor Core (VCC) Active and Idle Mode DC Voltage and Current Specifications

Symbol	Parameter	Segment	Min	Typ	Max	Unit	Note
HFM_VID	VID Range for Highest Frequency Mode	SV ULV	0.800 0.750		1.4 1.4	V	1,2,7
LFM_VID	VID Range for Lowest Frequency Mode	SV ULV	0.775 0.725		1.0 1.0	V	1,2
V_{CC}	V_{CC} for processor core		See Figure 13 and Figure 14			V	2, 3, 4
I_{CCMAX}	Maximum Processor Core I_{CC}	SV ULV			48 27	A	5,7
I_{CC_TDC}	Thermal Design I_{CC}	SV ULV			32 16	A	6,7
I_{CC_LFM}	I_{CC} at LFM	SV ULV			18 8	A	6
I_{C6}	I_{CC} at C6 Idle-state	SV ULV			0.3 0.3	A	
TOL_{VID}	VID Tolerance		See Figure 13 and Figure 14				
VR Step	VID resolution			12.5		mV	
$SLOPE_{LL}$	Processor Loadline	SV ULV		-1.9 -3.0		mΩ	
Non-VR LL contribution	Non-VR Loadline Contribution for V_{CC}			-0.9		mΩ	

NOTES:
1. Unless otherwise noted, all specifications in this table are based on pre-silicon estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
2. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and cannot be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within the VID range. Please note this differs from the VID employed by the processor during a power or thermal management event (Intel Adaptive Thermal Monitor, Enhanced Intel SpeedStep Technology, or Low Power States).
3. The voltage specification requirements are defined across VCC_SENSE and VSS_SENSE pins on the bottom side of the baseboard. Please refer to 7.10.2 for core voltage validation.
4. Refer to Figure 13 and Figure 14 for the minimum, typical, and maximum V_{CC} allowed for a given current. The processor should not be subjected to any V_{CC} and I_{CC} combination wherein V_{CC} exceeds V_{CC_MAX} for a given current.
5. Processor core VR to be designed to electrically support this current
6. Processor core VR to be designed to thermally support this current indefinitely.
7. This specification assumes that Intel Turbo Boost Technology with Intelligent Power Sharing is enabled.

Figure 13. Active V_{CC} and I_{CC} Loadline (PSI# Asserted)

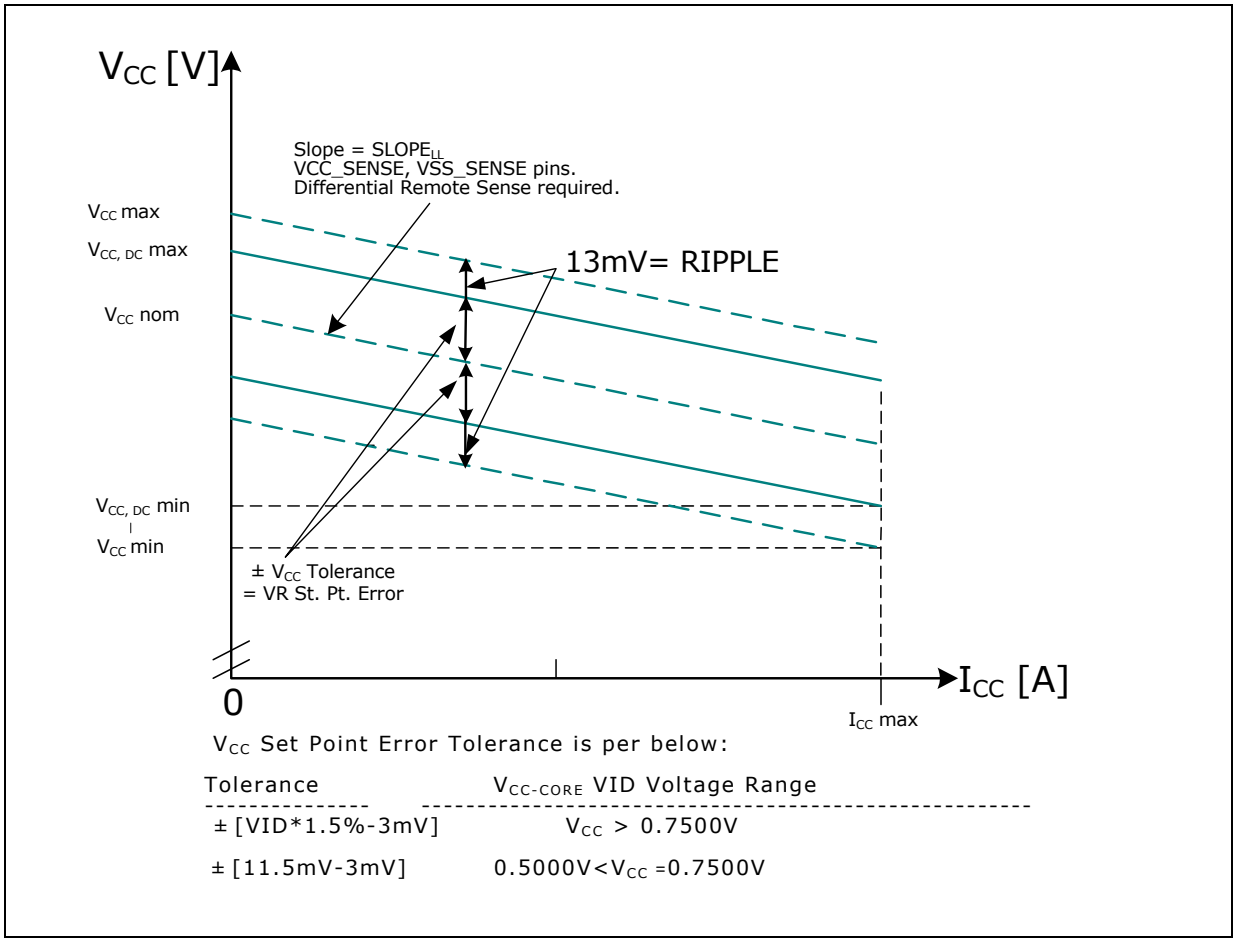
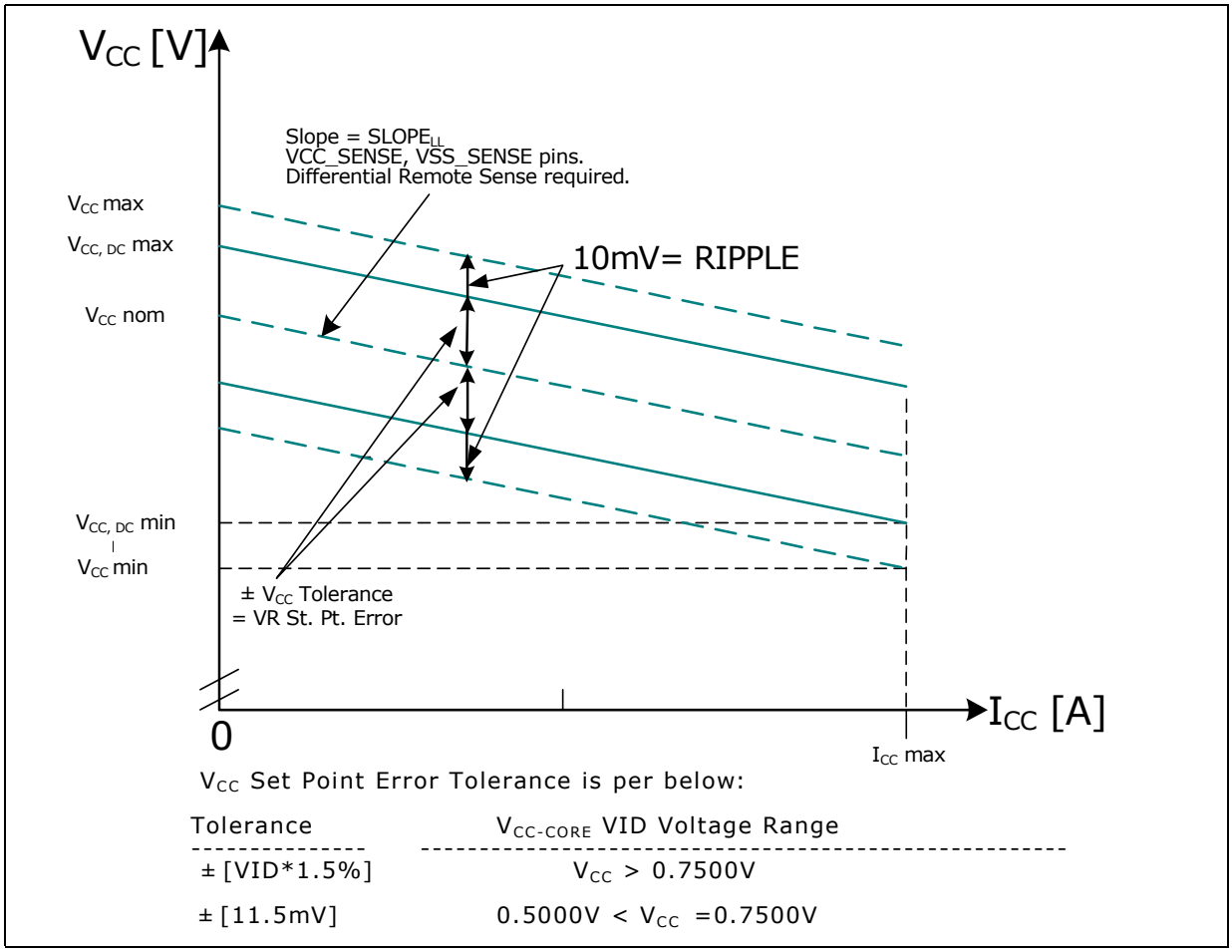


Figure 14. Active V_{CC} and I_{CC} Loadline (PSI# Not Asserted)



V_{CC} Set Point Error Tolerance is per below:

Tolerance	$V_{CC-CORE}$ VID Voltage Range
± [VID*1.5%]	V_{CC} > 0.7500V
± [11.5mV]	0.5000V < V_{CC} =0.7500V

Table 46. Processor Uncore I/O Buffer Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
V_{TT}	Voltage for the memory controller and shared cache defined at the motherboard Vtt pinfield via	0.9975	1.05	1.1025	V	1
	Voltage for the memory controller and shared cache defined across VTT_SENSE and VSS_SENSE_VTT	0.9765	1.05	1.1235	V	2
V_{DDQ}(DC+AC)	Processor I/O supply voltage for DDR3 (DC + AC specification)	1.425	1.5	1.575	V	
V_{CCPLL}	PLL supply voltage (DC + AC specification)	1.710	1.8	1.890	V	
TOL_{TT}	V_{TT} Tolerance defined at the socket motherboard VTT pinfield via	DC: ±2% AC: ±3% including ripple			%	1
	V_{TT} Tolerance defined across VTT_SENSE and VSS_SENSE_VTT	DC: ±2% AC: ±5% including ripple				2
TOL_{DDQ}	VDDQ Tolerance	DC= ±3% AC= ±2% AC+DC= ±5%			%	
TOL_{CCPLL}	VCCPLL Tolerance	AC+DC= ±5%			%	
I_{CCMAX_VTT}	Max Current for V_{TT} Rail SV ULV		-	 18 16	A	3
I_{CCMAX_VDDQ}	Max Current for V_{DDQ} Rail		-	3	A	
$I_{CCMAX\_VDDQ\_CK}$	BGA Only.			0.2	A	4
$I_{CCMAX\_VTT0\_DDR}$	BGA Only			2.6	A	4
I_{CCMAX_VCCPLL}	Max Current for V_{CCPLL} Rail		-	1.35	A	
I_{CCTDC_VTT}	Thermal Design Current (TDC) for V_{TT} Rail SV ULV		-	 18 16	A	3
I_{CCAVG_VDDQ} (Standby)	Average Current for V_{DDQ} Rail during Standby		-	0.33	A	5

NOTES:
1. The voltage specification requirements are defined across at the socket motherboard pinfield vias on the bottom side of the baseboard. Please refer to 7.10.3 for uncore voltage validation.
2. The voltage specification requirements are defined across VTT_SENSE and VSS_SENSE_VTT pins on the bottom side of the baseboard. Please refer to 7.10.3 for uncore voltage validation.
3. Defined at nominal VTT voltage
4. These are pre-silicon estimates and are subject to change.
5. Based on junction temperature of 50°C.

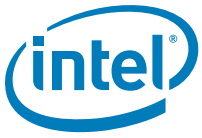
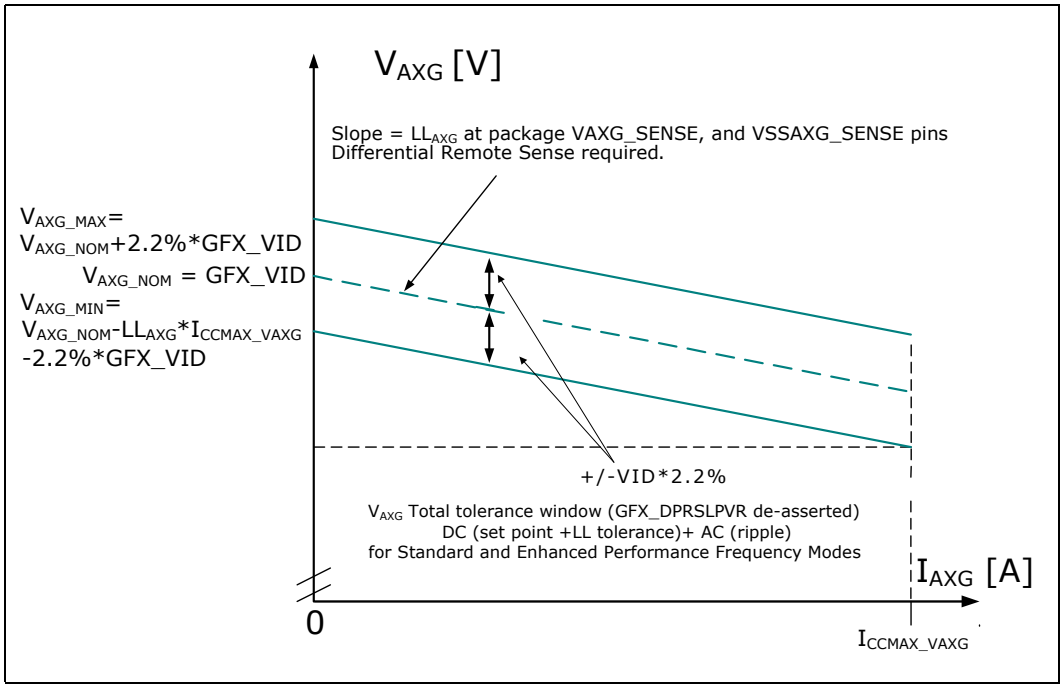


Table 47. Processor Graphics VID based (V_{AXG}) Supply DC Voltage and Current Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note[1]
GFX_VID	VID Range for V_{AXG} SV ULV	 0 0		 1.4 1.35	 V V	2,3,4
V_{AXG}	Graphics core voltage	See Figure 15				
TOL_{AXG}	V_{AXG} Tolerance	See Figure 15				
Non-VR LL contribution	Non-VR Load Line Contribution for V_{AXG} rPGA BGA	 4 4.25			 mΩ mΩ	
LL_{AXG}	V_{AXG} Loadline	-7			mΩ	
I_{CCMAX_VAXG}	Max Current for Integrated Graphics Rail SV ULV		-	 22 12	A	4
I_{CCTDC_VAXG}	Thermal Design Current (TDC) for Integrated Graphics Rail SV ULV		-	 12 6	A	4

NOTES:
1. These are pre-silicon estimates and are subject to change.
2. Minimum values assume Graphics Render C-state (RC6) is enabled.
3. V_{AXG} is a VID-Based rail driven by an Intel MVP6.5 compliant voltage regulator.
4. This specification assumes Intel Turbo Boost Technology with Intelligent Power Sharing is enabled.
5. Please refer to Section 7.10.2 for V_{AXG} Validation.

Figure 15. V_{AXG} / I_{AXG} Static and Ripple Voltage Regulation



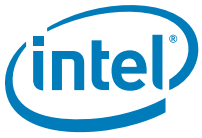


Table 48. DDR3 Signal Group DC Specifications

Symbol	Parameter	Alpha Group	Min	Typ	Max	Units	Notes[1]
V_{IL}	Input Low Voltage	(e,f)			0.43*V_{DDQ}	V	2,4
V_{IH}	Input High Voltage	(e,f)	0.57*V_{DDQ}			V	3
V_{OL}	Output Low Voltage	(c,d,e,f)		(V_{DDQ} / 2)* (R_{ON} / (R_{ON}+R_{VTT_TERM}))			6
V_{OH}	Output High Voltage	(c,d,e,f)		V_{DDQ} - ((V_{DDQ} / 2)* (R_{ON}/ (R_{ON}+R_{VTT_TERM}))		V	4,6
R_{ON}	DDR3 Clock Buffer On Resistance		21		31	Ω	5
R_{ON}	DDR3 Clock Buffer On Resistance		21		36	Ω	5
R_{ON}	DDR3 Command Buffer On Resistance		16		24	Ω	5
R_{ON}	DDR3 Command Buffer On Resistance		20		31	Ω	5
R_{ON}	DDR3 Control Buffer On Resistance		21		31	Ω	5
R_{ON}	DDR3 Control Buffer On Resistance		20		31	Ω	5
R_{ON}	DDR3 Data Buffer On Resistance		21		31	Ω	5
R_{ON}	DDR3 Data Buffer On Resistance		21		36	Ω	5
Data ODT	On-Die Termination for Data Signals	(d)	102 51		138 69	Ω	7
I_{LI}	Input Leakage Current				±500	µA	
SM_RCOMP0	COMP Resistance	(t)	99	100	101	Ω	8
SM_RCOMP1	COMP Resistance	(t)	24.7	24.9	25.1	Ω	8
SM_RCOMP2	COMP Resistance	(t)	128.7	130	131.3	Ω	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{DDQ}. However, input signal drivers must comply with the signal quality specifications.
5. This is the pull down driver resistance. Refer to processor *I/O Buffer Models* for I/V characteristics.
6. R_{VTT_TERM} is the termination on the DIMM and in not controlled by the Processor.
7. The minimum and maximum values for these signals are programmable by BIOS to one of the two sets.
8. COMP resistance must be provided on the system board with 1% resistors. COMP resistors are to V_{SS}.

Table 49. Control Sideband and TAP Signal Group DC Specifications

Symbol	Alpha Group	Parameter	Min	Typ	Max	Units	Notes[1,8]
V_{IL}	(m),(n),(p),(s)	Input Low Voltage			$0.64 * V_{TT}$	V	2,3
V_{IH}	(m),(n),(p),(s)	Input High Voltage	$0.76 * V_{TT}$			V	2,3,5
V_{IL}	(g)	Input Low Voltage			$0.25 * V_{TT}$	V	2,3
V_{IH}	(g)	Input High Voltage	$0.80 * V_{TT}$			V	2,3,5
V_{IL}	(ga)	Input Low Voltage			$0.4 * V_{TT}$	V	2,3
V_{IH}	(ga)	Input High Voltage	$0.75 * V_{TT}$			V	2,3,5
V_{IL}	(qa)	Input Low Voltage			$0.38 * V_{TT}$	V	2,3
V_{IH}	(qa)	Input High Voltage	$0.70 * V_{TT}$			V	2,3,5
V_{IL}	(ja),(qb)	Input Low Voltage			$0.25 * V_{TT}$	V	2,3
V_{IH}	(ja),(qb)	Input High Voltage	$0.75 * V_{TT}$			V	2,3,5
V_{IL}	(jb)	Input Low Voltage			0.29		2,3
V_{IH}	(jb)	Input High Voltage	0.87			V	2,3,5
V_{OL}	(k),(l),(n),(p),(r),(s),(ab),(h),(i)	Output Low Voltage			$V_{TT} * R_{ON} / (R_{ON} + R_{SYS\_TERM})$	V	2,7
V_{OH}	(k),(l),(n),(p),(r),(s),(ab),(i)	Output High Voltage	V_{TT}			V	2,5
R_{ON}	(k),(l),(n),(p),(r),(s),(i)	Buffer on Resistance	10		18	Ω	
R_{ON}	(ab)	Buffer on Resistance	20-30		27-45	Ω	
I_{LI}	(ja),(jb),(m),(n),(p),(qa),(s),(t),(aa),(g)	Input Leakage Current			±200	µA	4
I_{LI}	(qb)	Input Leakage Current			±150	µA	4
COMP0	(t)	COMP Resistance	49.4	49.9	50.4	Ω	6
COMP1	(t)	COMP Resistance	49.4	49.9	50.4	Ω	6
COMP2	(t)	COMP Resistance	19.8	20	20.2	Ω	6
COMP3	(t)	COMP Resistance	19.8	20	20.2	Ω	6

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
3. Refer to the processor *I/O Buffer Models* for I/V characteristics.
4. For V_{IN} between "0" V and V_{TT}. Measured when the driver is tristated.
5. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications.
6. COMP resistance must be provided on the system board with 1% resistors. COMP resistors are to V_{SS}.
7. R_{SYS_TERM} is the system termination on the signal.

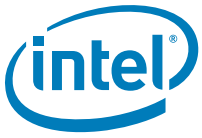


Table 50. PCI Express DC Specifications

Symbol	Alpha Group	Parameter	Min	Typ	Max	Units	Notes[1]
$V_{TX-DIFF-p-p}$	(ad)	Differential Peak-to-Peak Tx Voltage Swing	0.8		1.2	V	4
$V_{TX\_CM-AC-p}$	(ad)	Tx AC Peak Common Mode Output Voltage (Gen 1 Only)			20	mV	1,2,7
$Z_{TX-DIFF-DC}$	(ad)	DC Differential Tx Impedance (Gen 1 Only)	80		120	Ω	1,11
Z_{RX-DC}	(ac)	DC Common Mode Rx Impedance	40		60	Ω	1,9,10
$Z_{RX-DIFF-DC}$	(ac)	DC Differential Rx Impedance (Gen1 Only)	80		120	Ω	1
$V_{RX-DIFFp-p}$	(ac)	Differential Rx Input Peak-to-Peak Voltage (Gen 1 only)	0.175		1.2	V	1,3,12
$V_{RX\_CM-AC-p}$	(ac)	Rx AC Peak Common Mode Input Voltage			150	mV	1,8
PEG_ICOMPO	(ae)	Comp Resistance	49.5	50	50.5	Ω	5,6
PEG_ICOMPI	(ae)	Comp Resistance	49.5	50	50.5	Ω	5,6
PEG_RCOMPO	(ae)	Comp Resistance	49.5	50	50.5	Ω	5,6
PEG_RBIAS	(ae)	Comp Resistance	742.5	750	757.5	Ω	5,6

NOTES:
1. Refer to the *PCI Express Base Specification* for more details.
2. $V_{TX-AC-CM-PP}$ and $V_{TX-AC-CM-P}$ are defined in the *PCI Express Base Specification*. Measurement is made over at least 10^6 UI.
3. Refer to Figure 22, "PCI Express Receiver Eye Margins" on page 119.
4. As measured with compliance test load. Defined as $2*|V_{TXD+} - V_{TXD-}|$.
5. COMP resistance must be provided on the system board with 1% resistors. COMP resistors are to V_{SS}.
6. PEG_ICOMPO, PEG_ICOMPI, PEG_RCOMPO are the same resistor
7. RMS value.
8. Measured at Rx pins into a pair of 50-Ω terminations into ground. Common mode peak voltage is defined by the expression: max{|(Vd+ - Vd-) - V-CMDC|}.
9. DC impedance limits are needed to guarantee Receiver detect.
10. The Rx DC Common Mode Impedance must be present when the Receiver terminations are first enabled to ensure that the Receiver Detect occurs properly. Compensation of this impedance can start immediately and the 15 Rx Common Mode Impedance (constrained by RLRX-CM to 50 Ω ±20%) must be within the specified range by the time Detect is entered.
11. Low impedance defined during signaling. Parameter is captured for 5.0 GHz by RLTX-DIFF.

Table 51. eDP DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[4]
eDP_HPD#						
V_{IL}	Input Low Voltage	-0.3		0.3	V	
V_{IH}	Input High Voltage	0.6		1.155	V	
eDP_AUX, eDP_AUX#						
$V_{AUX-DIFFp-p}$ (Tx)	AUX Peak-to-Peak Voltage at the transmitting device	0.39		1.38		1
$V_{AUX-DIFFp-p}$ (Rx)	AUX Peak-to-Peak Voltage at the receiving device	0.32		1.36	V	1
eDP COMPs						
eDP_ICOMPO	Comp Resistance	49.5	50	50.5	Ω	2,3
eDP_ICOMPI	Comp Resistance	49.5	50	50.5	Ω	2,3
eDP_RCOMPO	Comp Resistance	49.5	50	50.5	Ω	2,3
eDP_RBIAS	Comp Resistance	742.5	750	757.5	Ω	2,3

NOTES:
1. $V_{AUX-DIFFp-p} = 2*|V_{AUXP} - V_{AUXM}|$. Please refer to the VESA DisplayPort Standard specification for more details.
2. COMP resistance must be provided on the system board with 1% resistors. See the applicable platform design guide for implementation details. COMP resistors are to V_{SS}.
3. eDP_ICOMPO, eDP_ICOMPI, eDP_RCOMPO are the same resistor.
4. These are pre-silicon estimates and are subject to change.

7.10.2 V_{CC} and V_{AXG} Validation

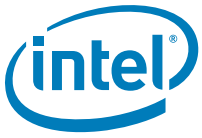
The following calculation for spec minimum V_{CC} voltage is applicable to both Arrandale rPGA and BGA platforms at $V_{CC\_SENSE}/V_{SS\_SENSE}$ with 20-MHz bandwidth limiting.

$$V\min = VID - I_{CCMAX} * Slope_{LL} - x\% * VID - ripple$$

VID under maximum load, x% set-point tolerance, and ripple have to be measured on the system under test. Use the spec loadline slope and I_{CCMAX} for the spec minimum voltage Vmin calculation. It might be difficult to reach spec max current in lab environment and please try different stresses on Vcc core rail. Then, compare the measured Vmin to the calculated spec Vmin to determine if system passes or fails.

The following calculation for spec minimum V_{AXG} voltage is applicable to both Calpella rPGA and BGA platforms at $V_{AXG\_SENSE}/V_{SSAXG\_SENSE}$ with 20-MHz bandwidth limiting.

$$V\min = VID - I_{CCMAX\_AXG} * Slope_{LLAXG} - x\% * VID$$



VID under maximum load, x% total tolerance, and ripple have to be measured on the system under test. Notice the tolerance on AXG rail combined set-point tolerance and ripple. Use the spec AXG loadline slope and I_{CCMAX_AXG} for the spec minimum voltage Vmin calculation. It might be difficult to reach spec max current in lab environment and please try different stresses on Vcc core rail. Then, compare the measured Vmin to the calculated spec Vmin to determine if system passes or fails.

The following step-by-step procedure is recommended for minimum V_{CC} and V_{AXG} validation. Step 1 to 5 is for the calculation of spec minimum voltage and step 6 is to collect actual minimum voltage on the system under test.

1. Measure the DC voltage at test points with V_{RTT} or Chroma load. Calculate set-point tolerance.
2. Land differential probes at the designated test points under CPU on the secondary layer.
3. Operating the CPU with maximum load on all threads. For example, try Prime95*, CPU2000*, 3D games, etc., on CPU V_{CC_CORE} rail. For V_{AXG}, try various 3D games and benchmarks.
4. Measure VID signals and find the corresponding voltage in EDS. The VID signals should be very stable with max load.

Measure ripple. 20-MHz bandwidth limiting or Low-pass filter function can be applied.Set manual trigger on the voltage waveform. Lower the trigger level slowly to capture the worst case Vmin with 20-MHz bandwidth limiting. Low-pass filtering function with 20-MHz cut-off frequency can be used for bandwidth limiting.

Table 52. eDP DC Specifications

Symbol	Parameter	Min	Typ	Max	Units	Notes[4]
eDP_HPD#						
V_{IL}	Input Low Voltage	-0.3		0.3	V	
V_{IH}	Input High Voltage	0.6		1.155	V	
eDP_AUX, eDP_AUX#						
$V_{AUX\text{-}DIFFp\text{-}p}$ (Tx)	AUX Peak-to-Peak Voltage at the transmitting device	0.39		1.38		1
$V_{AUX\text{-}DIFFp\text{-}p}$ (Rx)	AUX Peak-to-Peak Voltage at the receiving device	0.32		1.36	V	1
eDP COMPs						
eDP_ICOMPO	Comp Resistance	49.5	50	50.5	Ω	2,3
eDP_ICOMPI	Comp Resistance	49.5	50	50.5	Ω	2,3
eDP_RCOMPO	Comp Resistance	49.5	50	50.5	Ω	2,3
eDP_RBIAS	Comp Resistance	742.5	750	757.5	Ω	2,3

NOTES:

1. $V_{AUX\text{-}DIFFp\text{-}p} = 2*|V_{AUXP} - V_{AUXM}|$. Please refer to the VESA DisplayPort Standard specification for more details.
2. COMP resistance must be provided on the system board with 1% resistors. See the applicable platform design guide for implementation details. COMP resistors are to V_{SS}.
3. eDP_ICOMPO, eDP_ICOMPI, eDP_RCOMPO are the same resistor.
4. These are pre-silicon estimates and are subject to change.

7.10.3 Uncore Voltage Validation

AC tolerance is defined at power/ground pins where the voltage transient has to be within spec with 20-MHz bandwidth limiting. DC tolerance is defined at power/ground pins where the DC voltage error has to be within spec. The new tolerance spec for V_{TT} rail defined at $V_{TT\_SENSE}/V_{SS\_SENSE\_VTT}$ pins with 20-MHz bandwidth limiting has to be met along with the tolerance spec defined at power/ground pins.

The following procedure is recommended for DC tolerance validation.

1. Connect Chroma load
2. Start at 0 A
3. Measure DC voltage at test points with multimeter.
4. Increase load current by small step and re-measure DC voltage again till reach spec maximum current. Check if all voltage points are within DC tolerance spec.

The following procedure is recommended for AC tolerance validation.

1. Land differential probes at test points under CPU on the secondary layer.
2. Operate the CPU with maximum load on all threads. For example, try Prime95, CPU2000, 3D games, etc. For V_{DDQ}, try Mem stress and other DDR stresses
3. Measure the average voltage on scope with at least 2 µs/div
4. Set manual trigger on the voltage waveform.

- Lower the trigger level slowly to capture the worst case V_{MIN} with 20-MHz bandwidth limiting.
  - Check V_{MIN} against min voltage spec
  - Droop (undershoot) = V_{AVG}-V_{MIN} has to be within AC tolerance spec
- Raise the trigger level slowly to capture the worst case V_{MAX} with 20-MHz bandwidth limiting.
  - Check V_{MAX} against max voltage spec
  - Overshoot = V_{MAX}-V_{AVG} has to be within AC tolerance spec

7.11 Platform Environmental Control Interface (PECI) DC Specifications

PECI is an Intel proprietary interface that provides a communication channel between Intel processors and chipset components to external Adaptive Thermal Monitor devices. The processor contains a Digital Thermal Sensor (DTS) that reports a relative die temperature as an offset from Thermal Control Circuit (TCC) activation temperature. Temperature sensors located throughout the die are implemented as analog-to-digital converters calibrated at the factory. PECI provides an interface for external devices to read the DTS temperature for thermal management and fan speed control. More detailed information may be found in the *Platform Environment Control Interface (PECI) Specification*.

7.11.1 DC Characteristics

The PECI interface operates at a nominal voltage set by V_{TT}. The set of DC electrical specifications shown in Table 53 is used with devices normally operating from a V_{TT} interface supply. V_{TT} nominal levels will vary between processor families. All PECI devices will operate at the V_{TT} level determined by the processor installed in the system. For specific nominal V_{TT} levels, refer to Table 48.

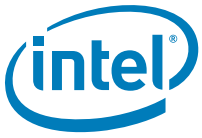


Table 53. PECI DC Electrical Limits

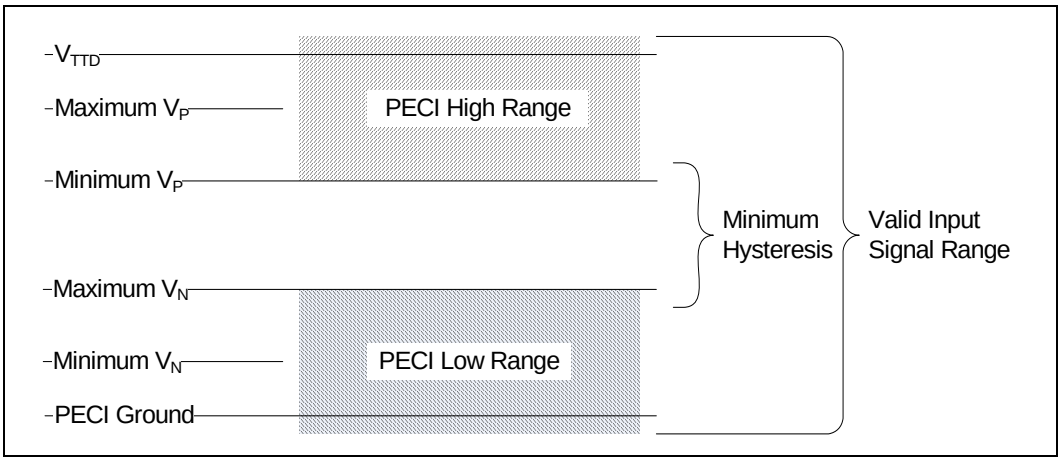
Symbol	Definition and Conditions	Min	Max	Units	Notes[1]
V_{in}	Input Voltage Range	-0.150	V_{TT}	V	
$V_{hysteresis}$	Hysteresis	0.1 * V_{TT}	N/A	V	
V_n	Negative-edge Threshold Voltage	0.275 * V_{TT}	0.500 * V_{TT}	V	
V_p	Positive-edge Threshold Voltage	0.550 * V_{TT}	0.725 * V_{TT}	V	
I_{source}	High-Level Output Source (V_{OH} = 0.75 * V_{TT})	-6.0	N/A	mA	
I_{sink}	Low-Level Output Sink (V_{OL} = 0.25 * V_{TT})	0.5	1.0	mA	
I_{leak+}	High-Impedance State Leakage to V_{TT} (V_{leak} = V_{OL})	N/A	100	µA	2
I_{leak-}	High-Impedance Leakage to GND (V_{leak} = V_{OH})	N/A	100	µA	2
C_{bus}	Bus Capacitance Per Node	N/A	10	pF	
V_{noise}	Signal Noise Immunity above 300 MHz	0.1 * V_{TT}	N/A	V_{p-p}	

NOTES:
1. V_{TT} supplies the PECI interface. PECI behavior does not affect V_{TT} min/max specifications.
2. The leakage specification applies to powered devices on the PECI bus.

7.11.2 Input Device Hysteresis

The input buffers in both client and host models must use a Schmitt-triggered input design for improved noise immunity. Use Figure 16 as a guide for input buffer design.

Figure 16. Input Device Hysteresis



7.12 AC Specifications

The processor timings specified in this section are defined at the processor pads. Therefore, proper simulation of the signals is the only means to verify proper timing and signal quality.

See Chapter 8 for the pin listing and Chapter 6 for signal definitions. Table 63 through Table 65 list the AC specifications associated with the processor.

The timings specified in this section should be used in conjunction with the processor signal integrity models provided by Intel.

Note: Care should be taken to read all notes associated with a particular timing parameter.

Table 54. Differential Clocks (SSC on)

SSC ON	1CLK	1 µs	0.1 s		0.1 s	1 µs	1CLK	
Signal Name	-Jitter c-c Abs PerMin	-SSC Short AvgMin	-ppm Long AvgMin	Ideal DC Target	+ppm Long AvgMax	+SSC Short AvgMax	+Jitter c-c Abs PerMax	Units
BCLK	7.349297	7.499297	7.518043	7.518797	7.519551	7.538399	7.688399	ns
PEG_CLK	9.849063	9.999063	10.02406	10.02506	10.02607	10.05120	10.20120	ns
DPLL_REF_SSCLK	7.982552	8.332552	8.353381	8.354219	8.355056	8.375999	8.725999	ns

NOTES:
1. Ideal DC Target: This serves only as an ideal reference target (0 ppm) to use for calculating the rest of the period measurement values
2. 0.1-second Measurement Window (frequency counter): Valuable measurement done using a frequency counter to determine near DC average frequency (filtering out all jitter including SSC and cycle to cycle). This is used to determine if the system has a frequency static offset caused usually by incorrect crystal, crystal loading or incorrect clock configuration.
3. 1.0-µs Measurement Window (scope): This measurement is only used in conjunction with clock post processing software (Jit3 Advanced for example) with "filters = LPF 3RD order 1-MHz pole" to filter out high frequency jitter (FM) and show the underlying SSC profile. The numbers here bound the SSC min/max excursions (SSC magnitude).
4. 1CLK - No Filter: Any 1 Period measured with a scope. Measured on a real time Oscilloscope using no filters, a simple period measurement (or a Jit3 period measurement - more accurate), provides absolute Min/Max timing information.

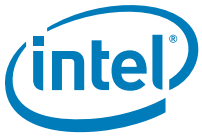


Table 55. Differential Clocks (SSC off)

SSC OFF	1CLK	0.1s		0.1s	1CLK	
Signal Name	-Jitter c-c AbsPerMin	-ppm LongAvgMin	Ideal DC target	+ppm LongAvgMax	+Jitter c-c AbsPerMax	Units
BCLK	7.34925	7.499250	7.500000	7.50075	7.650750	ns
PEG_CLK	9.849000	9.999000	10.00000	10.00100	10.15100	ns
DPLL_REF_SSCLK	7.98250	8.322500	8.333333	8.33417	8.684167	ns

NOTES:
1. Ideal DC Target: This serves only as an ideal reference target (0ppm) to use for calculating the rest of the period measurement values
2. 0.1-second Measurement Window (frequency counter): Valuable measurement done using a frequency counter to determine near DC average frequency (filtering out all jitter including SSC and cycle to cycle). This is used to determine if the system has a frequency static offset caused usually by incorrect crystal, crystal loading or incorrect clock configuration.
3. 1CLK - No Filter: Any 1 Period measured with a scope. Measured on a real time Oscilloscope using no filters, a simple period measurement (or a Jit3 period measurement - more accurate), provides absolute Min / Max timing information.

Table 56. Processor Clock Jitter Specifications (cycle-cycle)

Symbol	Frequency (MHz)	Type	Source (ps)	Destination	Notes
$BCLK_{JIT\_CC}$	133	Input Diff	150	processor/memory/graphics	1
$PEG\_CLK_{JIT\_CC}$	100	Input Diff	150	PCI Express*/DMI/Intel® FDI	1
$DPLL\_REF\_SSCLK_{JIT\_CC}$	120	Input Diff	350	eDP	1

NOTES:
1. On all jitter measurements care should be taken to set the zero crossing voltage (for rising edge) of the clock to be the point where the edge rate is the fastest. Using a Math function = Average(Derivative(Ch1)) and set the averages to 64, place the cursors where the slope is the highest on the rising edge - usually the lower half of the rising edge. This is defined because Flip Chip components prevent probing at the end of the transmission line. This will result in a reflection induced ledge in the middle of the rising edge and will significantly increase measured jitter.

Table 57. Intel 5 Series Chipset Clock Jitter Specifications (cycle-cycle)

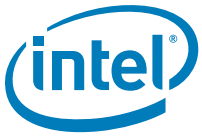
Symbol	Frequency (MHz)	Type	Source (ps)	Destination	Notes
$BCLK_{JIT\_CC}$	133	Input Diff	150	processor/memory/graphics	1,2
$PEG\_CLK_{JIT\_CC}$	100	Input Diff	150	PCI Express*/DMI/Intel® FDI	1,2
$DPLL\_REF\_SSCLK_{JIT\_CC}$	120	Input Diff	350	eDP	1,2

NOTES:
1. On all jitter measurements care should be taken to set the zero crossing voltage (for rising edge) of the clock to be the point where the edge rate is the fastest. Using a Math function = Average (Derivative(Ch1)) and set the averages to 64, place the cursors where the slope is the highest on the rising edge - usually the lower half of the rising edge. This is defined because Flip Chip components prevent probing at the end of the transmission line. This will result in a reflection induced ledge in the middle of the rising edge and will significantly increase measured jitter.
2. The values in these table are sourced from the CK505 Platform clock synthesizer; they have been derrated slightly to account for in system noise etc. (duty cycle and cycle-cycle jitter). See the CK505 clock specification for additional information on these specific clocks.

Table 58. System Reference Clock DC and AC Specifications

Symbol	Parameter	Signal	Min	Max	Unit	Meas	Figure	Notes
Slew_rise	Rising Slew Rate	Diff	1.5	4.0	V/ns	Avg	Figure 17	2,3
Slew_fall	Falling Slew Rate	Diff	1.5	4.0	V/ns	Avg	Figure 17	2,3
Slew_var	Slew Rate Matching	Single Ended		20	%	Avg	Figure 18	1,9
V_{SWING}	Differential Output Swing	Diff	300		mV	RT	Figure 17	2
V_{CROSS}	Crossing Point Voltage	Single Ended	300	550	mV	RT	Figure 18	1,4,5
V_{CROSS_DELTA}	Variation of V_{CROSS}	Single Ended		140	mV	RT	Figure 18	1,4,8
V_{MAX}	Max Output Voltage	Single Ended		1.15	V	RT	Figure 18	1,6
V_{MIN}	Min Output Voltage	Single Ended	-0.3		V	RT	Figure 18	1,7
DTY_CYC	Duty Cycle	Diff	40	60	%	Avg	Figure 17	2

NOTES:
1. Measurement taken from single-ended waveform on a component test board.
2. Measurement taken from differential waveform on a component test board.
3. Slew rate measured through V_{SWING} voltage range centered about differential zero.
4. V_{CROSS} is defined as the voltage where Clock = Clock#.
5. Only applies to the differential rising edge (i.e., Clock rising and Clock# falling).
6. The max voltage including overshoot.
7. The min voltage including undershoot.
8. The total variation of all V_{CROSS} measurements in any particular system. Note that this is a subset of $V_{CROSS\_MIN/MAX}$ (V_{CROSS} absolute) allowed. The intent is to limit V_{CROSS} induced modulation by setting V_{CROSS_DELTA} to be smaller than V_{CROSS} absolute.
9. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75 mV window centered on the average cross point where Clock rising meets Clock# falling (See Figure 17, "Differential Clock – Differential Measurements" on page 117). The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.



7.12.1 DDR3 AC Specifications

The following notes apply to Table 59, Table 60.

Note	Definition
1	Unless otherwise noted, all specifications in this table apply to all processor frequencies. Timing specifications only depend on the operating frequency of the memory channel and not the maximum rated frequency.
2	When the single ended slew rate of the input Data or Strobe signals, within a byte group, are below 1.0 V/ns, the T_{SU} and T_{HD} specifications must be increased by a derrating factor. The input single ended slew rate is measured DC to AC levels; V_{IL_DC} to V_{IH_AC} for rising edges, and V_{IH_DC} to V_{IL_AC} for falling edges. Use the worse case minimum slew rate measured between Data and Strobe, within a byte group, to determine the required derrating value. No derrating is required for single ended slew rates equal to or greater than 1.0 V/ns.
3	Edge Placement Accuracy (EPA): The silicon contains digital logic that automatically adjusts the timing relationship between the DDR reference clocks and DDR signals. The BIOS initiates a training procedure that will place a given signal appropriately within the clock period. The difference in delay between the signal and clock is accurate to within ±EPA. This EPA includes jitter, skew, within die variation and several other effects.
4	Data to Strobe read setup and Data from Strobe read hold minimum requirements specified at the processor pad are determined with the minimum Read DQS/DQS# delay.
5	C_{WL} (CAS Write Latency) is the delay, in clock cycles, between the rising edge of CK where a write command is referenced and the first rising strobe edge where the first byte of write data is present. The C_{WL} value is determined by the value of the CL (CAS Latency) setting.
6	The system memory clock outputs are differential (CLK and CLK#), the CLK rising edge is referenced at the crossing point where CLK is rising and CLK# is falling.
7	The system memory strobe outputs are differential (DQS and DQS#), the DQS rising edge is referenced at the crossing point where DQS is rising and DQS# is falling, and the DQS falling edge is referenced at the crossing point where DQS is falling and DQS# is rising.
8	This value specifies the parameter after write levelling, representing the residual error in the controller after training, and does not include any effects from the DRAM itself.

Table 59. DDR3 Electrical Characteristics and AC Timings at 800 MT/s, V_{DDQ} = 1.5 V ±0.075 V

Symbol	Parameter	Channel A Channel B		Unit	Figure	Note[1,9]
		Max	Min			
System Memory Latency Timings						
T_{CL} – T_{RCD} – T_{RP}	CAS Latency – RAS to CAS Delay – Pre-charge Command Period	6 – 6 – 6		T_{CK}		
Electrical Characteristics						
T_{SLR_D}	DQ[63:0], DQS[7:0], DQS#[7:0] Input Slew Rate	4.0	1.0	V/ns		2
System Memory Clock Timings						
T_{CK}	CK Period	2.50		ns		
T_{CH}	CK High Time		1.17	ns		
T_{CL}	CK Low Time		1.17	ns		
T_{SKEW}	Skew Between Any System Memory Differential Clock Pair (CK/CKB)		+155	ps		
System Memory Command Signal Timings						
T_{CMD_CO}	RAS#, CAS#, WE#, MA[14:0], BA[2:0] Edge Placement Accuracy	+375	-375	ps	Figure 19	3,4,6
System Memory Control Signal Timings						
T_{CTRL_CO}	CS#[1:0], CKE[1:0], ODT[1:0] Edge Placement Accuracy	+375	-375	ps	Figure 19	3,6
System Memory Data and Strobe Signal Timings						
T_{DVB}+T_{DVA}	DQ[63:0] Valid before DQS[7:0] Rising or Falling Edge		0.67*UI	UI		7
T_{Su+HD}	DQ Input Setup plus Hold Time to DQS Rising or Falling Edge		0.25*UI	ns	Figure 20	1,2,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge **BEFORE** write levelling	+375	-375	ns	Figure 21	3,6,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge **AFTER** write levelling	+275	-275	ns	Figure 21	8
T_{WPRE}	DQS/DQS# Write Preamble Duration		2.750	ns		
T_{WPST}	DQS/DQS# Write Postamble Duration	1.375	1.125	ns		
T_{DQSS}	CK Rising Edge Output Access Time, Where a Write Command Is Referenced, to the First DQS Rising Edge	C_{WL} x (T_{CK} + 4)		ns		5,6

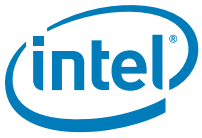


Table 60. DDR3 Electrical Characteristics and AC Timings at 1066 MT/s, V_{DDQ} = 1.5 V ±0.075 V

Symbol	Parameter	Channel A Channel B		Unit	Figure	Note[1,9]
		Max	Min			
System Memory Latency Timings						
T_{CL} – T_{RCD} – T_{RP}	CAS Latency – RAS to CAS Delay – Pre-charge Command Period	7 – 7– 7 8– 8– 8		T_{CK}		
Electrical Characteristics						
T_{SLR_D}	DQ[63:0], DQS[7:0], DQS#[7:0] Input Slew Rate	4.0	1.0	V/ns		2
System Memory Clock Timings						
T_{CK}	CK Period	1.875		ns		
T_{CH}	CK High Time		0.88	ns		
T_{CL}	CK Low Time		0.88	ns		
T_{SKEW}	Skew Between Any System Memory Differential Clock Pair (CK/CKB)		+155	ps		
System Memory Command Signal Timings						
T_{CMD_CO}	RAS#, CAS#, WE#, MA[14:0], BA[2:0] Edge Placement Accuracy	+300	-300	ps	Figure 19	3,4,6
System Memory Control Signal Timings						
T_{CTRL_CO}	CS#[1:0], CKE[1:0], ODT[1:0] Edge Placement Accuracy	+300	-300	ps	Figure 19	3,6
System Memory Data and Strobe Signal Timings						
T_{DVB}+T_{DVA}	DQ[63:0] Valid before DQS[7:0] Rising or Falling Edge		0.67*UI	UI		7
T_{Su+HD}	DQ Input Setup plus Hold Time to DQS Rising or Falling Edge		0.25*UI	ns	Figure 20	1,2,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge **BEFORE** write levelling	+300	-300	ns	Figure 21	3,6,7
T_{DQS_CO}	DQS Edge Placement Accuracy to CK Rising Edge **AFTER** write levelling	+206	-206	ns	Figure 21	8
T_{WPRE}	DQS/DQS# Write Preamble Duration		2.063	ns		
T_{WPST}	DQS/DQS# Write Postamble Duration	1.031	0.844	ns		
T_{DQSS}	CK Rising Edge Output Access Time, Where a Write Command Is Referenced, to the First DQS Rising Edge	C_{WL} x (T_{CK} + 4)		ns		5,6

Table 61. PCI Express AC Specification

Symbol	Parameter	Min	Max	Units	Figure	Notes[1]
UI	Unit Interval (Gen 1)	399.88	400.12	ps		3,4 for Tx, 5 for Rx
T_{TX-EYE}	Minimum Transmission Eye Width	0.75		UI		6,7,8,9,10
$T_{TX-RISE/FALL}$	D+/D- TX Out put Rise/Fall time (Gen 1)	0.125		UI		7,11
T_{RX-EYE}	Minimum Receiver Eye Width (Gen 1)	0.4		UI	Figure 22	12,14

1. Refer to the *PCI Express Base Specification* for more details.
2. Max Rx inherent total timing error for common Refclk Rx architecture.
3. The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.
4. SSC permits a +0, - 5000 ppm modulation of the clock frequency at a modulation rate not to exceed 33 kHz.
5. UI does not account for SSC caused variations.
6. Does not include SSC or Refclk jitter. Includes Rj at 10^{-12}
7. Measurements made at 2.5 GT/s require a scope with at least 6.2 GHz bandwidth. 2.5 GT/s may be measured within 200 mils of Tx device's pins, although deconvolution is recommended. For measurement setup details, refer to the *PCI Express Base Specification*. At least 10^{6} UI of data must be acquired.
8. Transmitter jitter is measured by driving the Transmitter under test with a low jitter "ideal" clock and connecting the DUT to a reference load.
9. Transmitter raw jitter data must be convolved with a filtering function that represents the worst case CDR tracking BW. 2.5 GT/s use different filter functions that are defined in the PCI Express Base Specification. After the convolution process has been applied, the center of the resulting eye must be determined and used as a reference point for obtaining eye voltage and margins.
10. For 5.0 GT/s, de-emphasis timing jitter must be removed. An additional HPF function must be applied as shown in the *PCI Express Base Specification*. This parameter is measured by accumulating a record length of 10^6 UI while the DUT outputs a compliance pattern. TMIN-PULSE is defined to be nominally 1 UI wide and is bordered on both sides by pulses of the opposite polarity. Refer to the *PCI Express Base Specification* for more details.
11. Measured differentially from 20% to 80% of swing.
12. Receiver eye margins are defined into a 2 x 50 Ω reference load. A Receiver is characterized by driving it with a signal whose characteristics are defined by the parameters specified in the *PCI Express Base Specification*.
13. The four inherent timing error parameters are defined for the convenience of Rx designers, and they are measured during Receiver tolerancing.
14. Minimum eye time at Rx pins to yield a 10^{-12} BER.

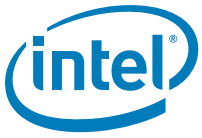


Table 62. eDP AC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
UI_{HR}	Unit Interval for High Bit Rate (2.7 Gbps/ lane)		370		pS	3
UI_{LR}	Unit Interval for Reduced Bit Rate (1.62 Gbps/lane)		617		pS	3
Down_Spread_ Amplitude	Link clock down spreading	0		0.5	%	
Down_Spread_ Frequency	Link clock down-spreading frequency	30		33	kHz	
$V_{TX-DIFFp-p-level1}$	Differential Peak-to-peak Output Voltage Level 1	0.34	0.40	0.46	V	2
$V_{TX-DIFFp-p-level2}$	Differential Peak-to-peak Output Voltage Level 2	0.51	0.60	0.68	V	2
Pre-emphasis 0dB	No Pre-emphasis	0	0	0	dB	2
Pre-emphasis 3.5dB	3.5 dB Pre-emphasis Level	2.8	3.5	4.2	dB	2
$L_{TX-SKEW-INTER\_PAIR}$	Lane-to-Lane Output Skew at Tx package pins			2	UI	
TJ_{HBR}	Total Jitter at Tx package pins. High-Bit Rate (2.7 Gbps/lane)			0.294	UI	
TJ_{RBR}	Total Jitter at Tx package pins. Reduced-Bit Rate (1.62 Gbps/lane)			0.180	UI	

NOTES:
1. All values are measured at the processor package pin level.
2. For embedded connection, support of level 2 pre-emphasis and V_{SWING} is optional.
3. Range is nominal +300 to -5300 ppm.

7.12.2 Miscellaneous AC Specifications

Table 63. Miscellaneous AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1,2,3
T1: Asynchronous GTL input pulse width	8	-	BCLKs	24	
T4: PROCHOT# pulse width	500	-	µs	24	
T5: THERMTRIP# assertion until V_{CC} removed	-	500	ms	25	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. All AC timing for the Asynchronous GTL signals are referenced to the BCLK rising edge at Crossing Voltage (V_{CROSS}). $V_{CCPWRGOOD\_0}$, $V_{CCPWRGOOD\_1}$, $V_{TTPWRGOOD}$, and SM_DRAMPWROK are referenced to the BCLK rising edge at 0.5 * V_{TT}.
3. These signals may be driven asynchronously.

7.12.3 TAP Signal Group AC Specifications

Table 64. TAP Signal Group AC Specifications

T# Parameter	Min	Max	Unit	Figure	Notes 1, 2,3
T14: TCK Period	31.25		ns		
T15: TDI, TMS Setup Time	8		ns	23	
T16: TDI, TMS Hold Time	5		ns	23	
T17: TDO Clock to Output Delay	0.5	7	ns	23	
T18: TRST# Assert Time	2		T_{TCK}	24	

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Not 100% tested. Specified by design characterization.
3. It is recommended that TMS be asserted while TRST# is being deasserted.

7.12.4 VID Signal Group AC Specifications

Table 65. VID Signal Group AC Specifications

T # Parameter	Min	Max	Unit	Figure	Notes[1, 2]
T19: VID Step Time	2.5	-	µs	27	
T20: VID Down Transition to Valid V_{CC} (min)	-	0	µs	26, 27	
T21: VID Up Transition to Valid V_{CC} (min)	-	15	µs	26, 27	
T22: VID Down Transition to Valid V_{CC} (max)	-	15	µs	26, 27	
T23: VID Up Transition to Valid V_{CC} (max)	-	0	µs	26, 27	

NOTES:
1. See the voltage regulator design guidelines for additional information.
2. Platform support for VID transitions is required for the processor to operate within specifications.

7.13 Processor AC Timing Waveforms

The following figures are used in conjunction with the AC timing tables, Table 63 through Table 65.

Note: For Figure 17 through Figure 27, the following apply:

1. All common clock AC timings signals are referenced to the Crossing Voltage (V_{CROSS}) of the BCLK, BCLK# at rising edge of BCLK.
2. All source synchronous AC timings are referenced to their associated strobe (address or data). Source synchronous data signals are referenced to the falling edge of their associated data strobe. Source synchronous address signals are referenced to the rising and falling edge of their associated address strobe.
3. All AC timings for the TAP signals are referenced to the TCK at 0.5 * V_{TT} at the processor lands. All TAP signal timings (TMS, TDI, etc.) are referenced at 0.5 * V_{TT} at the processor die (pads).
4. All CMOS signal timings are referenced at 0.5 * V_{TT} at the processor pins.

Figure 17. Differential Clock – Differential Measurements

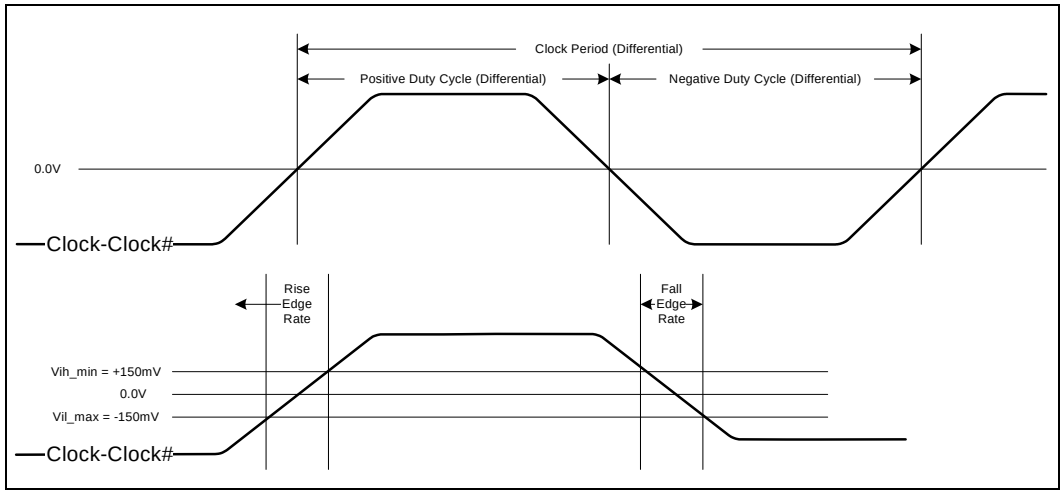


Figure 18. Differential Clock – Single Ended Measurements

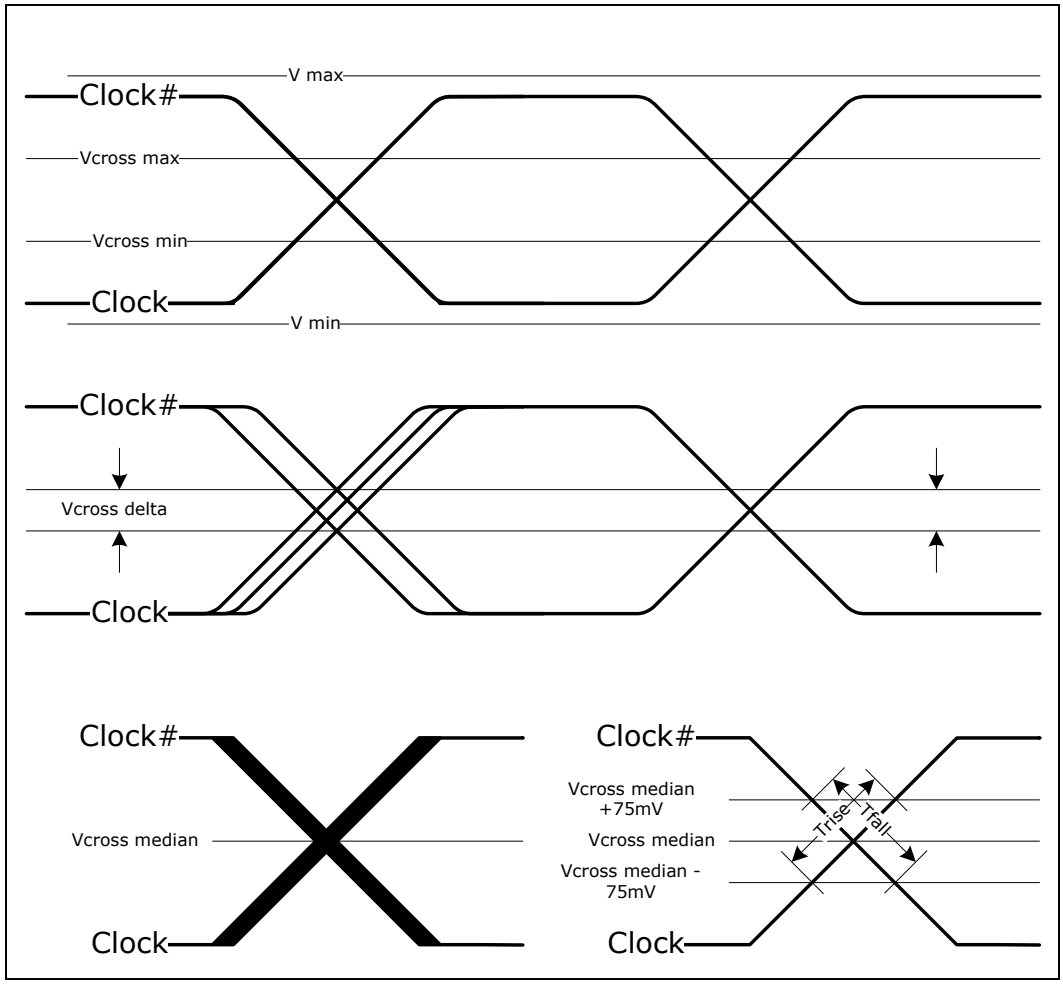


Figure 19. DDR3 Command / Control and Clock Timing Waveform

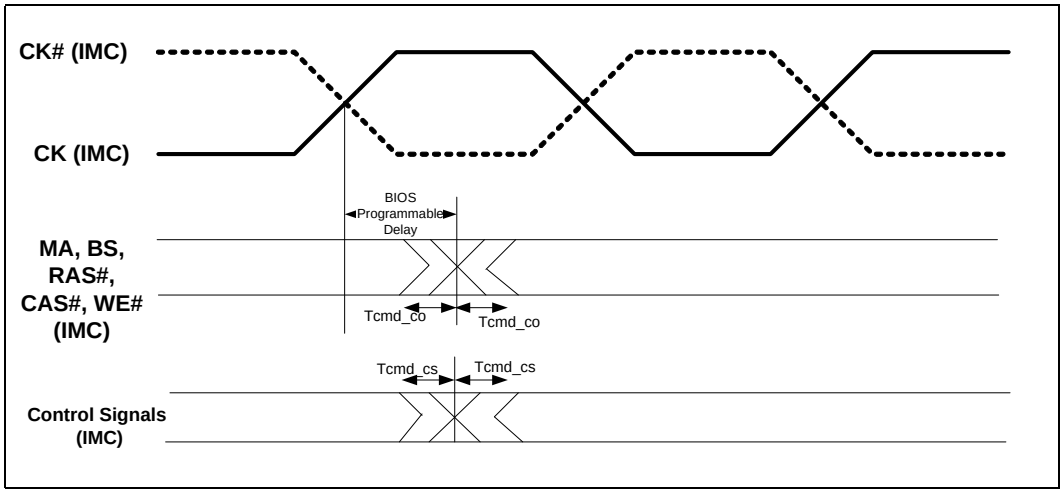


Figure 20. DDR3 Receiver Eye Mask

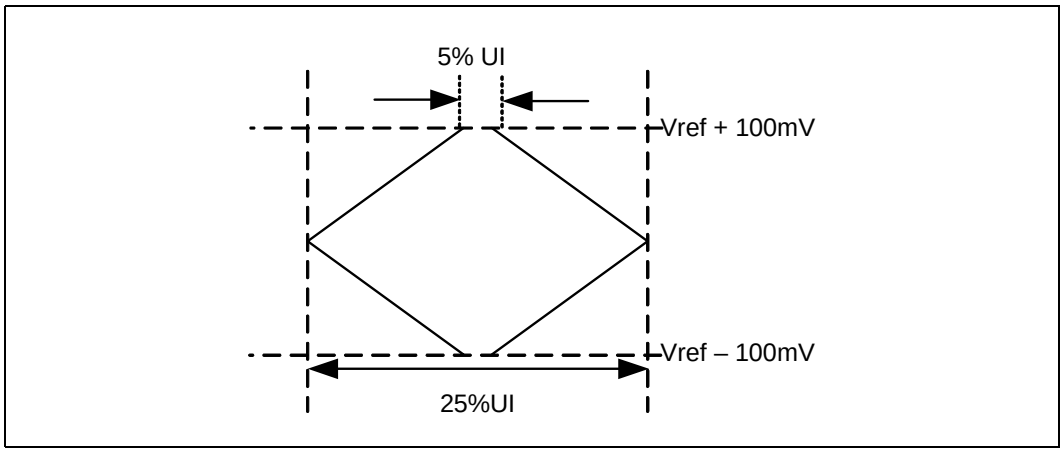


Figure 21. DDR3 Clock to DQS Skew Timing Waveform

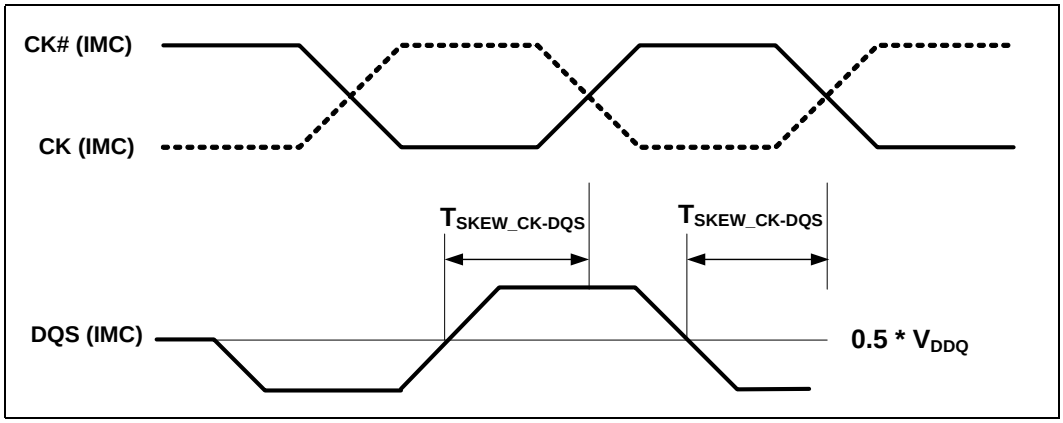


Figure 22. PCI Express Receiver Eye Margins

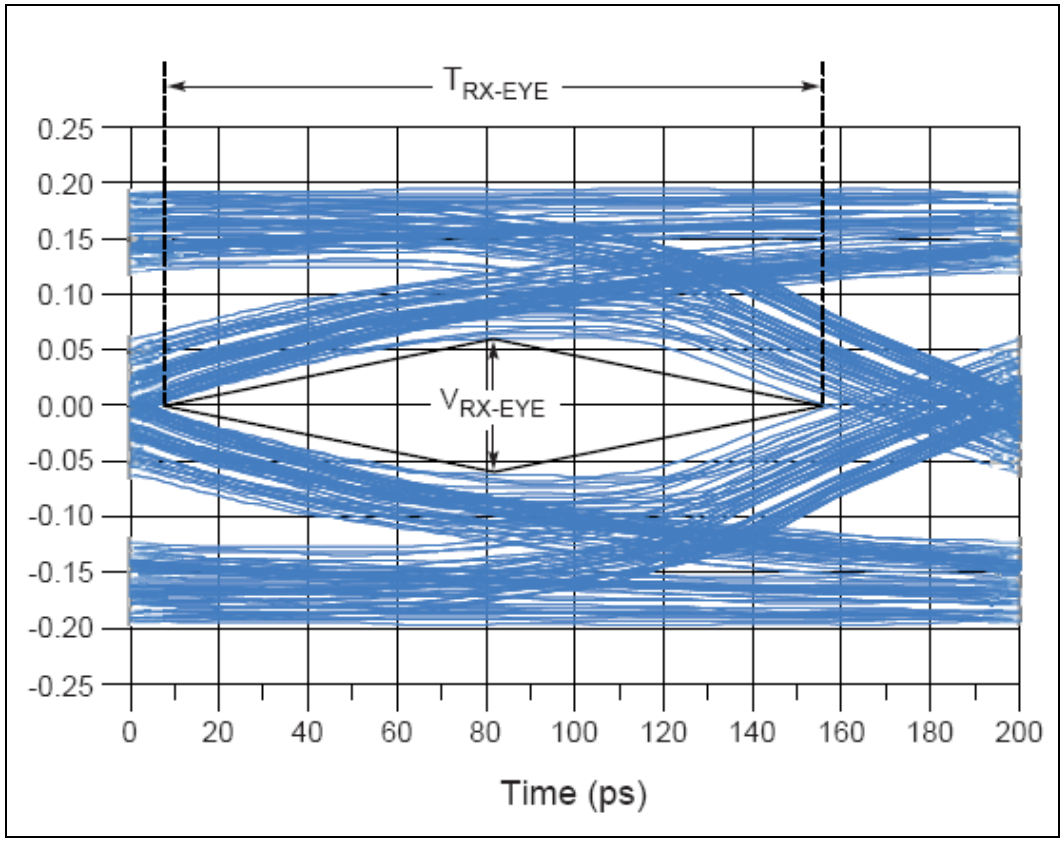
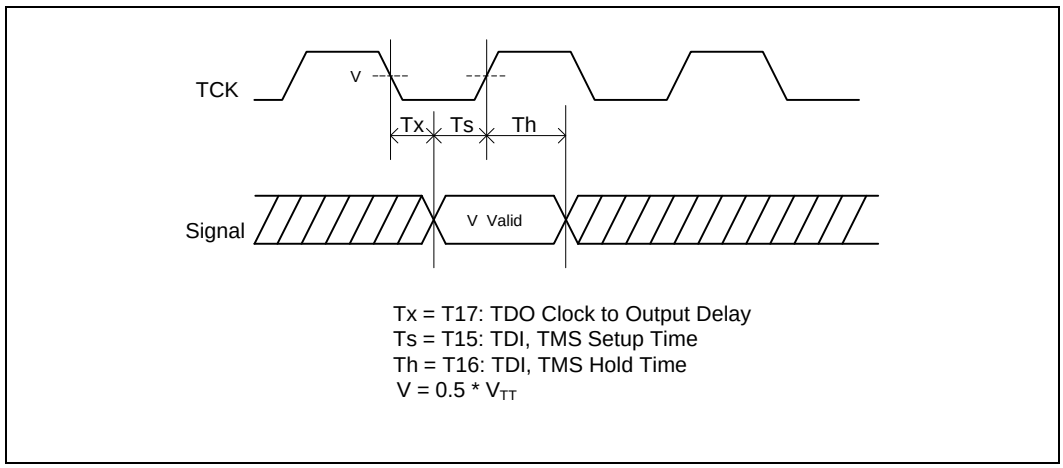


Figure 23. TAP Valid Delay Timing Waveform



NOTE: Refer to Table 49 for TAP Signal Group DC specifications and Table 64 for TAP Signal Group AC specifications.

Figure 24. Test Reset (TRST#), Async GTL Input, and PROCHOT# Timing Waveform

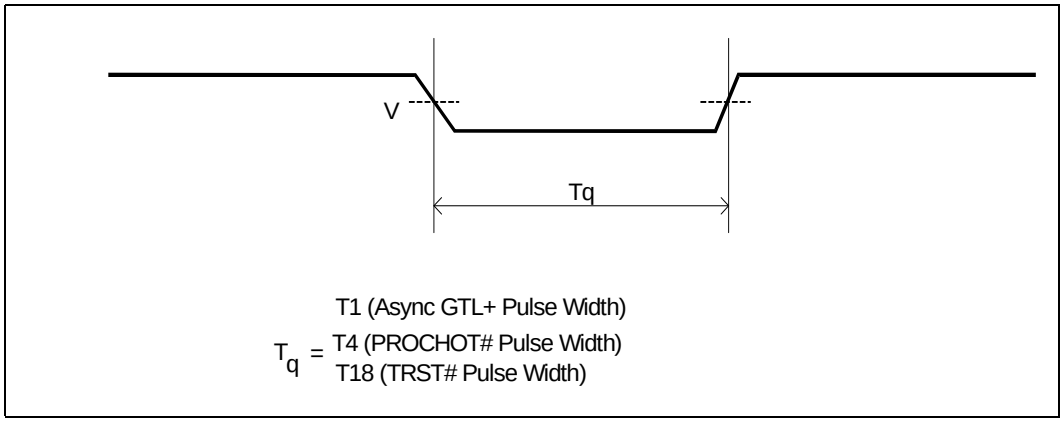


Figure 25. THERMTRIP# Power Down Sequence

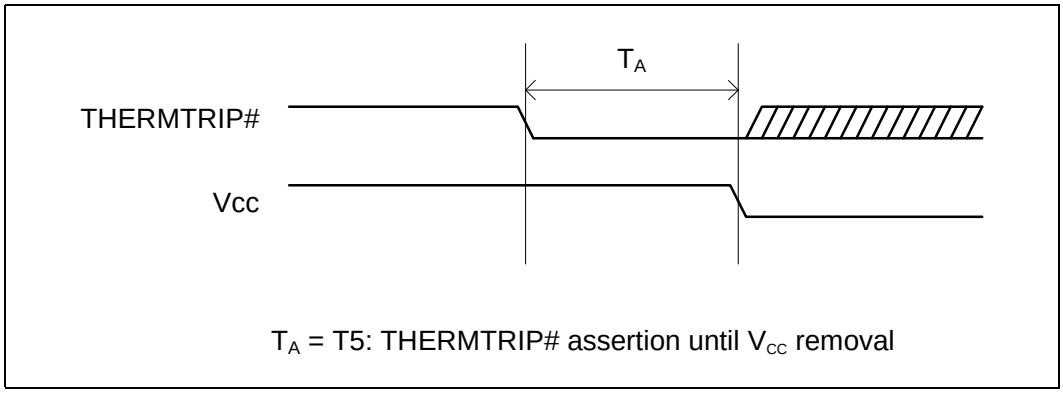
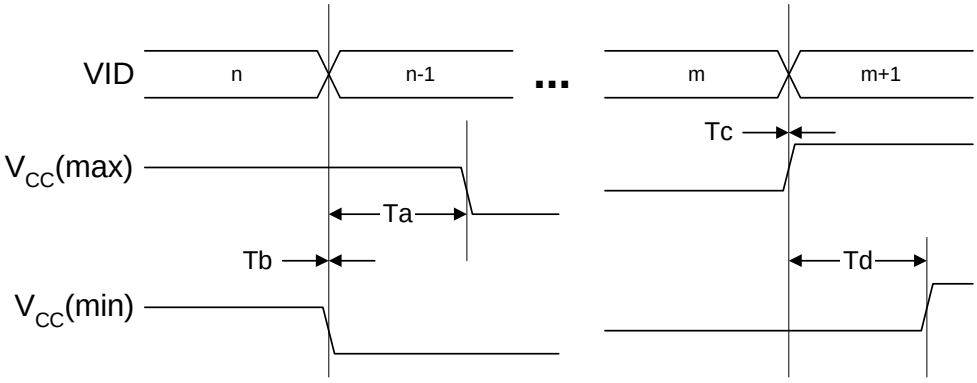
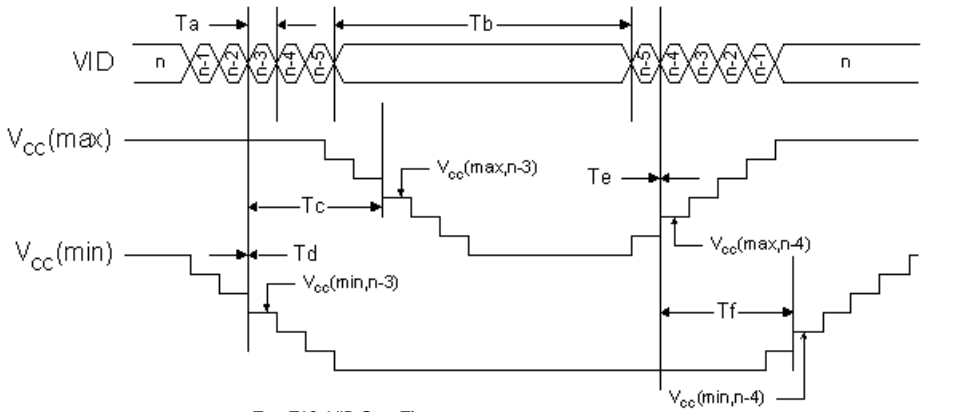


Figure 26. VID Step Timings



T_A = T22: VID Down Transition to Valid Vcc (max)
T_B = T20: VID Down Transition to Valid Vcc (min)
T_C = T23: VID Up Transition to Valid Vcc (max)
T_D = T21: VID Up Transition to Valid Vcc (min)

Figure 27. VID Step Times and V_{CC} Waveforms



T_a = T19: VID Step Time
T_c = T22: VID Down Transition to Valid Vcc (max)
T_d = T20: VID Down Transition to Valid Vcc (min)
T_e = T23: VID Up Transition to Valid Vcc (max)
T_f = T21: VID Up Transition to Valid Vcc (min)

7.14 Signal Quality

Data transfer requires the clean reception of data signals and clock signals. Ringing below receiver thresholds, non-monotonic signal edges, and excessive voltage swings will adversely affect system timings. Ringback and signal non-monotonicity cannot be tolerated since these phenomena may inadvertently advance receiver state machines. Excessive signal swings (overshoot and undershoot) are detrimental to silicon gate oxide integrity, and can cause device failure if absolute voltage limits are exceeded. Overshoot and undershoot can also cause timing degradation due to the build up of inter-symbol interference (ISI) effects.

For these reasons, it is crucial that the designer work towards a solution that provides acceptable signal quality across all systematic variations encountered in volume manufacturing.

This section documents signal quality metrics used to derive topology and routing guidelines through simulation. All specifications are specified at the processor die (pad measurements).

Specifications for signal quality are for measurements at the processor core only and are only observable through simulation. Therefore, proper simulation is the only way to verify proper timing and signal quality.

7.14.1 Input Reference Clock Signal Quality Specifications

Overshoot/Undershoot and Ringback specifications for BCLK/BCLK# are found in Table 67. Overshoot/Undershoot and Ringback specifications for the DDR3 Reference Clocks are specified by the DIMM.

7.14.2 DDR3 Signal Quality Specifications

Signal Quality specifications for Differential DDR3 Signals are included as part of the DDR3 DC specifications and DDR3 AC specifications. Various scenarios have been simulated to generate a set of layout guidelines which are available in the Platform Design Guide.

7.14.3 I/O Signal Quality Specifications

Signal Quality specifications for PC I Signals are included as part of the PCIDC specifications and PCIe AC specifications. Various scenarios have been simulated to generate a set of layout guidelines which are available in the Platform Design Guide.

7.15 Overshoot/Undershoot Guidelines

Overshoot (or undershoot) is the absolute value of the maximum voltage above or below V_{SS}. The overshoot/undershoot specifications limit transitions beyond V_{CCIO} or V_{SS} due to the fast signal edge rates. The processor can be damaged by single and/or repeated overshoot or undershoot events on any input, output, or I/O buffer if the charge is large enough (i.e., if the over/undershoot is great enough). Baseboard designs which meet signal integrity and timing requirements and which do not exceed the maximum overshoot or undershoot limits listed in Table 66 will insure reliable IO performance for the lifetime of the processor.

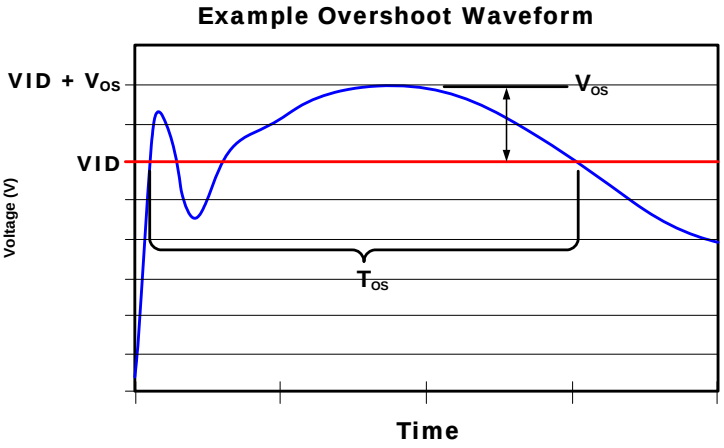
7.15.1 V_{CC} Overshoot Specification

When transitioning from a high-to-low current load condition, the processor can tolerate short transient overshoot events where V_{CC} exceeds the HFM_VID voltage. This overshoot cannot exceed VID + V_{OS_MAX}. V_{OS_MAX} is the maximum allowable overshoot above VID. These specifications apply to the processor die voltage as measured across the V_{CC_SENSE} and V_{SS_SENSE} lands.

Table 66. V_{CC} and V_{AXG} Overshoot Specifications

Symbol	Parameter	Min	Max	Units	Figure	Notes
V_{OS_MAX}	Magnitude of V_{CC} overshoot above VID	-	50	mV	28	
$T_{VCC\_OS\_MAX}$	Time duration of V_{CC} overshoot above VID	-	10	µs	28	
$T_{VAXG\_OS\_MAX}$	Time duration of V_{AXG} overshoot above VID	-	10	µs	28	

Figure 28. V_{CC} Overshoot Example Waveform



Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/ undershoot pulse duration.

7.15.2 Overshoot / Undershoot Magnitude

Magnitude describes the maximum potential difference between a signal and its voltage reference level. For the processor, both are referenced to V_{SS}. It is important to note that the overshoot and undershoot conditions are separate and their impact must be determined independently.

The pulse magnitude and duration must be used to determine if the overshoot/ undershoot pulse is within specifications.

7.15.3 Overshoot/Undershoot Pulse Duration

Pulse duration describes the total amount of time that an overshoot/undershoot event exceeds the overshoot/undershoot reference voltage. The total time could encompass several oscillations above the reference voltage. Multiple overshoot/undershoot pulses within a single overshoot/undershoot event may need to be measured to determine the total pulse duration.

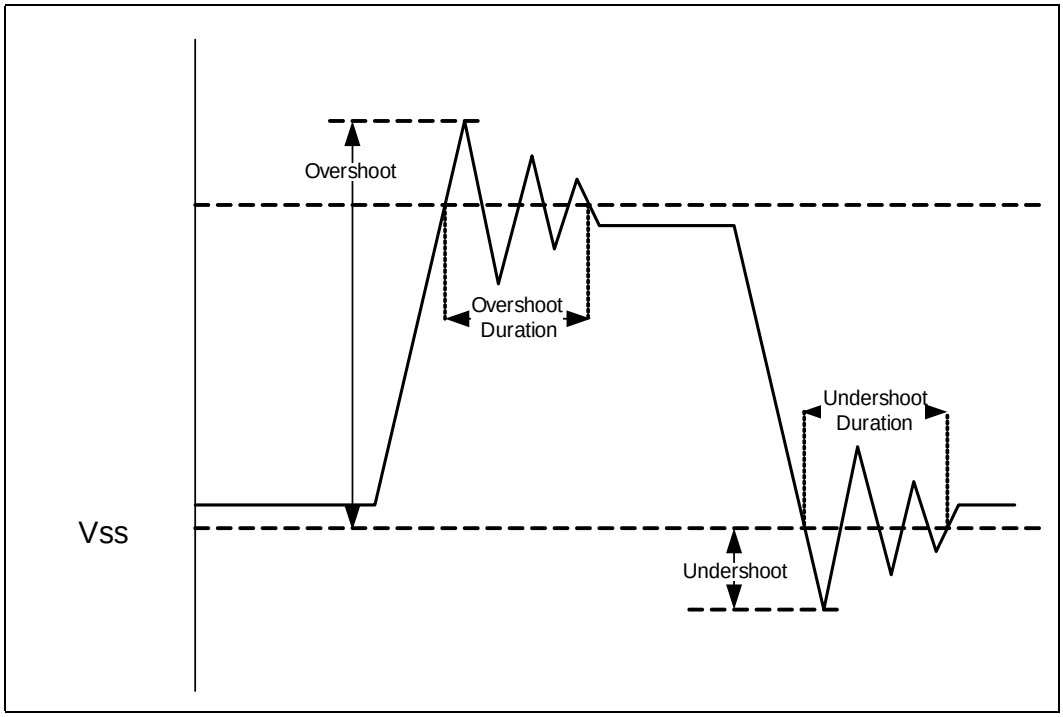
Note: Oscillations below the reference voltage cannot be subtracted from the total overshoot/undershoot pulse duration.

Table 67. Processor Overshoot/Undershoot Specifications

Signal Group	Maximum Overshoot	Overshoot Duration	Minimum Undershoot	Undershoot Duration	Notes
DDR3	1.2 * V_{DDQ}	0.5 * T_{CH}	-0.2 * V_{DDQ}	0.5 * T_{CH}	1,2
Control Sideband, Graphics and TAP Signals groups	1.2 * V_{TT}	50 ns	-0.2 * V_{TT}	50 ns	1,2
PCIe and eDP	1.2 * V_{TT}	0.25 UI	-0.2 * V_{TT}	0.25 UI	

NOTES:
1. These specifications are measured at the processor pin.
2. Refer to Figure 29 for description of allowable Overshoot/Undershoot magnitude and duration.

Figure 29. Maximum Acceptable Overshoot/Undershoot Waveform



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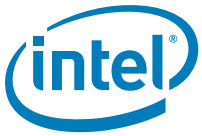

8 Processor Pin and Signal Information

8.1 Processor Pin Assignments

- provides a listing of all processor pins ordered alphabetically by pin name for the rPGA988A and BGA1288 package respectively.
- Table 69 and Table 71 provides a listing of all processor pins ordered alphabetically by pin number for the rPGA988A and BGA1288 package respectively.
- Figure 30, Figure 31, Figure 32, Figure 33 show the Top-Down view of the rPGA988A pinmap.
- Figure 34, Figure 35, Figure 36, Figure 37 show the Top-Down view of the BGA1288 ballmap.

Figure 30. Socket-G (rPGA988A) Pinmap (Top View, Upper-Left Quadrant)

	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
AT	VSS_NCTF	RSVD_NCTF	RSVD_NCTF	RSVD	RSVD	BCLK_ITP#	TDI	PRDY#	TRST#	COMP0	GFX_DPRSLPVR	COMP2	COMP3	VSSAXG_SENSE	VAXG	VSS	VAXG	VAXG
AR	RSVD_NCTF	VSS_NCTF	RSVD	RSVD	VSS	BCLK_ITP	TDI_M	VSS	TDO	VSS	GFX_VR_EN	VSS	VSS	VAXG_SENSE	VAXG	VSS	VAXG	VAXG
AP	RSVD_NCTF	VSS	RSVD	RSVD	CFG[2]	RSVD	TDO_M	TMS	PREQ#	RESET_OBS#	RSVD	GFX_VID[5]	GFX_VID[3]	GFX_VID[1]	VAXG	VSS	VAXG	VAXG
AN	ISENSE	VSS	PSI#	CFG[13]	VSS	CFG[12]	CFG[6]	TCK	VCCPWRGOOD0	PROCHOT#	DBR#	GFX_VID[6]	VSS	GFX_VID[2]	VAXG	VSS	VAXG	VAXG
AM	VID[6]	PROC_DPRSLPVR	VID[5]	CFG[7]	CFG[5]	CFG[0]	VSS	CFG[1]	VSS	TAPPWRGOOD	VSS	GFX_IMON	GFX_VID[4]	GFX_VID[0]	VAXG	VSS	VAXG	VAXG
AL	VID[3]	VSS	VID[4]	CFG[3]	VSS	CFG[4]	RSVD	RSVD	RSVD	RSVD_TP	RSVD	RSVD	VSS	RSVD	VAXG	VSS	VAXG	VAXG
AK	VID[0]	VID[2]	VID[1]	CFG[8]	CFG[9]	CFG[17]	VSS	CFG[10]	VSS	RSVD_TP	VSS	BPM#[2]	BPM#[6]	BPM#[1]	VAXG	VSS	VAXG	VAXG
AJ	VSS_SENSE	VCC_SENSE	RSVD	CFG[14]	VSS	CFG[16]	CFG[15]	CFG[11]	RSVD	RSVD	BPM#[4]	BPM#[3]	VSS	BPM#[0]	VAXG	VSS	VAXG	VAXG
AH	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	RSVD	SKTOCC#	BPM#[7]	BPM#[5]	VAXG	VSS	VAXG	VAXG
AG	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AF	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
AD	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
AB	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
AA	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
Y	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
W	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
V	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								

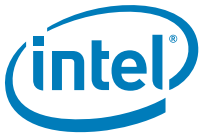

Figure 31. Socket-G (rPGA988A) Pinmap (Top View, Upper-Right Quadrant)

17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VSS	VAXG	PECI	SA_DQ[59]	SA_DQS#[7]	SA_DQ[60]	SA_DQ[54]	SB_DQ[63]	SB_DQ[59]	SB_DM[7]	SB_DQ[60]	SB_DQ[55]	SB_DQ[54]	SB_DQ[50]	RSVD_NCTF	RSVD_TP	VSS_NCTF	AT
VSS	VAXG	VSS	SA_DQ[62]	SA_DQS[7]	VSS	SA_DQ[50]	SB_DQ[62]	VSS	SB_DQS#[7]	SB_DQS[7]	VSS	SB_DQS#[6]	SB_DM[6]	VSS	RSVD_NCTF	RSVD_NCTF	AR
VSS	VAXG	PM_EXT_TS#[1]	SA_DQ[63]	VSS	SA_DQ[55]	SA_DQS#[6]	VSS	SB_DQ[61]	SB_DQ[58]	VSS	SB_DQ[57]	SB_DQS[6]	VSS	SB_DQ[48]	VSS	RSVD_NCTF	AP
VSS	VAXG	PM_EXT_TS#[0]	VCCPWRGOOD1	SA_DM[7]	SA_DQ[57]	SA_DQS[6]	SA_DM[6]	SA_DQ[53]	SA_DQ[48]	SB_DQ[56]	SB_DQ[51]	SB_DQ[49]	SB_DQ[52]	SB_DQ[53]	SB_DQ[43]	SM_RCOMP[2]	AN
VSS	VAXG	VTTPWRGOOD	VSS	SA_DQ[58]	SA_DQ[56]	VSS	SA_DQ[49]	SA_DQ[52]	VSS	SA_DM[5]	SB_DQ[42]	VSS	SB_DQ[46]	SB_DQ[47]	VSS	SM_RCOMP[1]	AM
VSS	VAXG	PM_SYNC	RSTIN#	SA_DQ[61]	VSS	SA_DQ[51]	SA_DQ[42]	VSS	SA_DQ[47]	SA_DQ[45]	VSS	SB_DQS[5]	SB_DQS#[5]	VSS	SB_DM[5]	SM_RCOMP[0]	AL
VSS	VAXG	THERMTRIP#	CATERR#	SM_DRAMPWROK	SA_DQ[43]	SA_DQ[46]	SA_DQS[5]	SA_DQS#[5]	SA_DQ[44]	SA_DQ[35]	SA_DQ[34]	SB_DQ[44]	SB_DQ[41]	SB_DQ[40]	SB_DQ[45]	SB_DQ[35]	AK
VSS	VAXG	RSVD	VSS	RSVD_TP	RSVD_TP	VSS	SA_DQ[40]	SA_DQ[41]	VSS	SA_DQ[38]	SA_DQ[39]	VSS	SB_DQ[38]	SB_DQ[34]	VSS	VDDQ	AJ
VSS	VAXG	RSVD	VTT0	VSS	VTT0	VTT0	VTT0	VSS	SA_DQS[4]	SA_DQS#[4]	VSS	SA_DQ[32]	SB_DQ[39]	VSS	SB_DQS#[4]	SB_DM[4]	AH
							VSS	RSVD	SA_MA[13]	RSVD_TP	SA_DM[4]	SA_DQ[37]	SB_DQ[36]	SB_DQ[37]	SB_DQS[4]	SB_DQ[33]	AG
							VTT0	SA_ODT[1]	VSS	SB_MA[13]	SA_DQ[36]	SA_DQ[33]	VSS	SB_DQ[32]	VSS	VDDQ	AF
							VTT0	SA_WE#	SA_CS#[1]	VDDQ	VSS	RSVD_TP	VDDQ	RSVD_TP	SA_CS#[0]	SA_CAS#	AE
							VSS	RSVD_TP	SA_ODT[0]	RSVD_TP	SB_CS#[1]	RSVD_TP	SA_MA[10]	RSVD_TP	RSVD_TP	SB_ODT[1]	AD
							VTT0	RSVD	VSS	SB_ODT[0]	SB_WE#	SB_CAS#	VSS	SA_BS[0]	VSS	VDDQ	AC
							VTT0	RSVD	SB_CS#[0]	VDDQ	VSS	SB_MA[10]	VDDQ	SA_RAS#	SA_BS[1]	SB_BS[0]	AB
							VSS	SA_MA[5]	SA_MA[2]	SA_CK#[0]	SA_CK[0]	RSVD_TP	RSVD_TP	SA_MA[3]	RSVD_TP	RSVD_TP	AA
							VTT0	SA_MA[8]	VSS	SB_RAS#	SA_CK[1]	SA_CK#[1]	VSS	SA_MA[0]	VSS	VDDQ	Y
							VTT0	SB_CK#[0]	SB_CK[0]	VDDQ	VSS	SB_BS[1]	VDDQ	RSVD_TP	RSVD_TP	SA_MA[1]	W
							VSS	SA_MA[15]	SA_MA[6]	SB_CK[1]	SB_CK#[1]	RSVD_TP	RSVD_TP	SB_MA[3]	SB_MA[1]	SA_MA[4]	V

Figure 32. Socket-G (rPGA988A) Pinmap (Top View, Lower-Left Quadrant)

	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18
U	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
T	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
R	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
P	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC								
N	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS								
M	PEG_TX #[1]	PEG_TX [1]	PEG_TX #[2]	PEG_TX [2]	PEG_TX [4]	PEG_TX #[3]	PEG_TX #[6]	PEG_TX [6]	RSVD	VCCPLL								
L	VSS	PEG_TX [0]	PEG_TX #[0]	VSS	PEG_TX #[4]	PEG_TX [3]	VSS	RSVD	VCCPLL	VCCPLL								
K	PEG_RX #[0]	VSS	VSS	PEG_TX #[5]	PEG_TX [5]	VSS	PEG_TX #[8]	PEG_TX [8]	VSS	VTT1								
J	PEG_RX [0]	PEG_RX #[1]	PEG_RX #[2]	VSS	PEG_TX #[7]	VSS	RSVD	RSVD	VTT1	VTT1	VTT1	VTT1	VTT1	VTT1	VSS	VTT1	VSS	VTT1
H	VSS	PEG_RX [1]	PEG_RX [2]	VSS	PEG_TX [7]	PEG_TX #[9]	PEG_TX #[10]	VSS	VTT1	VSS	VTT1	VSS	DMI_TX #[3]	VSS	VTT1	VTT1	VTT1	VSS
G	PEG_RX #[3]	VSS	PEG_RX [4]	PEG_RX #[4]	VSS	PEG_TX [9]	PEG_TX [10]	VTT1	VTT1	VTT1	RSVD	DMI_TX #[1]	DMI_TX [3]	FDI_TX[4]	FDI_TX #[4]	VSS	FDI_TX[7]	FDI_TX #[7]
F	PEG_RX [3]	PEG_RX #[5]	PEG_RX [8]	PEG_RX [6]	PEG_RX #[6]	VSS	PEG_TX #[11]	PEG_TX [11]	VSS	VTT1	VSS	DMI_TX [1]	DMI_TX #[2]	VSS	FDI_TX #[6]	FDI_TX[6]	VSS	FDI_LSYNC[0]
E	VSS	PEG_RX [5]	PEG_RX #[8]	VSS	RSVD	RSVD	VSS	PEG_TX #[12]	PEG_TX [12]	VTT1	VTT1	VSS	DMI_TX [2]	FDI_TX #[0]	VSS	FDI_TX[5]	FDI_TX #[5]	VSS
D	PEG_RX #[7]	PEG_RX [7]	VSS	PEG_RX #[10]	PEG_RX [10]	VSS	PEG_TX #[13]	PEG_TX [13]	PEG_TX #[14]	VSS	DMI_TX [0]	DMI_TX #[0]	DMI_RX [1]	FDI_TX[0]	FDI_TX #[1]	FDI_TX[2]	FDI_TX #[2]	FDI_TX #[3]
C	RSVD_NCTF	VSS	PEG_RX #[9]	VSS	PEG_RX #[12]	PEG_RX [12]	VSS	VSS	PEG_TX [14]	PEG_TX #[15]	PEG_TX [15]	VSS	DMI_RX #[1]	VSS	FDI_TX[1]	VSS	VSS	FDI_TX[3]
B	RSVD_NCTF	VSS_NCTF	PEG_RX [9]	PEG_RX #[11]	VSS	PEG_RX #[14]	PEG_RX [14]	PEG_RX #[13]	PEG_RC OMPO	PEG_IC OMPI	VSS	DMI_RX [0]	DMI_RX [2]	DMI_RX #[2]	VSS	RSVD	RSVD	VSS
A	VSS_NCTF	RSVD_NCTF	RSVD_NCTF	PEG_RX [11]	PEG_RX #[15]	PEG_RX [15]	VSS	PEG_RX [13]	VSS	PEG_IC OMPO	PEG_RB IAS	DMI_RX #[0]	VSS	DMI_RX [3]	DMI_RX #[3]	RSVD	RSVD	DPLL_REF_SSCLK

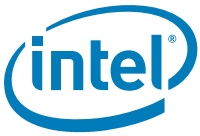

Figure 33. Socket-G (rPGA988A) Pinmap (Top View, Lower-Right Quadrant)

							VTT0	RSVD	VSS	SA_BS[2]	SA_MA[9]	SB_MA[0]	VSS	SA_MA[12]	VSS	VDDQ	U
							VTT0	RSVD	SB_MA[5]	VDDQ	VSS	SB_MA[2]	VDDQ	SA_MA[14]	SA_MA[11]	SA_MA[7]	T
							VSS	RSVD_TP	RSVD_TP	SB_BS[2]	SB_MA[7]	SB_MA[9]	SB_MA[8]	SB_MA[12]	SB_MA[6]	SB_MA[4]	R
							VTT0	SA_DQ[31]	VSS	SA_CKE[0]	SA_CKE[1]	SB_MA[14]	VSS	SB_MA[11]	VSS	VDDQ	P
							VTT0	SA_DQS#[3]	SA_DQ[30]	VDDQ	VSS	SB_DQ[31]	VDDQ	RSVD_TP	RSVD_TP	SB_MA[15]	N
							VSS	SA_DQS[3]	SA_DQ[26]	SA_DM[3]	SA_DQ[25]	SB_DQS[3]	SB_DQ[30]	SB_CKE[0]	SB_CKE[1]	SB_DQ[27]	M
							VTT0	SA_DQ[27]	VSS	SA_DQ[24]	SA_DQ[28]	VSS	SB_DQS#[3]	SB_DQ[26]	VSS	VDDQ	L
							VTT0	VSS	SA_DQ[29]	SA_DQ[18]	VSS	SB_DQ[28]	SB_DQ[29]	VSS	SB_DQ[25]	SB_DM[3]	K
SA_DIM_VREF	VTT0	VTT0	VTT0	VTT0	VTT0	VTT0	SA_DQ[23]	SA_DQS#[2]	SA_DQ[19]	SA_DQ[22]	SB_DQ[18]	SB_DQ[24]	SB_DQS#[2]	SB_DQ[19]	SB_DQ[22]	SB_DQ[23]	J
SB_DIM_VREF	RSVD_TP	VSS	VTT0	VSS	VTT0	VSS	SA_DQ[16]	SA_DQS[2]	VSS	SA_DM[2]	SB_DQ[16]	VSS	SB_DQS[2]	SB_DM[2]	VSS	VDDQ	H
RSVD	COMP1	VTT_SELECT	VTT0	VTT0	VTT0	VTT0	SA_DQ[21]	VSS	SA_DQ[17]	SA_DQ[20]	VSS	SB_DQ[21]	SB_DQ[15]	VSS	SB_DQ[17]	SB_DQ[20]	G
FDI_FSYNC[0]	VSS	RSVD_TP	VTT0	VTT0	VTT0	VTT0	SA_DQ[9]	SA_DQS[1]	SA_DQS#[1]	SA_DQ[11]	SM_DRAMRST#	SB_DQ[13]	SB_DQS#[1]	SB_DQ[14]	SB_DQ[10]	SB_DQ[11]	F
FDI_FSYNC[1]	PEG_CLK	RSVD_TP	VTT0	VSS	VTT0	VSS	SA_DQ[6]	SA_DQ[12]	VSS	SA_DQ[14]	SA_DQ[10]	VSS	SB_DQ[4]	SB_DQS[1]	VSS	SB_DM[1]	E
FDI_LSYNC[1]	PEG_CLK#	RSVD	VTT0	VTT0	VTT0	VTT0	SA_DQ[5]	VSS	SA_DQ[8]	SA_DM[1]	VSS	SB_DQS#[0]	SB_DM[0]	VSS	SB_DQ[9]	SB_DQ[8]	D
FDI_INT	VSS	RSVD	VTT0	VTT0	VTT0	VTT0	SA_DQ[1]	SA_DQS#[0]	SA_DQS[0]	SA_DQ[2]	SA_DQ[15]	SB_DQS[0]	SB_DQ[7]	SB_DQ[2]	SB_DQ[12]	RSVD_NCTF	C
VSS	BCLK#	VTT_SENSE	VTT0	VSS	VTT0	VSS	SA_DQ[4]	SA_DM[0]	VSS	SA_DQ[13]	VSS	SB_DQ[0]	VSS	SB_DQ[3]	VSS_NCTF	VSS_NCTF	B
DPLL_REF_SSCLK#	BCLK	VSS_SENSE_VTT	VTT0	VTT0	VTT0	VTT0	SA_DQ[0]	VSS	SA_DQ[7]	SA_DQ[3]	SB_DQ[5]	SB_DQ[1]	SB_DQ[6]	RSVD_NCTF	KEY		A
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
BCLK	A16	DIFF CLK	I
BCLK_ITP	AR30	DIFF CLK	O
BCLK_ITP#	AT30	DIFF CLK	O
BCLK#	B16	DIFF CLK	I
BPM#[0]	AJ22	GTL	I/O
BPM#[1]	AK22	GTL	I/O
BPM#[2]	AK24	GTL	I/O
BPM#[3]	AJ24	GTL	I/O
BPM#[4]	AJ25	GTL	I/O
BPM#[5]	AH22	GTL	I/O
BPM#[6]	AK23	GTL	I/O
BPM#[7]	AH23	GTL	I/O
CATERR#	AK14	GTL	I/O
CFG[0]	AM30	CMOS	I
CFG[1]	AM28	CMOS	I
CFG[2]	AP31	CMOS	I
CFG[3]	AL32	CMOS	I
CFG[4]	AL30	CMOS	I
CFG[5]	AM31	CMOS	I
CFG[6]	AN29	CMOS	I
CFG[7]	AM32	CMOS	I
CFG[8]	AK32	CMOS	I
CFG[9]	AK31	CMOS	I
CFG[10]	AK28	CMOS	I
CFG[11]	AJ28	CMOS	I
CFG[12]	AN30	CMOS	I
CFG[13]	AN32	CMOS	I
CFG[14]	AJ32	CMOS	I
CFG[15]	AJ29	CMOS	I
CFG[16]	AJ30	CMOS	I
CFG[17]	AK30	CMOS	I
COMP0	AT26	Analog	I
COMP1	G16	Analog	I
COMP2	AT24	Analog	I
COMP3	AT23	Analog	I
DBR#	AN25		O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
DMI_RX[0]	B24	DMI	I
DMI_RX[1]	D23	DMI	I
DMI_RX[2]	B23	DMI	I
DMI_RX[3]	A22	DMI	I
DMI_RX#[0]	A24	DMI	I
DMI_RX#[1]	C23	DMI	I
DMI_RX#[2]	B22	DMI	I
DMI_RX#[3]	A21	DMI	I
DMI_TX[0]	D25	DMI	O
DMI_TX[1]	F24	DMI	O
DMI_TX[2]	E23	DMI	O
DMI_TX[3]	G23	DMI	O
DMI_TX#[0]	D24	DMI	O
DMI_TX#[1]	G24	DMI	O
DMI_TX#[2]	F23	DMI	O
DMI_TX#[3]	H23	DMI	O
DPLL_REF_SSCLK	A18	DIFF CLK	I
DPLL_REF_SSCLK#	A17	DIFF CLK	I
FDI_FSYNC[0]	F17	CMOS	I
FDI_FSYNC[1]	E17	CMOS	I
FDI_INT	C17	CMOS	I
FDI_LSYNC[0]	F18	CMOS	I
FDI_LSYNC[1]	D17	CMOS	I
FDI_TX[0]	D22	FDI	O
FDI_TX[1]	C21	FDI	O
FDI_TX[2]	D20	FDI	O
FDI_TX[3]	C18	FDI	O
FDI_TX[4]	G22	FDI	O
FDI_TX[5]	E20	FDI	O
FDI_TX[6]	F20	FDI	O
FDI_TX[7]	G19	FDI	O
FDI_TX#[0]	E22	FDI	O
FDI_TX#[1]	D21	FDI	O
FDI_TX#[2]	D19	FDI	O
FDI_TX#[3]	D18	FDI	O
FDI_TX#[4]	G21	FDI	O

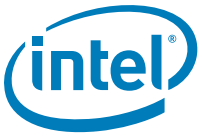

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
FDI_TX#[5]	E19	FDI	O
FDI_TX#[6]	F21	FDI	O
FDI_TX#[7]	G18	FDI	O
GFX_DPRSLPVR	AT25	CMOS	O
GFX_IMON	AM24	Analog	I
GFX_VID[0]	AM22	CMOS	O
GFX_VID[1]	AP22	CMOS	O
GFX_VID[2]	AN22	CMOS	O
GFX_VID[3]	AP23	CMOS	O
GFX_VID[4]	AM23	CMOS	O
GFX_VID[5]	AP24	CMOS	O
GFX_VID[6]	AN24	CMOS	O
GFX_VR_EN	AR25	CMOS	O
ISENSE	AN35	Analog	I
KEY	A2		
PECI	AT15	Async	I/O
PEG_CLK	E16	DIFF CLK	I
PEG_CLK#	D16	DIFF CLK	I
PEG_ICOMPI	B26	Analog	I
PEG_ICOMPO	A26	Analog	I
PEG_RBIAS	A25	Analog	I
PEG_RCOMPO	B27	Analog	I
PEG_RX[0]	J35	PCIe	I
PEG_RX[1]	H34	PCIe	I
PEG_RX[2]	H33	PCIe	I
PEG_RX[3]	F35	PCIe	I
PEG_RX[4]	G33	PCIe	I
PEG_RX[5]	E34	PCIe	I
PEG_RX[6]	F32	PCIe	I
PEG_RX[7]	D34	PCIe	I
PEG_RX[8]	F33	PCIe	I
PEG_RX[9]	B33	PCIe	I
PEG_RX[10]	D31	PCIe	I
PEG_RX[11]	A32	PCIe	I
PEG_RX[12]	C30	PCIe	I
PEG_RX[13]	A28	PCIe	I

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
PEG_RX[14]	B29	PCIe	I
PEG_RX[15]	A30	PCIe	I
PEG_RX#[0]	K35	PCIe	I
PEG_RX#[1]	J34	PCIe	I
PEG_RX#[2]	J33	PCIe	I
PEG_RX#[3]	G35	PCIe	I
PEG_RX#[4]	G32	PCIe	I
PEG_RX#[5]	F34	PCIe	I
PEG_RX#[6]	F31	PCIe	I
PEG_RX#[7]	D35	PCIe	I
PEG_RX#[8]	E33	PCIe	I
PEG_RX#[9]	C33	PCIe	I
PEG_RX#[10]	D32	PCIe	I
PEG_RX#[11]	B32	PCIe	I
PEG_RX#[12]	C31	PCIe	I
PEG_RX#[13]	B28	PCIe	I
PEG_RX#[14]	B30	PCIe	I
PEG_RX#[15]	A31	PCIe	I
PEG_TX[0]	L34	PCIe	O
PEG_TX[1]	M34	PCIe	O
PEG_TX[2]	M32	PCIe	O
PEG_TX[3]	L30	PCIe	O
PEG_TX[4]	M31	PCIe	O
PEG_TX[5]	K31	PCIe	O
PEG_TX[6]	M28	PCIe	O
PEG_TX[7]	H31	PCIe	O
PEG_TX[8]	K28	PCIe	O
PEG_TX[9]	G30	PCIe	O
PEG_TX[10]	G29	PCIe	O
PEG_TX[11]	F28	PCIe	O
PEG_TX[12]	E27	PCIe	O
PEG_TX[13]	D28	PCIe	O
PEG_TX[14]	C27	PCIe	O
PEG_TX[15]	C25	PCIe	O
PEG_TX#[0]	L33	PCIe	O
PEG_TX#[1]	M35	PCIe	O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
PEG_TX#[2]	M33	PCIe	O
PEG_TX#[3]	M30	PCIe	O
PEG_TX#[4]	L31	PCIe	O
PEG_TX#[5]	K32	PCIe	O
PEG_TX#[6]	M29	PCIe	O
PEG_TX#[7]	J31	PCIe	O
PEG_TX#[8]	K29	PCIe	O
PEG_TX#[9]	H30	PCIe	O
PEG_TX#[10]	H29	PCIe	O
PEG_TX#[11]	F29	PCIe	O
PEG_TX#[12]	E28	PCIe	O
PEG_TX#[13]	D29	PCIe	O
PEG_TX#[14]	D27	PCIe	O
PEG_TX#[15]	C26	PCIe	O
PM_EXT_TS#[0]	AN15	CMOS	I
PM_EXT_TS#[1]	AP15	CMOS	I
PM_SYNC	AL15	CMOS	I
PRDY#	AT28	Async GTL	O
PREQ#	AP27	Async GTL	I
PROC_DPRSLPVR	AM34	CMOS	O
PROCHOT#	AN26	Async GTL	I/O
PSI#	AN33	Async CMOS	O
RESET_OBS#	AP26	Async CMOS	O
RSTIN#	AL14	CMOS	I
RSVD	A19		
RSVD	A20		
RSVD	AB9		
RSVD	AC9		
RSVD	AG9		
RSVD	AH15		
RSVD	AH25		
RSVD	AJ15		
RSVD	AJ26		

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
RSVD	AJ27		
RSVD	AJ33		
RSVD	AL22		
RSVD	AL24		
RSVD	AL25		
RSVD	AL27		
RSVD	AL28		
RSVD	AL29		
RSVD	AP25		
RSVD	AP30		
RSVD	AP32		
RSVD	AP33		
RSVD	AR32		
RSVD	AR33		
RSVD	AT31		
RSVD	AT32		
RSVD	B19		
RSVD	B20		
RSVD	C15		
RSVD	D15		
RSVD	E30		
RSVD	E31		
RSVD	G17		
RSVD	G25		
RSVD	H17		
RSVD	J17		
RSVD	J28		
RSVD	J29		
RSVD	L28		
RSVD	M27		
RSVD	T9		
RSVD	U9		
RSVD_NCTF	A3		
RSVD_NCTF	A33		
RSVD_NCTF	A34		
RSVD_NCTF	AP1		

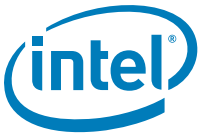

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
RSVD_NCTF	AP35		
RSVD_NCTF	AR1		
RSVD_NCTF	AR2		
RSVD_NCTF	AR35		
RSVD_NCTF	AT3		
RSVD_NCTF	AT33		
RSVD_NCTF	AT34		
RSVD_NCTF	B35		
RSVD_NCTF	C1		
RSVD_NCTF	C35		
RSVD_TP	AA1		
RSVD_TP	AA2		
RSVD_TP	AA4		
RSVD_TP	AA5		
RSVD_TP	AD2		
RSVD_TP	AD3		
RSVD_TP	AD5		
RSVD_TP	AD7		
RSVD_TP	AD9		
RSVD_TP	AE3		
RSVD_TP	AE5		
RSVD_TP	AG7		
RSVD_TP	AJ12		
RSVD_TP	AJ13		
RSVD_TP	AK26		
RSVD_TP	AL26		
RSVD_TP	AT2		
RSVD_TP	E15		
RSVD_TP	F15		
RSVD_TP	H16		
RSVD_TP	N2		
RSVD_TP	N3		
RSVD_TP	R8		
RSVD_TP	R9		
RSVD_TP	V4		
RSVD_TP	V5		

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
RSVD_TP	W2		
RSVD_TP	W3		
SA_BS[0]	AC3	DDR3	O
SA_BS[1]	AB2	DDR3	O
SA_BS[2]	U7	DDR3	O
SA_CAS#	AE1	DDR3	O
SA_CK[0]	AA6	DDR3	O
SA_CK[1]	Y6	DDR3	O
SA_CK#[0]	AA7	DDR3	O
SA_CK#[1]	Y5	DDR3	O
SA_CKE[0]	P7	DDR3	O
SA_CKE[1]	P6	DDR3	O
SA_CS#[0]	AE2	DDR3	O
SA_CS#[1]	AE8	DDR3	O
SA_DM[0]	B9	DDR3	O
SA_DM[1]	D7	DDR3	O
SA_DM[2]	H7	DDR3	O
SA_DM[3]	M7	DDR3	O
SA_DM[4]	AG6	DDR3	O
SA_DM[5]	AM7	DDR3	O
SA_DM[6]	AN10	DDR3	O
SA_DM[7]	AN13	DDR3	O
SA_DQ[0]	A10	DDR3	I/O
SA_DQ[1]	C10	DDR3	I/O
SA_DQ[2]	C7	DDR3	I/O
SA_DQ[3]	A7	DDR3	I/O
SA_DQ[4]	B10	DDR3	I/O
SA_DQ[5]	D10	DDR3	I/O
SA_DQ[6]	E10	DDR3	I/O
SA_DQ[7]	A8	DDR3	I/O
SA_DQ[8]	D8	DDR3	I/O
SA_DQ[9]	F10	DDR3	I/O
SA_DQ[10]	E6	DDR3	I/O
SA_DQ[11]	F7	DDR3	I/O
SA_DQ[12]	E9	DDR3	I/O
SA_DQ[13]	B7	DDR3	I/O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SA_DQ[14]	E7	DDR3	I/O
SA_DQ[15]	C6	DDR3	I/O
SA_DQ[16]	H10	DDR3	I/O
SA_DQ[17]	G8	DDR3	I/O
SA_DQ[18]	K7	DDR3	I/O
SA_DQ[19]	J8	DDR3	I/O
SA_DQ[20]	G7	DDR3	I/O
SA_DQ[21]	G10	DDR3	I/O
SA_DQ[22]	J7	DDR3	I/O
SA_DQ[23]	J10	DDR3	I/O
SA_DQ[24]	L7	DDR3	I/O
SA_DQ[25]	M6	DDR3	I/O
SA_DQ[26]	M8	DDR3	I/O
SA_DQ[27]	L9	DDR3	I/O
SA_DQ[28]	L6	DDR3	I/O
SA_DQ[29]	K8	DDR3	I/O
SA_DQ[30]	N8	DDR3	I/O
SA_DQ[31]	P9	DDR3	I/O
SA_DQ[32]	AH5	DDR3	I/O
SA_DQ[33]	AF5	DDR3	I/O
SA_DQ[34]	AK6	DDR3	I/O
SA_DQ[35]	AK7	DDR3	I/O
SA_DQ[36]	AF6	DDR3	I/O
SA_DQ[37]	AG5	DDR3	I/O
SA_DQ[38]	AJ7	DDR3	I/O
SA_DQ[39]	AJ6	DDR3	I/O
SA_DQ[40]	AJ10	DDR3	I/O
SA_DQ[41]	AJ9	DDR3	I/O
SA_DQ[42]	AL10	DDR3	I/O
SA_DQ[43]	AK12	DDR3	I/O
SA_DQ[44]	AK8	DDR3	I/O
SA_DQ[45]	AL7	DDR3	I/O
SA_DQ[46]	AK11	DDR3	I/O
SA_DQ[47]	AL8	DDR3	I/O
SA_DQ[48]	AN8	DDR3	I/O
SA_DQ[49]	AM10	DDR3	I/O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SA_DQ[50]	AR11	DDR3	I/O
SA_DQ[51]	AL11	DDR3	I/O
SA_DQ[52]	AM9	DDR3	I/O
SA_DQ[53]	AN9	DDR3	I/O
SA_DQ[54]	AT11	DDR3	I/O
SA_DQ[55]	AP12	DDR3	I/O
SA_DQ[56]	AM12	DDR3	I/O
SA_DQ[57]	AN12	DDR3	I/O
SA_DQ[58]	AM13	DDR3	I/O
SA_DQ[59]	AT14	DDR3	I/O
SA_DQ[60]	AT12	DDR3	I/O
SA_DQ[61]	AL13	DDR3	I/O
SA_DQ[62]	AR14	DDR3	I/O
SA_DQ[63]	AP14	DDR3	I/O
SA_DQS[0]	C8	DDR3	I/O
SA_DQS[1]	F9	DDR3	I/O
SA_DQS[2]	H9	DDR3	I/O
SA_DQS[3]	M9	DDR3	I/O
SA_DQS[4]	AH8	DDR3	I/O
SA_DQS[5]	AK10	DDR3	I/O
SA_DQS[6]	AN11	DDR3	I/O
SA_DQS[7]	AR13	DDR3	I/O
SA_DQS#[0]	C9	DDR3	I/O
SA_DQS#[1]	F8	DDR3	I/O
SA_DQS#[2]	J9	DDR3	I/O
SA_DQS#[3]	N9	DDR3	I/O
SA_DQS#[4]	AH7	DDR3	I/O
SA_DQS#[5]	AK9	DDR3	I/O
SA_DQS#[6]	AP11	DDR3	I/O
SA_DQS#[7]	AT13	DDR3	I/O
SA_MA[0]	Y3	DDR3	O
SA_MA[1]	W1	DDR3	O
SA_MA[2]	AA8	DDR3	O
SA_MA[3]	AA3	DDR3	O
SA_MA[4]	V1	DDR3	O
SA_MA[5]	AA9	DDR3	O

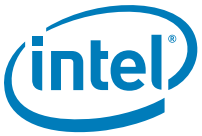

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SA_MA[6]	V8	DDR3	O
SA_MA[7]	T1	DDR3	O
SA_MA[8]	Y9	DDR3	O
SA_MA[9]	U6	DDR3	O
SA_MA[10]	AD4	DDR3	O
SA_MA[11]	T2	DDR3	O
SA_MA[12]	U3	DDR3	O
SA_MA[13]	AG8	DDR3	O
SA_MA[14]	T3	DDR3	O
SA_MA[15]	V9	DDR3	O
SA_ODT[0]	AD8	DDR3	O
SA_ODT[1]	AF9	DDR3	O
SA_RAS#	AB3	DDR3	O
SA_WE#	AE9	DDR3	O
SB_BS[0]	AB1	DDR3	O
SB_BS[1]	W5	DDR3	O
SB_BS[2]	R7	DDR3	O
SB_CAS#	AC5	DDR3	O
SB_CK[0]	W8	DDR3	O
SB_CK[1]	V7	DDR3	O
SB_CK#[0]	W9	DDR3	O
SB_CK#[1]	V6	DDR3	O
SB_CKE[0]	M3	DDR3	O
SB_CKE[1]	M2	DDR3	O
SB_CS#[0]	AB8	DDR3	O
SB_CS#[1]	AD6	DDR3	O
SB_DM[0]	D4	DDR3	O
SB_DM[1]	E1	DDR3	O
SB_DM[2]	H3	DDR3	O
SB_DM[3]	K1	DDR3	O
SB_DM[4]	AH1	DDR3	O
SB_DM[5]	AL2	DDR3	O
SB_DM[6]	AR4	DDR3	O
SB_DM[7]	AT8	DDR3	O
SB_DQ[0]	B5	DDR3	I/O
SB_DQ[1]	A5	DDR3	I/O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SB_DQ[2]	C3	DDR3	I/O
SB_DQ[3]	B3	DDR3	I/O
SB_DQ[4]	E4	DDR3	I/O
SB_DQ[5]	A6	DDR3	I/O
SB_DQ[6]	A4	DDR3	I/O
SB_DQ[7]	C4	DDR3	I/O
SB_DQ[8]	D1	DDR3	I/O
SB_DQ[9]	D2	DDR3	I/O
SB_DQ[10]	F2	DDR3	I/O
SB_DQ[11]	F1	DDR3	I/O
SB_DQ[12]	C2	DDR3	I/O
SB_DQ[13]	F5	DDR3	I/O
SB_DQ[14]	F3	DDR3	I/O
SB_DQ[15]	G4	DDR3	I/O
SB_DQ[16]	H6	DDR3	I/O
SB_DQ[17]	G2	DDR3	I/O
SB_DQ[18]	J6	DDR3	I/O
SB_DQ[19]	J3	DDR3	I/O
SB_DQ[20]	G1	DDR3	I/O
SB_DQ[21]	G5	DDR3	I/O
SB_DQ[22]	J2	DDR3	I/O
SB_DQ[23]	J1	DDR3	I/O
SB_DQ[24]	J5	DDR3	I/O
SB_DQ[25]	K2	DDR3	I/O
SB_DQ[26]	L3	DDR3	I/O
SB_DQ[27]	M1	DDR3	I/O
SB_DQ[28]	K5	DDR3	I/O
SB_DQ[29]	K4	DDR3	I/O
SB_DQ[30]	M4	DDR3	I/O
SB_DQ[31]	N5	DDR3	I/O
SB_DQ[32]	AF3	DDR3	I/O
SB_DQ[33]	AG1	DDR3	I/O
SB_DQ[34]	AJ3	DDR3	I/O
SB_DQ[35]	AK1	DDR3	I/O
SB_DQ[36]	AG4	DDR3	I/O
SB_DQ[37]	AG3	DDR3	I/O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SB_DQ[38]	AJ4	DDR3	I/O
SB_DQ[39]	AH4	DDR3	I/O
SB_DQ[40]	AK3	DDR3	I/O
SB_DQ[41]	AK4	DDR3	I/O
SB_DQ[42]	AM6	DDR3	I/O
SB_DQ[43]	AN2	DDR3	I/O
SB_DQ[44]	AK5	DDR3	I/O
SB_DQ[45]	AK2	DDR3	I/O
SB_DQ[46]	AM4	DDR3	I/O
SB_DQ[47]	AM3	DDR3	I/O
SB_DQ[48]	AP3	DDR3	I/O
SB_DQ[49]	AN5	DDR3	I/O
SB_DQ[50]	AT4	DDR3	I/O
SB_DQ[51]	AN6	DDR3	I/O
SB_DQ[52]	AN4	DDR3	I/O
SB_DQ[53]	AN3	DDR3	I/O
SB_DQ[54]	AT5	DDR3	I/O
SB_DQ[55]	AT6	DDR3	I/O
SB_DQ[56]	AN7	DDR3	I/O
SB_DQ[57]	AP6	DDR3	I/O
SB_DQ[58]	AP8	DDR3	I/O
SB_DQ[59]	AT9	DDR3	I/O
SB_DQ[60]	AT7	DDR3	I/O
SB_DQ[61]	AP9	DDR3	I/O
SB_DQ[62]	AR10	DDR3	I/O
SB_DQ[63]	AT10	DDR3	I/O
SB_DQS[0]	C5	DDR3	I/O
SB_DQS[1]	E3	DDR3	I/O
SB_DQS[2]	H4	DDR3	I/O
SB_DQS[3]	M5	DDR3	I/O
SB_DQS[4]	AG2	DDR3	I/O
SB_DQS[5]	AL5	DDR3	I/O
SB_DQS[6]	AP5	DDR3	I/O
SB_DQS[7]	AR7	DDR3	I/O
SB_DQS#[0]	D5	DDR3	I/O
SB_DQS#[1]	F4	DDR3	I/O

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
SB_DQS#[2]	J4	DDR3	I/O
SB_DQS#[3]	L4	DDR3	I/O
SB_DQS#[4]	AH2	DDR3	I/O
SB_DQS#[5]	AL4	DDR3	I/O
SB_DQS#[6]	AR5	DDR3	I/O
SB_DQS#[7]	AR8	DDR3	I/O
SB_MA[0]	U5	DDR3	O
SB_MA[1]	V2	DDR3	O
SB_MA[2]	T5	DDR3	O
SB_MA[3]	V3	DDR3	O
SB_MA[4]	R1	DDR3	O
SB_MA[5]	T8	DDR3	O
SB_MA[6]	R2	DDR3	O
SB_MA[7]	R6	DDR3	O
SB_MA[8]	R4	DDR3	O
SB_MA[9]	R5	DDR3	O
SB_MA[10]	AB5	DDR3	O
SB_MA[11]	P3	DDR3	O
SB_MA[12]	R3	DDR3	O
SB_MA[13]	AF7	DDR3	O
SB_MA[14]	P5	DDR3	O
SB_MA[15]	N1	DDR3	O
SB_ODT[0]	AC7	DDR3	O
SB_ODT[1]	AD1	DDR3	O
SB_RAS#	Y7	DDR3	O
SB_WE#	AC6	DDR3	O
SKTOCC#	AH24		
SM_DRAMPWROK	AK13	DDR3	O
SM_DRAMRST#	F6	DDR3	O
SM_RCOMP[0]	AL1	Analog	I
SM_RCOMP[1]	AM1	Analog	I
SM_RCOMP[2]	AN1	Analog	I
TAPPWRGOOD	AM26	Async CMOS	O
TCK	AN28	CMOS	I
TDI	AT29	CMOS	I
TDI_M	AR29	CMOS	I

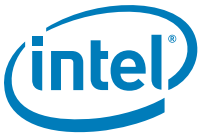

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
TDO	AR27	CMOS	O
TDO_M	AP29	CMOS	O
THERMTRIP#	AK15	Async GTL	O
TMS	AP28	CMOS	I
TRST#	AT27	CMOS	I
VAXG	AH16	REF	
VAXG	AH18	REF	
VAXG	AH19	REF	
VAXG	AH21	REF	
VAXG	AJ16	REF	
VAXG	AJ18	REF	
VAXG	AJ19	REF	
VAXG	AJ21	REF	
VAXG	AK16	REF	
VAXG	AK18	REF	
VAXG	AK19	REF	
VAXG	AK21	REF	
VAXG	AL16	REF	
VAXG	AL18	REF	
VAXG	AL19	REF	
VAXG	AL21	REF	
VAXG	AM16	REF	
VAXG	AM18	REF	
VAXG	AM19	REF	
VAXG	AM21	REF	
VAXG	AN16	REF	
VAXG	AN18	REF	
VAXG	AN19	REF	
VAXG	AN21	REF	
VAXG	AP16	REF	
VAXG	AP18	REF	
VAXG	AP19	REF	
VAXG	AP21	REF	
VAXG	AR16	REF	
VAXG	AR18	REF	
VAXG	AR19	REF	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VAXG	AR21	REF	
VAXG	AT16	REF	
VAXG	AT18	REF	
VAXG	AT19	REF	
VAXG	AT21	REF	
VAXG_SENSE	AR22	Analog	O
VCC	AA26	REF	
VCC	AA27	REF	
VCC	AA28	REF	
VCC	AA29	REF	
VCC	AA30	REF	
VCC	AA31	REF	
VCC	AA32	REF	
VCC	AA33	REF	
VCC	AA34	REF	
VCC	AA35	REF	
VCC	AC26	REF	
VCC	AC27	REF	
VCC	AC28	REF	
VCC	AC29	REF	
VCC	AC30	REF	
VCC	AC31	REF	
VCC	AC32	REF	
VCC	AC33	REF	
VCC	AC34	REF	
VCC	AC35	REF	
VCC	AD26	REF	
VCC	AD27	REF	
VCC	AD28	REF	
VCC	AD29	REF	
VCC	AD30	REF	
VCC	AD31	REF	
VCC	AD32	REF	
VCC	AD33	REF	
VCC	AD34	REF	
VCC	AD35	REF	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VCC	AF26	REF	
VCC	AF27	REF	
VCC	AF28	REF	
VCC	AF29	REF	
VCC	AF30	REF	
VCC	AF31	REF	
VCC	AF32	REF	
VCC	AF33	REF	
VCC	AF34	REF	
VCC	AF35	REF	
VCC	AG26	REF	
VCC	AG27	REF	
VCC	AG28	REF	
VCC	AG29	REF	
VCC	AG30	REF	
VCC	AG31	REF	
VCC	AG32	REF	
VCC	AG33	REF	
VCC	AG34	REF	
VCC	AG35	REF	
VCC	P26	REF	
VCC	P27	REF	
VCC	P28	REF	
VCC	P29	REF	
VCC	P30	REF	
VCC	P31	REF	
VCC	P32	REF	
VCC	P33	REF	
VCC	P34	REF	
VCC	P35	REF	
VCC	R26	REF	
VCC	R27	REF	
VCC	R28	REF	
VCC	R29	REF	
VCC	R30	REF	
VCC	R31	REF	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VCC	R32	REF	
VCC	R33	REF	
VCC	R34	REF	
VCC	R35	REF	
VCC	U26	REF	
VCC	U27	REF	
VCC	U28	REF	
VCC	U29	REF	
VCC	U30	REF	
VCC	U31	REF	
VCC	U32	REF	
VCC	U33	REF	
VCC	U34	REF	
VCC	U35	REF	
VCC	V26	REF	
VCC	V27	REF	
VCC	V28	REF	
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VCC	V30	REF	
VCC	V31	REF	
VCC	V32	REF	
VCC	V33	REF	
VCC	V34	REF	
VCC	V35	REF	
VCC	Y26	REF	
VCC	Y27	REF	
VCC	Y28	REF	
VCC	Y29	REF	
VCC	Y30	REF	
VCC	Y31	REF	
VCC	Y32	REF	
VCC	Y33	REF	
VCC	Y34	REF	
VCC	Y35	REF	
VCC_SENSE	AJ34	Analog	O
VCCPLL	L26	REF	

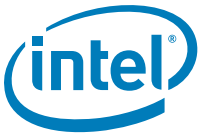


Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VCCPLL	L27	REF	
VCCPLL	M26	REF	
VCCPWRGOOD_0	AN27	Async CMOS	I
VCCPWRGOOD_1	AN14	Async CMOS	I
VDDQ	AB4	REF	
VDDQ	AB7	REF	
VDDQ	AC1	REF	
VDDQ	AE4	REF	
VDDQ	AE7	REF	
VDDQ	AF1	REF	
VDDQ	AJ1	REF	
VDDQ	H1	REF	
VDDQ	L1	REF	
VDDQ	N4	REF	
VDDQ	N7	REF	
VDDQ	P1	REF	
VDDQ	T4	REF	
VDDQ	T7	REF	
VDDQ	U1	REF	
VDDQ	W4	REF	
VDDQ	W7	REF	
VDDQ	Y1	REF	
VID[0]	AK35	CMOS	O
VID[1]	AK33	CMOS	O
VID[2]	AK34	CMOS	O
CSC[0]/VID[3]	AL35	CMOS	I/O
CSC[1]/VID[4]	AL33	CMOS	I/O
CSC[2]/VID[5]	AM33	CMOS	I/O
VID[6]	AM35	CMOS	O
VSS	A23	GND	
VSS	A27	GND	
VSS	A29	GND	
VSS	A9	GND	
VSS	AA10	GND	
VSS	AB26	GND	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	AB27	GND	
VSS	AB28	GND	
VSS	AB29	GND	
VSS	AB30	GND	
VSS	AB31	GND	
VSS	AB32	GND	
VSS	AB33	GND	
VSS	AB34	GND	
VSS	AB35	GND	
VSS	AB6	GND	
VSS	AC2	GND	
VSS	AC4	GND	
VSS	AC8	GND	
VSS	AD10	GND	
VSS	AE26	GND	
VSS	AE27	GND	
VSS	AE28	GND	
VSS	AE29	GND	
VSS	AE30	GND	
VSS	AE31	GND	
VSS	AE32	GND	
VSS	AE33	GND	
VSS	AE34	GND	
VSS	AE35	GND	
VSS	AE6	GND	
VSS	AF2	GND	
VSS	AF4	GND	
VSS	AF8	GND	
VSS	AG10	GND	
VSS	AH13	GND	
VSS	AH17	GND	
VSS	AH20	GND	
VSS	AH26	GND	
VSS	AH27	GND	
VSS	AH28	GND	
VSS	AH29	GND	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	AH3	GND	
VSS	AH30	GND	
VSS	AH31	GND	
VSS	AH32	GND	
VSS	AH33	GND	
VSS	AH34	GND	
VSS	AH35	GND	
VSS	AH6	GND	
VSS	AH9	GND	
VSS	AJ11	GND	
VSS	AJ14	GND	
VSS	AJ17	GND	
VSS	AJ2	GND	
VSS	AJ20	GND	
VSS	AJ23	GND	
VSS	AJ31	GND	
VSS	AJ5	GND	
VSS	AJ8	GND	
VSS	AK17	GND	
VSS	AK20	GND	
VSS	AK25	GND	
VSS	AK27	GND	
VSS	AK29	GND	
VSS	AL12	GND	
VSS	AL17	GND	
VSS	AL20	GND	
VSS	AL23	GND	
VSS	AL3	GND	
VSS	AL31	GND	
VSS	AL34	GND	
VSS	AL6	GND	
VSS	AL9	GND	
VSS	AM11	GND	
VSS	AM14	GND	
VSS	AM17	GND	
VSS	AM2	GND	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	AM20	GND	
VSS	AM25	GND	
VSS	AM27	GND	
VSS	AM29	GND	
VSS	AM5	GND	
VSS	AM8	GND	
VSS	AN17	GND	
VSS	AN20	GND	
VSS	AN23	GND	
VSS	AN31	GND	
VSS	AN34	GND	
VSS	AP10	GND	
VSS	AP13	GND	
VSS	AP17	GND	
VSS	AP2	GND	
VSS	AP20	GND	
VSS	AP34	GND	
VSS	AP4	GND	
VSS	AP7	GND	
VSS	AR12	GND	
VSS	AR15	GND	
VSS	AR17	GND	
VSS	AR20	GND	
VSS	AR23	GND	
VSS	AR24	GND	
VSS	AR26	GND	
VSS	AR28	GND	
VSS	AR3	GND	
VSS	AR31	GND	
VSS	AR6	GND	
VSS	AR9	GND	
VSS	AT17	GND	
VSS	AT20	GND	
VSS	B11	GND	
VSS	B13	GND	
VSS	B17	GND	

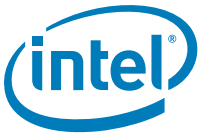


Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	B18	GND	
VSS	B21	GND	
VSS	B25	GND	
VSS	B31	GND	
VSS	B4	GND	
VSS	B6	GND	
VSS	B8	GND	
VSS	C16	GND	
VSS	C19	GND	
VSS	C20	GND	
VSS	C22	GND	
VSS	C24	GND	
VSS	C28	GND	
VSS	C29	GND	
VSS	C32	GND	
VSS	C34	GND	
VSS	D26	GND	
VSS	D3	GND	
VSS	D30	GND	
VSS	D33	GND	
VSS	D6	GND	
VSS	D9	GND	
VSS	E11	GND	
VSS	E13	GND	
VSS	E18	GND	
VSS	E2	GND	
VSS	E21	GND	
VSS	E24	GND	
VSS	E29	GND	
VSS	E32	GND	
VSS	E35	GND	
VSS	E5	GND	
VSS	E8	GND	
VSS	F16	GND	
VSS	F19	GND	
VSS	F22	GND	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	F25	GND	
VSS	F27	GND	
VSS	F30	GND	
VSS	G20	GND	
VSS	G3	GND	
VSS	G31	GND	
VSS	G34	GND	
VSS	G6	GND	
VSS	G9	GND	
VSS	H11	GND	
VSS	H13	GND	
VSS	H15	GND	
VSS	H18	GND	
VSS	H2	GND	
VSS	H22	GND	
VSS	H24	GND	
VSS	H26	GND	
VSS	H28	GND	
VSS	H32	GND	
VSS	H35	GND	
VSS	H5	GND	
VSS	H8	GND	
VSS	J19	GND	
VSS	J21	GND	
VSS	J30	GND	
VSS	J32	GND	
VSS	K27	GND	
VSS	K3	GND	
VSS	K30	GND	
VSS	K33	GND	
VSS	K34	GND	
VSS	K6	GND	
VSS	K9	GND	
VSS	L2	GND	
VSS	L29	GND	
VSS	L32	GND	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	L35	GND	
VSS	L5	GND	
VSS	L8	GND	
VSS	M10	GND	
VSS	N26	GND	
VSS	N27	GND	
VSS	N28	GND	
VSS	N29	GND	
VSS	N30	GND	
VSS	N31	GND	
VSS	N32	GND	
VSS	N33	GND	
VSS	N34	GND	
VSS	N35	GND	
VSS	N6	GND	
VSS	P2	GND	
VSS	P4	GND	
VSS	P8	GND	
VSS	R10	GND	
VSS	T26	GND	
VSS	T27	GND	
VSS	T28	GND	
VSS	T29	GND	
VSS	T30	GND	
VSS	T31	GND	
VSS	T32	GND	
VSS	T33	GND	
VSS	T34	GND	
VSS	T35	GND	
VSS	T6	GND	
VSS	U2	GND	
VSS	U4	GND	
VSS	U8	GND	
VSS	V10	GND	
VSS	W26	GND	
VSS	W27	GND	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VSS	W28	GND	
VSS	W29	GND	
VSS	W30	GND	
VSS	W31	GND	
VSS	W32	GND	
VSS	W33	GND	
VSS	W34	GND	
VSS	W35	GND	
VSS	W6	GND	
VSS	Y2	GND	
VSS	Y4	GND	
VSS	Y8	GND	
VSS_NCTF	A35		
VSS_NCTF	AR34		
VSS_NCTF	AT1		
VSS_NCTF	AT35		
VSS_NCTF	B1		
VSS_NCTF	B2		
VSS_NCTF	B34		
VSS_SENSE	AJ35	Analog	O
VSS_SENSE_VTT	A15	Analog	O
VSSAXG_SENSE	AT22	Analog	O
VTT_SELECT	G15	CMOS	O
VTT_SENSE	B15	Analog	O
VTT0	A11	REF	
VTT0	A12	REF	
VTT0	A13	REF	
VTT0	A14	REF	
VTT0	AB10	REF	
VTT0	AC10	REF	
VTT0	AE10	REF	
VTT0	AF10	REF	
VTT0	AH10	REF	
VTT0	AH11	REF	
VTT0	AH12	REF	
VTT0	AH14	REF	

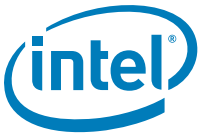


Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VTT0	B12	REF	
VTT0	B14	REF	
VTT0	C11	REF	
VTT0	C12	REF	
VTT0	C13	REF	
VTT0	C14	REF	
VTT0	D11	REF	
VTT0	D12	REF	
VTT0	D13	REF	
VTT0	D14	REF	
VTT0	E12	REF	
VTT0	E14	REF	
VTT0	F11	REF	
VTT0	F12	REF	
VTT0	F13	REF	
VTT0	F14	REF	
VTT0	G11	REF	
VTT0	G12	REF	
VTT0	G13	REF	
VTT0	G14	REF	
VTT0	H12	REF	
VTT0	H14	REF	
VTT0	J11	REF	
VTT0	J12	REF	
VTT0	J13	REF	
VTT0	J14	REF	
VTT0	J15	REF	
VTT0	J16	REF	
VTT0	K10	REF	
VTT0	L10	REF	
VTT0	N10	REF	
VTT0	P10	REF	
VTT0	T10	REF	
VTT0	U10	REF	
VTT0	W10	REF	
VTT0	Y10	REF	

Table 68. rPGA988A Processor Pin List by Pin Name

Pin Name	Pin Number	Buffer Type	Dir.
VTT1	E25	REF	
VTT1	E26	REF	
VTT1	F26	REF	
VTT1	G26	REF	
VTT1	G27	REF	
VTT1	G28	REF	
VTT1	H19	REF	
VTT1	H20	REF	
VTT1	H21	REF	
VTT1	H25	REF	
VTT1	H27	REF	
VTT1	J18	REF	
VTT1	J20	REF	
VTT1	J22	REF	
VTT1	J23	REF	
VTT1	J24	REF	
VTT1	J25	REF	
VTT1	J26	REF	
VTT1	J27	REF	
VTT1	K26	REF	
VTTPWRGOOD	AM15	Async CMOS	I

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
A2	KEY		
A3	RSVD_NCTF		
A4	SB_DQ[6]	DDR3	I/O
A5	SB_DQ[1]	DDR3	I/O
A6	SB_DQ[5]	DDR3	I/O
A7	SA_DQ[3]	DDR3	I/O
A8	SA_DQ[7]	DDR3	I/O
A9	VSS	GND	
A10	SA_DQ[0]	DDR3	I/O

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
A11	VTT0	REF	
A12	VTT0	REF	
A13	VTT0	REF	
A14	VTT0	REF	
A15	VSS_SENSE_VTT	Analog	O
A16	BCLK	DIFF CLK	I
A17	DPLL_REF_SSCLK#	DIFF CLK	I
A18	DPLL_REF_SSCLK	DIFF CLK	I
A19	RSVD		
A20	RSVD		
A21	DMI_RX#[3]	DMI	I
A22	DMI_RX[3]	DMI	I
A23	VSS	GND	
A24	DMI_RX#[0]	DMI	I
A25	PEG_RBIAS	Analog	I
A26	PEG_ICOMPO	Analog	I
A27	VSS	GND	
A28	PEG_RX[13]	PCIe	I
A29	VSS	GND	
A30	PEG_RX[15]	PCIe	I
A31	PEG_RX#[15]	PCIe	I
A32	PEG_RX[11]	PCIe	I
A33	RSVD_NCTF		
A34	RSVD_NCTF		
A35	VSS_NCTF		
AA1	RSVD_TP		
AA2	RSVD_TP		
AA3	SA_MA[3]	DDR3	O
AA4	RSVD_TP		
AA5	RSVD_TP		
AA6	SA_CK[0]	DDR3	O
AA7	SA_CK#[0]	DDR3	O
AA8	SA_MA[2]	DDR3	O
AA9	SA_MA[5]	DDR3	O

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AA10	VSS	GND	
AA26	VCC	REF	
AA27	VCC	REF	
AA28	VCC	REF	
AA29	VCC	REF	
AA30	VCC	REF	
AA31	VCC	REF	
AA32	VCC	REF	
AA33	VCC	REF	
AA34	VCC	REF	
AA35	VCC	REF	
AB1	SB_BS[0]	DDR3	O
AB2	SA_BS[1]	DDR3	O
AB3	SA_RAS#	DDR3	O
AB4	VDDQ	REF	
AB5	SB_MA[10]	DDR3	O
AB6	VSS	GND	
AB7	VDDQ	REF	
AB8	SB_CS#[0]	DDR3	O
AB9	RSVD		
AB10	VTT0	REF	
AB26	VSS	GND	
AB27	VSS	GND	
AB28	VSS	GND	
AB29	VSS	GND	
AB30	VSS	GND	
AB31	VSS	GND	
AB32	VSS	GND	
AB33	VSS	GND	
AB34	VSS	GND	
AB35	VSS	GND	
AC1	VDDQ	REF	
AC2	VSS	GND	
AC3	SA_BS[0]	DDR3	O
AC4	VSS	GND	
AC5	SB_CAS#	DDR3	O

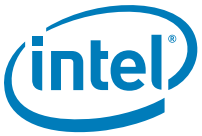


Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AC6	SB_WE#	DDR3	O
AC7	SB_ODT[0]	DDR3	O
AC8	VSS	GND	
AC9	RSVD		
AC10	VTT0	REF	
AC26	VCC	REF	
AC27	VCC	REF	
AC28	VCC	REF	
AC29	VCC	REF	
AC30	VCC	REF	
AC31	VCC	REF	
AC32	VCC	REF	
AC33	VCC	REF	
AC34	VCC	REF	
AC35	VCC	REF	
AD1	SB_ODT[1]	DDR3	O
AD2	RSVD_TP		
AD3	RSVD_TP		
AD4	SA_MA[10]	DDR3	O
AD5	RSVD_TP		
AD6	SB_CS#[1]	DDR3	O
AD7	RSVD_TP		
AD8	SA_ODT[0]	DDR3	O
AD9	RSVD_TP		
AD10	VSS	GND	
AD26	VCC	REF	
AD27	VCC	REF	
AD28	VCC	REF	
AD29	VCC	REF	
AD30	VCC	REF	
AD31	VCC	REF	
AD32	VCC	REF	
AD33	VCC	REF	
AD34	VCC	REF	
AD35	VCC	REF	
AE1	SA_CAS#	DDR3	O

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AE2	SA_CS#[0]	DDR3	O
AE3	RSVD_TP		
AE4	VDDQ	REF	
AE5	RSVD_TP		
AE6	VSS	GND	
AE7	VDDQ	REF	
AE8	SA_CS#[1]	DDR3	O
AE9	SA_WE#	DDR3	O
AE10	VTT0	REF	
AE26	VSS	GND	
AE27	VSS	GND	
AE28	VSS	GND	
AE29	VSS	GND	
AE30	VSS	GND	
AE31	VSS	GND	
AE32	VSS	GND	
AE33	VSS	GND	
AE34	VSS	GND	
AE35	VSS	GND	
AF1	VDDQ	REF	
AF2	VSS	GND	
AF3	SB_DQ[32]	DDR3	I/O
AF4	VSS	GND	
AF5	SA_DQ[33]	DDR3	I/O
AF6	SA_DQ[36]	DDR3	I/O
AF7	SB_MA[13]	DDR3	O
AF8	VSS	GND	
AF9	SA_ODT[1]	DDR3	O
AF10	VTT0	REF	
AF26	VCC	REF	
AF27	VCC	REF	
AF28	VCC	REF	
AF29	VCC	REF	
AF30	VCC	REF	
AF31	VCC	REF	
AF32	VCC	REF	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AF33	VCC	REF	
AF34	VCC	REF	
AF35	VCC	REF	
AG1	SB_DQ[33]	DDR3	I/O
AG2	SB_DQS[4]	DDR3	I/O
AG3	SB_DQ[37]	DDR3	I/O
AG4	SB_DQ[36]	DDR3	I/O
AG5	SA_DQ[37]	DDR3	I/O
AG6	SA_DM[4]	DDR3	O
AG7	RSVD_TP		
AG8	SA_MA[13]	DDR3	O
AG9	RSVD		
AG10	VSS	GND	
AG26	VCC	REF	
AG27	VCC	REF	
AG28	VCC	REF	
AG29	VCC	REF	
AG30	VCC	REF	
AG31	VCC	REF	
AG32	VCC	REF	
AG33	VCC	REF	
AG34	VCC	REF	
AG35	VCC	REF	
AH1	SB_DM[4]	DDR3	O
AH2	SB_DQS#[4]	DDR3	I/O
AH3	VSS	GND	
AH4	SB_DQ[39]	DDR3	I/O
AH5	SA_DQ[32]	DDR3	I/O
AH6	VSS	GND	
AH7	SA_DQS#[4]	DDR3	I/O
AH8	SA_DQS[4]	DDR3	I/O
AH9	VSS	GND	
AH10	VTT0	REF	
AH11	VTT0	REF	
AH12	VTT0	REF	
AH13	VSS	GND	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AH14	VTT0	REF	
AH15	RSVD		
AH16	VAXG	REF	
AH17	VSS	GND	
AH18	VAXG	REF	
AH19	VAXG	REF	
AH20	VSS	GND	
AH21	VAXG	REF	
AH22	BPM#[5]	GTL	I/O
AH23	BPM#[7]	GTL	I/O
AH24	SKTOCC#		
AH25	RSVD		
AH26	VSS	GND	
AH27	VSS	GND	
AH28	VSS	GND	
AH29	VSS	GND	
AH30	VSS	GND	
AH31	VSS	GND	
AH32	VSS	GND	
AH33	VSS	GND	
AH34	VSS	GND	
AH35	VSS	GND	
AJ1	VDDQ	REF	
AJ2	VSS	GND	
AJ3	SB_DQ[34]	DDR3	I/O
AJ4	SB_DQ[38]	DDR3	I/O
AJ5	VSS	GND	
AJ6	SA_DQ[39]	DDR3	I/O
AJ7	SA_DQ[38]	DDR3	I/O
AJ8	VSS	GND	
AJ9	SA_DQ[41]	DDR3	I/O
AJ10	SA_DQ[40]	DDR3	I/O
AJ11	VSS	GND	
AJ12	RSVD_TP		
AJ13	RSVD_TP		
AJ14	VSS	GND	

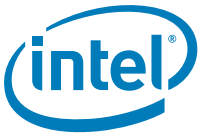


Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AJ15	RSVD		
AJ16	VAXG	REF	
AJ17	VSS	GND	
AJ18	VAXG	REF	
AJ19	VAXG	REF	
AJ20	VSS	GND	
AJ21	VAXG	REF	
AJ22	BPM#[0]	GTL	I/O
AJ23	VSS	GND	
AJ24	BPM#[3]	GTL	I/O
AJ25	BPM#[4]	GTL	I/O
AJ26	RSVD		
AJ27	RSVD		
AJ28	CFG[11]	CMOS	I
AJ29	CFG[15]	CMOS	I
AJ30	CFG[16]	CMOS	I
AJ31	VSS	GND	
AJ32	CFG[14]	CMOS	I
AJ33	RSVD		
AJ34	VCC_SENSE	Analog	O
AJ35	VSS_SENSE	Analog	O
AK1	SB_DQ[35]	DDR3	I/O
AK2	SB_DQ[45]	DDR3	I/O
AK3	SB_DQ[40]	DDR3	I/O
AK4	SB_DQ[41]	DDR3	I/O
AK5	SB_DQ[44]	DDR3	I/O
AK6	SA_DQ[34]	DDR3	I/O
AK7	SA_DQ[35]	DDR3	I/O
AK8	SA_DQ[44]	DDR3	I/O
AK9	SA_DQS#[5]	DDR3	I/O
AK10	SA_DQS[5]	DDR3	I/O
AK11	SA_DQ[46]	DDR3	I/O
AK12	SA_DQ[43]	DDR3	I/O
AK13	SM_DRAMPWROK	DDR3	O
AK14	CATERR#	GTL	I/O
AK15	THERMTRIP#	Async GTL	O

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AK16	VAXG	REF	
AK17	VSS	GND	
AK18	VAXG	REF	
AK19	VAXG	REF	
AK20	VSS	GND	
AK21	VAXG	REF	
AK22	BPM#[1]	GTL	I/O
AK23	BPM#[6]	GTL	I/O
AK24	BPM#[2]	GTL	I/O
AK25	VSS	GND	
AK26	RSVD_TP		
AK27	VSS	GND	
AK28	CFG[10]	CMOS	I
AK29	VSS	GND	
AK30	CFG[17]	CMOS	I
AK31	CFG[9]	CMOS	I
AK32	CFG[8]	CMOS	I
AK33	VID[1]	CMOS	O
AK34	VID[2]	CMOS	O
AK35	VID[0]	CMOS	O
AL1	SM_RCOMP[0]	Analog	I
AL2	SB_DM[5]	DDR3	O
AL3	VSS	GND	
AL4	SB_DQS#[5]	DDR3	I/O
AL5	SB_DQS[5]	DDR3	I/O
AL6	VSS	GND	
AL7	SA_DQ[45]	DDR3	I/O
AL8	SA_DQ[47]	DDR3	I/O
AL9	VSS	GND	
AL10	SA_DQ[42]	DDR3	I/O
AL11	SA_DQ[51]	DDR3	I/O
AL12	VSS	GND	
AL13	SA_DQ[61]	DDR3	I/O
AL14	RSTIN#	CMOS	I
AL15	PM_SYNC	CMOS	I
AL16	VAXG	REF	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AL17	VSS	GND	
AL18	VAXG	REF	
AL19	VAXG	REF	
AL20	VSS	GND	
AL21	VAXG	REF	
AL22	RSVD		
AL23	VSS	GND	
AL24	RSVD		
AL25	RSVD		
AL26	RSVD_TP		
AL27	RSVD		
AL28	RSVD		
AL29	RSVD		
AL30	CFG[4]	CMOS	I
AL31	VSS	GND	
AL32	CFG[3]	CMOS	I
AL33	CSC[1]/VID[4]	CMOS	I/O
AL34	VSS	GND	
AL35	CSC[0]/VID[3]	CMOS	I/O
AM1	SM_RCOMP[1]	Analog	I
AM2	VSS	GND	
AM3	SB_DQ[47]	DDR3	I/O
AM4	SB_DQ[46]	DDR3	I/O
AM5	VSS	GND	
AM6	SB_DQ[42]	DDR3	I/O
AM7	SA_DM[5]	DDR3	O
AM8	VSS	GND	
AM9	SA_DQ[52]	DDR3	I/O
AM10	SA_DQ[49]	DDR3	I/O
AM11	VSS	GND	
AM12	SA_DQ[56]	DDR3	I/O
AM13	SA_DQ[58]	DDR3	I/O
AM14	VSS	GND	
AM15	VTTPWRGOOD	Async CMOS	I
AM16	VAXG	REF	
AM17	VSS	GND	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AM18	VAXG	REF	
AM19	VAXG	REF	
AM20	VSS	GND	
AM21	VAXG	REF	
AM22	GFX_VID[0]	CMOS	O
AM23	GFX_VID[4]	CMOS	O
AM24	GFX_IMON	Analog	I
AM25	VSS	GND	
AM26	TAPPWRGOOD	Async CMOS	O
AM27	VSS	GND	
AM28	CFG[1]	CMOS	I
AM29	VSS	GND	
AM30	CFG[0]	CMOS	I
AM31	CFG[5]	CMOS	I
AM32	CFG[7]	CMOS	I
AM33	CSC[2]/VID[5]	CMOS	I/O
AM34	PROC_DPRSLPVR	CMOS	O
AM35	VID[6]	CMOS	O
AN1	SM_RCOMP[2]	Analog	I
AN2	SB_DQ[43]	DDR3	I/O
AN3	SB_DQ[53]	DDR3	I/O
AN4	SB_DQ[52]	DDR3	I/O
AN5	SB_DQ[49]	DDR3	I/O
AN6	SB_DQ[51]	DDR3	I/O
AN7	SB_DQ[56]	DDR3	I/O
AN8	SA_DQ[48]	DDR3	I/O
AN9	SA_DQ[53]	DDR3	I/O
AN10	SA_DM[6]	DDR3	O
AN11	SA_DQS[6]	DDR3	I/O
AN12	SA_DQ[57]	DDR3	I/O
AN13	SA_DM[7]	DDR3	O
AN14	VCCPWRGOOD_1	Async CMOS	I
AN15	PM_EXT_TS#[0]	CMOS	I
AN16	VAXG	REF	
AN17	VSS	GND	

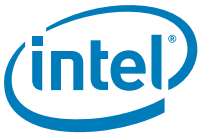


Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AN18	VAXG	REF	
AN19	VAXG	REF	
AN20	VSS	GND	
AN21	VAXG	REF	
AN22	GFX_VID[2]	CMOS	O
AN23	VSS	GND	
AN24	GFX_VID[6]	CMOS	O
AN25	DBR#		O
AN26	PROCHOT#	Async GTL	I/O
AN27	VCCPWRGOOD_0	Async CMOS	I
AN28	TCK	CMOS	I
AN29	CFG[6]	CMOS	I
AN30	CFG[12]	CMOS	I
AN31	VSS	GND	
AN32	CFG[13]	CMOS	I
AN33	PSI#	Async CMOS	O
AN34	VSS	GND	
AN35	ISENSE	Analog	I
AP1	RSVD_NCTF		
AP2	VSS	GND	
AP3	SB_DQ[48]	DDR3	I/O
AP4	VSS	GND	
AP4	VSS	GND	
AP5	SB_DQS[6]	DDR3	I/O
AP6	SB_DQ[57]	DDR3	I/O
AP7	VSS	GND	
AP8	SB_DQ[58]	DDR3	I/O
AP9	SB_DQ[61]	DDR3	I/O
AP10	VSS	GND	
AP11	SA_DQS#[6]	DDR3	I/O
AP12	SA_DQ[55]	DDR3	I/O
AP13	VSS	GND	
AP14	SA_DQ[63]	DDR3	I/O
AP15	PM_EXT_TS#[1]	CMOS	I

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AP16	VAXG	REF	
AP17	VSS	GND	
AP18	VAXG	REF	
AP19	VAXG	REF	
AP20	VSS	GND	
AP21	VAXG	REF	
AP22	GFX_VID[1]	CMOS	O
AP23	GFX_VID[3]	CMOS	O
AP24	GFX_VID[5]	CMOS	O
AP25	RSVD		
AP26	RESET_OBS#	Async CMOS	O
AP27	PREQ#	Async GTL	I
AP28	TMS	CMOS	I
AP29	TDO_M	CMOS	O
AP30	RSVD		
AP31	CFG[2]	CMOS	I
AP32	RSVD		
AP33	RSVD		
AP34	VSS	GND	
AP35	RSVD_NCTF		
AR1	RSVD_NCTF		
AR2	RSVD_NCTF		
AR3	VSS	GND	
AR4	SB_DM[6]	DDR3	O
AR5	SB_DQS#[6]	DDR3	I/O
AR6	VSS	GND	
AR7	SB_DQS[7]	DDR3	I/O
AR8	SB_DQS#[7]	DDR3	I/O
AR9	VSS	GND	
AR10	SB_DQ[62]	DDR3	I/O
AR11	SA_DQ[50]	DDR3	I/O
AR12	VSS	GND	
AR13	SA_DQS[7]	DDR3	I/O
AR14	SA_DQ[62]	DDR3	I/O
AR15	VSS	GND	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AR16	VAXG	REF	
AR17	VSS	GND	
AR18	VAXG	REF	
AR19	VAXG	REF	
AR20	VSS	GND	
AR21	VAXG	REF	
AR22	VAXG_SENSE	Analog	O
AR23	VSS	GND	
AR24	VSS	GND	
AR25	GFX_VR_EN	CMOS	O
AR26	VSS	GND	
AR27	TDO	CMOS	O
AR28	VSS	GND	
AR29	TDI_M	CMOS	I
AR30	BCLK_ITP	DIFF CLK	O
AR31	VSS	GND	
AR32	RSVD		
AR33	RSVD		
AR34	VSS_NCTF		
AR35	RSVD_NCTF		
AT1	VSS_NCTF		
AT2	RSVD_TP		
AT3	RSVD_NCTF		
AT4	SB_DQ[50]	DDR3	I/O
AT5	SB_DQ[54]	DDR3	I/O
AT6	SB_DQ[55]	DDR3	I/O
AT7	SB_DQ[60]	DDR3	I/O
AT8	SB_DM[7]	DDR3	O
AT9	SB_DQ[59]	DDR3	I/O
AT10	SB_DQ[63]	DDR3	I/O
AT11	SA_DQ[54]	DDR3	I/O
AT12	SA_DQ[60]	DDR3	I/O
AT13	SA_DQS#[7]	DDR3	I/O
AT14	SA_DQ[59]	DDR3	I/O
AT15	PECI	Async	I/O
AT16	VAXG	REF	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
AT17	VSS	GND	
AT18	VAXG	REF	
AT19	VAXG	REF	
AT20	VSS	GND	
AT21	VAXG	REF	
AT22	VSSAXG_SENSE	Analog	O
AT23	COMP3	Analog	I
AT24	COMP2	Analog	I
AT25	GFX_DPRSLPVR	CMOS	O
AT26	COMP0	Analog	I
AT27	TRST#	CMOS	I
AT28	PRDY#	Async GTL	O
AT29	TDI	CMOS	I
AT30	BCLK_ITP#	DIFF CLK	O
AT31	RSVD		
AT32	RSVD		
AT33	RSVD_NCTF		
AT34	RSVD_NCTF		
AT35	VSS_NCTF		
B1	VSS_NCTF		
B2	VSS_NCTF		
B3	SB_DQ[3]	DDR3	I/O
B4	VSS	GND	
B5	SB_DQ[0]	DDR3	I/O
B6	VSS	GND	
B7	SA_DQ[13]	DDR3	I/O
B8	VSS	GND	
B9	SA_DM[0]	DDR3	O
B10	SA_DQ[4]	DDR3	I/O
B11	VSS	GND	
B12	VTT0	REF	
B13	VSS	GND	
B14	VTT0	REF	
B15	VTT_SENSE	Analog	O

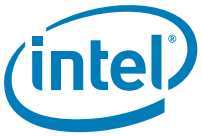


Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
B16	BCLK#	DIFF CLK	I
B17	VSS	GND	
B18	VSS	GND	
B19	RSVD		
B20	RSVD		
B21	VSS	GND	
B22	DMI_RX#[2]	DMI	I
B23	DMI_RX[2]	DMI	I
B24	DMI_RX[0]	DMI	I
B25	VSS	GND	
B26	PEG_ICOMPI	Analog	I
B27	PEG_RCOMPO	Analog	I
B28	PEG_RX#[13]	PCIe	I
B29	PEG_RX[14]	PCIe	I
B30	PEG_RX#[14]	PCIe	I
B31	VSS	GND	
B32	PEG_RX#[11]	PCIe	I
B33	PEG_RX[9]	PCIe	I
B34	VSS_NCTF		
B35	RSVD_NCTF		
C1	RSVD_NCTF		
C2	SB_DQ[12]	DDR3	I/O
C3	SB_DQ[2]	DDR3	I/O
C4	SB_DQ[7]	DDR3	I/O
C5	SB_DQS[0]	DDR3	I/O
C6	SA_DQ[15]	DDR3	I/O
C7	SA_DQ[2]	DDR3	I/O
C8	SA_DQS[0]	DDR3	I/O
C9	SA_DQS#[0]	DDR3	I/O
C10	SA_DQ[1]	DDR3	I/O
C11	VTT0	REF	
C12	VTT0	REF	
C13	VTT0	REF	
C14	VTT0	REF	
C15	RSVD		
C16	VSS	GND	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
C17	FDI_INT	CMOS	I
C18	FDI_TX[3]	FDI	O
C19	VSS	GND	
C20	VSS	GND	
C21	FDI_TX[1]	FDI	O
C22	VSS	GND	
C23	DMI_RX#[1]	DMI	I
C24	VSS	GND	
C25	PEG_TX[15]	PCIe	O
C26	PEG_TX#[15]	PCIe	O
C27	PEG_TX[14]	PCIe	O
C28	VSS	GND	
C29	VSS	GND	
C30	PEG_RX[12]	PCIe	I
C31	PEG_RX#[12]	PCIe	I
C32	VSS	GND	
C33	PEG_RX#[9]	PCIe	I
C34	VSS	GND	
C35	RSVD_NCTF		
D1	SB_DQ[8]	DDR3	I/O
D2	SB_DQ[9]	DDR3	I/O
D3	VSS	GND	
D4	SB_DM[0]	DDR3	O
D5	SB_DQS#[0]	DDR3	I/O
D6	VSS	GND	
D7	SA_DM[1]	DDR3	O
D8	SA_DQ[8]	DDR3	I/O
D9	VSS	GND	
D10	SA_DQ[5]	DDR3	I/O
D11	VTT0	REF	
D12	VTT0	REF	
D13	VTT0	REF	
D14	VTT0	REF	
D15	RSVD		
D16	PEG_CLK#	DIFF CLK	I
D17	FDI_LSYNC[1]	CMOS	I

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
D18	FDI_TX#[3]	FDI	O
D19	FDI_TX#[2]	FDI	O
D20	FDI_TX[2]	FDI	O
D21	FDI_TX#[1]	FDI	O
D22	FDI_TX[0]	FDI	O
D23	DMI_RX[1]	DMI	I
D24	DMI_TX#[0]	DMI	O
D25	DMI_TX[0]	DMI	O
D26	VSS	GND	
D27	PEG_TX#[14]	PCIe	O
D28	PEG_TX[13]	PCIe	O
D29	PEG_TX#[13]	PCIe	O
D30	VSS	GND	
D31	PEG_RX[10]	PCIe	I
D32	PEG_RX#[10]	PCIe	I
D33	VSS	GND	
D34	PEG_RX[7]	PCIe	I
D35	PEG_RX#[7]	PCIe	I
E1	SB_DM[1]	DDR3	O
E2	VSS	GND	
E3	SB_DQS[1]	DDR3	I/O
E4	SB_DQ[4]	DDR3	I/O
E5	VSS	GND	
E6	SA_DQ[10]	DDR3	I/O
E7	SA_DQ[14]	DDR3	I/O
E8	VSS	GND	
E9	SA_DQ[12]	DDR3	I/O
E10	SA_DQ[6]	DDR3	I/O
E11	VSS	GND	
E12	VTT0	REF	
E13	VSS	GND	
E14	VTT0	REF	
E15	RSVD_TP		
E16	PEG_CLK	DIFF CLK	I
E17	FDI_FSYNC[1]	CMOS	I
E18	VSS	GND	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
E19	FDI_TX#[5]	FDI	O
E20	FDI_TX[5]	FDI	O
E21	VSS	GND	
E22	FDI_TX#[0]	FDI	O
E23	DMI_TX[2]	DMI	O
E24	VSS	GND	
E25	VTT1	REF	
E26	VTT1	REF	
E27	PEG_TX[12]	PCIe	O
E28	PEG_TX#[12]	PCIe	O
E29	VSS	GND	
E30	RSVD		
E31	RSVD		
E32	VSS	GND	
E33	PEG_RX#[8]	PCIe	I
E34	PEG_RX[5]	PCIe	I
E35	VSS	GND	
F1	SB_DQ[11]	DDR3	I/O
F2	SB_DQ[10]	DDR3	I/O
F3	SB_DQ[14]	DDR3	I/O
F4	SB_DQS#[1]	DDR3	I/O
F5	SB_DQ[13]	DDR3	I/O
F6	SM_DRAMRST#	DDR3	O
F7	SA_DQ[11]	DDR3	I/O
F8	SA_DQS#[1]	DDR3	I/O
F9	SA_DQS[1]	DDR3	I/O
F10	SA_DQ[9]	DDR3	I/O
F11	VTT0	REF	
F12	VTT0	REF	
F13	VTT0	REF	
F14	VTT0	REF	
F15	RSVD_TP		
F16	VSS	GND	
F17	FDI_FSYNC[0]	CMOS	I
F18	FDI_LSYNC[0]	CMOS	I
F19	VSS	GND	

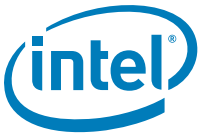


Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
F20	FDI_TX[6]	FDI	O
F21	FDI_TX#[6]	FDI	O
F22	VSS	GND	
F23	DMI_TX#[2]	DMI	O
F24	DMI_TX[1]	DMI	O
F25	VSS	GND	
F26	VTT1	REF	
F27	VSS	GND	
F28	PEG_TX[11]	PCIe	O
F29	PEG_TX#[11]	PCIe	O
F30	VSS	GND	
F31	PEG_RX#[6]	PCIe	I
F32	PEG_RX[6]	PCIe	I
F33	PEG_RX[8]	PCIe	I
F34	PEG_RX#[5]	PCIe	I
F35	PEG_RX[3]	PCIe	I
G1	SB_DQ[20]	DDR3	I/O
G2	SB_DQ[17]	DDR3	I/O
G3	VSS	GND	
G4	SB_DQ[15]	DDR3	I/O
G5	SB_DQ[21]	DDR3	I/O
G6	VSS	GND	
G7	SA_DQ[20]	DDR3	I/O
G8	SA_DQ[17]	DDR3	I/O
G9	VSS	GND	
G10	SA_DQ[21]	DDR3	I/O
G11	VTT0	REF	
G12	VTT0	REF	
G13	VTT0	REF	
G14	VTT0	REF	
G15	VTT_SELECT	CMOS	O
G16	COMP1	Analog	I
G17	RSVD		
G18	FDI_TX#[7]	FDI	O
G19	FDI_TX[7]	FDI	O
G20	VSS	GND	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
G21	FDI_TX#[4]	FDI	O
G22	FDI_TX[4]	FDI	O
G23	DMI_TX[3]	DMI	O
G24	DMI_TX#[1]	DMI	O
G25	RSVD		
G26	VTT1	REF	
G27	VTT1	REF	
G28	VTT1	REF	
G29	PEG_TX[10]	PCIe	O
G30	PEG_TX[9]	PCIe	O
G31	VSS	GND	
G32	PEG_RX#[4]	PCIe	I
G33	PEG_RX[4]	PCIe	I
G34	VSS	GND	
G35	PEG_RX#[3]	PCIe	I
H1	VDDQ	REF	
H2	VSS	GND	
H3	SB_DM[2]	DDR3	O
H4	SB_DQS[2]	DDR3	I/O
H5	VSS	GND	
H6	SB_DQ[16]	DDR3	I/O
H7	SA_DM[2]	DDR3	O
H8	VSS	GND	
H9	SA_DQS[2]	DDR3	I/O
H10	SA_DQ[16]	DDR3	I/O
H11	VSS	GND	
H12	VTT0	REF	
H13	VSS	GND	
H14	VTT0	REF	
H15	VSS	GND	
H16	RSVD_TP		
H17	RSVD		
H18	VSS	GND	
H19	VTT1	REF	
H20	VTT1	REF	
H21	VTT1	REF	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
H22	VSS	GND	
H23	DMI_TX#[3]	DMI	O
H24	VSS	GND	
H25	VTT1	REF	
H26	VSS	GND	
H27	VTT1	REF	
H28	VSS	GND	
H29	PEG_TX#[10]	PCIe	O
H30	PEG_TX#[9]	PCIe	O
H31	PEG_TX[7]	PCIe	O
H32	VSS	GND	
H33	PEG_RX[2]	PCIe	I
H34	PEG_RX[1]	PCIe	I
H35	VSS	GND	
J1	SB_DQ[23]	DDR3	I/O
J2	SB_DQ[22]	DDR3	I/O
J3	SB_DQ[19]	DDR3	I/O
J4	SB_DQS#[2]	DDR3	I/O
J5	SB_DQ[24]	DDR3	I/O
J6	SB_DQ[18]	DDR3	I/O
J7	SA_DQ[22]	DDR3	I/O
J8	SA_DQ[19]	DDR3	I/O
J9	SA_DQS#[2]	DDR3	I/O
J10	SA_DQ[23]	DDR3	I/O
J11	VTT0	REF	
J12	VTT0	REF	
J13	VTT0	REF	
J14	VTT0	REF	
J15	VTT0	REF	
J16	VTT0	REF	
J17	RSVD		
J18	VTT1	REF	
J19	VSS	GND	
J20	VTT1	REF	
J21	VSS	GND	
J22	VTT1	REF	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
J23	VTT1	REF	
J24	VTT1	REF	
J25	VTT1	REF	
J26	VTT1	REF	
J27	VTT1	REF	
J28	RSVD		
J29	RSVD		
J30	VSS	GND	
J31	PEG_TX#[7]	PCIe	O
J32	VSS	GND	
J33	PEG_RX#[2]	PCIe	I
J34	PEG_RX#[1]	PCIe	I
J35	PEG_RX[0]	PCIe	I
K1	SB_DM[3]	DDR3	O
K2	SB_DQ[25]	DDR3	I/O
K3	VSS	GND	
K4	SB_DQ[29]	DDR3	I/O
K5	SB_DQ[28]	DDR3	I/O
K6	VSS	GND	
K7	SA_DQ[18]	DDR3	I/O
K8	SA_DQ[29]	DDR3	I/O
K9	VSS	GND	
K10	VTT0	REF	
K26	VTT1	REF	
K27	VSS	GND	
K28	PEG_TX[8]	PCIe	O
K29	PEG_TX#[8]	PCIe	O
K30	VSS	GND	
K31	PEG_TX[5]	PCIe	O
K32	PEG_TX#[5]	PCIe	O
K33	VSS	GND	
K34	VSS	GND	
K35	PEG_RX#[0]	PCIe	I
L1	VDDQ	REF	
L2	VSS	GND	
L3	SB_DQ[26]	DDR3	I/O

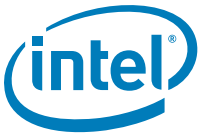


Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
L4	SB_DQS#[3]	DDR3	I/O
L5	VSS	GND	
L6	SA_DQ[28]	DDR3	I/O
L7	SA_DQ[24]	DDR3	I/O
L8	VSS	GND	
L9	SA_DQ[27]	DDR3	I/O
L10	VTT0	REF	
L26	VCCPLL	REF	
L27	VCCPLL	REF	
L28	RSVD		
L29	VSS	GND	
L30	PEG_TX[3]	PCIe	O
L31	PEG_TX#[4]	PCIe	O
L32	VSS	GND	
L33	PEG_TX#[0]	PCIe	O
L34	PEG_TX[0]	PCIe	O
L35	VSS	GND	
M1	SB_DQ[27]	DDR3	I/O
M2	SB_CKE[1]	DDR3	O
M3	SB_CKE[0]	DDR3	O
M4	SB_DQ[30]	DDR3	I/O
M5	SB_DQS[3]	DDR3	I/O
M6	SA_DQ[25]	DDR3	I/O
M7	SA_DM[3]	DDR3	O
M8	SA_DQ[26]	DDR3	I/O
M9	SA_DQS[3]	DDR3	I/O
M10	VSS	GND	
M26	VCCPLL	REF	
M27	RSVD		
M28	PEG_TX[6]	PCIe	O
M29	PEG_TX#[6]	PCIe	O
M30	PEG_TX#[3]	PCIe	O
M31	PEG_TX[4]	PCIe	O
M32	PEG_TX[2]	PCIe	O
M33	PEG_TX#[2]	PCIe	O
M34	PEG_TX[1]	PCIe	O

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
M35	PEG_TX#[1]	PCIe	O
N1	SB_MA[15]	DDR3	O
N2	RSVD_TP		
N3	RSVD_TP		
N4	VDDQ	REF	
N5	SB_DQ[31]	DDR3	I/O
N6	VSS	GND	
N7	VDDQ	REF	
N8	SA_DQ[30]	DDR3	I/O
N9	SA_DQS#[3]	DDR3	I/O
N10	VTT0	REF	
N26	VSS	GND	
N27	VSS	GND	
N28	VSS	GND	
N29	VSS	GND	
N30	VSS	GND	
N31	VSS	GND	
N32	VSS	GND	
N33	VSS	GND	
N34	VSS	GND	
N35	VSS	GND	
P1	VDDQ	REF	
P2	VSS	GND	
P3	SB_MA[11]	DDR3	O
P4	VSS	GND	
P5	SB_MA[14]	DDR3	O
P6	SA_CKE[1]	DDR3	O
P7	SA_CKE[0]	DDR3	O
P8	VSS	GND	
P9	SA_DQ[31]	DDR3	I/O
P10	VTT0	REF	
P26	VCC	REF	
P27	VCC	REF	
P28	VCC	REF	
P29	VCC	REF	
P30	VCC	REF	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
P31	VCC	REF	
P32	VCC	REF	
P33	VCC	REF	
P34	VCC	REF	
P35	VCC	REF	
R1	SB_MA[4]	DDR3	O
R2	SB_MA[6]	DDR3	O
R3	SB_MA[12]	DDR3	O
R4	SB_MA[8]	DDR3	O
R5	SB_MA[9]	DDR3	O
R6	SB_MA[7]	DDR3	O
R7	SB_BS[2]	DDR3	O
R8	RSVD_TP		
R9	RSVD_TP		
R10	VSS	GND	
R26	VCC	REF	
R27	VCC	REF	
R28	VCC	REF	
R29	VCC	REF	
R30	VCC	REF	
R31	VCC	REF	
R32	VCC	REF	
R33	VCC	REF	
R34	VCC	REF	
R35	VCC	REF	
T1	SA_MA[7]	DDR3	O
T2	SA_MA[11]	DDR3	O
T3	SA_MA[14]	DDR3	O
T4	VDDQ	REF	
T5	SB_MA[2]	DDR3	O
T6	VSS	GND	
T7	VDDQ	REF	
T8	SB_MA[5]	DDR3	O
T9	RSVD		
T10	VTT0	REF	
T26	VSS	GND	

Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
T27	VSS	GND	
T28	VSS	GND	
T29	VSS	GND	
T30	VSS	GND	
T31	VSS	GND	
T32	VSS	GND	
T33	VSS	GND	
T34	VSS	GND	
T35	VSS	GND	
U1	VDDQ	REF	
U2	VSS	GND	
U3	SA_MA[12]	DDR3	O
U4	VSS	GND	
U5	SB_MA[0]	DDR3	O
U6	SA_MA[9]	DDR3	O
U7	SA_BS[2]	DDR3	O
U8	VSS	GND	
U9	RSVD		
U10	VTT0	REF	
U26	VCC	REF	
U27	VCC	REF	
U28	VCC	REF	
U29	VCC	REF	
U30	VCC	REF	
U31	VCC	REF	
U32	VCC	REF	
U33	VCC	REF	
U34	VCC	REF	
U35	VCC	REF	
V1	SA_MA[4]	DDR3	O
V2	SB_MA[1]	DDR3	O
V3	SB_MA[3]	DDR3	O
V4	RSVD_TP		
V5	RSVD_TP		
V6	SB_CK#[1]	DDR3	O
V7	SB_CK[1]	DDR3	O

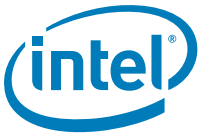


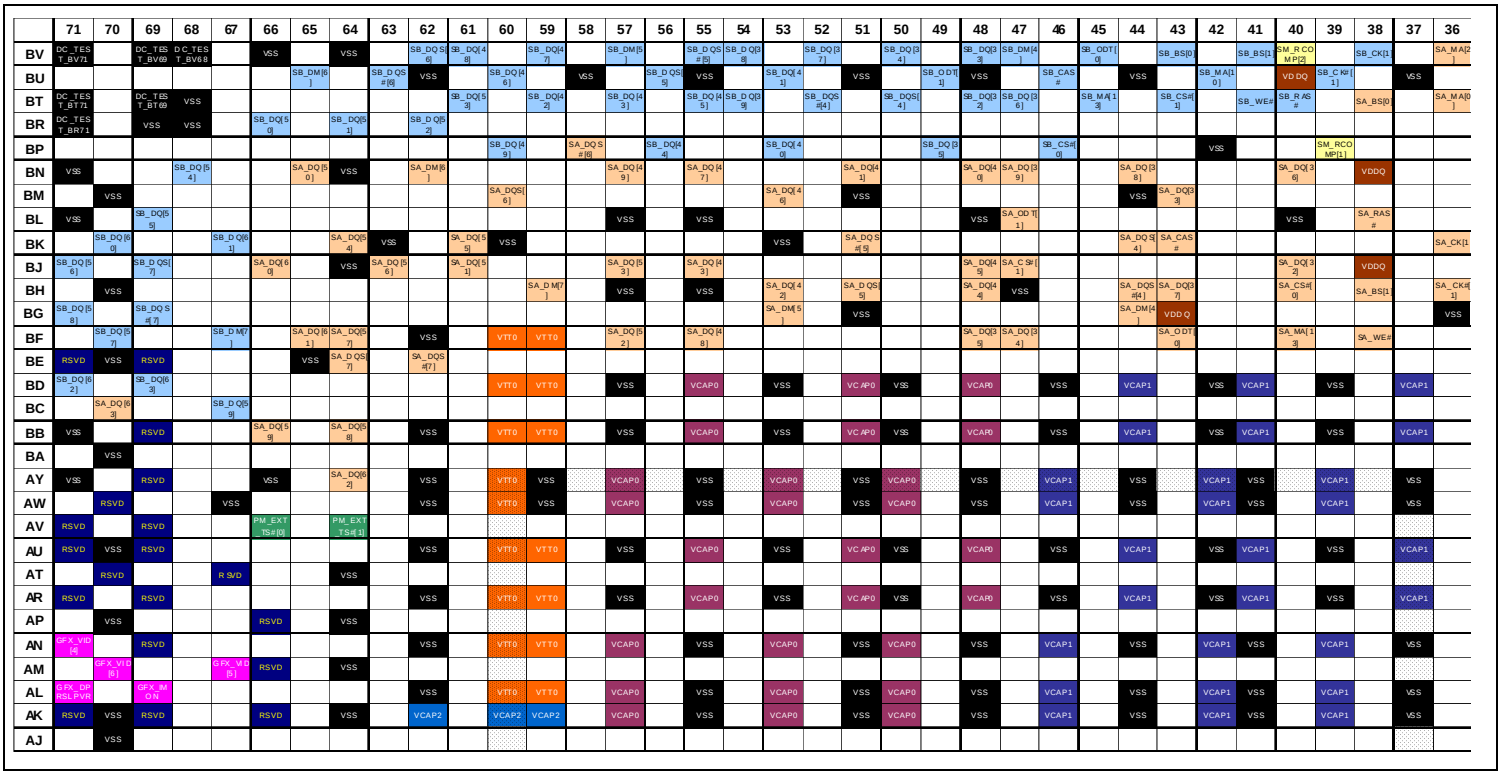
Table 69. rPGA988A Processor Pin List by Pin Number

Pin Number	Pin Name	Buffer Type	Dir.
V8	SA_MA[6]	DDR3	O
V9	SA_MA[15]	DDR3	O
V10	VSS	GND	
V26	VCC	REF	
V27	VCC	REF	
V28	VCC	REF	
V29	VCC	REF	
V30	VCC	REF	
V31	VCC	REF	
V32	VCC	REF	
V33	VCC	REF	
V34	VCC	REF	
V35	VCC	REF	
W1	SA_MA[1]	DDR3	O
W2	RSVD_TP		
W3	RSVD_TP		
W4	VDDQ	REF	
W5	SB_BS[1]	DDR3	O
W6	VSS	GND	
W7	VDDQ	REF	
W8	SB_CK[0]	DDR3	O
W9	SB_CK#[0]	DDR3	O
W10	VTT0	REF	
W26	VSS	GND	
W27	VSS	GND	
W28	VSS	GND	
W29	VSS	GND	
W30	VSS	GND	
W31	VSS	GND	
W32	VSS	GND	
W33	VSS	GND	
W34	VSS	GND	
W35	VSS	GND	
Y1	VDDQ	REF	
Y2	VSS	GND	
Y3	SA_MA[0]	DDR3	O

Table 69. rPGA988A Processor Pin List by Pin Number

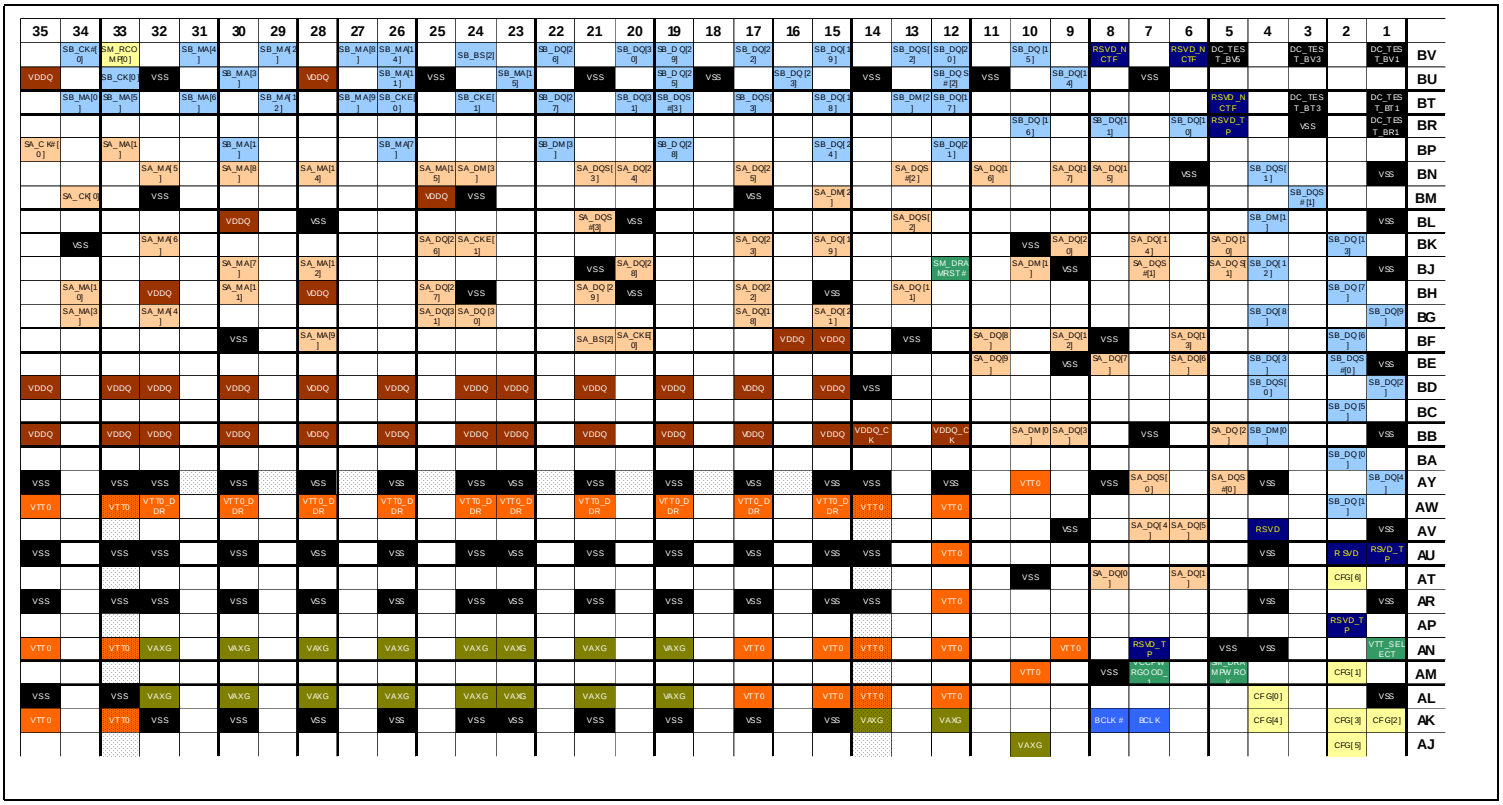
Pin Number	Pin Name	Buffer Type	Dir.
Y4	VSS	GND	
Y5	SA_CK#[1]	DDR3	O
Y6	SA_CK[1]	DDR3	O
Y7	SB_RAS#	DDR3	O
Y8	VSS	GND	
Y9	SA_MA[8]	DDR3	O
Y10	VTT0	REF	
Y26	VCC	REF	
Y27	VCC	REF	
Y28	VCC	REF	
Y29	VCC	REF	
Y30	VCC	REF	
Y31	VCC	REF	
Y32	VCC	REF	
Y33	VCC	REF	
Y34	VCC	REF	
Y35	VCC	REF	

Figure 34. BGA1288 Ballmap (Top View, Upper-Left Quadrant)



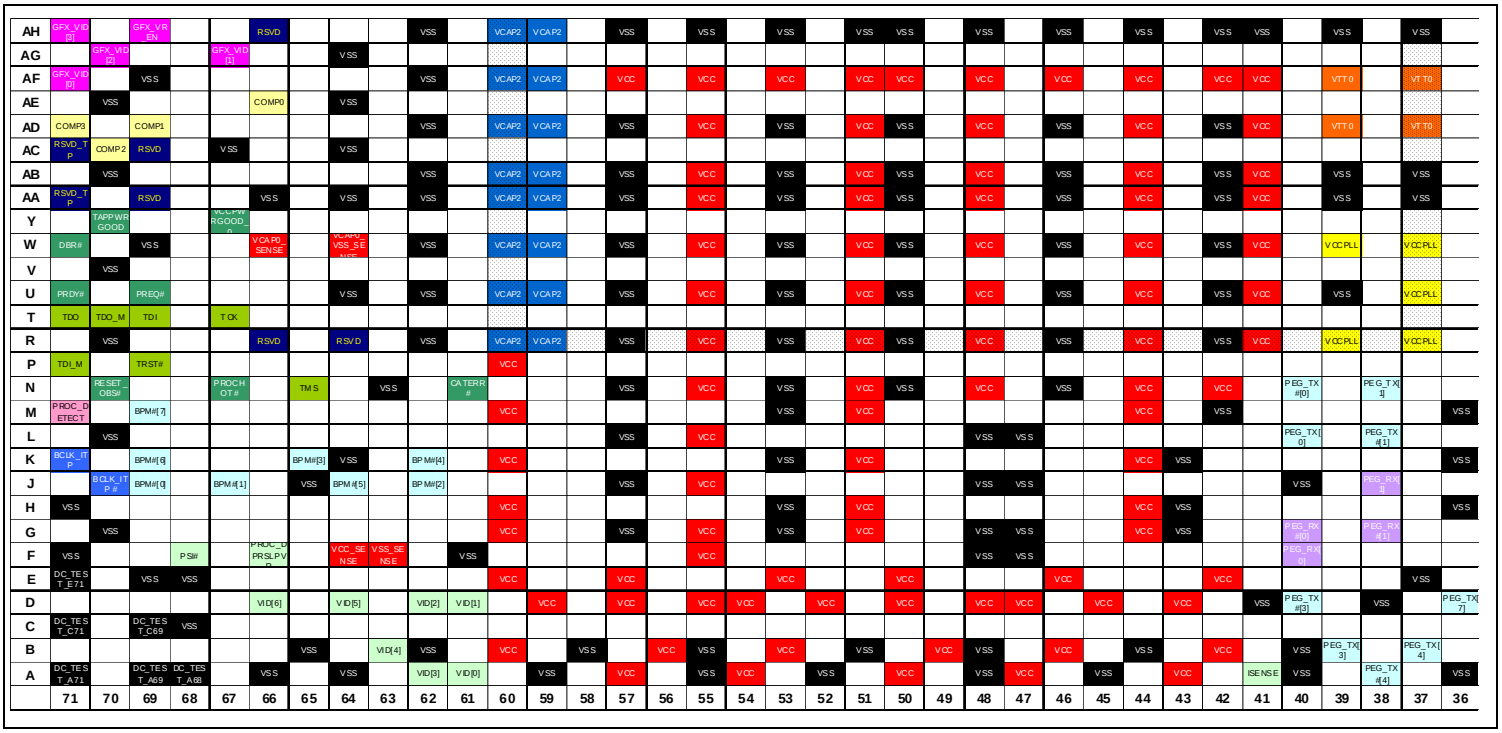
	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36
BV	DC_TEST_BV71		DC_TEST_BV69	DC_TEST_BV68		VSS		VSS		SB_DQS[6]	SB_DQ[48]		SB_DQ[47]		SB_DM[5]		SB_DQS#[5]			SB_DQ[37]		SB_DQ[34]		SB_DM[4]		SB_ODT[0]		SB_BS[0]		SB_BS[1]	SM_RCOMP[2]		SB_CK[1]		SA_MA[2]
BU							SB_DM[6]		SB_DQS#[6]	VSS		SB_DQ[46]		VSS		SB_DQS[5]	VSS		SB_DQ[41]		VSS		SB_ODT[1]	VSS		SB_CAS#		VSS		SB_MA[10]		VDDQ	SB_CK#[1]		VSS	
BT	DC_TEST_BT71		DC_TEST_BT69	VSS							SB_DQ[53]		SB_DQ[43]		SB_DQ[43]		SB_DQ[45]	SB_DQ[39]		SB_DQS#[4]		SB_DQS[4]		SB_DQ[36]		SB_MA[13]		SB_CS#[1]		SB_WE#	SB_RAS#		SA_BS[0]		SA_MA[0]
BR	DC_TEST_BR71		VSS	VSS		SB_DQ[50]		SB_DQ[51]		SB_DQS[2]																										
BP												SB_DQ[49]		SA_DQS#[6]		SB_DQ[44]			SB_DQ[40]				SB_DQ[33]		SB_CS#[0]			VSS			SM_RCOMP[1]				
BN	VSS			SB_DQ[54]			SA_DQ[50]	VSS		SA_DM[6]					SA_DQ[49]		SA_DQ[47]				SA_DQ[41]			SA_DQ[40]	SA_DQ[39]			SA_DQ[38]				SA_DQ[36]	VDDQ		
BM		VSS										SA_DQS[6]							SA_DQ[46]		VSS							VSS	SA_DQ[33]							
BL	VSS		SB_DQ[55]												VSS		VSS															VSS		SA_RAS#		
BK		SB_DQ[60]			SB_DQ[61]			SA_DQ[54]	VSS		SA_DQ[55]	VSS							VSS		SA_DQS#[5]						SA_DQ[34]	SA_CAS#							SA_CK[1]
BJ	SB_DQ[56]		SB_DQS[7]			SA_DQ[60]		VSS	SA_DQ[56]		SA_DQ[51]				SA_DQ[53]		SA_DQ[43]							SA_DQ[45]	SA_CS#[1]						SA_DQ[32]		VDDQ		
BH		VSS											SA_DM[7]		VSS		VSS		SA_DQ[42]		SA_DQS[5]			SA_DQ[44]	VSS			SA_DQS#[4]	SA_DQ[37]			SA_CS#[0]		SA_BS[1]		SA_CK#[1]
BG	SB_DQ[58]		SB_DQS#[7]																SA_DM[5]		VSS							SA_DM[4]	VDDQ							VSS
BF		SB_DQ[57]			SB_DM[7]		SA_DQ[61]	SA_DQS[7]		VSS		VTT0	VTT0		SA_DQ[52]		SA_DQ[48]							SA_DQ[35]	SA_DQ[34]				SA_ODT[0]			SA_MA[13]		SA_WE#		
BE	RSVD	VSS	RSVD				VSS	SA_DQS[7]		SA_DQS#[7]																										
BD	SB_DQ[62]		SB_DQ[63]									VTT0	VTT0		VSS		VCAP0		VSS		VCAP0	VSS		VCAP0		VSS		VCAP1		VSS	VCAP1		VSS		VCAP1	
BC		SA_DQ[63]			SB_DQ[59]																															
BB	VSS		RSVD			SA_DQ[59]		SA_DQ[58]		VSS		VTT0	VTT0		VSS		VCAP0		VSS		VCAP0	VSS		VCAP0		VSS		VCAP1		VSS	VCAP1		VSS		VCAP1	
BA		VSS																																		
AY	VSS		RSVD			VSS		SA_DQ[62]		VSS		VTT0	VSS		VCAP0		VSS		VCAP0		VSS	VCAP0		VSS		VCAP1		VSS		VCAP1	VSS		VCAP1		VSS	
AW		RSVD			VSS					VSS		VTT0	VSS		VCAP0		VSS		VCAP0		VSS	VCAP0		VSS		VCAP1		VSS		VCAP1	VSS		VCAP1		VSS	
AV	RSVD		RSVD			PM_EXTTS#[0]		PM_EXTTS#[1]																													
AU	RSVD	VSS	RSVD							VSS		VTT0	VTT0		VSS		VCAP0		VSS		VCAP0	VSS		VCAP0		VSS		VCAP1		VSS	VCAP1		VSS		VCAP1	
AT		RSVD			RSVD			VSS																												
AR	RSVD		RSVD							VSS		VTT0	VTT0		VSS		VCAP0		VSS		VCAP0	VSS		VCAP0		VSS		VCAP1		VSS	VCAP1		VSS		VCAP1	
AP		VSS				RSVD		VSS																												
AN	GFX_VID[4]		RSVD							VSS		VTT0	VTT0		VCAP0		VSS		VCAP0		VSS	VCAP0		VSS		VCAP1		VSS		VCAP1	VSS		VCAP1		VSS	
AM		GFX_VID[5]			GFX_VID[5]	RSVD		VSS																												
AL	GFX_DIS_RSLPVR		GFX_MON							VSS		VTT0	VTT0		VCAP0		VSS		VCAP0		VSS	VCAP0		VSS		VCAP1		VSS		VCAP1	VSS		VCAP1		VSS	
AK	RSVD	VSS	RSVD			RSVD		VSS		VCAP2		VCAP2	VCAP2		VCAP0		VSS		VCAP0		VSS	VCAP0		VSS		VCAP1		VSS		VCAP1	VSS		VCAP1		VSS	
AJ		VSS																																		

Figure 35. BGA1288 Ballmap (Top View, Upper-Right Quadrant)



35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
	SB_CK#[0]	SM_RCOMP[0]		SB_MA[4]		SB_MA[2]		SB_MA[8]	SB_MA[14]		SB_BS[2]		SB_DQ[26]		SB_DQ[30]	SB_DQ[29]		SB_DQ[22]		SB_DQ[19]		SB_DQS[2]	SB_DQS[20]		SB_DQ[15]		RSVD_NCTF		RSVD_NCTF	DC_TEST_BV5		DC_TEST_BV3		DC_TEST_BV1	BV
VDDQ		SB_CK[0]	VSS		SB_MA[3]		VDDQ		SB_MA[11]	VSS		SB_MA[15]		VSS		SB_DQ[25]	VSS		SB_DQ[23]		VSS		SB_DQS#[2]	VSS		SB_DQ[14]		VSS							BU
	SB_MA[0]	SB_MA[5]		SB_MA[6]		SB_MA[12]		SB_MA[9]	SB_CKE[0]		SB_CKE[1]		SB_DQ[27]		SB_DQ[31]	SB_DQS#[3]		SB_DQS[3]		SB_DQ[18]		SB_DM[2]	SB_DQ[17]				SB_DQ[11]		SB_DQ[10]	RSVD_NCTF		DC_TEST_BT3		DC_TEST_BT1	BT
																									SB_DQ[16]		SB_DQ[1]		SB_DQ[0]	RSVD_TP		VSS		DC_TEST_BR1	BR
SA_CK#[0]		SA_MA[1]			SB_MA[1]				SB_MA[7]				SB_DM[3]			SB_DQ[28]				SB_DQ[24]			SB_DQ[21]											BP
			SA_MA[5]		SA_MA[8]		SA_MA[14]			SA_MA[15]	SA_DM[3]			SA_DQS[33]	SA_DQ[24]			SA_DQ[25]				SA_DQS#[2]		SA_DQ[16]		SA_DQ[17]	SA_DQ[15]		VSS		SB_DQS[1]			VSS	BN
	SA_CK[0]		VSS							VDDQ	VSS							VSS		SA_DM[2]												SB_DQS#[1]			BM
					VDDQ		VSS							SA_DQS#[3]	VSS							SA_DQS[2]								SB_DM[1]			VSS	BL
	VSS		SA_MA[6]							SA_DQ[26]	SA_CKE[1]							SA_DQ[23]		SA_DQ[19]					VSS	SA_DQ[20]		SA_DQ[14]		SA_DQ[10]			SB_DQ[13]		BK
					SA_MA[7]		SA_MA[12]							VSS	SA_DQ[28]								SM_DRAMRST#		SA_DM[1]	VSS		SA_DQS#[1]		SA_DQ[9]	SB_DQ[12]			VSS	BJ
	SA_MA[10]		VDDQ		SA_MA[11]		VDDQ			SA_DQ[27]	VSS			SA_DQ[29]	VSS			SA_DQ[22]		VSS		SA_DQ[11]										SB_DQ[7]		BH
	SA_MA[3]		SA_MA[4]							SA_DQ[31]	SA_DQ[30]							SA_DQ[18]		SA_DQ[21]										SB_DQ[8]			SB_DQ[9]	BG
					VSS		SA_MA[9]							SA_BS[2]	SA_CKE[0]				VDDQ	VDDQ		VSS		SA_DQ[8]		SA_DQ[12]	VSS		SA_DQ[13]				SB_DQ[6]		BF
																								SA_DQ[9]		VSS	SA_DQ[7]		SA_DQ[5]		SB_DQ[3]		SB_DQS#[0]	VSS	BE
VDDQ		VDDQ	VDDQ		VDDQ		VDDQ		VDDQ		VDDQ	VDDQ		VDDQ		VDDQ		VDDQ		VDDQ	VSS										SB_DQS[0]		SB_DQ[2]	BD
																																SB_DQ[5]		BC
VDDQ		VDDQ	VDDQ		VDDQ		VDDQ		VDDQ		VDDQ	VDDQ		VDDQ		VDDQ		VDDQ		VDDQ	VDDQ_CK		VDDQ_CK		SA_DM[0]	SA_DQ[3]		VSS		SA_DQ[2]	SB_DM[0]		VSS	BB
																																SB_DQ[0]		BA
VSS		VSS	VSS		VSS		VSS		VSS		VSS	VSS		VSS		VSS		VSS		VSS	VSS		VSS		VTT0		VSS	SA_DQS[0]		SA_DQS#[0]	VSS			SB_DQ[4]	AY
VTT0		VTT0	VTT0_DDR		VTT0_DDR		VTT0_DDR		VTT0_DDR		VTT0_DDR	VTT0_DDR		VTT0_DDR		VTT0_DDR		VTT0_DDR		VTT0_DDR	VTT0		VTT0										SB_DQ[1]		AW
																										VSS		SA_DQ[4]	SA_DQ[5]		RSVD			VSS	AV
VSS		VSS	VSS		VSS		VSS		VSS		VSS	VSS		VSS		VSS		VSS		VSS	VSS		VTT0								VSS		RSVD	RSVD_TP	AU
																									VSS		SA_DQ[0]		SA_DQ[1]				CFG[6]		AT
VSS		VSS	VSS		VSS		VSS		VSS		VSS	VSS		VSS		VSS		VSS		VSS	VSS		VTT0								VSS			VSS	AR
																																	RSVD_TP		AP
VTT0		VTT0	VAXG		VAXG		VAXG		VAXG		VAXG	VAXG		VAXG		VAXG		VTT0		VTT0	VTT0		VTT0			VTT0		RSVD_TP		VSS	VSS			VTT_SELECT	AN
																									VTT0		VSS	RSVD_TP					CFG[1]		AM
VSS		VSS	VAXG		VAXG		VAXG		VAXG		VAXG	VAXG		VAXG		VAXG		VTT0		VTT0	VTT0		VTT0								CFG[0]			VSS	AL
VTT0		VTT0	VSS		VSS		VSS		VSS		VSS	VSS		VSS		VSS		VSS		VSS	VAXG		VAXG				BCLK#	BCLK			CFG[4]		CFG[3]	CFG[2]	AK
																									VAXG								CFG[5]		AJ

Figure 36. BGA1288 Ballmap (Top View, Lower-Left Quadrant)



	71	70	69	68	67	66	65	64	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36
AH	GFX_VID[0]		GFX_VR_EN			RSVD				VSS		VCAP2	VCAP2		VSS		VSS		VSS		VSS	VSS		VSS		VSS		VSS		VSS	VSS		VSS		VSS	
AG		GFX_VID[2]			GFX_VID[1]			VSS																												
AF	GFX_VID[0]		VSS							VSS		VCAP2	VCAP2		VCC		VCC		VCC		VCC	VCC		VCC		VCC		VCC		VCC	VCC		VTT0		VTT0	
AE		VSS				COMP0		VSS																												
AD	COMP3		COMP1							VSS		VCAP2	VCAP2		VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC		VSS	VCC		VTT0		VTT0	
AC	RSVD_TP	COMP2	RSVD		VSS			VSS																												
AB		VSS								VSS		VCAP2	VCAP2		VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC		VSS	VCC		VSS		VSS	
AA	RSVD_TP		RSVD			VSS		VSS		VSS		VCAP2	VCAP2		VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC		VSS	VCC		VSS		VSS	
Y		TAPPWRGOOD			VCCPWRGOOD_0																															
W	DBR#		VSS			VCAP0_SENSE		VCAP0_VSS_SENSE		VSS		VCAP2	VCAP2		VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC		VSS	VCC		VCCPLL		VCCPLL	
V		VSS																																		
U	PRDY#		PREQ#					VSS		VSS		VCAP2	VCAP2		VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC		VSS	VCC		VSS		VCCPLL	
T	TDO	TDO_M	TDI		TCK																															
R		VSS				RSVD		RSVD		VSS		VCAP2	VCAP2		VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC		VSS	VCC		VCCPLL		VCCPLL	
P	TDI_M		TRST#									VCC																								
N		RESET_OBS#			PROCHOT#		TMS		VSS		CATERR#				VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC		VCC		PEG_TX#[0]		PEG_TX[1]		
M	PROC_DETECT		BPM#[7]									VCC							VSS		VCC							VCC		VSS						VSS
L		VSS													VSS		VCC							VSS	VSS						PEG_TX[0]		PEG_TX#[1]		
K	BCLK_ITP		BPM#[6]				BPM#[3]	VSS		BPM#[4]		VCC							VSS		VCC							VCC	VSS							VSS
J		BCLK_ITP#	BPM#[3]		BPM#[1]		VSS	BPM#[5]		BPM#[2]					VSS		VCC							VSS	VSS						VSS		PEG_RX[1]			
H	VSS											VCC							VSS		VCC							VCC	VSS							VSS
G		VSS										VCC			VSS		VCC		VSS		VCC			VSS	VSS			VCC	VSS		PEG_RX#[0]		PEG_RX#[1]		
F	VSS			PSI#		PROC_DPRSLPVR		VCC_SENSE	VSS_SENSE		VSS						VCC							VSS	VSS						PEG_RX#[1]					
E	DC_TEST_E71		VSS	VSS								VCC			VCC				VCC			VCC				VCC				VCC					VSS	
D						VID[6]		VID[5]		VID[2]	VID[1]		VCC		VCC		VCC	VCC		VCC		VCC		VCC	VCC		VCC		VCC		VSS	PEG_TX#[3]		VSS		PEG_TX[7]
C	DC_TEST_C71		DC_TEST_C69	VSS																																
B							VSS		VID[4]	VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC	VSS		VCC		VSS		VCC		VSS	PEG_TX[3]		PEG_TX[4]	
A	DC_TEST_A71		DC_TEST_A69	DC_TEST_A68		VSS		VSS		VID[3]	VID[0]		VSS		VCC		VSS	VCC		VSS		VCC		VSS	VCC		VSS		VCC	ISENSE	VSS		PEG_TX#[4]		VSS

Figure 37. BGA1288 Ballmap (Top View, Lower-Right Quadrant)

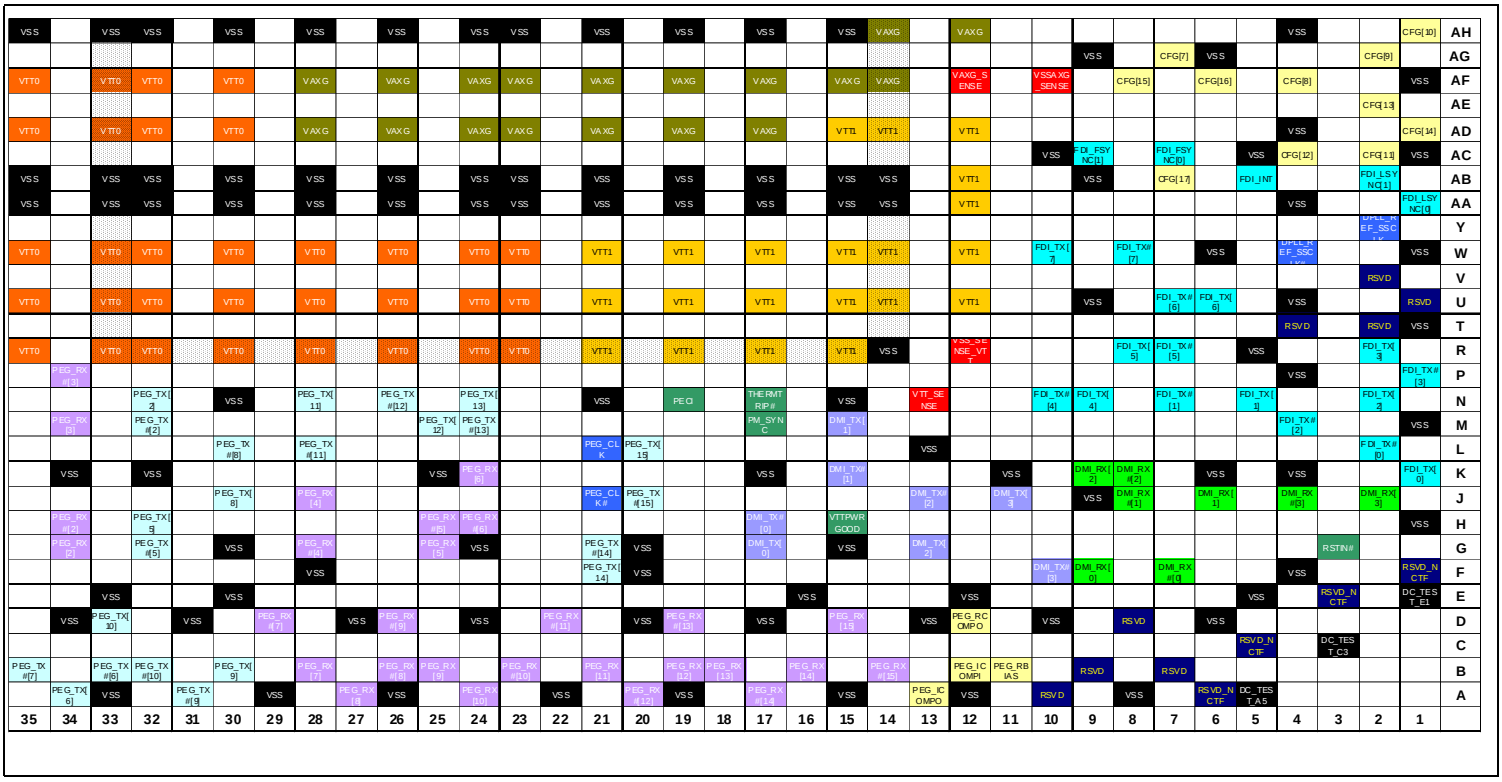


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
BCLKac71	AK7	DIFF CLK	I
BCLK #	AK8	DIFF CLK	I
BCLK_ITP	K71	DIFF CLK	O
BCLK_ITP #	J70	DIFF CLK	O
BPM#[0]	J69	GTL	I/O
BPM#[1]	J67	GTL	I/O
BPM#[2]	J62	GTL	I/O
BPM#[3]	K65	GTL	I/O
BPM#[4]	K62	GTL	I/O
BPM#[5]	J64	GTL	I/O
BPM#[6]	K69	GTL	I/O
BPM#[7]	M69	GTL	I/O
CATERR#	N61	GTL	I/O
CFG[0]	AL4	CMOS	I
CFG[1]	AM2	CMOS	I
CFG[2]	AK1	CMOS	I
CFG[3]	AK2	CMOS	I
CFG[4]	AK4	CMOS	I
CFG[5]	AJ2	CMOS	I
CFG[6]	AT2	CMOS	I
CFG[7]	AG7	CMOS	I
CFG[8]	AF4	CMOS	I
CFG[9]	AG2	CMOS	I
CFG[10]	AH1	CMOS	I
CFG[11]	AC2	CMOS	I
CFG[12]	AC4	CMOS	I
CFG[13]	AE2	CMOS	I
CFG[14]	AD1	CMOS	I
CFG[15]	AF8	CMOS	I
CFG[16]	AF6	CMOS	I
CFG[17]	AB7	CMOS	I
COMP0	AE66	Analog	I
COMP1	AD69	Analog	I
COMP2	AC70	Analog	I
COMP3	AD71	Analog	I
DBR#	W71		O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
DC_TEST_A5	A5		
DC_TEST_A68	A68		
DC_TEST_A69	A69		
DC_TEST_A71	A71		
DC_TEST_BR1	BR1		
DC_TEST_BR71	BR71		
DC_TEST_BT1	BT1		
DC_TEST_BT3	BT3		
DC_TEST_BT69	BT69		
DC_TEST_BT71	BT71		
DC_TEST_BV1	BV1		
DC_TEST_BV3	BV3		
DC_TEST_BV5	BV5		
DC_TEST_BV68	BV68		
DC_TEST_BV69	BV69		
DC_TEST_BV71	BV71		
DC_TEST_C3	C3		
DC_TEST_C69	C69		
DC_TEST_C71	C71		
DC_TEST_E1	E1		
DC_TEST_E71	E71		
DMI_RX[0]	F9	DMI	I
DMI_RX[1]	J6	DMI	I
DMI_RX[2]	K9	DMI	I
DMI_RX[3]	J2	DMI	I
DMI_RX#[0]	F7	DMI	I
DMI_RX#[1]	J8	DMI	I
DMI_RX#[2]	K8	DMI	I
DMI_RX#[3]	J4	DMI	I
DMI_TX[0]	G17	DMI	O
DMI_TX[1]	M15	DMI	O
DMI_TX[2]	G13	DMI	O
DMI_TX[3]	J11	DMI	O
DMI_TX#[0]	H17	DMI	O
DMI_TX#[1]	K15	DMI	O
DMI_TX#[2]	J13	DMI	O

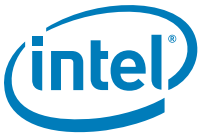


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
DMI_TX#[3]	F10	DMI	O
DPLL_REF_SSCLK	Y2	DIFF CLK	I
DPLL_REF_SSCLK#	W4	DIFF CLK	I
FDI_FSYNC[0]	AC7	CMOS	I
FDI_FSYNC[1]	AC9	CMOS	I
FDI_INT	AB5	CMOS	I
FDI_LSYNC[0]	AA1	CMOS	I
FDI_LSYNC[1]	AB2	CMOS	I
FDI_TX[0]	K1	FDI	O
FDI_TX[1]	N5	FDI	O
FDI_TX[2]	N2	FDI	O
FDI_TX[3]	R2	FDI	O
FDI_TX[4]	N9	FDI	O
FDI_TX[5]	R8	FDI	O
FDI_TX[6]	U6	FDI	O
FDI_TX[7]	W10	FDI	O
FDI_TX#[0]	L2	FDI	O
FDI_TX#[1]	N7	FDI	O
FDI_TX#[2]	M4	FDI	O
FDI_TX#[3]	P1	FDI	O
FDI_TX#[4]	N10	FDI	O
FDI_TX#[5]	R7	FDI	O
FDI_TX#[6]	U7	FDI	O
FDI_TX#[7]	W8	FDI	O
GFX_DPRSLPVR	AL71	CMOS	O
GFX_IMON	AL69	CMOS	O
GFX_VID[0]	AF71	CMOS	O
GFX_VID[1]	AG67	CMOS	O
GFX_VID[2]	AG70	CMOS	O
GFX_VID[3]	AH71	CMOS	O
GFX_VID[4]	AN71	CMOS	O
GFX_VID[5]	AM67	CMOS	O
GFX_VID[6]	AM70	CMOS	O
GFX_VR_EN	AH69	CMOS	O
ISENSE	A41	Analog	I
PECI	N19	Async	I/O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
PEG_CLK	L21	Diff CLK	I
PEG_CLK#	J21	DIFF CLK	I
PEG_ICOMPI	B12	Analog	I
PEG_ICOMPO	A13	Analog	I
PEG_RBIAS	B11	Analog	I
PEG_RCOMPO	D12	Analog	I
PEG_RX[0]	F40	PCIe	I
PEG_RX[1]	J38	PCIe	I
PEG_RX[2]	G34	PCIe	I
PEG_RX[3]	M34	PCIe	I
PEG_RX[4]	J28	PCIe	I
PEG_RX[5]	G25	PCIe	I
PEG_RX[6]	K24	PCIe	I
PEG_RX[7]	B28	PCIe	I
PEG_RX[8]	A27	PCIe	I
PEG_RX[9]	B25	PCIe	I
PEG_RX[10]	A24	PCIe	I
PEG_RX[11]	B21	PCIe	I
PEG_RX[12]	B19	PCIe	I
PEG_RX[13]	B18	PCIe	I
PEG_RX[14]	B16	PCIe	I
PEG_RX[15]	D15	PCIe	I
PEG_RX#[0]	G40	PCIe	I
PEG_RX#[1]	G38	PCIe	I
PEG_RX#[2]	H34	PCIe	I
PEG_RX#[3]	P34	PCIe	I
PEG_RX#[4]	G28	PCIe	I
PEG_RX#[5]	H25	PCIe	I
PEG_RX#[6]	H24	PCIe	I
PEG_RX#[7]	D29	PCIe	I
PEG_RX#[8]	B26	PCIe	I
PEG_RX#[9]	D26	PCIe	I
PEG_RX#[10]	B23	PCIe	I
PEG_RX#[11]	D22	PCIe	I
PEG_RX#[12]	A20	PCIe	I
PEG_RX#[13]	D19	PCIe	I

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
PEG_RX#[14]	A17	PCIe	I
PEG_RX#[15]	B14	PCIe	I
PEG_TX[0]	L40	PCIe	O
PEG_TX[1]	N38	PCIe	O
PEG_TX[2]	N32	PCIe	O
PEG_TX[3]	B39	PCIe	O
PEG_TX[4]	B37	PCIe	O
PEG_TX[5]	H32	PCIe	O
PEG_TX[6]	A34	PCIe	O
PEG_TX[7]	D36	PCIe	O
PEG_TX[8]	J30	PCIe	O
PEG_TX[9]	B30	PCIe	O
PEG_TX[10]	D33	PCIe	O
PEG_TX[11]	N28	PCIe	O
PEG_TX[12]	M25	PCIe	O
PEG_TX[13]	N24	PCIe	O
PEG_TX[14]	F21	PCIe	O
PEG_TX[15]	L20	PCIe	O
PEG_TX#[0]	N40	PCIe	O
PEG_TX#[1]	L38	PCIe	O
PEG_TX#[2]	M32	PCIe	O
PEG_TX#[3]	D40	PCIe	O
PEG_TX#[4]	A38	PCIe	O
PEG_TX#[5]	G32	PCIe	O
PEG_TX#[6]	B33	PCIe	O
PEG_TX#[7]	B35	PCIe	O
PEG_TX#[8]	L30	PCIe	O
PEG_TX#[9]	A31	PCIe	O
PEG_TX#[10]	B32	PCIe	O
PEG_TX#[11]	L28	PCIe	O
PEG_TX#[12]	N26	PCIe	O
PEG_TX#[13]	M24	PCIe	O
PEG_TX#[14]	G21	PCIe	O
PEG_TX#[15]	J20	PCIe	O
PM_EXT_TS#[0]	AV66	CMOS	I/O
PM_EXT_TS#[1]	AV64	CMOS	I/O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
PM_SYNC	M17	CMOS	I
PRDY#	U71	Async GTL	O
PREQ#	U69	Async GTL	I
PROC_DETECT	M71		
PROC_DPRSLPVR	F66	CMOS	O
PROCHOT#	N67	Async GTL	I/O
PSI#	F68	Async CMOS	O
RESET_OBS#	N70	Async CMOS	O
RSTIN#	G3	CMOS	I
RSVD	BE71		
RSVD	BE69		
RSVD	BB69		
RSVD	AY69		
RSVD	AW70		I/O
RSVD	A10		
RSVD	AA69		
RSVD_TP	AA71		
RSVD	AC69		
RSVD_TP	AC71		
RSVD	AH66		
RSVD	AK66		
RSVD	AK69		
RSVD	AK71		
RSVD	AM66		
RSVD	AN69		
RSVD	AP66		
RSVD	AR69		
RSVD	AR71		
RSVD	AT67		
RSVD	AT70		
RSVD	AU2		
RSVD	AU69		
RSVD	AU71		
RSVD	AV4		

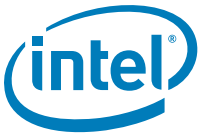


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
RSVD	AV69		
RSVD	AV71		
RSVD	B7		
RSVD	B9		
RSVD	D8		
RSVD	R64		
RSVD	R66		
RSVD	T2		
RSVD	T4		
RSVD	U1		
RSVD	V2		
VCAP0_VSS_SENSE	W64		
VCAP0_SENSE	W66		
RSVD_NCTF	A6		
RSVD_TP	BR5		
RSVD_NCTF	BT5		
RSVD_NCTF	BV6		
RSVD_NCTF	BV8		
RSVD_NCTF	C5		
RSVD_NCTF	E3		
RSVD_NCTF	F1		
RSVD_TP	AN7		
RSVD_TP	AP2		
RSVD_TP	AU1		
SA_BS[0]	BT38	DDR3	O
SA_BS[1]	BH38	DDR3	O
SA_BS[2]	BF21	DDR3	O
SA_CAS#	BK43	DDR3	O
SA_CK[0]	BM34	DDR3	O
SA_CK[1]	BK36	DDR3	O
SA_CK#[0]	BP35	DDR3	O
SA_CK#[1]	BH36	DDR3	O
SA_CKE[0]	BF20	DDR3	O
SA_CKE[1]	BK24	DDR3	O
SA_CS#[0]	BH40	DDR3	O
SA_CS#[1]	BJ47	DDR3	I/O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SA_DM[0]	BB10	DDR3	O
SA_DM[1]	BJ10	DDR3	I/O
SA_DM[2]	BM15	DDR3	O
SA_DM[3]	BN24	DDR3	O
SA_DM[4]	BG44	DDR3	O
SA_DM[5]	BG53	DDR3	O
SA_DM[6]	BN62	DDR3	O
SA_DM[7]	BH59	DDR3	I/O
SA_DQ[0]	AT8	DDR3	I/O
SA_DQ[1]	AT6	DDR3	I/O
SA_DQ[2]	BB5	DDR3	I/O
SA_DQ[3]	BB9	DDR3	I/O
SA_DQ[4]	AV7	DDR3	I/O
SA_DQ[5]	AV6	DDR3	I/O
SA_DQ[6]	BE6	DDR3	I/O
SA_DQ[7]	BE8	DDR3	I/O
SA_DQ[8]	BF11	DDR3	I/O
SA_DQ[9]	BE11	DDR3	I/O
SA_DQ[10]	BK5	DDR3	I/O
SA_DQ[11]	BH13	DDR3	I/O
SA_DQ[12]	BF9	DDR3	I/O
SA_DQ[13]	BF6	DDR3	I/O
SA_DQ[14]	BK7	DDR3	I/O
SA_DQ[15]	BN8	DDR3	I/O
SA_DQ[16]	BN11	DDR3	I/O
SA_DQ[17]	BN9	DDR3	I/O
SA_DQ[18]	BG17	DDR3	I/O
SA_DQ[19]	BK15	DDR3	I/O
SA_DQ[20]	BK9	DDR3	I/O
SA_DQ[21]	BG15	DDR3	I/O
SA_DQ[22]	BH17	DDR3	I/O
SA_DQ[23]	BK17	DDR3	I/O
SA_DQ[24]	BN20	DDR3	I/O
SA_DQ[25]	BN17	DDR3	I/O
SA_DQ[26]	BK25	DDR3	I/O
SA_DQ[27]	BH25	DDR3	I/O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SA_DQ[28]	BJ20	DDR3	I/O
SA_DQ[29]	BH21	DDR3	I/O
SA_DQ[30]	BG24	DDR3	I/O
SA_DQ[31]	BG25	DDR3	I/O
SA_DQ[32]	BJ40	DDR3	I/O
SA_DQ[33]	BM43	DDR3	I/O
SA_DQ[34]	BF47	DDR3	I/O
SA_DQ[35]	BF48	DDR3	I/O
SA_DQ[36]	BN40	DDR3	I/O
SA_DQ[37]	BH43	DDR3	I/O
SA_DQ[38]	BN44	DDR3	I/O
SA_DQ[39]	BN47	DDR3	I/O
SA_DQ[40]	BN48	DDR3	I/O
SA_DQ[41]	BN51	DDR3	I/O
SA_DQ[42]	BH53	DDR3	I/O
SA_DQ[43]	BJ55	DDR3	I/O
SA_DQ[44]	BH48	DDR3	I/O
SA_DQ[45]	BJ48	DDR3	I/O
SA_DQ[46]	BM53	DDR3	I/O
SA_DQ[47]	BN55	DDR3	I/O
SA_DQ[48]	BF55	DDR3	I/O
SA_DQ[49]	BN57	DDR3	I/O
SA_DQ[50]	BN65	DDR3	I/O
SA_DQ[51]	BJ61	DDR3	I/O
SA_DQ[52]	BF57	DDR3	I/O
SA_DQ[53]	BJ57	DDR3	I/O
SA_DQ[54]	BK64	DDR3	I/O
SA_DQ[55]	BK61	DDR3	I/O
SA_DQ[56]	BJ63	DDR3	I/O
SA_DQ[57]	BF64	DDR3	I/O
SA_DQ[58]	BB64	DDR3	I/O
SA_DQ[59]	BB66	DDR3	I/O
SA_DQ[60]	BJ66	DDR3	I/O
SA_DQ[61]	BF65	DDR3	I/O
SA_DQ[62]	AY64	DDR3	I/O
SA_DQ[63]	BC70	DDR3	I/O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SA_DQS[0]	AY7	DDR3	I/O
SA_DQS[1]	BJ5	DDR3	I/O
SA_DQS[2]	BL13	DDR3	I/O
SA_DQS[3]	BN21	DDR3	I/O
SA_DQS[4]	BK44	DDR3	I/O
SA_DQS[5]	BH51	DDR3	I/O
SA_DQS[6]	BM60	DDR3	I/O
SA_DQS[7]	BE64	DDR3	I/O
SA_DQS#[0]	AY5	DDR3	I/O
SA_DQS#[1]	BJ7	DDR3	I/O
SA_DQS#[2]	BN13	DDR3	I/O
SA_DQS#[3]	BL21	DDR3	I/O
SA_DQS#[4]	BH44	DDR3	I/O
SA_DQS#[5]	BK51	DDR3	I/O
SA_DQS#[6]	BP58	DDR3	I/O
SA_DQS#[7]	BE62	DDR3	I/O
SA_MA[0]	BT36	DDR3	O
SA_MA[1]	BP33	DDR3	O
SA_MA[2]	BV36	DDR3	O
SA_MA[3]	BG34	DDR3	O
SA_MA[4]	BG32	DDR3	O
SA_MA[5]	BN32	DDR3	O
SA_MA[6]	BK32	DDR3	O
SA_MA[7]	BJ30	DDR3	O
SA_MA[8]	BN30	DDR3	O
SA_MA[9]	BF28	DDR3	O
SA_MA[10]	BH34	DDR3	O
SA_MA[11]	BH30	DDR3	O
SA_MA[12]	BJ28	DDR3	O
SA_MA[13]	BF40	DDR3	O
SA_MA[14]	BN28	DDR3	O
SA_MA[15]	BN25	DDR3	O
SA_ODT[0]	BF43	DDR3	O
SA_ODT[1]	BL47	DDR3	O
SA_RAS#	BL38	DDR3	O
SA_WE#	BF38	DDR3	O

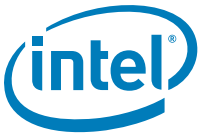


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SB_BS[0]	BV43	DDR3	O
SB_BS[1]	BV41	DDR3	O
SB_BS[2]	BV24	DDR3	O
SB_CAS#	BU46	DDR3	O
SB_CK[0]	BU33	DDR3	O
SB_CK[1]	BV38	DDR3	O
SB_CK#[0]	BV34	DDR3	O
SB_CK#[1]	BU39	DDR3	O
SB_CKE[0]	BT26	DDR3	O
SB_CKE[1]	BT24	DDR3	O
SB_CS#[0]	BP46	DDR3	O
SB_CS#[1]	BT43	DDR3	O
SB_DM[0]	BB4	DDR3	O
SB_DM[1]	BL4	DDR3	O
SB_DM[2]	BT13	DDR3	O
SB_DM[3]	BP22	DDR3	O
SB_DM[4]	BV47	DDR3	O
SB_DM[5]	BV57	DDR3	O
SB_DM[6]	BU65	DDR3	O
SB_DM[7]	BF67	DDR3	O
SB_DQ[0]	BA2	DDR3	I/O
SB_DQ[1]	AW2	DDR3	I/O
SB_DQ[2]	BD1	DDR3	I/O
SB_DQ[3]	BE4	DDR3	I/O
SB_DQ[4]	AY1	DDR3	I/O
SB_DQ[5]	BC2	DDR3	I/O
SB_DQ[6]	BF2	DDR3	I/O
SB_DQ[7]	BH2	DDR3	I/O
SB_DQ[8]	BG4	DDR3	I/O
SB_DQ[9]	BG1	DDR3	I/O
SB_DQ[10]	BR6	DDR3	I/O
SB_DQ[11]	BR8	DDR3	I/O
SB_DQ[12]	BJ4	DDR3	I/O
SB_DQ[13]	BK2	DDR3	I/O
SB_DQ[14]	BU9	DDR3	I/O
SB_DQ[15]	BV10	DDR3	I/O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SB_DQ[16]	BR10	DDR3	I/O
SB_DQ[17]	BT12	DDR3	I/O
SB_DQ[18]	BT15	DDR3	I/O
SB_DQ[19]	BV15	DDR3	I/O
SB_DQ[20]	BV12	DDR3	I/O
SB_DQ[21]	BP12	DDR3	I/O
SB_DQ[22]	BV17	DDR3	I/O
SB_DQ[23]	BU16	DDR3	I/O
SB_DQ[24]	BP15	DDR3	I/O
SB_DQ[25]	BU19	DDR3	I/O
SB_DQ[26]	BV22	DDR3	I/O
SB_DQ[27]	BT22	DDR3	I/O
SB_DQ[28]	BP19	DDR3	I/O
SB_DQ[29]	BV19	DDR3	I/O
SB_DQ[30]	BV20	DDR3	I/O
SB_DQ[31]	BT20	DDR3	I/O
SB_DQ[32]	BT48	DDR3	I/O
SB_DQ[33]	BV48	DDR3	I/O
SB_DQ[34]	BV50	DDR3	I/O
SB_DQ[35]	BP49	DDR3	I/O
SB_DQ[36]	BT47	DDR3	I/O
SB_DQ[37]	BV52	DDR3	I/O
SB_DQ[38]	BV54	DDR3	I/O
SB_DQ[39]	BT54	DDR3	I/O
SB_DQ[40]	BP53	DDR3	I/O
SB_DQ[41]	BU53	DDR3	I/O
SB_DQ[42]	BT59	DDR3	I/O
SB_DQ[43]	BT57	DDR3	I/O
SB_DQ[44]	BP56	DDR3	I/O
SB_DQ[45]	BT55	DDR3	I/O
SB_DQ[46]	BU60	DDR3	I/O
SB_DQ[47]	BV59	DDR3	I/O
SB_DQ[48]	BV61	DDR3	I/O
SB_DQ[49]	BP60	DDR3	I/O
SB_DQ[50]	BR66	DDR3	I/O
SB_DQ[51]	BR64	DDR3	I/O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SB_DQ[52]	BR62	DDR3	I/O
SB_DQ[53]	BT61	DDR3	I/O
SB_DQ[54]	BN68	DDR3	I/O
SB_DQ[55]	BL69	DDR3	I/O
SB_DQ[56]	BJ71	DDR3	I/O
SB_DQ[57]	BF70	DDR3	I/O
SB_DQ[58]	BG71	DDR3	I/O
SB_DQ[59]	BC67	DDR3	I/O
SB_DQ[60]	BK70	DDR3	I/O
SB_DQ[61]	BK67	DDR3	I/O
SB_DQ[62]	BD71	DDR3	I/O
SB_DQ[63]	BD69	DDR3	I/O
SB_DQS[0]	BD4	DDR3	I/O
SB_DQS[1]	BN4	DDR3	I/O
SB_DQS[2]	BV13	DDR3	I/O
SB_DQS[3]	BT17	DDR3	I/O
SB_DQS[4]	BT50	DDR3	I/O
SB_DQS[5]	BU56	DDR3	I/O
SB_DQS[6]	BV62	DDR3	I/O
SB_DQS[7]	BJ69	DDR3	I/O
SB_DQS#[0]	BE2	DDR3	I/O
SB_DQS#[1]	BM3	DDR3	I/O
SB_DQS#[2]	BU12	DDR3	I/O
SB_DQS#[3]	BT19	DDR3	I/O
SB_DQS#[4]	BT52	DDR3	I/O
SB_DQS#[5]	BV55	DDR3	I/O
SB_DQS#[6]	BU63	DDR3	I/O
SB_DQS#[7]	BG69	DDR3	I/O
SB_MA[0]	BT34	DDR3	O
SB_MA[1]	BP30	DDR3	O
SB_MA[2]	BV29	DDR3	O
SB_MA[3]	BU30	DDR3	O
SB_MA[4]	BV31	DDR3	O
SB_MA[5]	BT33	DDR3	O
SB_MA[6]	BT31	DDR3	O
SB_MA[7]	BP26	DDR3	O

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
SB_MA[8]	BV27	DDR3	O
SB_MA[9]	BT27	DDR3	O
SB_MA[10]	BU42	DDR3	O
SB_MA[11]	BU26	DDR3	O
SB_MA[12]	BT29	DDR3	O
SB_MA[13]	BT45	DDR3	O
SB_MA[14]	BV26	DDR3	O
SB_MA[15]	BU23	DDR3	O
SB_ODT[0]	BV45	DDR3	O
SB_ODT[1]	BU49	DDR3	O
SB_RAS#	BT40	DDR3	O
SB_WE#	BT41	DDR3	O
SM_DRAMPWROK	AM5	Async CMOS	I
SM_DRAMRST#	BJ12	DDR3	O
SM_RCOMP[0]	BV33	Analog	I
SM_RCOMP[1]	BP39	Analog	
SM_RCOMP[2]	BV40	Analog	I
TAPPWRGOOD	Y70	Async CMOS	O
TCK	T67	CMOS	I
TDI	T69	CMOS	I
TDI_M	P71	CMOS	I
TDO	T71	CMOS	O
TDO_M	T70	CMOS	O
THERMTRIP#	N17	Async GTL	O
TMS	N65	CMOS	I
TRST#	P69	CMOS	I
VAXG	AD17	REF	
VAXG	AD19	REF	
VAXG	AD21	REF	
VAXG	AD23	REF	
VAXG	AD24	REF	
VAXG	AD26	REF	
VAXG	AD28	REF	
VAXG	AF14	REF	
VAXG	AF15	REF	

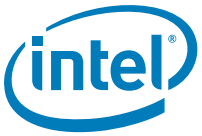


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VAXG	AF17	REF	
VAXG	AF19	REF	
VAXG	AF21	REF	
VAXG	AF23	REF	
VAXG	AF24	REF	
VAXG	AF26	REF	
VAXG	AF28	REF	
VAXG	AH12	REF	
VAXG	AH14	REF	
VAXG	AJ10	REF	
VAXG	AK12	REF	
VAXG	AK14	REF	
VAXG	AL19	REF	
VAXG	AL21	REF	
VAXG	AL23	REF	
VAXG	AL24	REF	
VAXG	AL26	REF	
VAXG	AL28	REF	
VAXG	AL30	REF	
VAXG	AL32	REF	
VAXG	AN19	REF	
VAXG	AN21	REF	
VAXG	AN23	REF	
VAXG	AN24	REF	
VAXG	AN26	REF	
VAXG	AN28	REF	
VAXG	AN30	REF	
VAXG	AN32	REF	
VAXG_SENSE	AF12	Analog	O
VCAP0	AK50	PWR	
VCAP0	AK53	PWR	
VCAP0	AK57	PWR	
VCAP0	AL50	PWR	
VCAP0	AL53	PWR	
VCAP0	AL57	PWR	
VCAP0	AN50	PWR	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCAP0	AN53	PWR	
VCAP0	AN57	PWR	
VCAP0	AR48	PWR	
VCAP0	AR51	PWR	
VCAP0	AR55	PWR	
VCAP0	AU48	PWR	
VCAP0	AU51	PWR	
VCAP0	AU55	PWR	
VCAP0	AW50	PWR	
VCAP0	AW53	PWR	
VCAP0	AW57	PWR	
VCAP0	AY50	PWR	
VCAP0	AY53	PWR	
VCAP0	AY57	PWR	
VCAP0	BB48	PWR	
VCAP0	BB51	PWR	
VCAP0	BB55	PWR	
VCAP0	BD48	PWR	
VCAP0	BD51	PWR	
VCAP0	BD55	PWR	
VCAP1	AK39	PWR	
VCAP1	AK42	PWR	
VCAP1	AK46	PWR	
VCAP1	AL39	PWR	
VCAP1	AL42	PWR	
VCAP1	AL46	PWR	
VCAP1	AN39	PWR	
VCAP1	AN42	PWR	
VCAP1	AN46	PWR	
VCAP1	AR37	PWR	
VCAP1	AR41	PWR	
VCAP1	AR44	PWR	
VCAP1	AU37	PWR	
VCAP1	AU41	PWR	
VCAP1	AU44	PWR	
VCAP1	AW39	PWR	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCAP1	AW42	PWR	
VCAP1	AW46	PWR	
VCAP1	AY39	PWR	
VCAP1	AY42	PWR	
VCAP1	AY46	PWR	
VCAP1	BB37	PWR	
VCAP1	BB41	PWR	
VCAP1	BB44	PWR	
VCAP1	BD37	PWR	
VCAP1	BD41	PWR	
VCAP1	BD44	PWR	
VCAP2	AA59	PWR	
VCAP2	AA60	PWR	
VCAP2	AB59	PWR	
VCAP2	AB60	PWR	
VCAP2	AD59	PWR	
VCAP2	AD60	PWR	
VCAP2	AF59	PWR	
VCAP2	AF60	PWR	
VCAP2	AH59	PWR	
VCAP2	AH60	PWR	
VCAP2	AK59	PWR	
VCAP2	AK60	PWR	
VCAP2	AK62	PWR	
VCAP2	R59	PWR	
VCAP2	R60	PWR	
VCAP2	U59	PWR	
VCAP2	U60	PWR	
VCAP2	W59	PWR	
VCAP2	W60	PWR	
VCC	A43	REF	
VCC	A47	REF	
VCC	A50	REF	
VCC	A54	REF	
VCC	A57	REF	
VCC	AA41	REF	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCC	AA44	REF	
VCC	AA48	REF	
VCC	AA51	REF	
VCC	AA55	REF	
VCC	AB41	REF	
VCC	AB44	REF	
VCC	AB48	REF	
VCC	AB51	REF	
VCC	AB55	REF	
VCC	AD41	REF	
VCC	AD44	REF	
VCC	AD48	REF	
VCC	AD51	REF	
VCC	AD55	REF	
VCC	AF41	REF	
VCC	AF42	REF	
VCC	AF44	REF	
VCC	AF46	REF	
VCC	AF48	REF	
VCC	AF50	REF	
VCC	AF51	REF	
VCC	AF53	REF	
VCC	AF55	REF	
VCC	AF57	REF	
VCC	B42	REF	
VCC	B46	REF	
VCC	B49	REF	
VCC	B53	REF	
VCC	B56	REF	
VCC	B60	REF	
VCC	D43	REF	
VCC	D45	REF	
VCC	D47	REF	
VCC	D48	REF	
VCC	D50	REF	
VCC	D52	REF	

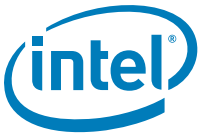


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCC	D54	REF	
VCC	D55	REF	
VCC	D57	REF	
VCC	D59	REF	
VCC	E42	REF	
VCC	E46	REF	
VCC	E50	REF	
VCC	E53	REF	
VCC	E57	REF	
VCC	E60	REF	
VCC	F55	REF	
VCC	G44	REF	
VCC	G51	REF	
VCC	G55	REF	
VCC	G60	REF	
VCC	H44	REF	
VCC	H51	REF	
VCC	H60	REF	
VCC	J55	REF	
VCC	K44	REF	
VCC	K51	REF	
VCC	K60	REF	
VCC	L55	REF	
VCC	M44	REF	
VCC	M51	REF	
VCC	M60	REF	
VCC	N42	REF	
VCC	N44	REF	
VCC	N48	REF	
VCC	N51	REF	
VCC	N55	REF	
VCC	P60	REF	
VCC	R41	REF	
VCC	R44	REF	
VCC	R48	REF	
VCC	R51	REF	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VCC	R55	REF	
VCC	U41	REF	
VCC	U44	REF	
VCC	U48	REF	
VCC	U51	REF	
VCC	U55	REF	
VCC	W41	REF	
VCC	W44	REF	
VCC	W48	REF	
VCC	W51	REF	
VCC	W55	REF	
VCC_SENSE	F64	Analog	O
VCCPLL	R37	REF	
VCCPLL	R39	REF	
VCCPLL	U37	REF	
VCCPLL	W37	REF	
VCCPLL	W39	REF	
VCCPWRGOOD_0	Y67	Async CMOS	I
VCCPWRGOOD_1	AM7	Async CMOS	I
VDDQ	BB15	REF	
VDDQ	BB17	REF	
VDDQ	BB19	REF	
VDDQ	BB21	REF	
VDDQ	BB23	REF	
VDDQ	BB24	REF	
VDDQ	BB26	REF	
VDDQ	BB28	REF	
VDDQ	BB30	REF	
VDDQ	BB32	REF	
VDDQ	BB33	REF	
VDDQ	BB35	REF	
VDDQ	BD15	REF	
VDDQ	BD17	REF	
VDDQ	BD19	REF	
VDDQ	BD21	REF	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VDDQ	BD23	REF	
VDDQ	BD24	REF	
VDDQ	BD26	REF	
VDDQ	BD28	REF	
VDDQ	BD30	REF	
VDDQ	BD32	REF	
VDDQ	BD33	REF	
VDDQ	BD35	REF	
VDDQ	BF15	REF	
VDDQ	BF16	REF	
VDDQ	BG43	REF	
VDDQ	BH28	REF	
VDDQ	BH32	REF	
VDDQ	BJ38	REF	
VDDQ	BL30	REF	
VDDQ	BM25	REF	
VDDQ	BN38	REF	
VDDQ	BU28	REF	
VDDQ	BU35	REF	
VDDQ	BU40	REF	
VDDQ_CK	BB12	REF	
VDDQ_CK	BB14	REF	
VID[0]	A61	CMOS	O
VID[1]	D61	CMOS	O
VID[2]	D62	CMOS	O
CSC[0]/VID[3]	A62	CMOS	I/O
CSC[1]VID[4]	B63	CMOS	I/O
CSC[2]VID[5]	D64	CMOS	I/O
VID[6]	D66	CMOS	O
VSS	A12	GND	
VSS	A15	GND	
VSS	A19	GND	
VSS	A22	GND	
VSS	A26	GND	
VSS	A29	GND	
VSS	A33	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	A36	GND	
VSS	A40	GND	
VSS	A45	GND	
VSS	A48	GND	
VSS	A52	GND	
VSS	A55	GND	
VSS	A59	GND	
VSS	A64	GND	
VSS	A66	GND	
VSS	A8	GND	
VSS	AA14	GND	
VSS	AA15	GND	
VSS	AA17	GND	
VSS	AA19	GND	
VSS	AA21	GND	
VSS	AA23	GND	
VSS	AA24	GND	
VSS	AA26	GND	
VSS	AA28	GND	
VSS	AA30	GND	
VSS	AA32	GND	
VSS	AA33	GND	
VSS	AA35	GND	
VSS	AA37	GND	
VSS	AA39	GND	
VSS	AA4	GND	
VSS	AA42	GND	
VSS	AA46	GND	
VSS	AA50	GND	
VSS	AA53	GND	
VSS	AA57	GND	
VSS	AA62	GND	
VSS	AA64	GND	
VSS	AA66	GND	
VSS	AB14	GND	
VSS	AB15	GND	

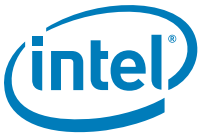


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AB17	GND	
VSS	AB19	GND	
VSS	AB21	GND	
VSS	AB23	GND	
VSS	AB24	GND	
VSS	AB26	GND	
VSS	AB28	GND	
VSS	AB30	GND	
VSS	AB32	GND	
VSS	AB33	GND	
VSS	AB35	GND	
VSS	AB37	GND	
VSS	AB39	GND	
VSS	AB42	GND	
VSS	AB46	GND	
VSS	AB50	GND	
VSS	AB53	GND	
VSS	AB57	GND	
VSS	AB62	GND	
VSS	AB70	GND	
VSS	AB9	GND	
VSS	AC1	GND	
VSS	AC10	GND	
VSS	AC5	GND	
VSS	AC64	GND	
VSS	AC67	GND	
VSS	AD4	GND	
VSS	AD42	GND	
VSS	AD46	GND	
VSS	AD50	GND	
VSS	AD53	GND	
VSS	AD57	GND	
VSS	AD62	GND	
VSS	AE64	GND	
VSS	AE70	GND	
VSS	AF1	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AF62	GND	
VSS	AF69	GND	
VSS	AG6	GND	
VSS	AG64	GND	
VSS	AG9	GND	
VSS	AH15	GND	
VSS	AH17	GND	
VSS	AH19	GND	
VSS	AH21	GND	
VSS	AH23	GND	
VSS	AH24	GND	
VSS	AH26	GND	
VSS	AH28	GND	
VSS	AH30	GND	
VSS	AH32	GND	
VSS	AH33	GND	
VSS	AH35	GND	
VSS	AH37	GND	
VSS	AH39	GND	
VSS	AH4	GND	
VSS	AH41	GND	
VSS	AH42	GND	
VSS	AH44	GND	
VSS	AH46	GND	
VSS	AH48	GND	
VSS	AH50	GND	
VSS	AH51	GND	
VSS	AH53	GND	
VSS	AH55	GND	
VSS	AH57	GND	
VSS	AH62	GND	
VSS	AJ70	GND	
VSS	AK15	GND	
VSS	AK17	GND	
VSS	AK19	GND	
VSS	AK21	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AK23	GND	
VSS	AK24	GND	
VSS	AK26	GND	
VSS	AK28	GND	
VSS	AK30	GND	
VSS	AK32	GND	
VSS	AK37	GND	
VSS	AK41	GND	
VSS	AK44	GND	
VSS	AK48	GND	
VSS	AK51	GND	
VSS	AK55	GND	
VSS	AK64	GND	
VSS	AK70	GND	
VSS	AL1	GND	
VSS	AL33	GND	
VSS	AL35	GND	
VSS	AL37	GND	
VSS	AL41	GND	
VSS	AL44	GND	
VSS	AL48	GND	
VSS	AL51	GND	
VSS	AL55	GND	
VSS	AL62	GND	
VSS	AM64	GND	
VSS	AM8	GND	
VSS	AN37	GND	
VSS	AN4	GND	
VSS	AN41	GND	
VSS	AN44	GND	
VSS	AN48	GND	
VSS	AN5	GND	
VSS	AN51	GND	
VSS	AN55	GND	
VSS	AN62	GND	
VSS	AP64	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AP70	GND	
VSS	AR1	GND	
VSS	AR14	GND	
VSS	AR15	GND	
VSS	AR17	GND	
VSS	AR19	GND	
VSS	AR21	GND	
VSS	AR23	GND	
VSS	AR24	GND	
VSS	AR26	GND	
VSS	AR28	GND	
VSS	AR30	GND	
VSS	AR32	GND	
VSS	AR33	GND	
VSS	AR35	GND	
VSS	AR39	GND	
VSS	AR4	GND	
VSS	AR42	GND	
VSS	AR46	GND	
VSS	AR50	GND	
VSS	AR53	GND	
VSS	AR57	GND	
VSS	AR62	GND	
VSS	AT10	GND	
VSS	AT64	GND	
VSS	AU14	GND	
VSS	AU15	GND	
VSS	AU17	GND	
VSS	AU19	GND	
VSS	AU21	GND	
VSS	AU23	GND	
VSS	AU24	GND	
VSS	AU26	GND	
VSS	AU28	GND	
VSS	AU30	GND	
VSS	AU32	GND	

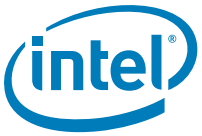


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AU33	GND	
VSS	AU35	GND	
VSS	AU39	GND	
VSS	AU4	GND	
VSS	AU42	GND	
VSS	AU46	GND	
VSS	AU50	GND	
VSS	AU53	GND	
VSS	AU57	GND	
VSS	AU62	GND	
VSS	AU70	GND	
VSS	AV1	GND	
VSS	AV9	GND	
VSS	AW37	GND	
VSS	AW41	GND	
VSS	AW44	GND	
VSS	AW48	GND	
VSS	AW51	GND	
VSS	AW55	GND	
VSS	AW59	GND	
VSS	AW62	GND	
VSS	AW67	GND	
VSS	AY12	GND	
VSS	AY14	GND	
VSS	AY15	GND	
VSS	AY17	GND	
VSS	AY19	GND	
VSS	AY21	GND	
VSS	AY23	GND	
VSS	AY24	GND	
VSS	AY26	GND	
VSS	AY28	GND	
VSS	AY30	GND	
VSS	AY32	GND	
VSS	AY33	GND	
VSS	AY35	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	AY37	GND	
VSS	AY4	GND	
VSS	AY41	GND	
VSS	AY44	GND	
VSS	AY48	GND	
VSS	AY51	GND	
VSS	AY55	GND	
VSS	AY59	GND	
VSS	AY62	GND	
VSS	AY66	GND	
VSS	AY71	GND	
VSS	AY8	GND	
VSS	B40	GND	
VSS	B44	GND	
VSS	B48	GND	
VSS	B51	GND	
VSS	B55	GND	
VSS	B58	GND	
VSS	B62	GND	
VSS	B65	GND	
VSS	BA70	GND	
VSS	BB1	GND	
VSS	BB39	GND	
VSS	BB42	GND	
VSS	BB46	GND	
VSS	BB50	GND	
VSS	BB53	GND	
VSS	BB57	GND	
VSS	BB62	GND	
VSS	BB7	GND	
VSS	BB71	GND	
VSS	BD14	GND	
VSS	BD39	GND	
VSS	BD42	GND	
VSS	BD46	GND	
VSS	BD50	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	BD53	GND	
VSS	BD57	GND	
VSS	BE1	GND	
VSS	BE65	GND	
VSS	BE70	GND	
VSS	BE9	GND	
VSS	BF13	GND	
VSS	BF30	GND	
VSS	BF62	GND	
VSS	BF8	GND	
VSS	BG36	GND	
VSS	BG51	GND	
VSS	BH15	GND	
VSS	BH20	GND	
VSS	BH24	GND	
VSS	BH47	GND	
VSS	BH55	GND	
VSS	BH57	GND	
VSS	BH70	GND	
VSS	BJ1	GND	
VSS	BJ21	GND	
VSS	BJ64	GND	
VSS	BJ9	GND	
VSS	BK10	GND	
VSS	BK34	GND	
VSS	BK53	GND	
VSS	BK60	GND	
VSS	BK63	GND	
VSS	BL1	GND	
VSS	BL20	GND	
VSS	BL28	GND	
VSS	BL40	GND	
VSS	BL48	GND	
VSS	BL55	GND	
VSS	BL57	GND	
VSS	BL71	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	BM17	GND	
VSS	BM24	GND	
VSS	BM32	GND	
VSS	BM44	GND	
VSS	BM51	GND	
VSS	BM70	GND	
VSS	BN1	GND	
VSS	BN6	GND	
VSS	BN64	GND	
VSS	BN71	GND	
VSS	BP42	GND	
VSS	BR3	GND	
VSS	BR68	GND	
VSS	BR69	GND	
VSS	BT68	GND	
VSS	BU11	GND	
VSS	BU14	GND	
VSS	BU18	GND	
VSS	BU21	GND	
VSS	BU25	GND	
VSS	BU32	GND	
VSS	BU37	GND	
VSS	BU44	GND	
VSS	BU48	GND	
VSS	BU51	GND	
VSS	BU55	GND	
VSS	BU58	GND	
VSS	BU62	GND	
VSS	BU7	GND	
VSS	BV64	GND	
VSS	BV66	GND	
VSS	C68	GND	
VSS	D10	GND	
VSS	D13	GND	
VSS	D17	GND	
VSS	D20	GND	

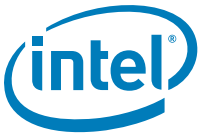


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	D24	GND	
VSS	D27	GND	
VSS	D31	GND	
VSS	D34	GND	
VSS	D38	GND	
VSS	D41	GND	
VSS	D6	GND	
VSS	E12	GND	
VSS	E16	GND	
VSS	E30	GND	
VSS	E33	GND	
VSS	E37	GND	
VSS	E5	GND	
VSS	E68	GND	
VSS	E69	GND	
VSS	F20	GND	
VSS	F28	GND	
VSS	F4	GND	
VSS	F47	GND	
VSS	F48	GND	
VSS	F61	GND	
VSS	F71	GND	
VSS	G15	GND	
VSS	G20	GND	
VSS	G24	GND	
VSS	G30	GND	
VSS	G43	GND	
VSS	G47	GND	
VSS	G48	GND	
VSS	G53	GND	
VSS	G57	GND	
VSS	G70	GND	
VSS	H1	GND	
VSS	H36	GND	
VSS	H43	GND	
VSS	H53	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	H71	GND	
VSS	J40	GND	
VSS	J47	GND	
VSS	J48	GND	
VSS	J57	GND	
VSS	J65	GND	
VSS	J9	GND	
VSS	K11	GND	
VSS	K17	GND	
VSS	K25	GND	
VSS	K32	GND	
VSS	K34	GND	
VSS	K36	GND	
VSS	K4	GND	
VSS	K43	GND	
VSS	K53	GND	
VSS	K6	GND	
VSS	K64	GND	
VSS	L13	GND	
VSS	L47	GND	
VSS	L48	GND	
VSS	L57	GND	
VSS	L70	GND	
VSS	M1	GND	
VSS	M36	GND	
VSS	M42	GND	
VSS	M53	GND	
VSS	N15	GND	
VSS	N21	GND	
VSS	N30	GND	
VSS	N46	GND	
VSS	N50	GND	
VSS	N53	GND	
VSS	N57	GND	
VSS	N63	GND	
VSS	P4	GND	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VSS	R14	GND	
VSS	R42	GND	
VSS	R46	GND	
VSS	R5	GND	
VSS	R50	GND	
VSS	R53	GND	
VSS	R57	GND	
VSS	R62	GND	
VSS	R70	GND	
VSS	T1	GND	
VSS	U39	GND	
VSS	U4	GND	
VSS	U42	GND	
VSS	U46	GND	
VSS	U50	GND	
VSS	U53	GND	
VSS	U57	GND	
VSS	U62	GND	
VSS	U64	GND	
VSS	U9	GND	
VSS	V70	GND	
VSS	W1	GND	
VSS	W42	GND	
VSS	W46	GND	
VSS	W50	GND	
VSS	W53	GND	
VSS	W57	GND	
VSS	W6	GND	
VSS	W62	GND	
VSS	W69	GND	
VSS_SENSE	F63	Analog	O
VSS_SENSE_VTT	R12	Analog	O
VSSAXG_SENSE	AF10	Analog	O
VTT_SELECT	AN1	CMOS	O
VTT_SENSE	N13	Analog	O
VTT0	AD30	REF	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VTT0	AD32	REF	
VTT0	AD33	REF	
VTT0	AD35	REF	
VTT0	AD37	REF	
VTT0	AD39	REF	
VTT0	AF30	REF	
VTT0	AF32	REF	
VTT0	AF33	REF	
VTT0	AF35	REF	
VTT0	AF37	REF	
VTT0	AF39	REF	
VTT0	AK33	REF	
VTT0	AK35	REF	
VTT0	AL12	REF	
VTT0	AL14	REF	
VTT0	AL15	REF	
VTT0	AL17	REF	
VTT0	AL59	REF	
VTT0	AL60	REF	
VTT0	AM10	REF	
VTT0	AN12	REF	
VTT0	AN14	REF	
VTT0	AN15	REF	
VTT0	AN17	REF	
VTT0	AN33	REF	
VTT0	AN35	REF	
VTT0	AN59	REF	
VTT0	AN60	REF	
VTT0	AN9	REF	
VTT0	AR12	REF	
VTT0	AR59	REF	
VTT0	AR60	REF	
VTT0	AU12	REF	
VTT0	AU59	REF	
VTT0	AU60	REF	
VTT0	AW12	REF	

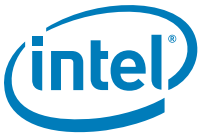


Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VTT0	AW14	REF	
VTT0	AW33	REF	
VTT0	AW35	REF	
VTT0	AW60	REF	
VTT0	AY10	REF	
VTT0	AY60	REF	
VTT0	BB59	REF	
VTT0	BB60	REF	
VTT0	BD59	REF	
VTT0	BD60	REF	
VTT0	BF59	REF	
VTT0	BF60	REF	
VTT0	R23	REF	
VTT0	R24	REF	
VTT0	R26	REF	
VTT0	R28	REF	
VTT0	R30	REF	
VTT0	R32	REF	
VTT0	R33	REF	
VTT0	R35	REF	
VTT0	U23	REF	
VTT0	U24	REF	
VTT0	U26	REF	
VTT0	U28	REF	
VTT0	U30	REF	
VTT0	U32	REF	
VTT0	U33	REF	
VTT0	U35	REF	
VTT0	W23	REF	
VTT0	W24	REF	
VTT0	W26	REF	
VTT0	W28	REF	
VTT0	W30	REF	
VTT0	W32	REF	
VTT0	W33	REF	
VTT0	W35	REF	

Table 70. BGA1288 Processor Ball List by Ball Name

Pin Name	Pin #	Buffer Type	Dir
VTT0_DDR	AW15	REF	
VTT0_DDR	AW17	REF	
VTT0_DDR	AW19	REF	
VTT0_DDR	AW21	REF	
VTT0_DDR	AW23	REF	
VTT0_DDR	AW24	REF	
VTT0_DDR	AW26	REF	
VTT0_DDR	AW28	REF	
VTT0_DDR	AW30	REF	
VTT0_DDR	AW32	REF	
VTT1	AA12	REF	
VTT1	AB12	REF	
VTT1	AD12	REF	
VTT1	AD14	REF	
VTT1	AD15	REF	
VTT1	R15	REF	
VTT1	R17	REF	
VTT1	R19	REF	
VTT1	R21	REF	
VTT1	U12	REF	
VTT1	U14	REF	
VTT1	U15	REF	
VTT1	U17	REF	
VTT1	U19	REF	
VTT1	U21	REF	
VTT1	W12	REF	
VTT1	W14	REF	
VTT1	W15	REF	
VTT1	W17	REF	
VTT1	W19	REF	
VTT1	W21	REF	
VTTPWRGOOD	H15	Async CMOS	I

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
A5	DC_TEST_A5		
A6	RSVD_NCTF		
A8	VSS	GND	
A10	RSVD		
A12	VSS	GND	
A13	PEG_ICOMPO	Analog	I
A15	VSS	GND	
A17	PEG_RX#[14]	PCIe	I
A19	VSS	GND	
A20	PEG_RX#[12]	PCIe	I
A22	VSS	GND	
A24	PEG_RX[10]	PCIe	I
A26	VSS	GND	
A27	PEG_RX[8]	PCIe	I
A29	VSS	GND	
A31	PEG_TX#[9]	PCIe	O
A33	VSS	GND	
A34	PEG_TX[6]	PCIe	O
A36	VSS	GND	
A38	PEG_TX#[4]	PCIe	O
A40	VSS	GND	
A41	ISENSE	Analog	I
A43	VCC	REF	
A45	VSS	GND	
A47	VCC	REF	
A48	VSS	GND	
A50	VCC	REF	
A52	VSS	GND	
A54	VCC	REF	
A55	VSS	GND	
A57	VCC	REF	
A59	VSS	GND	
A61	VID[0]	CMOS	O
A62	CSC[0]/VID[3]	CMOS	I/O
A64	VSS	GND	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
A66	VSS	GND	
A68	DC_TEST_A68		
A69	DC_TEST_A69		
A71	DC_TEST_A71		
AA1	FDI_LSYNC[0]	CMOS	I
AA4	VSS	GND	
AA12	VTT1	REF	
AA14	VSS	GND	
AA15	VSS	GND	
AA17	VSS	GND	
AA19	VSS	GND	
AA21	VSS	GND	
AA23	VSS	GND	
AA24	VSS	GND	
AA26	VSS	GND	
AA28	VSS	GND	
AA30	VSS	GND	
AA32	VSS	GND	
AA33	VSS	GND	
AA35	VSS	GND	
AA37	VSS	GND	
AA39	VSS	GND	
AA41	VCC	REF	
AA42	VSS	GND	
AA44	VCC	REF	
AA46	VSS	GND	
AA48	VCC	REF	
AA50	VSS	GND	
AA51	VCC	REF	
AA53	VSS	GND	
AA55	VCC	REF	
AA57	VSS	GND	
AA59	VCAP2	PWR	
AA60	VCAP2	PWR	
AA62	VSS	GND	
AA64	VSS	GND	

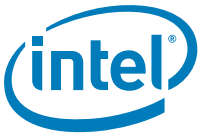


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AA66	VSS	GND	
AA69	RSVD		
AA71	RSVD_TP		
AB2	FDI_LSYNC[1]	CMOS	I
AB5	FDI_INT	CMOS	I
AB7	CFG[17]	CMOS	I
AB9	VSS	GND	
AB12	VTT1	REF	
AB14	VSS	GND	
AB15	VSS	GND	
AB17	VSS	GND	
AB19	VSS	GND	
AB21	VSS	GND	
AB23	VSS	GND	
AB24	VSS	GND	
AB26	VSS	GND	
AB28	VSS	GND	
AB30	VSS	GND	
AB32	VSS	GND	
AB33	VSS	GND	
AB35	VSS	GND	
AB37	VSS	GND	
AB39	VSS	GND	
AB41	VCC	REF	
AB42	VSS	GND	
AB44	VCC	REF	
AB46	VSS	GND	
AB48	VCC	REF	
AB50	VSS	GND	
AB51	VCC	REF	
AB53	VSS	GND	
AB55	VCC	REF	
AB57	VSS	GND	
AB59	VCAP2	PWR	
AB60	VCAP2	PWR	
AB62	VSS	GND	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AB70	VSS	GND	
AC1	VSS	GND	
AC2	CFG[11]	CMOS	I
AC4	CFG[12]	CMOS	I
AC5	VSS	GND	
AC7	FDI_FSYNC[0]	CMOS	I
AC9	FDI_FSYNC[1]	CMOS	I
AC10	VSS	GND	
AC64	VSS	GND	
AC67	VSS	GND	
AC69	RSVD		
AC70	COMP2	Analog	I
AC71	RSVD_TP		
AD1	CFG[14]	CMOS	I
AD4	VSS	GND	
AD12	VTT1	REF	
AD14	VTT1	REF	
AD15	VTT1	REF	
AD17	VAXG	REF	
AD19	VAXG	REF	
AD21	VAXG	REF	
AD23	VAXG	REF	
AD24	VAXG	REF	
AD26	VAXG	REF	
AD28	VAXG	REF	
AD30	VTT0	REF	
AD32	VTT0	REF	
AD33	VTT0	REF	
AD35	VTT0	REF	
AD37	VTT0	REF	
AD39	VTT0	REF	
AD41	VCC	REF	
AD42	VSS	GND	
AD44	VCC	REF	
AD46	VSS	GND	
AD48	VCC	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AD50	VSS	GND	
AD51	VCC	REF	
AD53	VSS	GND	
AD55	VCC	REF	
AD57	VSS	GND	
AD59	VCAP2	PWR	
AD60	VCAP2	PWR	
AD62	VSS	GND	
AD69	COMP1	Analog	I
AD71	COMP3	Analog	I
AE2	CFG[13]	CMOS	I
AE64	VSS	GND	
AE66	COMP0	Analog	I
AE70	VSS	GND	
AF1	VSS	GND	
AF4	CFG[8]	CMOS	I
AF10	VSSAXG_SENSE	Analog	O
AF12	VAXG_SENSE	Analog	O
AF14	VAXG	REF	
AF15	VAXG	REF	
AF17	VAXG	REF	
AF19	VAXG	REF	
AF21	VAXG	REF	
AF23	VAXG	REF	
AF24	VAXG	REF	
AF26	VAXG	REF	
AF28	VAXG	REF	
AF30	VTT0	REF	
AF32	VTT0	REF	
AF33	VTT0	REF	
AF35	VTT0	REF	
AF37	VTT0	REF	
AF39	VTT0	REF	
AF41	VCC	REF	
AF42	VCC	REF	
AF44	VCC	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AF46	VCC	REF	
AF48	VCC	REF	
AF50	VCC	REF	
AF51	VCC	REF	
AF53	VCC	REF	
AF55	VCC	REF	
AF57	VCC	REF	
AF59	VCAP2	PWR	
AF6	CFG[16]	CMOS	I
AF60	VCAP2	PWR	
AF62	VSS	GND	
AF69	VSS	GND	
AF71	GFX_VID[0]	CMOS	O
AF8	CFG[15]	CMOS	I
AG2	CFG[9]	CMOS	I
AG6	VSS	GND	
AG7	CFG[7]	CMOS	I
AG9	VSS	GND	
AG64	VSS	GND	
AG67	GFX_VID[1]	CMOS	O
AG70	GFX_VID[2]	CMOS	O
AH1	CFG[10]	CMOS	I
AH4	VSS	GND	
AH12	VAXG	REF	
AH14	VAXG	REF	
AH15	VSS	GND	
AH17	VSS	GND	
AH19	VSS	GND	
AH21	VSS	GND	
AH23	VSS	GND	
AH24	VSS	GND	
AH26	VSS	GND	
AH28	VSS	GND	
AH30	VSS	GND	
AH32	VSS	GND	
AH33	VSS	GND	

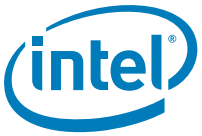


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AH35	VSS	GND	
AH37	VSS	GND	
AH39	VSS	GND	
AH41	VSS	GND	
AH42	VSS	GND	
AH44	VSS	GND	
AH46	VSS	GND	
AH48	VSS	GND	
AH50	VSS	GND	
AH51	VSS	GND	
AH53	VSS	GND	
AH55	VSS	GND	
AH57	VSS	GND	
AH59	VCAP2	PWR	
AH60	VCAP2	PWR	
AH62	VSS	GND	
AH66	RSVD		
AH69	GFX_VR_EN	CMOS	O
AH71	GFX_VID[3]	CMOS	O
AJ10	VAXG	REF	
AJ2	CFG[5]	CMOS	I
AJ70	VSS	GND	
AK1	CFG[2]	CMOS	I
AK2	CFG[3]	CMOS	I
AK4	CFG[4]	CMOS	I
AK7	BCLK	DIFF CLK	I
AK8	BCLK #	DIFF CLK	I
AK12	VAXG	REF	
AK14	VAXG	REF	
AK15	VSS	GND	
AK17	VSS	GND	
AK19	VSS	GND	
AK21	VSS	GND	
AK23	VSS	GND	
AK24	VSS	GND	
AK26	VSS	GND	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AK28	VSS	GND	
AK30	VSS	GND	
AK32	VSS	GND	
AK33	VTT0	REF	
AK35	VTT0	REF	
AK37	VSS	GND	
AK39	VCAP1	PWR	
AK41	VSS	GND	
AK42	VCAP1	PWR	
AK44	VSS	GND	
AK46	VCAP1	PWR	
AK48	VSS	GND	
AK50	VCAP0	PWR	
AK51	VSS	GND	
AK53	VCAP0	PWR	
AK55	VSS	GND	
AK57	VCAP0	PWR	
AK59	VCAP2	PWR	
AK60	VCAP2	PWR	
AK62	VCAP2	PWR	
AK64	VSS	GND	
AK66	RSVD		
AK69	RSVD		
AK70	VSS	GND	
AK71	RSVD		
AL1	VSS	GND	
AL4	CFG[0]	CMOS	I
AL12	VTT0	REF	
AL14	VTT0	REF	
AL15	VTT0	REF	
AL17	VTT0	REF	
AL19	VAXG	REF	
AL21	VAXG	REF	
AL23	VAXG	REF	
AL24	VAXG	REF	
AL26	VAXG	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AL28	VAXG	REF	
AL30	VAXG	REF	
AL32	VAXG	REF	
AL33	VSS	GND	
AL35	VSS	GND	
AL37	VSS	GND	
AL39	VCAP1	PWR	
AL41	VSS	GND	
AL42	VCAP1	PWR	
AL44	VSS	GND	
AL46	VCAP1	PWR	
AL48	VSS	GND	
AL50	VCAP0	PWR	
AL51	VSS	GND	
AL53	VCAP0	PWR	
AL55	VSS	GND	
AL57	VCAP0	PWR	
AL59	VTT0	REF	
AL60	VTT0	REF	
AL62	VSS	GND	
AL69	GFX_IMON	CMOS	O
AL71	GFX_DPRSLPVR	CMOS	O
AM10	VTT0	REF	
AM2	CFG[1]	CMOS	I
AM5	SM_DRAMPWROK	Async CMOS	I
AM7	VCCPWRGOOD_1	Async CMOS	I
AM8	VSS	GND	
AM64	VSS	GND	
AM66	RSVD		
AM67	GFX_VID[5]	CMOS	O
AM70	GFX_VID[6]	CMOS	O
AN1	VTT_SELECT	CMOS	O
AN4	VSS	GND	
AN5	VSS	GND	
AN7	RSVD_TP		

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AN9	VTT0	REF	
AN12	VTT0	REF	
AN14	VTT0	REF	
AN15	VTT0	REF	
AN17	VTT0	REF	
AN19	VAXG	REF	
AN21	VAXG	REF	
AN23	VAXG	REF	
AN24	VAXG	REF	
AN26	VAXG	REF	
AN28	VAXG	REF	
AN30	VAXG	REF	
AN32	VAXG	REF	
AN33	VTT0	REF	
AN35	VTT0	REF	
AN37	VSS	GND	
AN39	VCAP1	PWR	
AN41	VSS	GND	
AN42	VCAP1	PWR	
AN44	VSS	GND	
AN46	VCAP1	PWR	
AN48	VSS	GND	
AN50	VCAP0	PWR	
AN51	VSS	GND	
AN53	VCAP0	PWR	
AN55	VSS	GND	
AN57	VCAP0	PWR	
AN59	VTT0	REF	
AN60	VTT0	REF	
AN62	VSS	GND	
AN69	RSVD		
AN71	GFX_VID[4]	CMOS	O
AP2	RSVD_TP		
AP64	VSS	GND	
AP66	RSVD		
AP70	VSS	GND	

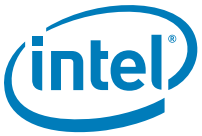


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AR1	VSS	GND	
AR4	VSS	GND	
AR12	VTT0	REF	
AR14	VSS	GND	
AR15	VSS	GND	
AR17	VSS	GND	
AR19	VSS	GND	
AR21	VSS	GND	
AR23	VSS	GND	
AR24	VSS	GND	
AR26	VSS	GND	
AR28	VSS	GND	
AR30	VSS	GND	
AR32	VSS	GND	
AR33	VSS	GND	
AR35	VSS	GND	
AR37	VCAP1	PWR	
AR39	VSS	GND	
AR41	VCAP1	PWR	
AR42	VSS	GND	
AR44	VCAP1	PWR	
AR46	VSS	GND	
AR48	VCAP0	PWR	
AR50	VSS	GND	
AR51	VCAP0	PWR	
AR53	VSS	GND	
AR55	VCAP0	PWR	
AR57	VSS	GND	
AR59	VTT0	REF	
AR60	VTT0	REF	
AR62	VSS	GND	
AR69	RSVD		
AR71	RSVD		
AT2	CFG[6]	CMOS	I
AT6	SA_DQ[1]	DDR3	I/O
AT8	SA_DQ[0]	DDR3	I/O

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AT10	VSS	GND	
AT64	VSS	GND	
AT67	RSVD		
AT70	RSVD		
AU1	RSVD_TP		
AU2	RSVD		
AU4	VSS	GND	
AU12	VTT0	REF	
AU14	VSS	GND	
AU15	VSS	GND	
AU17	VSS	GND	
AU19	VSS	GND	
AU21	VSS	GND	
AU23	VSS	GND	
AU24	VSS	GND	
AU26	VSS	GND	
AU28	VSS	GND	
AU30	VSS	GND	
AU32	VSS	GND	
AU33	VSS	GND	
AU35	VSS	GND	
AU37	VCAP1	PWR	
AU39	VSS	GND	
AU41	VCAP1	PWR	
AU42	VSS	GND	
AU44	VCAP1	PWR	
AU46	VSS	GND	
AU48	VCAP0	PWR	
AU50	VSS	GND	
AU51	VCAP0	PWR	
AU53	VSS	GND	
AU55	VCAP0	PWR	
AU57	VSS	GND	
AU59	VTT0	REF	
AU60	VTT0	REF	
AU62	VSS	GND	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AU69	RSVD		
AU70	VSS	GND	
AU71	RSVD		
AV1	VSS	GND	
AV4	RSVD		
AV6	SA_DQ[5]	DDR3	I/O
AV7	SA_DQ[4]	DDR3	I/O
AV9	VSS	GND	
AV64	PM_EXT_TS#[1]	CMOS	I/O
AV66	PM_EXT_TS#[0]	CMOS	I/O
AV69	RSVD		
AV71	RSVD		
AW12	VTT0	REF	
AW14	VTT0	REF	
AW15	VTT0_DDR	REF	
AW17	VTT0_DDR	REF	
AW19	VTT0_DDR	REF	
AW2	SB_DQ[1]	DDR3	I/O
AW21	VTT0_DDR	REF	
AW23	VTT0_DDR	REF	
AW24	VTT0_DDR	REF	
AW26	VTT0_DDR	REF	
AW28	VTT0_DDR	REF	
AW30	VTT0_DDR	REF	
AW32	VTT0_DDR	REF	
AW33	VTT0	REF	
AW35	VTT0	REF	
AW37	VSS	GND	
AW39	VCAP1	PWR	
AW41	VSS	GND	
AW42	VCAP1	PWR	
AW44	VSS	GND	
AW46	VCAP1	PWR	
AW48	VSS	GND	
AW50	VCAP0	PWR	
AW51	VSS	GND	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AW53	VCAP0	PWR	
AW55	VSS	GND	
AW57	VCAP0	PWR	
AW59	VSS	GND	
AW60	VTT0	REF	
AW62	VSS	GND	
AW67	VSS	GND	
AW70	RSVD	DDR3	I/O
AY1	SB_DQ[4]	DDR3	I/O
AY4	VSS	GND	
AY5	SA_DQS#[0]	DDR3	I/O
AY7	SA_DQS[0]	DDR3	I/O
AY8	VSS	GND	
AY10	VTT0	REF	
AY12	VSS	GND	
AY14	VSS	GND	
AY15	VSS	GND	
AY17	VSS	GND	
AY19	VSS	GND	
AY21	VSS	GND	
AY23	VSS	GND	
AY24	VSS	GND	
AY26	VSS	GND	
AY28	VSS	GND	
AY30	VSS	GND	
AY32	VSS	GND	
AY33	VSS	GND	
AY35	VSS	GND	
AY37	VSS	GND	
AY39	VCAP1	PWR	
AY41	VSS	GND	
AY42	VCAP1	PWR	
AY44	VSS	GND	
AY46	VCAP1	PWR	
AY48	VSS	GND	
AY50	VCAP0	PWR	

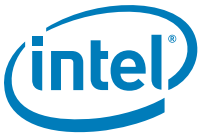


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
AY51	VSS	GND	
AY53	VCAP0	PWR	
AY55	VSS	GND	
AY57	VCAP0	PWR	
AY59	VSS	GND	
AY60	VTT0	REF	
AY62	VSS	GND	
AY64	SA_DQ[62]	DDR3	I/O
AY66	VSS	GND	
AY69	RSVD		
AY71	VSS	GND	
B7	RSVD		
B9	RSVD		
B11	PEG_RBIAS	Analog	I
B12	PEG_ICOMPI	Analog	I
B14	PEG_RX#[15]	PCIe	I
B16	PEG_RX[14]	PCIe	I
B18	PEG_RX[13]	PCIe	I
B19	PEG_RX[12]	PCIe	I
B21	PEG_RX[11]	PCIe	I
B23	PEG_RX#[10]	PCIe	I
B25	PEG_RX[9]	PCIe	I
B26	PEG_RX#[8]	PCIe	I
B28	PEG_RX[7]	PCIe	I
B30	PEG_TX[9]	PCIe	O
B32	PEG_TX#[10]	PCIe	O
B33	PEG_TX#[6]	PCIe	O
B35	PEG_TX#[7]	PCIe	O
B37	PEG_TX[4]	PCIe	O
B39	PEG_TX[3]	PCIe	O
B40	VSS	GND	
B42	VCC	REF	
B44	VSS	GND	
B46	VCC	REF	
B48	VSS	GND	
B49	VCC	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
B51	VSS	GND	
B53	VCC	REF	
B55	VSS	GND	
B56	VCC	REF	
B58	VSS	GND	
B60	VCC	REF	
B62	VSS	GND	
B63	CSC[1]/VID[4]	CMOS	I/O
B65	VSS	GND	
BA2	SB_DQ[0]	DDR3	I/O
BA70	VSS	GND	
BB1	VSS	GND	
BB4	SB_DM[0]	DDR3	O
BB5	SA_DQ[2]	DDR3	I/O
BB7	VSS	GND	
BB9	SA_DQ[3]	DDR3	I/O
BB10	SA_DM[0]	DDR3	O
BB12	VDDQ_CK	REF	
BB14	VDDQ_CK	REF	
BB15	VDDQ	REF	
BB17	VDDQ	REF	
BB19	VDDQ	REF	
BB21	VDDQ	REF	
BB23	VDDQ	REF	
BB24	VDDQ	REF	
BB26	VDDQ	REF	
BB28	VDDQ	REF	
BB30	VDDQ	REF	
BB32	VDDQ	REF	
BB33	VDDQ	REF	
BB35	VDDQ	REF	
BB37	VCAP1	PWR	
BB39	VSS	GND	
BB41	VCAP1	PWR	
BB42	VSS	GND	
BB44	VCAP1	PWR	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BB46	VSS	GND	
BB48	VCAP0	PWR	
BB50	VSS	GND	
BB51	VCAP0	PWR	
BB53	VSS	GND	
BB55	VCAP0	PWR	
BB57	VSS	GND	
BB59	VTT0	REF	
BB60	VTT0	REF	
BB62	VSS	GND	
BB64	SA_DQ[58]	DDR3	I/O
BB66	SA_DQ[59]	DDR3	I/O
BB69	RSVD		
BB71	VSS	GND	
BC2	SB_DQ[5]	DDR3	I/O
BC67	SB_DQ[59]	DDR3	I/O
BC70	SA_DQ[63]	DDR3	I/O
BD1	SB_DQ[2]	DDR3	I/O
BD4	SB_DQS[0]	DDR3	I/O
BD14	VSS	GND	
BD15	VDDQ	REF	
BD17	VDDQ	REF	
BD19	VDDQ	REF	
BD21	VDDQ	REF	
BD23	VDDQ	REF	
BD24	VDDQ	REF	
BD26	VDDQ	REF	
BD28	VDDQ	REF	
BD30	VDDQ	REF	
BD32	VDDQ	REF	
BD33	VDDQ	REF	
BD35	VDDQ	REF	
BD37	VCAP1	PWR	
BD39	VSS	GND	
BD41	VCAP1	PWR	
BD42	VSS	GND	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BD44	VCAP1	PWR	
BD46	VSS	GND	
BD48	VCAP0	PWR	
BD50	VSS	GND	
BD51	VCAP0	PWR	
BD53	VSS	GND	
BD55	VCAP0	PWR	
BD57	VSS	GND	
BD59	VTT0	REF	
BD60	VTT0	REF	
BD69	SB_DQ[63]	DDR3	I/O
BD71	SB_DQ[62]	DDR3	I/O
BE1	VSS	GND	
BE2	SB_DQS#[0]	DDR3	I/O
BE4	SB_DQ[3]	DDR3	I/O
BE6	SA_DQ[6]	DDR3	I/O
BE8	SA_DQ[7]	DDR3	I/O
BE9	VSS	GND	
BE11	SA_DQ[9]	DDR3	I/O
BE62	SA_DQS#[7]	DDR3	I/O
BE64	SA_DQS[7]	DDR3	I/O
BE65	VSS	GND	
BE69	RSVD		
BE70	VSS	GND	
BE71	RSVD		
BF2	SB_DQ[6]	DDR3	I/O
BF6	SA_DQ[13]	DDR3	I/O
BF8	VSS	GND	
BF9	SA_DQ[12]	DDR3	I/O
BF11	SA_DQ[8]	DDR3	I/O
BF13	VSS	GND	
BF15	VDDQ	REF	
BF16	VDDQ	REF	
BF20	SA_CKE[0]	DDR3	O
BF21	SA_BS[2]	DDR3	O
BF28	SA_MA[9]	DDR3	O

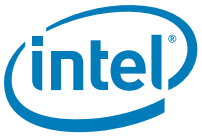


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BF30	VSS	GND	
BF38	SA_WE#	DDR3	O
BF40	SA_MA[13]	DDR3	O
BF43	SA_ODT[0]	DDR3	O
BF47	SA_DQ[34]	DDR3	I/O
BF48	SA_DQ[35]	DDR3	I/O
BF55	SA_DQ[48]	DDR3	I/O
BF57	SA_DQ[52]	DDR3	I/O
BF59	VTT0	REF	
BF60	VTT0	REF	
BF62	VSS	GND	
BF64	SA_DQ[57]	DDR3	I/O
BF65	SA_DQ[61]	DDR3	I/O
BF67	SB_DM[7]	DDR3	O
BF70	SB_DQ[57]	DDR3	I/O
BG1	SB_DQ[9]	DDR3	I/O
BG4	SB_DQ[8]	DDR3	I/O
BG15	SA_DQ[21]	DDR3	I/O
BG17	SA_DQ[18]	DDR3	I/O
BG24	SA_DQ[30]	DDR3	I/O
BG25	SA_DQ[31]	DDR3	I/O
BG32	SA_MA[4]	DDR3	O
BG34	SA_MA[3]	DDR3	O
BG36	VSS	GND	
BG43	VDDQ	REF	
BG44	SA_DM[4]	DDR3	O
BG51	VSS	GND	
BG53	SA_DM[5]	DDR3	O
BG69	SB_DQS#[7]	DDR3	I/O
BG71	SB_DQ[58]	DDR3	I/O
BH2	SB_DQ[7]	DDR3	I/O
BH13	SA_DQ[11]	DDR3	I/O
BH15	VSS	GND	
BH17	SA_DQ[22]	DDR3	I/O
BH20	VSS	GND	
BH21	SA_DQ[29]	DDR3	I/O

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BH24	VSS	GND	
BH25	SA_DQ[27]	DDR3	I/O
BH28	VDDQ	REF	
BH30	SA_MA[11]	DDR3	O
BH32	VDDQ	REF	
BH34	SA_MA[10]	DDR3	O
BH36	SA_CK#[1]	DDR3	O
BH38	SA_BS[1]	DDR3	O
BH40	SA_CS#[0]	DDR3	O
BH43	SA_DQ[37]	DDR3	I/O
BH44	SA_DQS#[4]	DDR3	I/O
BH47	VSS	GND	
BH48	SA_DQ[44]	DDR3	I/O
BH51	SA_DQS[5]	DDR3	I/O
BH53	SA_DQ[42]	DDR3+C285	I/O
BH55	VSS	GND	
BH57	VSS	GND	
BH59	SA_DM[7]	DDR3	I/O
BH70	VSS	GND	
BJ1	VSS	GND	
BJ4	SB_DQ[12]	DDR3	I/O
BJ5	SA_DQS[1]	DDR3	I/O
BJ7	SA_DQS#[1]	DDR3	I/O
BJ9	VSS	GND	
BJ10	SA_DM[1]	DDR3	I/O
BJ12	SM_DRAMRST#	DDR3	O
BJ20	SA_DQ[28]	DDR3	I/O
BJ21	VSS	GND	
BJ28	SA_MA[12]	DDR3	O
BJ30	SA_MA[7]	DDR3	O
BJ38	VDDQ	REF	
BJ40	SA_DQ[32]	DDR3	I/O
BJ47	SA_CS#[1]	DDR3	I/O
BJ48	SA_DQ[45]	DDR3	I/O
BJ55	SA_DQ[43]	DDR3	I/O
BJ57	SA_DQ[53]	DDR3	I/O

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BJ61	SA_DQ[51]	DDR3	I/O
BJ63	SA_DQ[56]	DDR3	I/O
BJ64	VSS	GND	
BJ66	SA_DQ[60]	DDR3	I/O
BJ69	SB_DQS[7]	DDR3	I/O
BJ71	SB_DQ[56]	DDR3	I/O
BK2	SB_DQ[13]	DDR3	I/O
BK5	SA_DQ[10]	DDR3	I/O
BK7	SA_DQ[14]	DDR3	I/O
BK9	SA_DQ[20]	DDR3	I/O
BK10	VSS	GND	
BK15	SA_DQ[19]	DDR3	I/O
BK17	SA_DQ[23]	DDR3	I/O
BK24	SA_CKE[1]	DDR3	O
BK25	SA_DQ[26]	DDR3	I/O
BK32	SA_MA[6]	DDR3	O
BK34	VSS	GND	
BK36	SA_CK[1]	DDR3	O
BK43	SA_CAS#	DDR3	O
BK44	SA_DQS[4]	DDR3	I/O
BK51	SA_DQS#[5]	DDR3	I/O
BK53	VSS	GND	
BK60	VSS	GND	
BK61	SA_DQ[55]	DDR3	I/O
BK63	VSS	GND	
BK64	SA_DQ[54]	DDR3	I/O
BK67	SB_DQ[61]	DDR3	I/O
BK70	SB_DQ[60]	DDR3	I/O
BL1	VSS	GND	
BL4	SB_DM[1]	DDR3	O
BL13	SA_DQS[2]	DDR3	I/O
BL20	VSS	GND	
BL21	SA_DQS#[3]	DDR3	I/O
BL28	VSS	GND	
BL30	VDDQ	REF	
BL38	SA_RAS#	DDR3	O

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BL40	VSS	GND	
BL47	SA_ODT[1]	DDR3	O
BL48	VSS	GND	
BL55	VSS	GND	
BL57	VSS	GND	
BL69	SB_DQ[55]	DDR3	I/O
BL71	VSS	GND	
BM3	SB_DQS#[1]	DDR3	I/O
BM15	SA_DM[2]	DDR3	O
BM17	VSS	GND	
BM24	VSS	GND	
BM25	VDDQ	REF	
BM32	VSS	GND	
BM34	SA_CK[0]	DDR3	O
BM43	SA_DQ[33]	DDR3	I/O
BM44	VSS	GND	
BM51	VSS	GND	
BM53	SA_DQ[46]	DDR3	I/O
BM60	SA_DQS[6]	DDR3	I/O
BM70	VSS	GND	
BN1	VSS	GND	
BN4	SB_DQS[1]	DDR3	I/O
BN6	VSS	GND	
BN8	SA_DQ[15]	DDR3	I/O
BN9	SA_DQ[17]	DDR3	I/O
BN11	SA_DQ[16]	DDR3	I/O
BN13	SA_DQS#[2]	DDR3	I/O
BN17	SA_DQ[25]	DDR3	I/O
BN20	SA_DQ[24]	DDR3	I/O
BN21	SA_DQS[3]	DDR3	I/O
BN24	SA_DM[3]	DDR3	O
BN25	SA_MA[15]	DDR3	O
BN28	SA_MA[14]	DDR3	O
BN30	SA_MA[8]	DDR3	O
BN32	SA_MA[5]	DDR3	O
BN38	VDDQ	REF	

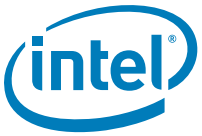


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BN40	SA_DQ[36]	DDR3	I/O
BN44	SA_DQ[38]	DDR3	I/O
BN47	SA_DQ[39]	DDR3	I/O
BN48	SA_DQ[40]	DDR3	I/O
BN51	SA_DQ[41]	DDR3	I/O
BN55	SA_DQ[47]	DDR3	I/O
BN57	SA_DQ[49]	DDR3	I/O
BN62	SA_DM[6]	DDR3	O
BN64	VSS	GND	
BN65	SA_DQ[50]	DDR3	I/O
BN68	SB_DQ[54]	DDR3	I/O
BN71	VSS	GND	
BP12	SB_DQ[21]	DDR3	I/O
BP15	SB_DQ[24]	DDR3	I/O
BP19	SB_DQ[28]	DDR3	I/O
BP22	SB_DM[3]	DDR3	O
BP26	SB_MA[7]	DDR3	O
BP30	SB_MA[1]	DDR3	O
BP33	SA_MA[1]	DDR3	O
BP35	SA_CK#[0]	DDR3	O
BP39	SM_RCOMP[1]	Analog	
BP42	VSS	GND	
BP46	SB_CS#[0]	DDR3	O
BP49	SB_DQ[35]	DDR3	I/O
BP53	SB_DQ[40]	DDR3	I/O
BP56	SB_DQ[44]	DDR3	I/O
BP58	SA_DQS#[6]	DDR3	I/O
BP60	SB_DQ[49]	DDR3	I/O
BR1	DC_TEST_BR1		
BR3	VSS	GND	
BR5	RSVD_TP		
BR6	SB_DQ[10]	DDR3	I/O
BR8	SB_DQ[11]	DDR3	I/O
BR10	SB_DQ[16]	DDR3	I/O
BR62	SB_DQ[52]	DDR3	I/O
BR64	SB_DQ[51]	DDR3	I/O

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BR66	SB_DQ[50]	DDR3	I/O
BR68	VSS	GND	
BR69	VSS	GND	
BR71	DC_TEST_BR71		
BT1	DC_TEST_BT1		
BT3	DC_TEST_BT3		
BT5	RSVD_NCTF		
BT12	SB_DQ[17]	DDR3	I/O
BT13	SB_DM[2]	DDR3	O
BT15	SB_DQ[18]	DDR3	I/O
BT17	SB_DQS[3]	DDR3	I/O
BT19	SB_DQS#[3]	DDR3	I/O
BT20	SB_DQ[31]	DDR3	I/O
BT22	SB_DQ[27]	DDR3	I/O
BT24	SB_CKE[1]	DDR3	O
BT26	SB_CKE[0]	DDR3	O
BT27	SB_MA[9]	DDR3	O
BT29	SB_MA[12]	DDR3	O
BT31	SB_MA[6]	DDR3	O
BT33	SB_MA[5]	DDR3	O
BT34	SB_MA[0]	DDR3	O
BT36	SA_MA[0]	DDR3	O
BT38	SA_BS[0]	DDR3	O
BT40	SB_RAS#	DDR3	O
BT41	SB_WE#	DDR3	O
BT43	SB_CS#[1]	DDR3	O
BT45	SB_MA[13]	DDR3	O
BT47	SB_DQ[36]	DDR3	I/O
BT48	SB_DQ[32]	DDR3	I/O
BT50	SB_DQS[4]	DDR3	I/O
BT52	SB_DQS#[4]	DDR3	I/O
BT54	SB_DQ[39]	DDR3	I/O
BT55	SB_DQ[45]	DDR3	I/O
BT57	SB_DQ[43]	DDR3	I/O
BT59	SB_DQ[42]	DDR3	I/O
BT61	SB_DQ[53]	DDR3	I/O

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BT68	VSS	GND	
BT69	DC_TEST_BT69		
BT71	DC_TEST_BT71		
BU7	VSS	GND	
BU9	SB_DQ[14]	DDR3	I/O
BU11	VSS	GND	
BU12	SB_DQS#[2]	DDR3	I/O
BU14	VSS	GND	
BU16	SB_DQ[23]	DDR3	I/O
BU18	VSS	GND	
BU19	SB_DQ[25]	DDR3	I/O
BU21	VSS	GND	
BU23	SB_MA[15]	DDR3	O
BU25	VSS	GND	
BU26	SB_MA[11]	DDR3	O
BU28	VDDQ	REF	
BU30	SB_MA[3]	DDR3	O
BU32	VSS	GND	
BU33	SB_CK[0]	DDR3	O
BU35	VDDQ	REF	
BU37	VSS	GND	
BU39	SB_CK#[1]	DDR3	O
BU40	VDDQ	REF	
BU42	SB_MA[10]	DDR3	O
BU44	VSS	GND	
BU46	SB_CAS#	DDR3	O
BU48	VSS	GND	
BU49	SB_ODT[1]	DDR3	O
BU51	VSS	GND	
BU53	SB_DQ[41]	DDR3	I/O
BU55	VSS	GND	
BU56	SB_DQS[5]	DDR3	I/O
BU58	VSS	GND	
BU60	SB_DQ[46]	DDR3	I/O
BU62	VSS	GND	
BU63	SB_DQS#[6]	DDR3	I/O

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BU65	SB_DM[6]	DDR3	O
BV1	DC_TEST_BV1		
BV3	DC_TEST_BV3		
BV5	DC_TEST_BV5		
BV6	RSVD_NCTF		
BV8	RSVD_NCTF		
BV10	SB_DQ[15]	DDR3	I/O
BV12	SB_DQ[20]	DDR3	I/O
BV13	SB_DQS[2]	DDR3	I/O
BV15	SB_DQ[19]	DDR3	I/O
BV17	SB_DQ[22]	DDR3	I/O
BV19	SB_DQ[29]	DDR3	I/O
BV20	SB_DQ[30]	DDR3	I/O
BV22	SB_DQ[26]	DDR3	I/O
BV24	SB_BS[2]	DDR3	O
BV26	SB_MA[14]	DDR3	O
BV27	SB_MA[8]	DDR3	O
BV29	SB_MA[2]	DDR3	O
BV31	SB_MA[4]	DDR3	O
BV33	SM_RCOMP[0]	Analog	I
BV34	SB_CK#[0]	DDR3	O
BV36	SA_MA[2]	DDR3	O
BV38	SB_CK[1]	DDR3	O
BV40	SM_RCOMP[2]	Analog	I
BV41	SB_BS[1]	DDR3	O
BV43	SB_BS[0]	DDR3	O
BV45	SB_ODT[0]	DDR3	O
BV47	SB_DM[4]	DDR3	O
BV48	SB_DQ[33]	DDR3	I/O
BV50	SB_DQ[34]	DDR3	I/O
BV52	SB_DQ[37]	DDR3	I/O
BV54	SB_DQ[38]	DDR3	I/O
BV55	SB_DQS#[5]	DDR3	I/O
BV57	SB_DM[5]	DDR3	O
BV59	SB_DQ[47]	DDR3	I/O
BV61	SB_DQ[48]	DDR3	I/O

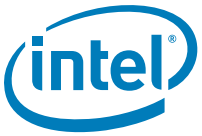


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
BV62	SB_DQS[6]	DDR3	I/O
BV64	VSS	GND	
BV66	VSS	GND	
BV68	DC_TEST_BV68		
BV69	DC_TEST_BV69		
BV71	DC_TEST_BV71		
C3	DC_TEST_C3		
C5	RSVD_NCTF		
C68	VSS	GND	
C69	DC_TEST_C69		
C71	DC_TEST_C71		
D6	VSS	GND	
D8	RSVD		
D10	VSS	GND	
D12	PEG_RCOMPO	Analog	I
D13	VSS	GND	
D15	PEG_RX[15]	PCIe	I
D17	VSS	GND	
D19	PEG_RX#[13]	PCIe	I
D20	VSS	GND	
D22	PEG_RX#[11]	PCIe	I
D24	VSS	GND	
D26	PEG_RX#[9]	PCIe	I
D27	VSS	GND	
D29	PEG_RX#[7]	PCIe	I
D31	VSS	GND	
D33	PEG_TX[10]	PCIe	O
D34	VSS	GND	
D36	PEG_TX[7]	PCIe	O
D38	VSS	GND	
D40	PEG_TX#[3]	PCIe	O
D41	VSS	GND	
D43	VCC	REF	
D45	VCC	REF	
D47	VCC	REF	
D48	VCC	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
D50	VCC	REF	
D52	VCC	REF	
D54	VCC	REF	
D55	VCC	REF	
D57	VCC	REF	
D59	VCC	REF	
D61	VID[1]	CMOS	O
D62	VID[2]	CMOS	O
D64	CSC[2]/VID[5]	CMOS	I/O
D66	VID[6]	CMOS	O
E1	DC_TEST_E1		
E3	RSVD_NCTF		
E5	VSS	GND	
E12	VSS	GND	
E16	VSS	GND	
E30	VSS	GND	
E33	VSS	GND	
E37	VSS	GND	
E42	VCC	REF	
E46	VCC	REF	
E50	VCC	REF	
E53	VCC	REF	
E57	VCC	REF	
E60	VCC	REF	
E68	VSS	GND	
E69	VSS	GND	
E71	DC_TEST_E71		
F1	RSVD_NCTF		
F4	VSS	GND	
F7	DMI_RX#[0]	DMI	I
F9	DMI_RX[0]	DMI	I
F10	DMI_TX#[3]	DMI	O
F20	VSS	GND	
F21	PEG_TX[14]	PCIe	O
F28	VSS	GND	
F40	PEG_RX[0]	PCIe	I

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
F47	VSS	GND	
F48	VSS	GND	
F55	VCC	REF	
F61	VSS	GND	
F63	VSS_SENSE	Analog	O
F64	VCC_SENSE	Analog	O
F66	PROC_DPRSLPVR	CMOS	O
F68	PSI#	Async CMOS	O
F71	VSS	GND	
G3	RSTIN#	CMOS	I
G13	DMI_TX[2]	DMI	O
G15	VSS	GND	
G17	DMI_TX[0]	DMI	O
G20	VSS	GND	
G21	PEG_TX#[14]	PCIe	O
G24	VSS	GND	
G25	PEG_RX[5]	PCIe	I
G28	PEG_RX#[4]	PCIe	I
G30	VSS	GND	
G32	PEG_TX#[5]	PCIe	O
G34	PEG_RX[2]	PCIe	I
G38	PEG_RX#[1]	PCIe	I
G40	PEG_RX#[0]	PCIe	I
G43	VSS	GND	
G44	VCC	REF	
G47	VSS	GND	
G48	VSS	GND	
G51	VCC	REF	
G53	VSS	GND	
G55	VCC	REF	
G57	VSS	GND	
G60	VCC	REF	
G70	VSS	GND	
H1	VSS	GND	
H15	VTTPWRGOOD	Async CMOS	I

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
H17	DMI_TX#[0]	DMI	O
H24	PEG_RX#[6]	PCIe	I
H25	PEG_RX#[5]	PCIe	I
H32	PEG_TX[5]	PCIe	O
H34	PEG_RX#[2]	PCIe	I
H36	VSS	GND	
H43	VSS	GND	
H44	VCC	REF	
H51	VCC	REF	
H53	VSS	GND	
H60	VCC	REF	
H71	VSS	GND	
J11	DMI_TX[3]	DMI	O
J13	DMI_TX#[2]	DMI	O
J2	DMI_RX[3]	DMI	I
J4	DMI_RX#[3]	DMI	I
J6	DMI_RX[1]	DMI	I
J8	DMI_RX#[1]	DMI	I
J9	VSS	GND	
J20	PEG_TX#[15]	PCIe	O
J21	PEG_CLK#	DIFF CLK	I
J28	PEG_RX[4]	PCIe	I
J30	PEG_TX[8]	PCIe	O
J38	PEG_RX[1]	PCIe	I
J40	VSS	GND	
J47	VSS	GND	
J48	VSS	GND	
J55	VCC	REF	
J57	VSS	GND	
J62	BPM#[2]	GTL	I/O
J64	BPM#[5]	GTL	I/O
J65	VSS	GND	
J67	BPM#[1]	GTL	I/O
J69	BPM#[0]	GTL	I/O
J70	BCLK_ITP #	DIFF CLK	O
K1	FDI_TX[0]	FDI	O

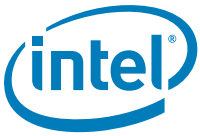


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
K4	VSS	GND	
K6	VSS	GND	
K8	DMI_RX#[2]	DMI	I
K9	DMI_RX[2]	DMI	I
K11	VSS	GND	
K15	DMI_TX#[1]	DMI	O
K17	VSS	GND	
K24	PEG_RX[6]	PCIe	I
K25	VSS	GND	
K32	VSS	GND	
K34	VSS	GND	
K36	VSS	GND	
K43	VSS	GND	
K44	VCC	REF	
K51	VCC	REF	
K53	VSS	GND	
K60	VCC	REF	
K62	BPM#[4]	GTL	I/O
K64	VSS	GND	
K65	BPM#[3]	GTL	I/O
K69	BPM#[6]	GTL	I/O
K71	BCLK_ITP	DIFF CLK	O
L2	FDI_TX#[0]	FDI	O
L13	VSS	GND	
L20	PEG_TX[15]	PCIe	O
L21	PEG_CLK	Diff CLK	I
L28	PEG_TX#[11]	PCIe	O
L30	PEG_TX#[8]	PCIe	O
L38	PEG_TX#[1]	PCIe	O
L40	PEG_TX[0]	PCIe	O
L47	VSS	GND	
L48	VSS	GND	
L55	VCC	REF	
L57	VSS	GND	
L70	VSS	GND	
M1	VSS	GND	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
M4	FDI_TX#[2]	FDI	O
M15	DMI_TX[1]	DMI	O
M17	PM_SYNC	CMOS	I
M24	PEG_TX#[13]	PCIe	O
M25	PEG_TX[12]	PCIe	O
M32	PEG_TX#[2]	PCIe	O
M34	PEG_RX[3]	PCIe	I
M36	VSS	GND	
M42	VSS	GND	
M44	VCC	REF	
M51	VCC	REF	
M53	VSS	GND	
M60	VCC	REF	
M69	BPM#[7]	GTL	I/O
M71	PROC_DETECT		
N2	FDI_TX[2]	FDI	O
N5	FDI_TX[1]	FDI	O
N7	FDI_TX#[1]	FDI	O
N9	FDI_TX[4]	FDI	O
N10	FDI_TX#[4]	FDI	O
N13	VTT_SENSE	Analog	O
N15	VSS	GND	
N17	THERMTRIP#	Async GTL	O
N19	PECI	Async	I/O
N21	VSS	GND	
N24	PEG_TX[13]	PCIe	O
N26	PEG_TX#[12]	PCIe	O
N28	PEG_TX[11]	PCIe	O
N30	VSS	GND	
N32	PEG_TX[2]	PCIe	O
N38	PEG_TX[1]	PCIe	O
N40	PEG_TX#[0]	PCIe	O
N42	VCC	REF	
N44	VCC	REF	
N46	VSS	GND	
N48	VCC	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
N50	VSS	GND	
N51	VCC	REF	
N53	VSS	GND	
N55	VCC	REF	
N57	VSS	GND	
N61	CATERR#	GTL	I/O
N63	VSS	GND	
N65	TMS	CMOS	I
N67	PROCHOT#	Async GTL	I/O
N70	RESET_OBS#	Async CMOS	O
P1	FDI_TX#[3]	FDI	O
P4	VSS	GND	
P34	PEG_RX#[3]	PCIe	I
P60	VCC	REF	
P69	TRST#	CMOS	I
P71	TDI_M	CMOS	I
R2	FDI_TX[3]	FDI	O
R5	VSS	GND	
R7	FDI_TX#[5]	FDI	O
R8	FDI_TX[5]	FDI	O
R12	VSS_SENSE_VTT	Analog	O
R14	VSS	GND	
R15	VTT1	REF	
R17	VTT1	REF	
R19	VTT1	REF	
R21	VTT1	REF	
R23	VTT0	REF	
R24	VTT0	REF	
R26	VTT0	REF	
R28	VTT0	REF	
R30	VTT0	REF	
R32	VTT0	REF	
R33	VTT0	REF	
R35	VTT0	REF	
R37	VCCPLL	REF	
R39	VCCPLL	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
R41	VCC	REF	
R42	VSS	GND	
R44	VCC	REF	
R46	VSS	GND	
R48	VCC	REF	
R50	VSS	GND	
R51	VCC	REF	
R53	VSS	GND	
R55	VCC	REF	
R57	VSS	GND	
R59	VCAP2	PWR	
R60	VCAP2	PWR	
R62	VSS	GND	
R64	RSVD		
R66	RSVD		
R70	VSS	GND	
T1	VSS	GND	
T2	RSVD		
T4	RSVD		
U6	FDI_TX[6]	FDI	O
U7	FDI_TX#[6]	FDI	O
U9	VSS	GND	
T67	TCK	CMOS	I
T69	TDI	CMOS	I
T70	TDO_M	CMOS	O
T71	TDO	CMOS	O
U1	RSVD		
U4	VSS	GND	
U12	VTT1	REF	
U14	VTT1	REF	
U15	VTT1	REF	
U17	VTT1	REF	
U19	VTT1	REF	
U21	VTT1	REF	
U23	VTT0	REF	
U24	VTT0	REF	

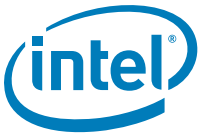


Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
U26	VTT0	REF	
U28	VTT0	REF	
U30	VTT0	REF	
U32	VTT0	REF	
U33	VTT0	REF	
U35	VTT0	REF	
U37	VCCPLL	REF	
U39	VSS	GND	
U41	VCC	REF	
U42	VSS	GND	
U44	VCC	REF	
U46	VSS	GND	
U48	VCC	REF	
U50	VSS	GND	
U51	VCC	REF	
U53	VSS	GND	
U55	VCC	REF	
U57	VSS	GND	
U59	VCAP2	PWR	
U60	VCAP2	PWR	
U62	VSS	GND	
U64	VSS	GND	
U69	PREQ#	Async GTL	I
U71	PRDY#	Async GTL	O
V2	RSVD		
V70	VSS	GND	
W1	VSS	GND	
W4	DPLL_REF_SSCLK#	DIFF CLK	I
W6	VSS	GND	
W8	FDI_TX#[7]	FDI	O
W10	FDI_TX[7]	FDI	O
W12	VTT1	REF	
W14	VTT1	REF	
W15	VTT1	REF	
W17	VTT1	REF	
W19	VTT1	REF	

Table 71. BGA1288 Processor Ball List by Ball Number

Pin #	Pin Name	Buffer Type	Dir
W21	VTT1	REF	
W23	VTT0	REF	
W24	VTT0	REF	
W26	VTT0	REF	
W28	VTT0	REF	
W30	VTT0	REF	
W32	VTT0	REF	
W33	VTT0	REF	
W35	VTT0	REF	
W37	VCCPLL	REF	
W39	VCCPLL	REF	
W41	VCC	REF	
W42	VSS	GND	
W44	VCC	REF	
W46	VSS	GND	
W48	VCC	REF	
W50	VSS	GND	
W51	VCC	REF	
W53	VSS	GND	
W55	VCC	REF	
W57	VSS	GND	
W59	VCAP2	PWR	
W60	VCAP2	PWR	
W62	VSS	GND	
W64	VCAP0_VSS_SENSE		
W66	VCAP0_SENSE		
W69	VSS	GND	
W71	DBR#		O
Y2	DPLL_REF_SSCLK	DIFF CLK	I
Y67	VCCPWRGOOD_0	Async CMOS	I
Y70	TAPPWRGOOD	Async CMOS	O

8.2 Package Mechanical Information

Figure 38. Arrandale rPGA Mechanical Package (Sheet 1 of 2)

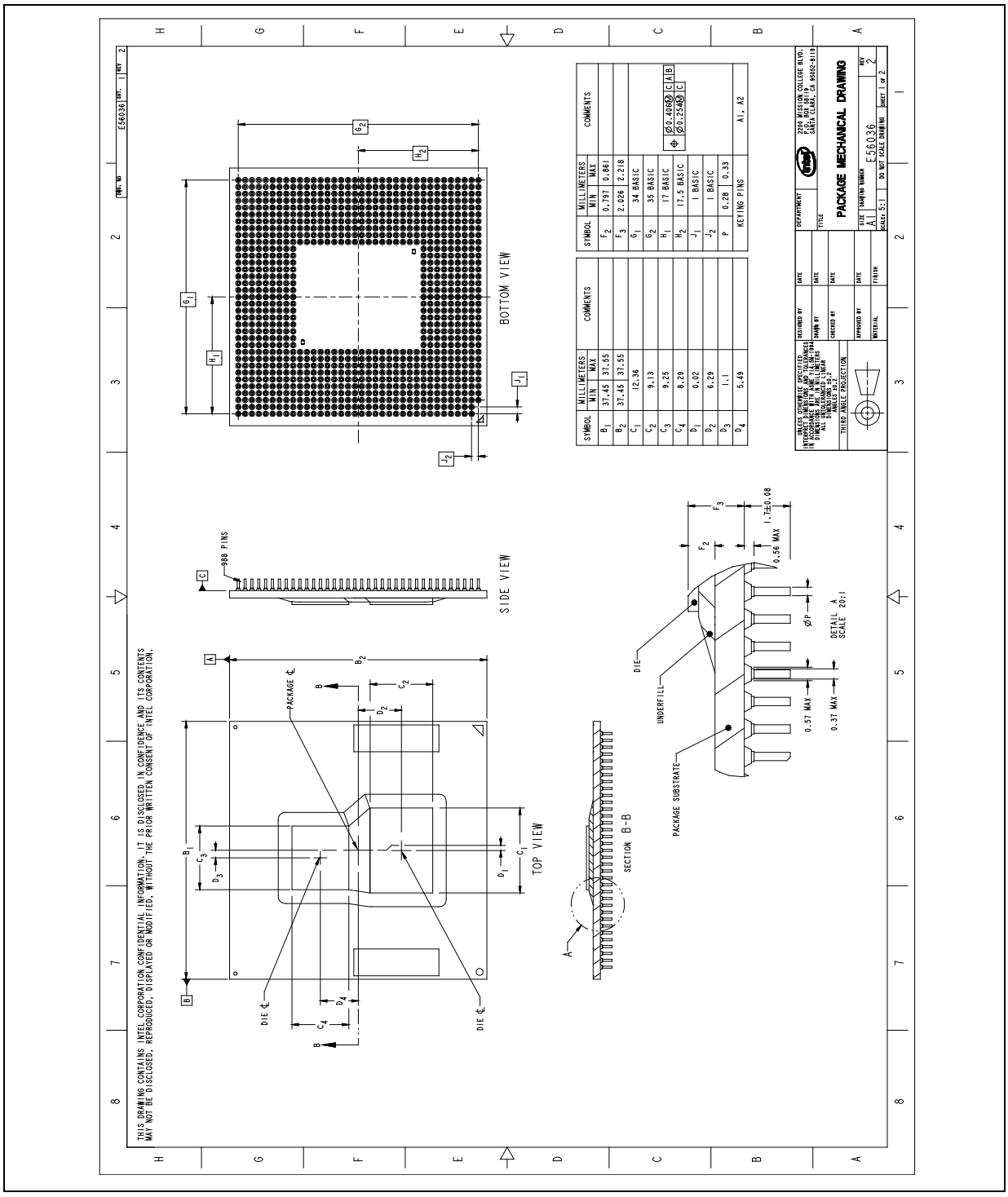


Figure 39. Arrandale rPGA Mechanical Package (Sheet 2 of 2)

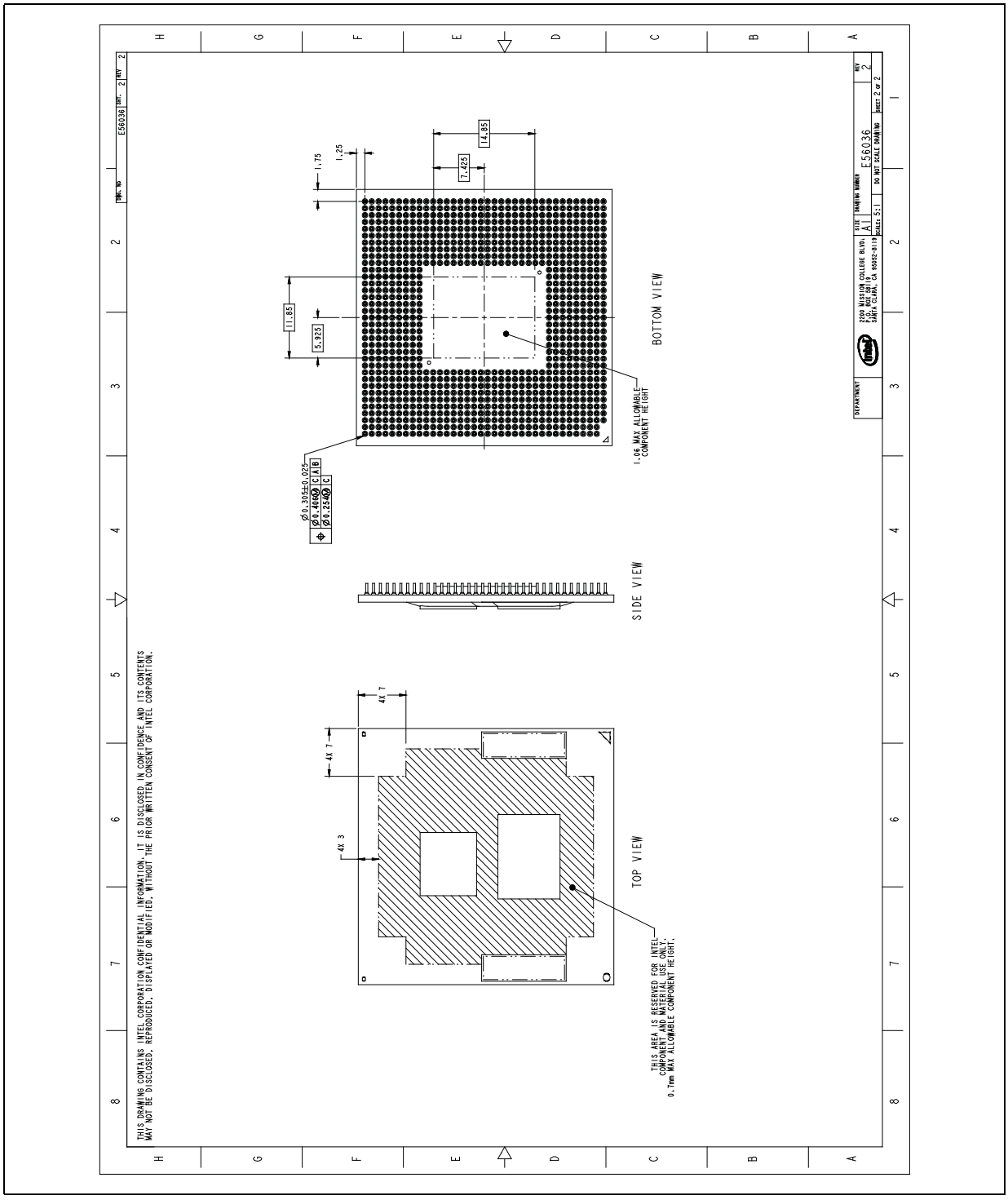


Figure 40. Arrandale BGA Mechanical Package (Sheet 1 of 2)

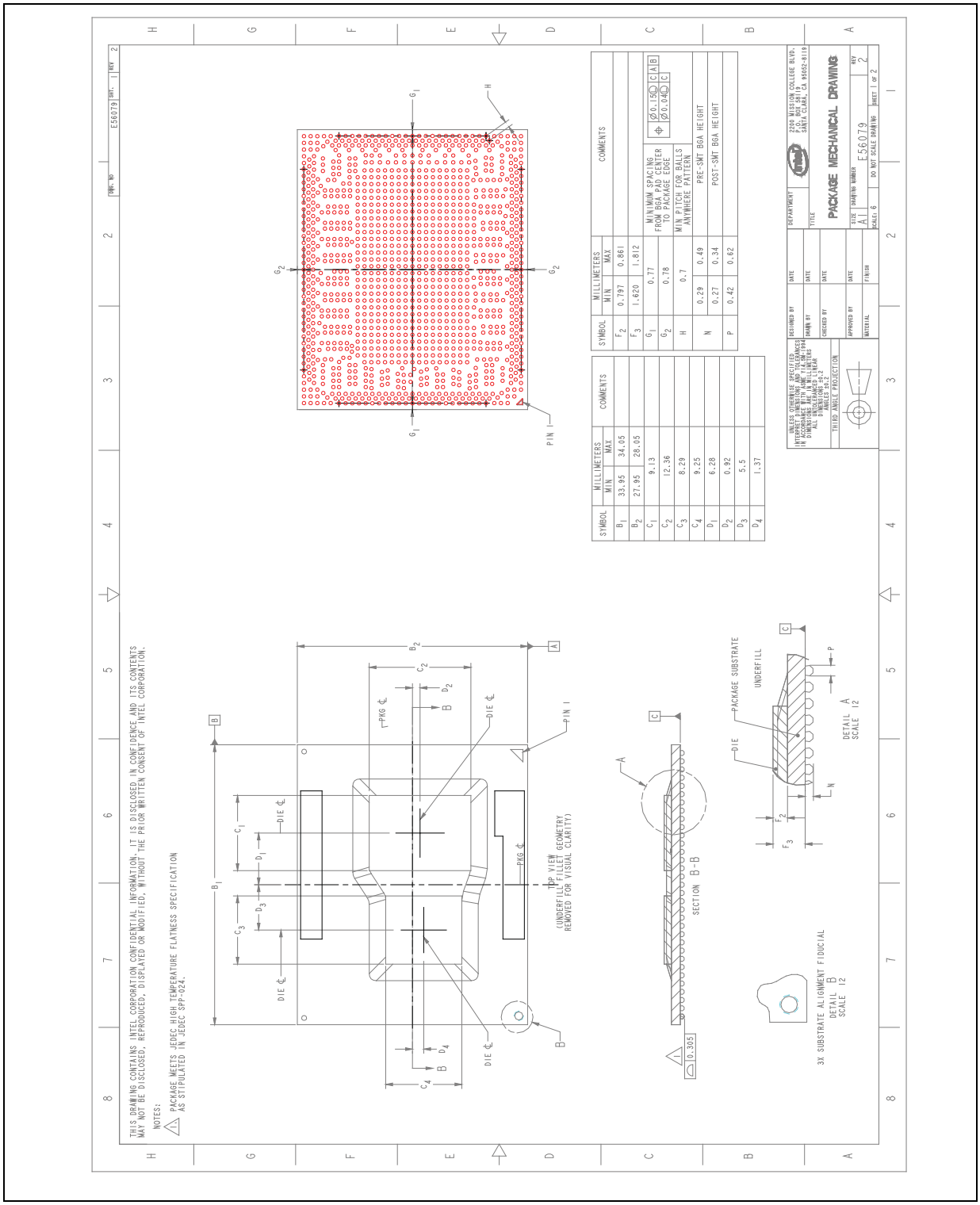
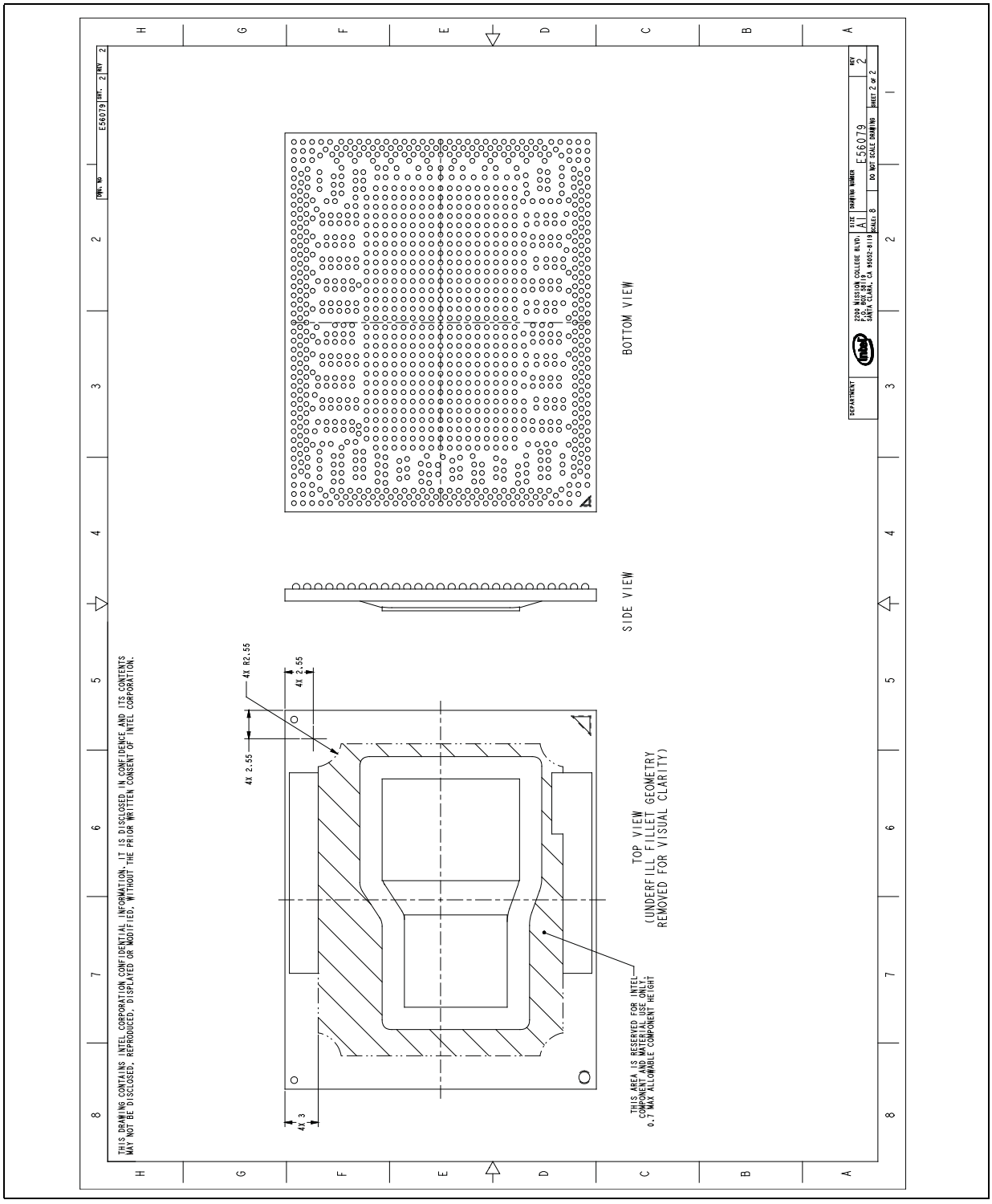


Figure 41. Arrandale BGA Mechanical Package (Sheet 2 of 2)



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9 Testability

The processor includes boundary-scan for board and system level testability. Refer to the *[Calpella] Program Auburndale and Clarksfield Processor Testability Information – Boundary Scan Description Language (BSDL) File – Rev. 1.1* for more details on testability.

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