ON Semiconductor®

Product Bulletin

Document # :PB21785X
Issue Date: 17 July 2017

Title of Change:	Datasheet Corrections for AR0238: 1/2.7-Inch 2.1 Mp/Full HD Digital Image Sensor.
Effective date:	17 July 2017
Contact information:	Contact your local ON Semiconductor Sales Office or <Sonya.Yip@onsemi.com>
Type of notification:	ON Semiconductor will consider this change accepted.
Change category:	☐ Wafer Fab Change ☐ Assembly Change ☐ Test Change ☒ Other _____

Change Sub-Category(s):
☐ Manufacturing Site Change/Addition
☐ Manufacturing Process Change
☐ Material Change
☐ Product specific change
☒ Datasheet/Product Doc change
☐ Shipping/Packaging/Marking
☐ Other: _____

Sites Affected:
☒ All site(s) ☐ not applicable
☐ ON Semiconductor site(s) :
☐ External Foundry/Subcon site(s)

Description and Purpose:

Datasheet updated to include RGB-IR and recon die information. This includes the addition of new parts numbers and the updating of information to fit RGB-IR part.

AR0238 Datasheet Changes

1. Added RGB-IR to Color Filter Array in "Table 1, Key Parameters"
Old Table 1:

Table 1:	Key Parameters
Color filter array	RGB Bayer

New Table 1:

Table 1. KEY PARAMETERS	
Color filter array	RGB Bayer, RGB–IR

2. Removed iBGA and added Recon Die to Package Options in "Table 1, Key Parameters"

Old Table 1:

Table 1:	Key Parameters
Package options	10x10 mm 80-pin iBGA 11.43x11.43 mm 48-pin mPLCC

New Table 1:

Table 1. KEY PARAMETERS	
Package options	11.43x11.43 mm 48–pin mPLCC Recon Die

3. Added Recon Die and RGB-IR part numbers to "Table 2, Available Part Numbers"

Old Table 2:

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
AR0238CSSC12SHRA0-DR-E	2 Mp 1/3" CIS RGB, 12deg CRA, mPLCC Package	Without protective film
AR0238CSSC12SHRA0-DP-E	2 Mp 1/3" CIS RGB, 12deg CRA, mPLCC Package	With protective film
AR0238CSSC12SHRAH3-GEVB	2MP 1/3 CIS RGB, 12 deg, mPLCC (HiSpi)	Headboard
AR0238CSSC12SHRAD3-GEVK	2MP 1/3 CIS RGB, 12 deg, mPLCC (HiSpi)	Evaluation Kit
AR0238CSSC12SPRA0-DR	2MP 1/3 CIS RGB, 12 deg CRA, mPLCC (Parallel)	Without Protective Film

See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

New Table 2:

Table 2. ORDERING INFORMATION

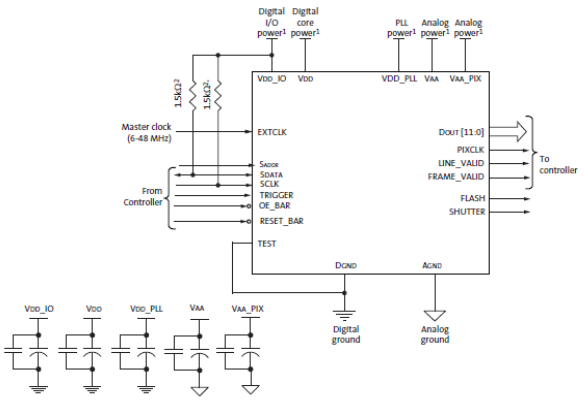
Part Number	Product Description	Orderable Product Attribute Description
AR0238CSSC12SHRA0–DR–E	2 Mp 1/3" CIS RGB, 12deg CRA, mPLCC (HiSPi)	Without protective film
AR0238CSSC12SHRA0–DP–E	2 Mp 1/3" CIS RGB, 12deg CRA, mPLCC (HiSPi)	With protective film
AR0238CSSC12SPRA0–DR	2 Mp 1/3" CIS RGB, 12deg CRA, mPLCC (Parallel)	Without Protective Film
AR0238CSSC12SUD20		RGB Recon die
AR0238IRSH12SUD20		RGB–IR Recon die

NOTE: See the ON Semiconductor Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

4. Replaced "Figure 3,Typical Configuration: Serial Four-Lane HiSPi Interface"

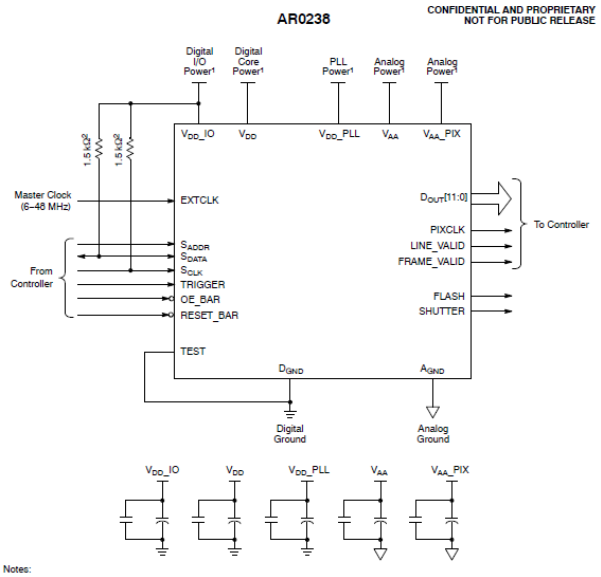
Old Figure 3:

Figure 3: Typical Configuration: Parallel Pixel Data Interface



Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two-wire speed.
3. ON Semiconductor recommends that 0.1 µF and 10 µF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on layout and design considerations. Refer to the AR0238 demo headboard schematics for circuit recommendations.
4. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
5. I/O signals voltage must be configured to match VDD_IO voltage to minimize any leakage currents.
6. The EXTCLK input is limited to 6-48 MHz.

New Figure 3:



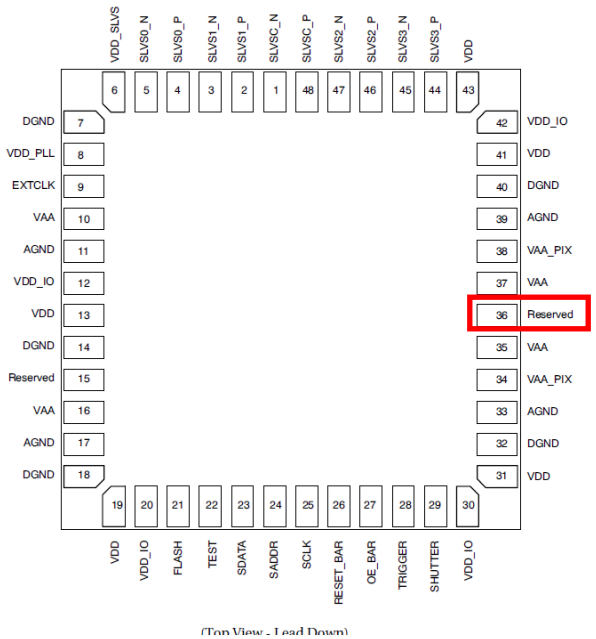
Notes:
1. All power supplies must be adequately decoupled.
2. ON Semiconductor recommends a resistor value of 1.5 kΩ, but a greater value may be used for slower two−wire speed.
3. The serial interface output pads can be left unconnected if the parallel output interface is used.
4. ON Semiconductor recommends that 0.1 μF and 10 μF decoupling capacitors for each power supply are mounted as close as possible to the pad. Actual values and results may vary depending on the layout and design considerations. Refer to the AR0237AT demo headboard schematics for circuit recommendations.
5. ON Semiconductor recommends that analog power planes are placed in a manner such that coupling with the digital power planes is minimized.
6. I/O signals voltage must be configured to match V_{DD_IO} voltage to minimize any leakage currents.
7. The EXTCLK input is limited to 6−48 MHz.

Figure 3. Typical Configuration: Parallel Pixel Data Interface

5. In " Figure 4, HiSPi 48-Lead mPLCC Package" changed pin 36 from Reserved to ATEST

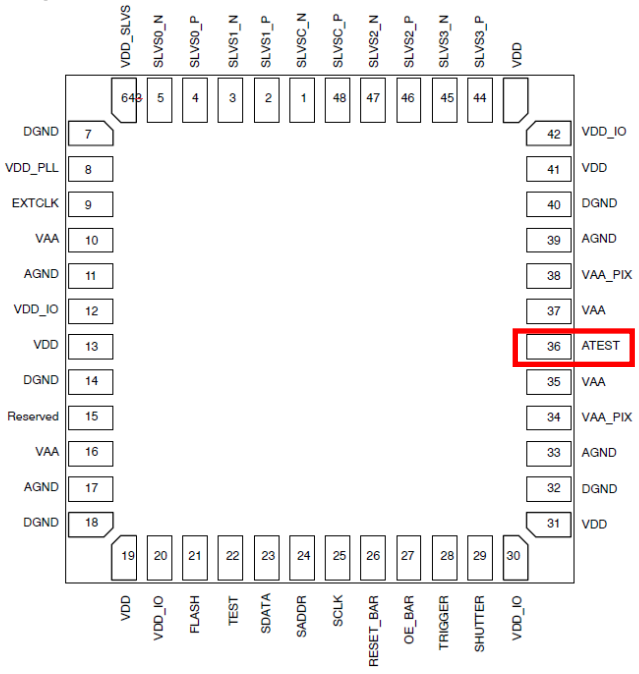
Old Figure 4:

Figure 4: HiSPi 48-Lead mPLCC Package



(Top View - Lead Down)

New Figure 4:



(Top View – Lead Down)

Figure 4. HiSPi 48-Lead mPLCC Package

6. In Figure 5, "48-Lead Parallel mPLCC" changed pin 6 from DOUT1 to DOUT 11

Old Figure 5:

Figure 5: 48-Lead Parallel mPLCC

(Top View - Lead Down)

New Figure 5:

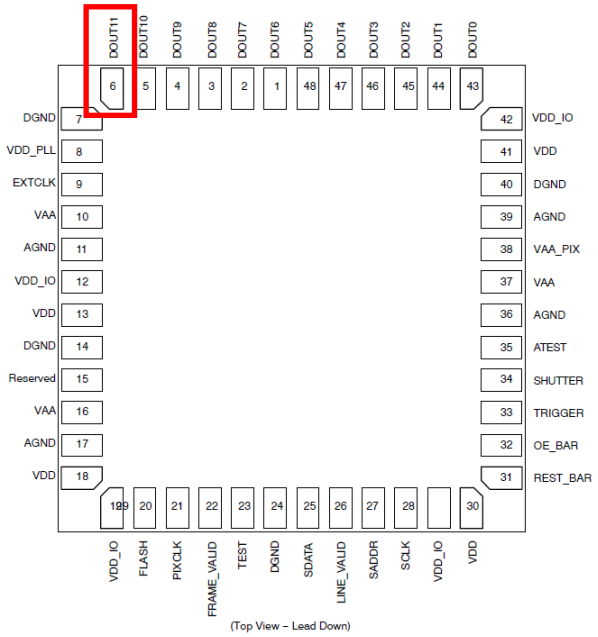


Figure 5. 48–Lead Parallel mPLCC

7. Replaced " Table 3,Pin Descriptions, HiSPi 48-Lead mPLCC"

Old Table 3:

Table 3: Pin Descriptions, HiSPi 48-Lead mPLCC

Name	mPLCC Pin	Type	Description
SLVSC_N	1	Output	HiSPi serial DDR clock differential N
SLVS1_P	2	Output	HiSPi serial data, lane 1, differential P
SLVS1_N	3	Output	HiSPi serial data, lane 1, differential N
SLVS0_P	4	Output	HiSPi serial data, lane 0, differential P
SLVS0_N	5	Output	HiSPi serial data, lane 0, differential N
VDD_SLVS	6	Power	0.3V-0.6V or 1.7V - 1.9V port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) bit to 1 when configuring VDD_SLVS to 1.7 – 1.9V.
DGND	7, 14, 18, 32, 40	Power	Digital ground
VDD_PLL	8	Power	PLL power
EXTCLK	9	Input	External input clock
VAA	10, 16, 35, 37	Power	Analog power
AGND	11, 17, 33, 39	Power	Analog ground.
VDD_IO	12, 20, 30, 42	Power	I/O supply power
VDD	13, 19, 31, 41	Power	Digital power
Reserved	15		
FLASH	21	Output	Flash control output
TEST	22	Input	Manufacturing test enable pin (connect to Dgnd)
SDATA	23	I/O	Two-Wire Serial data I/O
SADDR	24	Input	Two-Wire Serial address select. 0: 0x20. 1: 0x30
SCLK	25	Input	Two-Wire Serial clock input
RESET_BAR	26	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
OE_BAR	27	Input	Output enable (active LOW)
TRIGGER	28	Input	Exposure synchronization input
SHUTTER	29	Output	Control for external mechanical shutter. Can be left floating if not used.
VAA_PIX	34, 38	Power	Pixel power
SLVS3_P	44	Output	HiSPi serial data, lane 3, differential P
SLVS3_N	45	Output	HiSPi serial data, lane 3, differential N
SLVS2_P	46	Output	HiSPi serial data, lane 2, differential P
SLVS2_N	47	Output	HiSPi serial data, lane 2, differential N
SLVSC_P	48	Output	HiSPi serial DDR clock differential P

Note: The 36 thermal connection pads should be all soldered to DGND plane for better thermal conductivity. Refer to Figure 15 for details.

New Table 3:

Table 3. PIN DESCRIPTIONS, HiSPi 48−Lead mPLCC

DS Name	mPLCC Pin	Type	Description
SLVSC_N	1	Output	HiSPi serial DDR clock differential N
SLVS1_P	2	Output	HiSPi serial data, lane 1, differential P
SLVS1_N	3	Output	HiSPi serial data, lane 1, differential N
SLVS0_P	4	Output	HiSPi serial data, lane 0, differential P
SLVS0_N	5	Output	HiSPi serial data, lane 0, differential N
VDD_SLVS	6	Power	0.3 V−0.6 V or 1.7 V − 1.9 V port to HiSPi Output Driver. Set the High_VCM (R0x306E[9]) bit to 1 when configuring VDD_SLVS to 1.7 V − 1.9 V.
DGND	7, 14, 18, 32, 40	Power	Digital ground
VDD_PLL	8	Power	PLL power, 2.8 V nominal
EXTCLK	9	Input	External input clock
VAA	10, 16, 35, 37	Power	Analog power, 2.8 V nominal
AGND	11, 17, 33, 39	Power	Analog ground.
VDD_IO	12, 20, 30, 42	Power	I/O supply power, 1.8/2.8 V nominal
VDD	13, 19, 31, 41, 43	Power	Digital power, 1.8 V nominal
Reserved	15	−	Reserved, NC
FLASH	21	Output	Flash control output
TEST	22	Input	Manufacturing test enable pin (connect to Dgnd)
SDATA	23	I/O	Two−Wire Serial data I/O
SADDR	24	Input	Two−Wire Serial address select. 0: 0x20. 1: 0x30
SCLK	25	Input	Two−Wire Serial clock input
RESET_BAR	26	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
OE_BAR	27	Input	Output enable (active LOW)
TRIGGER	28	Input	Exposure synchronization input
SHUTTER	29	Output	Control for external mechanical shutter. Can be left floating if not used.
VAA_PIX	34, 38	Power	Pixel power, 2.8 V nominal
ATEST	36	−	Reserved, NC
SLVS3_P	44	Output	HiSPi serial data, lane 3, differential P
SLVS3_N	45	Output	HiSPi serial data, lane 3, differential N
SLVS2_P	46	Output	HiSPi serial data, lane 2, differential P
SLVS2_N	47	Output	HiSPi serial data, lane 2, differential N
SLVSC_P	48	Output	HiSPi serial DDR clock differential P

NOTE: The 36 thermal connection pads should be all soldered to DGND plane for better thermal conductivity. Refer to Figure 15 for details.

8. Replaced entire "Table 4, Pin Descriptions, 48-Lead Parallel mPLCC"

Old Table 4:

Table 4: 48-Lead Parallel mPLCC

Name	mPLCC Pin	Type	Description
DOUT6	1	Output	Data output 6
DOUT7	2	Output	Data output 7
DOUT8	3	Output	Data output 8
DOUT9	4	Output	Data output 9
DOUT10	5	Output	Data output 10
DOUT11	6	Power	Data output 11
DGND	7, 14, 24, 40	Power	Digital ground
VDD_PLL	8	Power	PLL power
EXTCLK	9	Input	External input clock
VAA	10, 16, 37	Power	Analog Power
AGND	11, 17, 36, 39	Power	Analog Ground
VDD_IO	12, 19, 29, 42	Power	I/O Power Supply
VDD	13, 18, 30, 41	Power	Digital Power
Reserved	15		
FLASH	20	Power	Flash control output
PIXCLK	21	Output	Pixel Clock
FRAME_VALID	22	Output	Frame Valid
TEST	23	Input	Manufacturing test enable pin (connect to DGNG)
SDATA	25	I/O	Two-Wire Serial data I/O
LINE_VALID	26	Output	Line Valid
SADDR	27	Input	Two-Wire Serial address select. 0: 0x20, 1: 0x30
SCLK	28	Input	Two-Wire Serial clock input
RESET_BAR	31	Input	Asynchronous reset (active LOW). All settings are restored to factory default.
OE_BAR	32	Input	Output enable (active LOW)
TRIGGER	33	Input	Exposure synchronization input
SHUTTER	34	Output	Control for external mechanical shutter. Can be left floating if not used.
ATEST	35	Input	Manufacturing test enable pin (connect to DGNG)
VAA_PIX	38	Power	Pixel Power
DOUT0	43	Output	Data Output 0
DOUT1	44	Output	Data Output 1
DOUT2	45	Output	Data Output 2
DOUT3	46	Output	Data Output 3
DOUT4	47	Output	Data Output 4
DOUT5	48	Output	Data Output 5

Note: The 29 thermal connection pads should be all soldered to DGND plane for better thermal conductivity. Refer to Figure 16 for details.

New Table 4:

Table 4. 48−Lead PARALLEL mPLCC

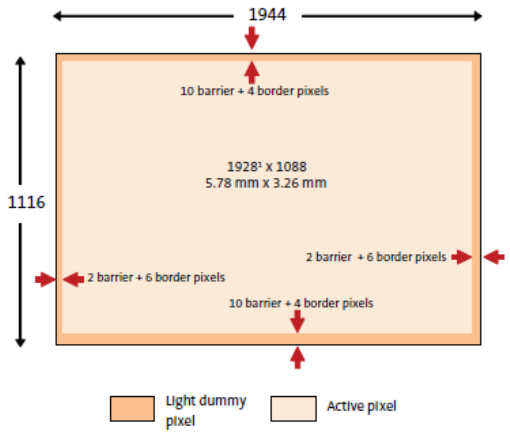
Name	mPLCC Pin	Type	Description
DOUT6	1	Output	Data output 6
DOUT7	2	Output	Data output 7
DOUT8	3	Output	Data output 8
DOUT9	4	Output	Data output 9
DOUT10	5	Output	Data output 10
DOUT11	6	Power	Data output 11
DGND	7, 14, 24, 40	Power	Digital ground
VDD_PLL	8	Power	PLL power, 2.8 V nominal
EXTCLK	9	Input	External input clock
VAA	10, 16, 37	Power	Analog power, 2.8 V nominal
[illegible]	[illegible]	Power	Analog ground
VDD_IO	12, 19, 29, 42	Power	I/O supply power, 1.8/2.8 V nominal
VDD	13, 18, 30, 41	Power	Digital power, 1.8 V nominal
Reserved	15	−	Reserved, NC
[illegible]	[illegible]	Power	Flash control output
PIXCLK	21	Output	Pixel Clock
FRAME_VALID	22	Output	Frame Valid
TEST	23	Input	Manufacturing test enable pin (connect to DGNG)
SDATA	25	I/O	Two−Wire Serial data I/O
LINE_VALID	26	Output	Line Valid
SADDR	27	Input	Two−Wire Serial address select. 0: 0x20, 1: 0x30
SCLK	28	Input	Two−Wire Serial clock input
RESET_BAR	31	Input	Asynchronous reset (active LOW). All settings are restored to factory default
OE_BAR	32	Input	Output enable (active LOW)
TRIGGER	33	Input	Exposure synchronization input
SHUTTER	34	Output	Control for external mechanical shutter. Can be left floating if not used.
ATEST	35	−	Reserved, NC
VAA_PIX	38	Power	Pixel power, 2.8 V nominal
DOUT0	43	Output	Data Output 0
DOUT1	44	Output	Data Output 1
DOUT2	45	Output	Data Output 2
DOUT3	46	Output	Data Output 3
DOUT4	47	Output	Data Output 4
DOUT5	48	Output	Data Output 5

NOTE: The 29 thermal connection pads should be all soldered to DGND plane for better thermal conductivity. Refer to Figure 16 for details.

9. Replaced “Figure 6, Pixel Array Description”

Old Figure 6:

Figure 6: Pixel Array Description



New Figure 6:

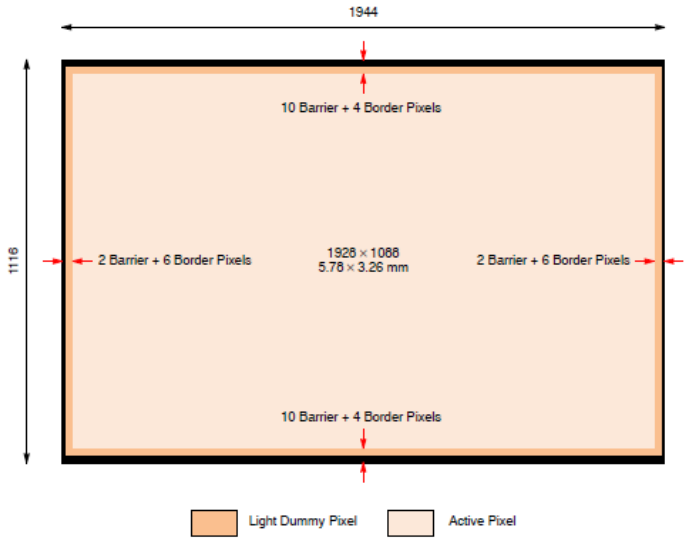
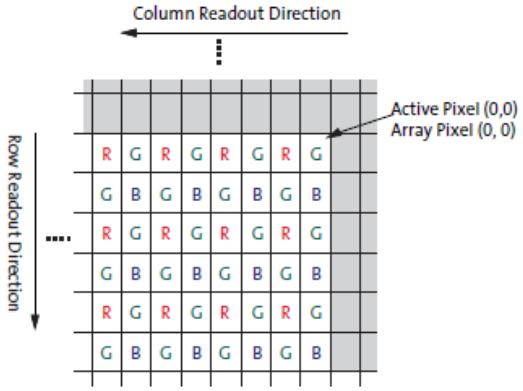


Figure 6. Pixel Array Description

10. Changed Figure 7 title to "Pixel Color Pattern Detail (RGB) (Top Right Corner)"

Old Figure 7:

Figure 7: Pixel Color Pattern Detail (Top Right Corner)



New Figure 7:

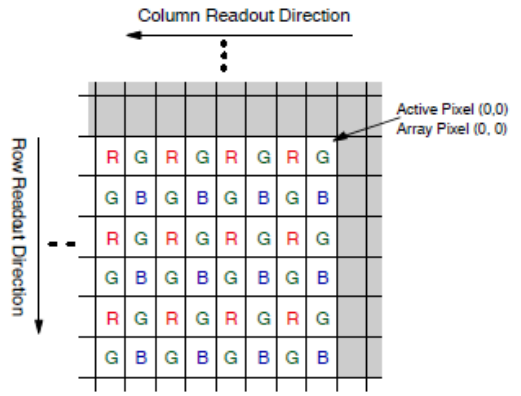


Figure 7. Pixel Color Pattern Detail (RGB) (Top Right Corner)

11. Added Figure 8, "Pixel Color Pattern Detail (RGB–IR) (Top Right Corner)"

New Figure 8:

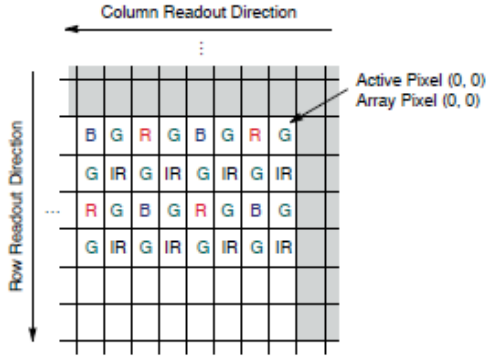
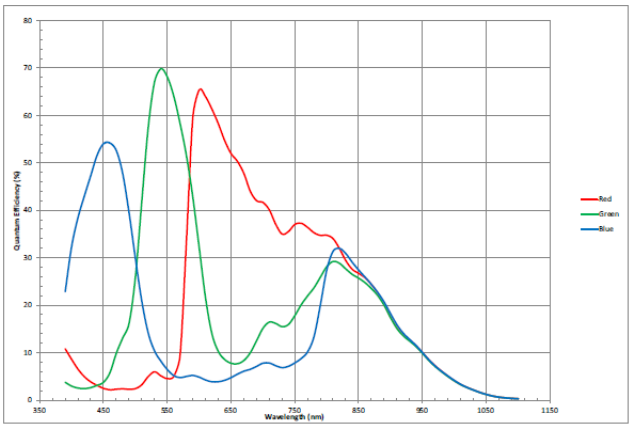


Figure 8. Pixel Color Pattern Detail (RGB–IR) (Top Right Corner)

12. Changed Figure 9 title to Figure 10, "Quantum Efficiency – RGB"

Old Figure 9:

Figure 9: Quantum Efficiency



New Figure 9:

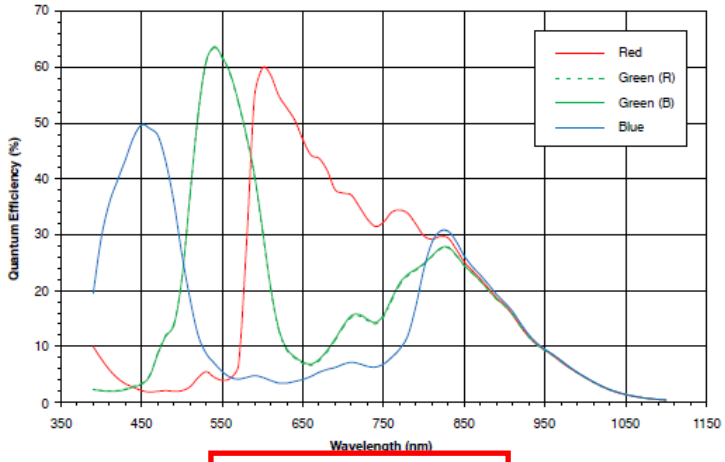


Figure 10. Quantum Efficiency – RGB

13. Added "Figure 11. Quantum Efficiency – RGB–IR Packaged Part"

New Figure 11:

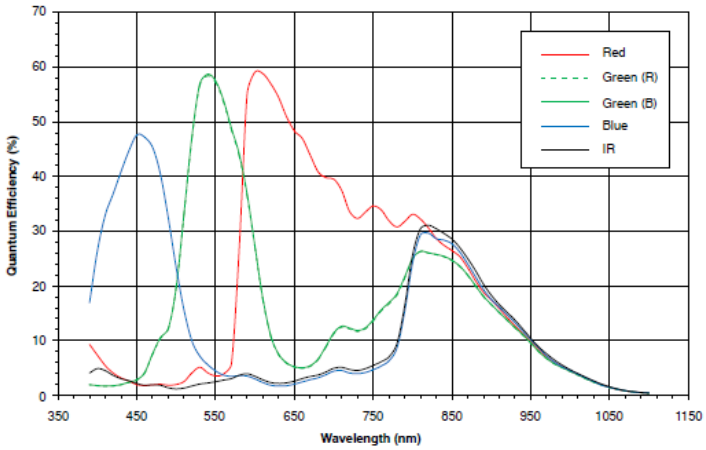
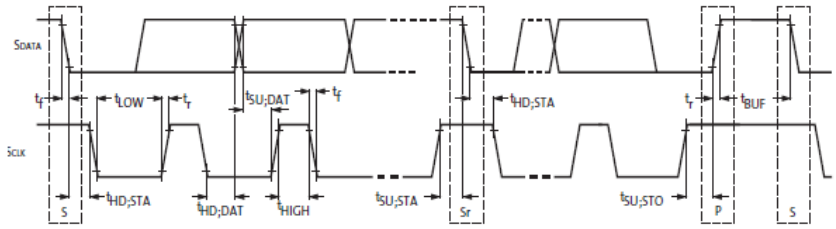


Figure 11. Quantum Efficiency – RGB–IR Packaged Part

14. Replaced Figure 11, "Two-Wire Serial Bus Timing Parameters" with "Figure 12, Two–Wire Serial Bus Timing Parameters

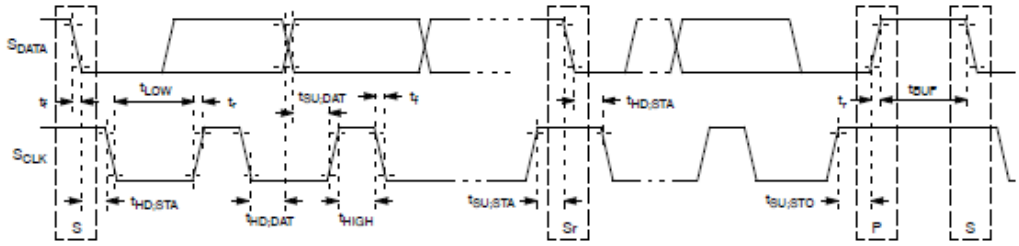
Old Figure 11:

Figure 11: Two-Wire Serial Bus Timing Parameters



Note: Read sequence: For an 8-bit READ, read waveforms start after WRITE command and register address are issued.

New Figure 12:



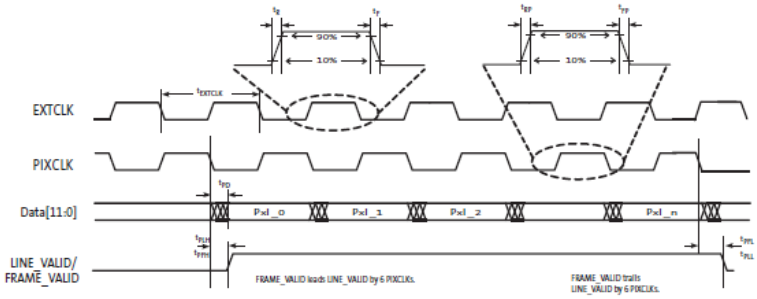
NOTE: Read sequence: For an 8–bit READ, read waveforms start after WRITE command and register address are issued.

Figure 12. Two–Wire Serial Bus Timing Parameters

15. Replaced Figure 12, "I/O Timing Diagram" with Figure 13, "I/O Timing Diagram"

Old Figure 12:

Figure 12: I/O Timing Diagram



New Figure 13:

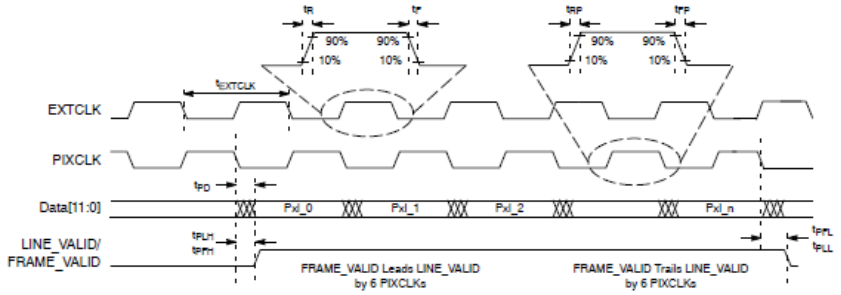


Figure 13. I/O Timing Diagram

16. Updated the note in "Table 9, Absolute Maximum Ratings"

Old Table 9:

Table 9: Absolute Maximum Ratings

Symbol	Definition	Condition	Min	Max	Unit
VDD_MAX	Core digital voltage		–0.3	2.4	V
VDD_IO_MAX	I/O digital voltage		–0.3	4	V
VAA_MAX	Analog voltage		–0.3	4	V
VAA_PIX	Pixel supply voltage		–0.3	4	V
VDD_PLL	PLL supply voltage		–0.3	4	V
VDD_SLVS_MAX	HISPI I/O digital voltage		–0.3	2.4	V
t_{ST}	Storage temperature		–40	85	°C

Note: Exposure to absolute maximum rating conditions for extended periods may affect reliability.

New Table 9:

Table 9. ABSOLUTE MAXIMUM RATINGS

Symbol	Definition	Condition	Min	Max	Unit
VDD_MAX	Core digital voltage		–0.3	2.4	V
VDD_IO_MAX	I/O digital voltage		–0.3	4	V
VAA_MAX	Analog voltage		–0.3	4	V
VAA_PIX	Pixel supply voltage		–0.3	4	V
VDD_PLL	PLL supply voltage		–0.3	4	V
VDD_SLVS_MAX	HiSPi I/O digital voltage		–0.3	2.4	V
tST	Storage temperature		–40	85	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

17. Moved notes for "Table 10, 1080p30 Linear 74 MHz Parallel 2.8V"

Old Table 10:

Table 10: 1080p30 Linear 74 MHz Parallel 2.8V

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital operating current	Streaming 1080p30	IDD	1.8	20	34	50	mA
I/O digital operating current	Streaming 1080p30	IDD_IO	2.8	15	28	50	mA
Analog operating current	Streaming 1080p30	IAA	2.8	15	26	50	mA
Pixel supply current	Streaming 1080p30	IAA_PIX	2.8	1	3	7	mA
PLL supply current	Streaming 1080p30	IDD_PLL	2.8	5.5	6.4	7	mA
			Power	138.2	238.72	409.2	mW

Note: Operating currents are measured in mA at the following conditions:
- VAA = VAA_PIX = VDD_PLL = VDD_IO =2.8 V
- VDD= 1.8 V
- PLL Enabled and PIXCLK = 74.25 MHz
- Low power mode enabled
- TA = 25°C

New Table 10:

Table 10. 1080p30 LINEAR 74 MHZ PARALLEL 2.8 V

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA_PIX} = V_{DD_PLL} = V_{DD_IO} = 2.8 V; V_{DD} = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; Low power mode enabled; T_A = 25°C)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	20	34	50	mA
I/O Digital Operating Current	Streaming 1080p30	I_{DD_IO}	2.8	15	28	50	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	I_{AA_PIX}	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	I_{DD_PLL}	2.8	5.5	6.4	7	mA
			Power	138.2	238.72	409.2	mW

18. Moved notes for " Table 11, 1080p30 Linear 74 MHz Parallel 1.8V"

Old Table 11:

Table 11: 1080p30 Linear 74 MHz Parallel 1.8V

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital operating current	Streaming 1080p30	IDD	1.8	20	34	50	mA
I/O digital operating current	Streaming 1080p30	IDD_IO	1.8	10	14	30	mA
Analog operating current	Streaming 1080p30	IAA	2.8	15	26	50	mA
Pixel supply current	Streaming 1080p30	IAA_PIX	2.8	1	3	7	mA
PLL supply current	Streaming 1080p30	IDD_PLL	2.8	5.5	6.4	7	mA
			Power	114.2	185.52	323.2	mW

Note: Operating currents are measured in mA at the following conditions:
- VAA = VAA_PIX = VDD_PLL =2.8 V
- VDD = VDD_IO= 1.8 V
- PLL Enabled and PIXCLK = 74.25 MHz
- Low power mode enabled
- TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms integration time

New Table 11:

Table 11. 1080p30 LINEAR 74 MHZ PARALLEL 1.8 V

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA_PIX} = V_{DD_PLL} = 2.8 V; V_{DD} = V_{DD_IO} = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; Low power mode enabled; T_A = 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	20	34	50	mA
I/O Digital Operating Current	Streaming 1080p30	I_{DD_IO}	1.8	10	14	30	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	I_{AA_PIX}	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	I_{DD_PLL}	2.8	5.5	6.4	7	mA
			Power	114.2	185.52	323.2	mW

19. Moved notes for "Table 12, 1080p30 Linear 74 MHz HiSPi SLVS"

Old Table 12:

Table 12: 1080p30 Linear 74 MHz HISPI SLVS

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	IDD	1.8	25	44	65	mA
Analog Operating Current	Streaming 1080p30	IAA	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	IAA_PIX	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	IDD_PLL	2.8	6	7.5	8.5	mA
SLVS Supply Current	Streaming 1080p30	IDD_SLVS	0.4	6	9.5	14	mA
			Power	109	185.2	306	mW

Note: Operating currents are measured in mA at the following conditions:
- VAA = VAA_PIX = VDD_PLL =2.8 V
- VDD = VDD_IO= 1.8 V
- VDD_SLVS= 0.4V
- PLL Enabled and PIXCLK = 74.25 MHz
- 4-lane HISPI mode
- Low power mode enabled
- TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms integration time

New Table 12:

Table 12. 1080p30 LINEAR 74 MHZ HISPI SLVS

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA_PIX} = V_{DD_PLL} = 2.8 V; V_{DD} = V_{DD_IO} = 1.8 V; V_{DD_SLVS} = 0.4 V; PLL Enabled and PIXCLK = 74.25 MHz; 4−lane HiSPi mode; Low power mode enabled; T_A = 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	25	44	65	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	I_{AA_PIX}	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	I_{DD_PLL}	2.8	6	7.5	8.5	mA
SLVS Supply Current	Streaming 1080p30	I_{DD_SLVS}	0.4	6	9.5	14	mA
			Power	109	185.2	306	mW

20. Moved notes for " Table 13, 1080p30 Linear 74 MHz HiSPi HiVcm"

Old Table 13:

Table 13: 1080p30 Linear 74 MHz HiSPi HiVcm

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	IDD	1.8	25	44	65	mA
Analog Operating Current	Streaming 1080p30	IAA	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	IAA_PIX	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	IDD_PLL	2.8	6	7.5	8.5	mA
SLVS Supply Current	Streaming 1080p30	IDD_SLVS	1.8	12	20	35	mA
			Power	128.2	217.4	363.4	mW

Note: Operating currents are measured in mA at the following conditions:
- VAA = VAA_PIX = VDD_PLL =2.8 V
- VDD = VDD_IO = VDD_SLVS= 1.8 V
- PLL Enabled and PIXCLK = 74.25 MHz
- 4-lane HISPI mode
- Low power mode enabled
- TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms Integration time

New Table 13:

Table 13. 1080p30 LINEAR 74 MHZ HISPI HIV_{CM}

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA_PIX} = V_{DD_PLL} = 2.8 V; V_{DD} = V_{DD_IO} = V_{DD_SLVS} = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; 4−lane HiSPi mode; Low power mode enabled; T_A = 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	25	44	65	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	15	26	50	mA
Pixel Supply Current	Streaming 1080p30	I_{AA_PIX}	2.8	1	3	7	mA
PLL Supply Current	Streaming 1080p30	I_{DD_PLL}	2.8	6	7.5	8.5	mA
SLVS Supply Current	Streaming 1080p30	I_{DD_SLVS}	1.8	12	20	35	mA
			Power	128.2	217.4	363.4	mW

21. Moved notes for "Table 14, 1080p30 74 MHz Line Interleaved SLVS" with "Table 14, 1080p60 Linear 74 MHz HISPI SLVS

Old Table 14:

Table 14: 1080p30 74 MHz Line Interleaved SLVS

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	IDD	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p30	IAA	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p30	IAA_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p30	IDD_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p30	IDD_SLVS	0.4	6	9.5	14	mA
			Power	170.8	298	442.6	mW

Note: Operating currents are measured in mA at the following conditions:
- VAA = VAA_PIX = VDD_PLL =2.8 V
- VDD = VDD_IO= 1.8 V
- VDD_SLVS= 0.4V
- PLL Enabled and PIXCLK = 74.25 MHz
- 4-lane HISPI mode
- TA= 25°C Dark Image, 8x Analog Gain, HCG, 20ms Integration time

New Table 14:

Table 14. 1080p60 LINEAR 74 MHZ HISPI SLVS

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA_PIX} = V_{DD_PLL} = 2.8 V; V_{DD} = V_{DD_IO} = 1.8 V; V_{DD_SLVS} = 0.4 V; PLL Enabled and PIXCLK = 74.25 MHz; 4−lane HiSPi mode; T_A= 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p60	I_{DD}	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p60	I_{AA}	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p60	I_{AA_PIX}	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p60	I_{DD_PLL}	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p60	I_{DD_SLVS}	0.4	6	9.5	14	mA
			Power	170.8	298	442.6	mW

22. Moved notes for "Table 15,1080p60 LINEAR 74 MHZ HISPI HIVCM"

Old Table 15:

Table 15: 1080p30 74 MHz Line Interleaved HIVcm

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	IDD	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p30	IAA	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p30	IAA_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p30	IDD_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p30	IDD_SLVS	1.8	12	20	35	mA
			Power	190	330.2	500	mW

Note: Operating currents are measured in mA at the following conditions:
- VAA = VAA_PIX = VDD_PLL = 2.8 V
- VDD= VDD_IO = 1.8 V
- VDD_SLVS = 1.8 V
- PLL Enabled and PIXCLK = 74.25 MHz
- 4-lane HiSPi mode
- TA = 25°C Dark Image, 8x Analog Gain, HCG, 20ms integration time

New Table 15:

Table 15. 1080p60 LINEAR 74 MHZ HISPI HIV_{CM}

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; V_{DD}_SLVS = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; 4−lane HiSPi mode; T_A= 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p60	I_{DD}	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p60	I_{AA}	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p60	I_{AA}_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p60	I_{DD}_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p60	I_{DD}_SLVS	1.8	12	20	35	mA
			Power	190	330.2	500	mW

23. Added "Table 16, 1080p30 LINE−INLEAVED 74MHZ HISPI SLVS"

New Table 16:

Table 16. 1080p30 LINE−INLEAVED 74MHZ HISPI SLVS

(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; V_{DD}_SLVS = 0.4 V; PLL Enabled and PIXCLK = 74.25 MHz; 4−lane HiSPi mode; T_A= 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p30	I_{AA}_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p30	I_{DD}_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p30	I_{DD}_SLVS	0.4	6	9.5	14	mA
			Power	170.8	298	442.6	mW

24. Added "Table 17, 1080p30 LINE−INLEAVED 74MHZ HISPI HIVCM"

New Table 17:

Table 17. 1080p30 LINE−INLEAVED 74MHZ HISPI HIV_{CM}

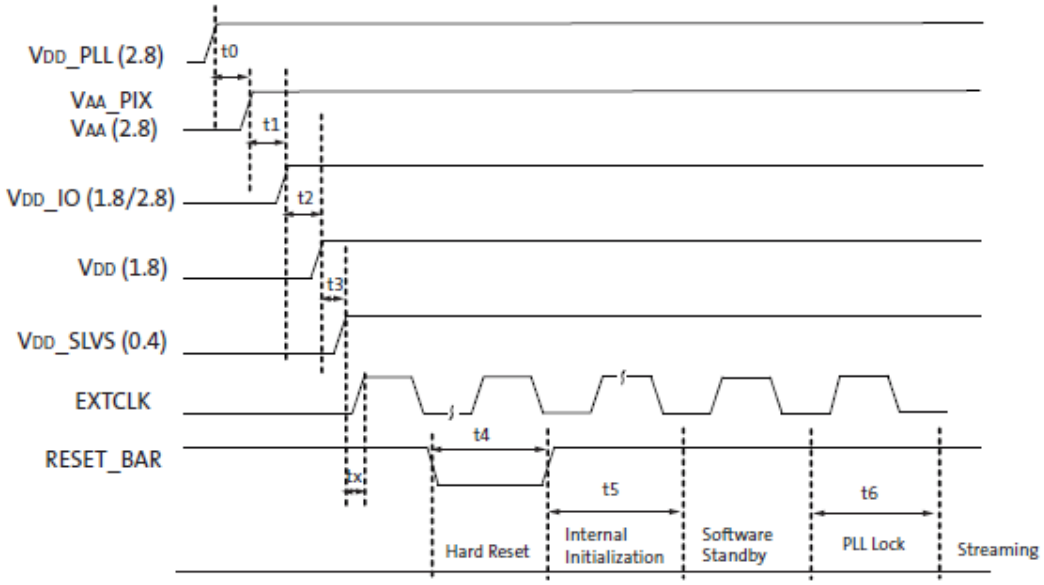
(Operating currents are measured in mA at the following conditions: V_{AA} = V_{AA}_PIX = V_{DD}_PLL = 2.8 V; V_{DD} = V_{DD}_IO = 1.8 V; V_{DD}_SLVS = 1.8 V; PLL Enabled and PIXCLK = 74.25 MHz; 4−lane HiSPi mode; T_A= 25°C Dark Image, 8× Analog Gain, HCG, 20 ms integration time)

Definition	Condition	Symbol	Voltage	Min	Typ	Max	Unit
Digital Operating Current	Streaming 1080p30	I_{DD}	1.8	50	88	130	mA
Analog Operating Current	Streaming 1080p30	I_{AA}	2.8	20	36	60	mA
Pixel Supply Current	Streaming 1080p30	I_{AA}_PIX	2.8	1	4	8	mA
PLL Supply Current	Streaming 1080p30	I_{DD}_PLL	2.8	7	8.5	9.5	mA
SLVS Supply Current	Streaming 1080p30	I_{DD}_SLVS	1.8	12	20	35	mA
			Power	190	330.2	500	mW

25. Replaced "Figure 13, Power Up" with new "Figure 14, Power Up"

Old Figure 13:

Figure 13: Power Up



New Figure 14:

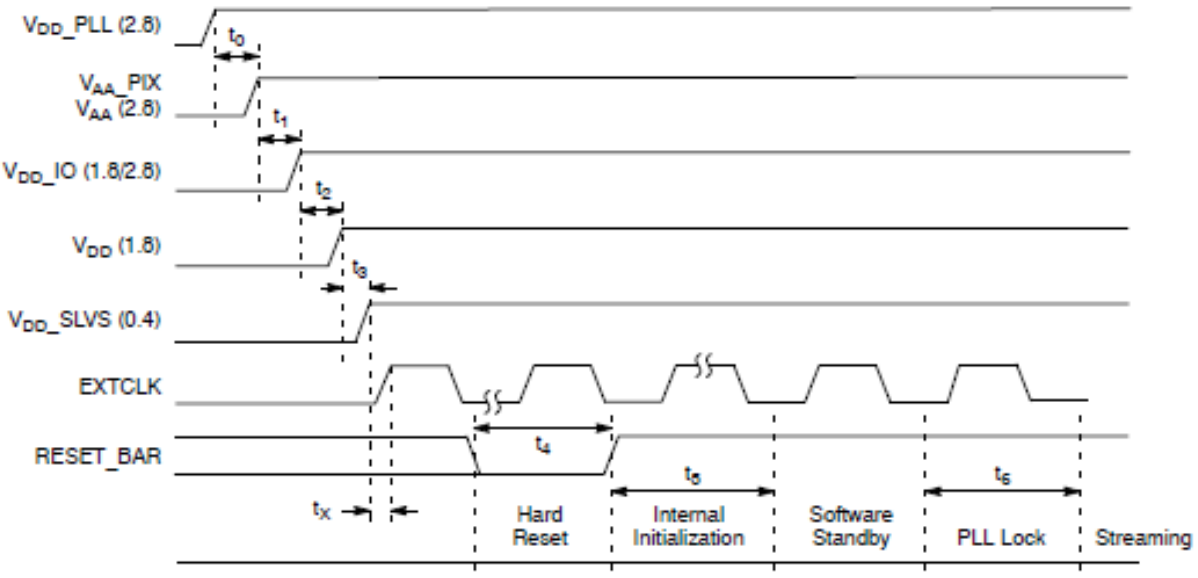
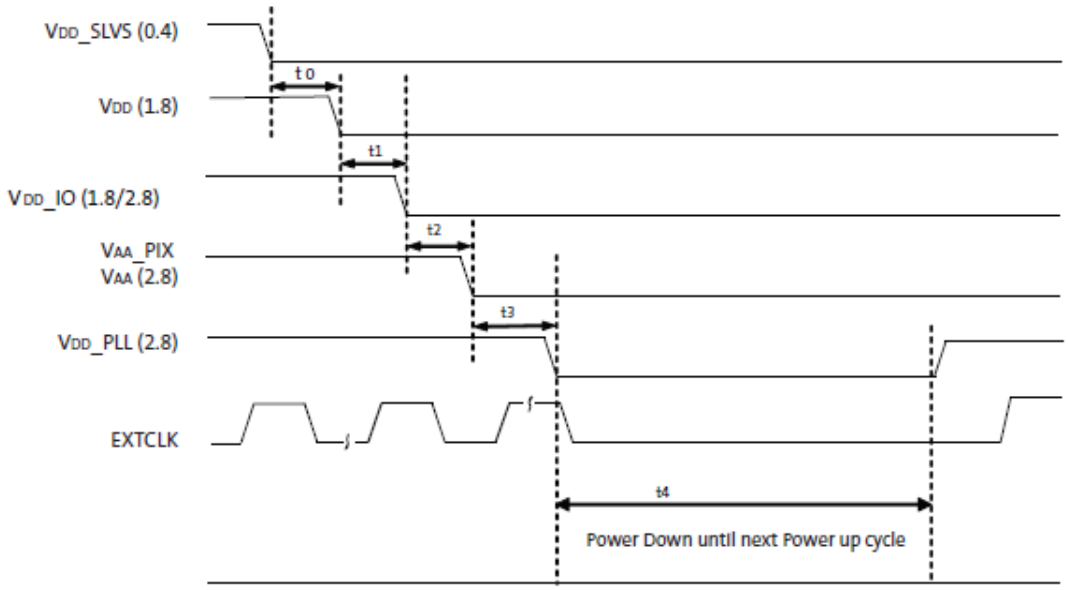


Figure 14. Power Up

26. Replaced "Figure 14, Power Down" with new "Figure 15 , Power Down"

Old Figure 14:

Figure 14: Power Down



New Figure 15:

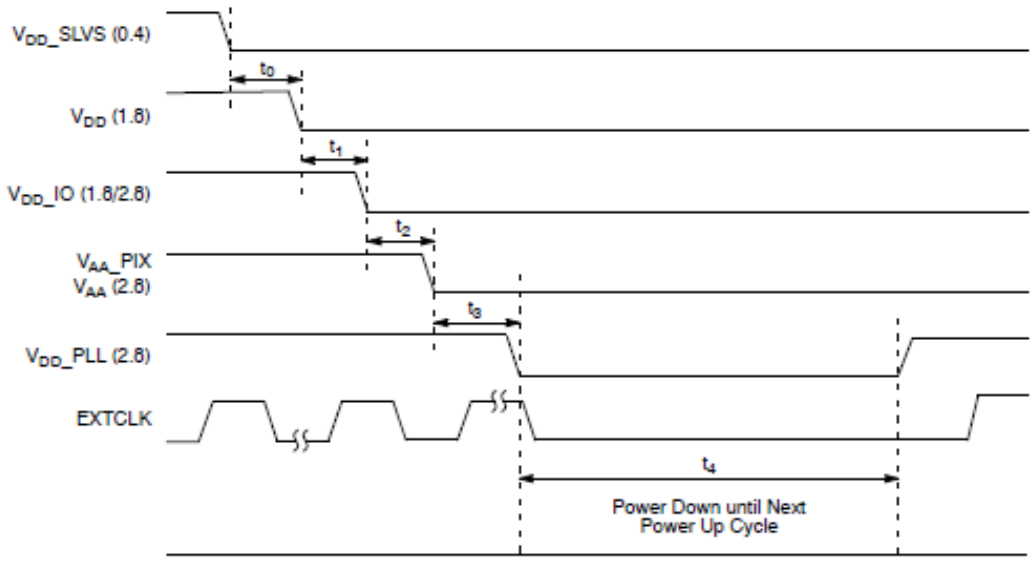


Figure 15. Power Down

List of Affected Standard Parts:
AR0238CSSC12SPRA0-DR