ISO5500 2.5-A Isolated IGBT, MOSFET Gate Driver

1 Features

- 2.5-A maximum peak output current
- Drives IGBTs up to I_C = 150 A, V_{CE} = 600 V
- Capacitive isolated fault feedback
- CMOS/TTL compatible inputs
- 300-ns maximum propagation delay
- Soft IGBT turnoff
- Integrated fail-safe IGBT protection
  - High V_{CE} (DESAT) detection
  - Undervoltage lockout (UVLO) protection with hysteresis
- User configurable functions
  - Inverting, non-inverting inputs
  - Auto-reset
  - Auto-shutdown
- Wide V_{CC1} range: 3 V to 5.5 V
- Wide V_{CC2} range: 15 V to 30 V
- Operating temperature: –40°C to 125°C
- Wide-body SO-16 package
- ±50-kV/us transient immunity typical
- Safety and Regulatory Approvals:
  - VDE 4000 V_{PK} Basic Isolation per DIN V VDE V 0884-11
  - 2500 V_{RMS} Isolation for One Minute per UL 1577
  - CSA 62368-1:19, CSA 61010-1-12, UPD1: 2015, UPD2:2016, AMD1:2018

2 Applications

- Isolated IGBT and MOSFET Drives in
  - Motor Control
  - Motion Control
  - Industrial Inverters
  - Switched-Mode Power Supplies

3 Description

The ISO5500 is an isolated gate driver for IGBTs and MOSFETs with power ratings of up to I_C = 150 A and V_{CE} = 600 V. Input TTL logic and output power stage are separated by a capacitive, silicon dioxide (SiO_2), isolation barrier. When used in conjunction with isolated power supplies, the device blocks high voltage, isolates ground, and prevents noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

The device provides over-current protection (DESAT) to an IGBT or MOSFET while an Undervoltage Lockout circuit (UVLO) monitors the output power supply to ensure sufficient gate drive voltage. If the output supply drops below 12 V, the UVLO turns the power transistor off by driving the gate drive output to a logic low state.

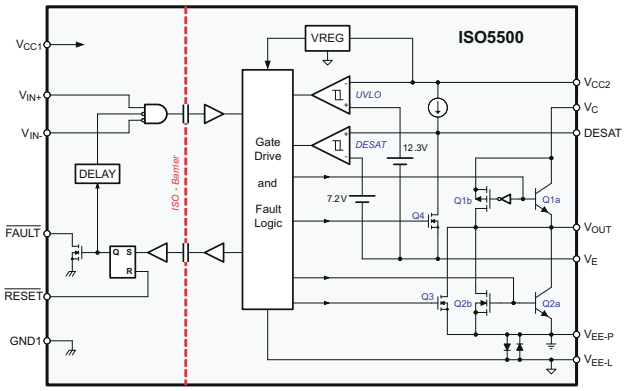
For a DESAT fault, the ISO5500 initiates a soft shutdown procedure that slowly reduces the IGBT/MOSFET current to zero while preventing large di/dt induced voltage spikes. A fault signal is then transmitted across the isolation barrier, actively driving the open-drain $\overline{\text{FAULT}}$ output low and disabling the device inputs. The inputs are blocked as long as the $\overline{\text{FAULT}}$-pin is low. $\overline{\text{FAULT}}$ remains low until the inputs are configured for an output low state, followed by a logic low input on the $\overline{\text{RESET}}$ pin.

The ISO5500 is available in a 16-pin SOIC package and is specified for operating temperatures from –40°C to 125°C.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
ISO5500	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Block Diagram

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4 Revision History

Changes from Revision D (January 2015) to Revision E (April 2022) **Page**

- Changed Safety and Regulatory Approvals....1
- Changed rows V_{IORM}, V_{PR}, V_{IOTM} and V_{ISO} 17
- Changed the Regulatory Information table....17

Changes from Revision C (June 2013) to Revision D (January 2015) **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 1
- Added $\overline{\text{FAULT}}$ limits to *Absolute Maximum Ratings* 4

5 Pin Configuration and Functions

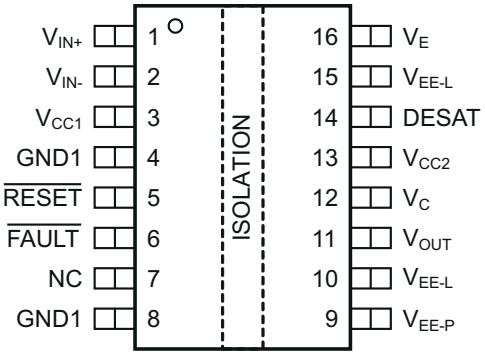


Figure 5-1. DW Package 16-Pin SOIC Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{IN+}	I	Noninverting gate drive voltage control input
2	$V_{IN–}$	I	Inverting gate drive voltage control input
3	V_{CC1}	Supply	Positive input supply (3 V to 5.5 V)
4,8	GND1	Ground	Input ground
5	$\overline{\text{RESET}}$	I	$\overline{\text{FAULT}}$ reset input
6	$\overline{\text{FAULT}}$	O	Open-drain output. Connect to 3.3k pullup resistor
7	NC	NC	Not connected
9	V_{EE-P}	Supply	Most negative output-supply potential of the power output. Connect externally to pin 10.
10, 15	V_{EE-L}	Supply	Most negative output-supply potential of the logic circuitry. Pin 10 and 15 are internally connected. Connect at least pin 10 externally to pin 9. Pin 15 can be floating.
11	V_{OUT}	O	Gate drive output voltage
12	V_C	Supply	Gate driver supply. Connect to V_{CC2}.
13	V_{CC2}	Supply	Most positive output supply potential
14	DESAT	I	Desaturation voltage input
16	V_E	Ground	Gate drive common. Connect to IGBT Emitter.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX[1]	UNIT
Supply voltage, V_{CC1}		–0.5	6	V
Total output supply voltage, $V_{OUT(total)}$	(V_{CC2} – V_{EE-P})	–0.5	35	V
Positive output supply voltage, V_{OUT+}	(V_{CC2} – V_E)	–0.5	35 – (V_E – V_{EE-P})	V
Negative output supply voltage, V_{OUT-}	(V_E – V_{EE-P})	–0.5	V_{CC2}	V
Voltage at	DESAT	V_E – 0.5	V_{CC2}	V
	V_{IN+}, $V_{IN–}$, $\overline{RESET}$, $\overline{FAULT}$	–0.5	6	
Peak gate drive output voltage	$V_{o(peak)}$	–0.5	V_{CC2}	V
Collector voltage, V_C		–0.5	V_{CC2}	V
Output current , I_O [2]			±2.8	A
$\overline{FAULT}$ output current, I_{FL}			±20	mA
Maximum junction temperature, T_J			170	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Maximum pulse width = 10 µs, maximum duty cycle = 0.2%.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	
		Machine model JEDEC JESD22-A115-A	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage	3		5.5	V
$V_{OUT(total)}$	Total output supply voltage (V_{CC2} – V_{EE-P})	15		30	V
V_{OUT+}	Positive output supply voltage (V_{CC2} – V_E)	15		30 – (V_E – V_{EE-P})	V
$V_{OUT–}$	Negative output supply voltage (V_E – V_{EE-P})	0		15	V
V_C	Collector voltage	V_{EE-P} + 8		V_{CC2}	V
t_{ui}	Input pulse width	0.1			µs
t_{uiR}	$\overline{RESET}$ Input pulse width	0.1			µs
V_{IH}	High-level input voltage (V_{IN+}, $V_{IN–}$, $\overline{RESET}$)	2		V_{CC}	V
V_{IL}	Low-level input voltage (V_{IN+}, $V_{IN–}$, $\overline{RESET}$)	0		0.8	V
f_{INP}	Input frequency			520[2]	kHz
V_{SUP_SR}	Supply Slew Rate (V_{CC1} or V_{CC2} – V_{EE-P}) [1]			75	V/ms
T_J	Junction temperature	–40		150	°C

6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Ambient temperature	-40	25	125	°C

(1) If V_{CC1} skew is faster than 75 V/ms (especially for the falling edge) then V_{CC2} must be powered up after V_{CC1} and powered down before V_{CC1} to avoid output glitches.
(2) If T_A = 125°C, V_{CC1}= 5.5 V, V_{CC2} = 30 V, R_G = 10 Ω, C_L = 1 nF

6.4 Thermal Information

THERMAL METRIC(1)		ISO5500 DW (SOIC) 16 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	76	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	34	
θ_{JB}	Junction-to-board thermal resistance	36	
ψ_{JT}	Junction-to-top characterization parameter	8	
ψ_{JB}	Junction-to-board characterization parameter	35	
T_{SHDN+}	Thermal Shutdown	185	°C
T_{SHDN-}		173	°C
$T_{SHDN-HYS}$	Thermal Shutdown Hysteresis	12	°C
P_D	Power Dissipation See Equation 2 through Equation 6	592	mW

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics

All typical values are at T_A = 25°C, V_{CC1} = 5 V, $V_{CC2} – V_E$ = 30 V, $V_E – V_{EE-P}$ = 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Supply current	Quiescent	V_I = V_{CC1} or 0 V, No load, See Figure 6-1, Figure 6-2, Figure 7-1, and Figure 7-2		5.5	8.5	mA
		300 kHz			5.7	8.7	
I_{CC2}	Supply current	Quiescent	V_I = V_{CC1} or 0 V, No load, See Figure 6-3 through Figure 6-5, Figure 7-3, and Figure 7-4		8.4	12	mA
		300 kHz			9	14	
I_{CH}	High-level collector current		I_{OUT} = 0, See Figure 6-27 and Figure 7-3			1.3	mA
			I_{OUT} = –650 µA, See Figure 6-27 and Figure 7-3			1.9	
I_{CL}	Low-level collector current		See Figure 6-27 and Figure 7-4			0.4	mA
I_{EH}	V_E High-level supply current		See Figure 6-6 and Figure 7-13	–0.5	–0.3		mA
I_{EL}	V_E Low-level supply current		See Figure 6-6 and Figure 7-14	–0.8	–0.53		mA
I_{IH}	High-level input leakage		IN from 0 to V_{CC}			10	µA
I_{IL}	Low-level input leakage			–10			
I_{FH}	High-level $\overline{FAULT}$ pin output current		$V_{\overline{FAULT}}$ = V_{CC1}, no pull-up, See Figure 7-6	–10		10	µA
I_{FL}	Low-level $\overline{FAULT}$ pin output current		$V_{\overline{FAULT}}$ = 0.4 V, no pull-up, See Figure 7-7	5	12		mA
$V_{IT+(UVLO)}$	Positive-going UVLO threshold voltage		See Figure 7-5	11.6	12.3	13.5	V
$V_{IT–(UVLO)}$	Negative-going UVLO threshold voltage				11.1	12.4	
$V_{HYS\ (UVLO)}$	UVLO Hysteresis voltage ($V_{IT+} – V_{IT–}$)			0.7	1.2		
I_{OH}	High-level output current		V_{OUT} = V_{CC2} – 4 V(1), See Figure 6-7 and Figure 7-8	–1	–1.6		A
			V_{OUT} = V_{CC2} – 15 V(2), See Figure 6-7 and Figure 7-8	–2.5			
I_{OL}	Low-level output current		V_{OUT} = V_{EE-P} + 2.5 V(1), See Figure 6-8 and Figure 7-9	1	1.8		A
			V_{OUT} = V_{EE-P} + 15 V(2), See Figure 6-8 and Figure 7-9	2.5			

6.5 Electrical Characteristics (continued)

All typical values are at T_A = 25°C, V_{CC1} = 5 V, $V_{CC2} – V_E$ = 30 V, $V_E – V_{EE-P}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OF}	Output-low fault current	$V_{OUT} – V_{EE-P}$ = 14 V, See Figure 6-9 and Figure 7-10	90	140	230	mA
V_{OH}	High-level output voltage	I_{OUT} = –100 mA, See Figure 6-10, Figure 6-11 and Figure 7-11	V_C-1.5	V_C-0.8		V
		I_{OUT} = –650 µA, See Figure 6-10, Figure 6-11 and Figure 7-11	V_C-0.15	V_C-0.05		
V_{OL}	Low-level output voltage	I_{OUT} = 100 mA, See Figure 6-12, Figure 6-13 and Figure 7-12		0.2	0.5	V
I_{CHG}	Blanking capacitor charging current	V_{DESAT} = 0 V to 6 V, See Figure 6-14 and Figure 7-15	–180	–270	–380	µA
I_{DSCHG}	Blanking capacitor discharge current	V_{DESAT} = 8 V, See Figure 7-15	20	45		mA
V_{DSTH}	DESAT threshold voltage	($V_{CC2} – V_E$) > $V_{TH-(UVLO)}$, See Figure 6-15 and Figure 7-15	6.7	7.2	7.7	V
CMTI	Common mode transient immunity	V_I = V_{CC1} or 0 V, V_{CM} at 1500 V, See Figure 7-16 though Figure 7-19	25	50		kV/µS

(1) Maximum pulse width is 50 µs, maximum duty cycle is 0.5%
(2) Maximum pulse width is 10 µs, maximum duty cycle is 0.2%

6.6 Switching Characteristics

All typical values are at T_A = 25°C, V_{CC1} = 5 V, $V_{CC2} – V_E$ = 30 V, $V_E – V_{EE-P}$ = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation Delay	R_G = 10 Ω, C_G = 10 nF, 50 % duty cycle, 10 kHz input, $V_{CC2} – V_{EE}$ = 30 V, $V_E – V_{EE}$ = 0 V, See Figure 6-16 through Figure 6-19, Figure 6-26, Figure 7-20, Figure 7-22, and Figure 7-23	150	200	300	ns
t_{sk-p}	Pulse Skew $\lvert t_{PHL} – t_{PLH} \rvert$			1.7	10	ns
t_{sk-pp}	Part-to-part skew(1)				45	ns
t_{sk2-pp}	Part-to-part skew(2)		–50		50	ns
t_r	Output signal rise time			55		ns
t_f	Output signal fall time			10		ns
$t_{DESAT\ (90\%)}$	DESAT sense to 90% VOUT delay	R_G = 10 Ω, C_G = 10 nF, $V_{CC2} – V_{EE-P}$ = 30 V, $V_E – V_{EE-P}$ = 0 V, See Figure 6-20 through Figure 6-25, Figure 7-21 and Figure 7-24		300	550	ns
$t_{DESAT\ (10\%)}$	DESAT sense to 10% VOUT delay			1.8	2.3	µs
$t_{DESAT\ (\overline{FAULT})}$	DESAT sense to $\overline{FAULT}$ low output delay			290	550	ns
$t_{DESAT\ (LOW)}$	DESAT sense to DESAT low propagation delay			180		ns
$t_{\overline{RESET}\ (\overline{FAULT})}$	$\overline{RESET}$ to high-level $\overline{FAULT}$ signal delay		3	8.2	13	µs
$t_{UVLO\ (ON)}$	UVLO to V_{OUT} high delay	1ms ramp from 0 V to 30 V		4		µs
$t_{UVLO\ (OFF)}$	UVLO to V_{OUT} low delay	1ms ramp from 30 V to 0 V		6		µs
t_{FS}	Failsafe output delay time from input power loss			2.8		µs

(1) t_{sk-pp} is the maximum difference in same edge propagation delay times (either V_{IN+} to V_{OUT} or $V_{IN–}$ to V_{OUT}) between two devices operating at the same supply voltage, same temperature, and having identical packages and test circuits.

$$\text{i.e. max} \left\{ \begin{matrix} \left[t_{PHL\text{-}max}\left(V_{CC1}, V_{CC2}, T_A\right) - t_{PHL\text{-}min}\left(V_{CC1}, V_{CC2}, T_A\right) \right], \\ \left[t_{PLH\text{-}max}\left(V_{CC1}, V_{CC2}, T_A\right) - t_{PLH\text{-}min}\left(V_{CC1}, V_{CC2}, T_A\right) \right] \end{matrix} \right\}$$

(2) t_{sk2-pp} is the propagation delay difference in high-to-low to low-to-high transition (any of the combinations V_{IN+} to V_{OUT} or $V_{IN–}$ to V_{OUT}) between two devices operating at the same supply voltage, same temperature, and having identical packages and test circuits.

$$\text{i.e.} \quad \text{min} = t_{PHL\text{-}min}\left(V_{CC1}, V_{CC2}, T_A\right) - t_{PLH\text{-}max}\left(V_{CC1}, V_{CC2}, T_A\right)$$
$$\text{max} = t_{PHL\text{-}max}\left(V_{CC1}, V_{CC2}, T_A\right) - t_{PLH\text{-}min}\left(V_{CC1}, V_{CC2}, T_A\right)$$

6.7 Typical Characteristics

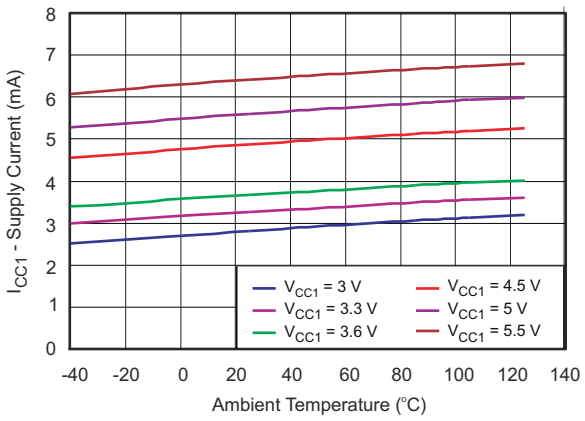


Figure 6-1. V_{CC1} Supply Current vs. Temperature

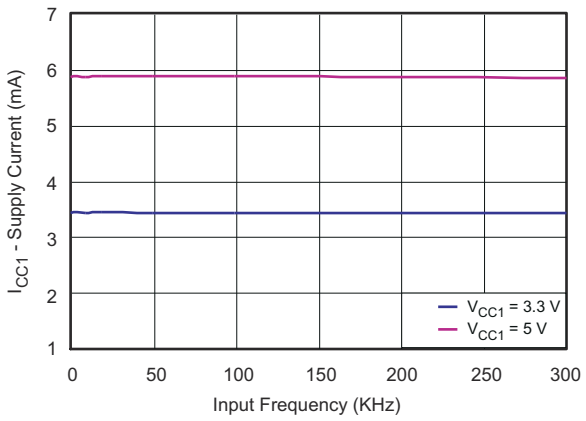


Figure 6-2. V_{CC1} Supply Current vs. Frequency

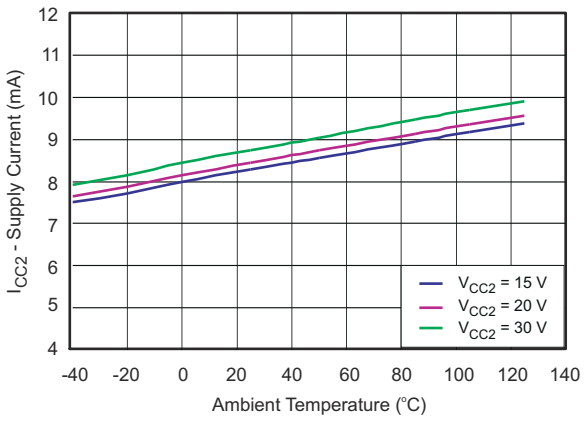


Figure 6-3. V_{CC2} Supply Current vs. Temperature

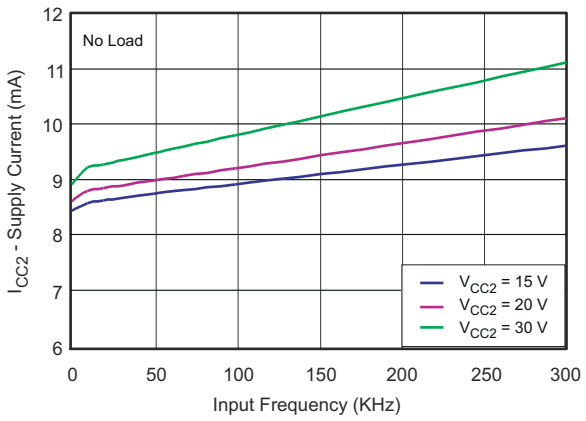


Figure 6-4. V_{CC2} Supply Current vs. Frequency

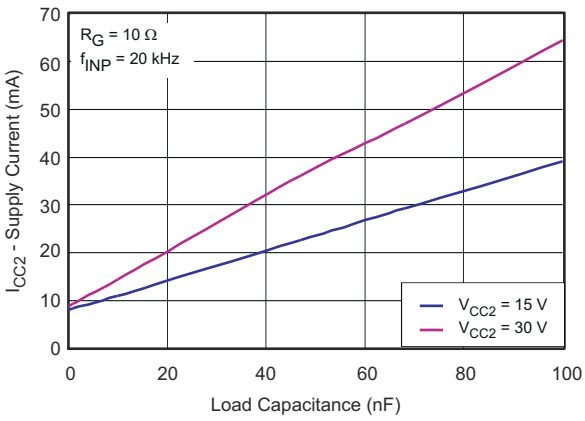


Figure 6-5. V_{CC2} Supply Current vs. Load Capacitance

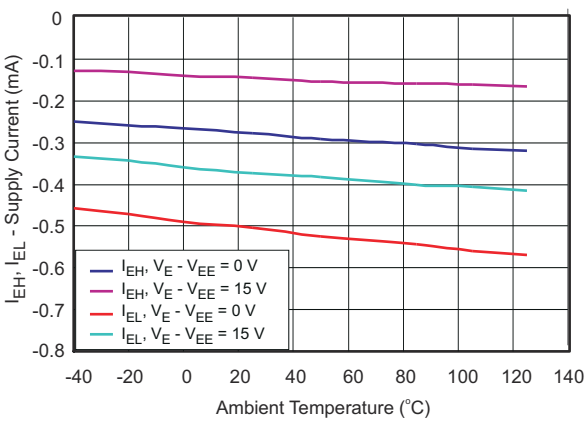


Figure 6-6. V_E Supply Current vs. Temperature

6.7 Typical Characteristics (continued)

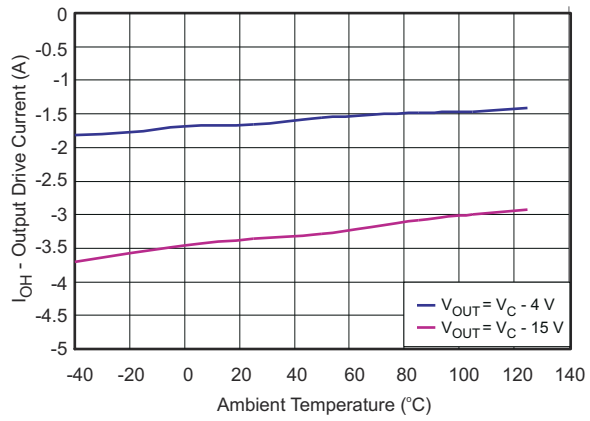


Figure 6-7. Output Drive Current vs. Temperature

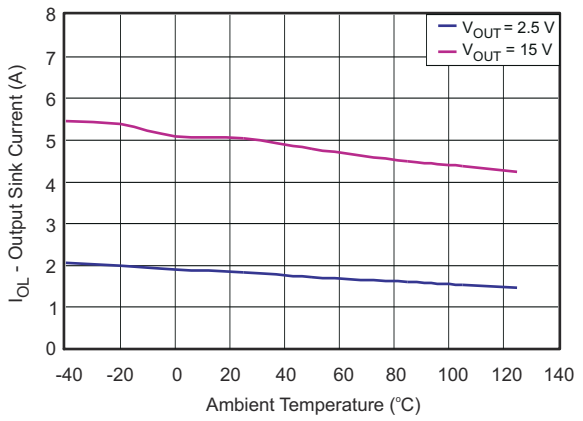


Figure 6-8. Output Sink Current vs. Temperature

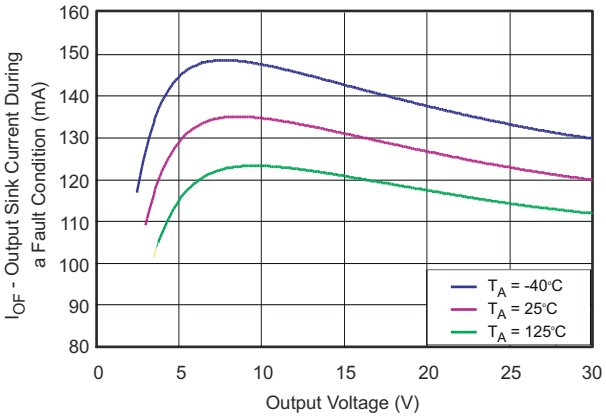


Figure 6-9. Output Sink Current During a Fault Condition vs. Output Voltage

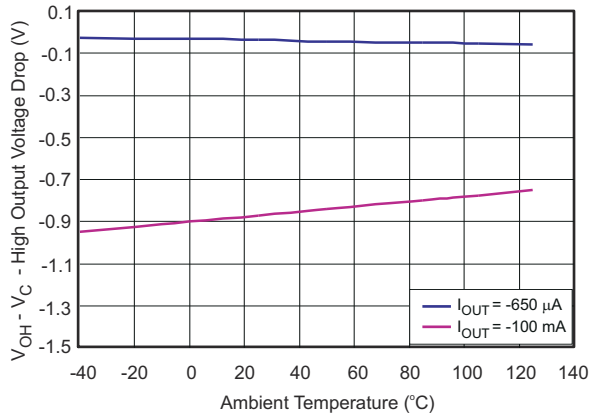


Figure 6-10. High Output Voltage Drop vs. Temperature

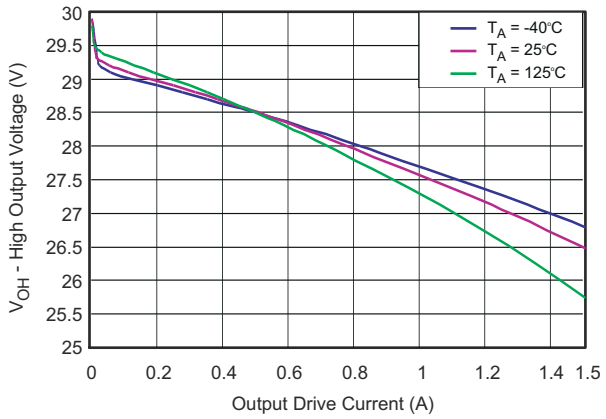


Figure 6-11. High Output Voltage vs. Output Drive Current

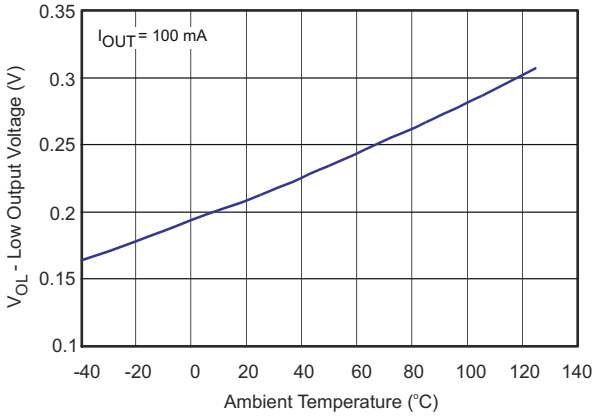


Figure 6-12. Low Output Voltage vs. Temperature

6.7 Typical Characteristics (continued)

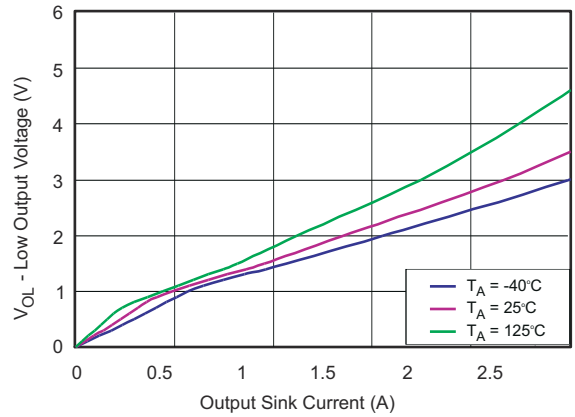


Figure 6-13. Low Output Voltage vs. Output Sink Current

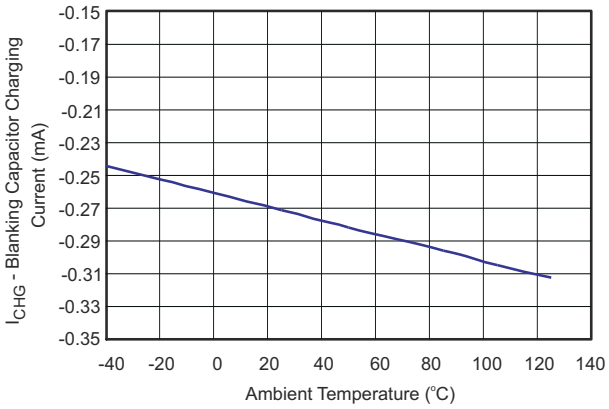


Figure 6-14. Blanking Capacitance Charging Current vs. Temperature

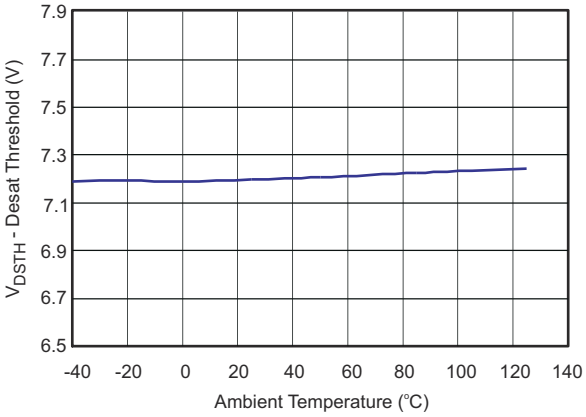


Figure 6-15. DESAT Threshold vs. Temperature

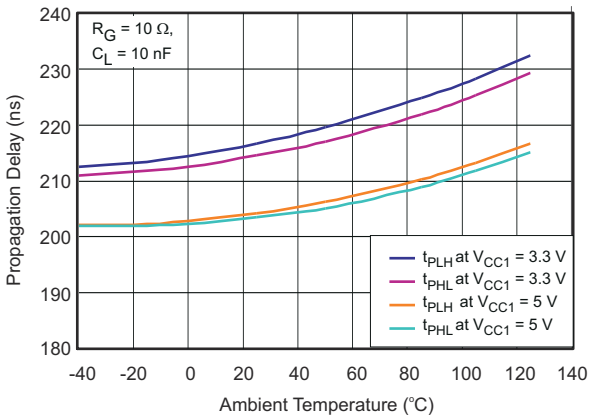


Figure 6-16. Propagation Delay vs. Temperature

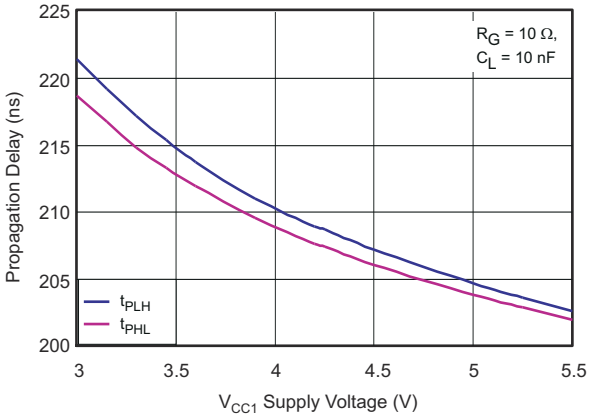


Figure 6-17. Propagation Delay vs. V_{CC1} Supply Voltage

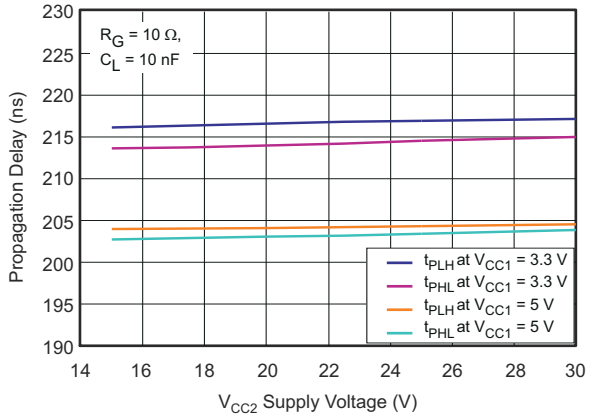


Figure 6-18. Propagation Delay vs. V_{CC2} Supply Voltage

6.7 Typical Characteristics (continued)

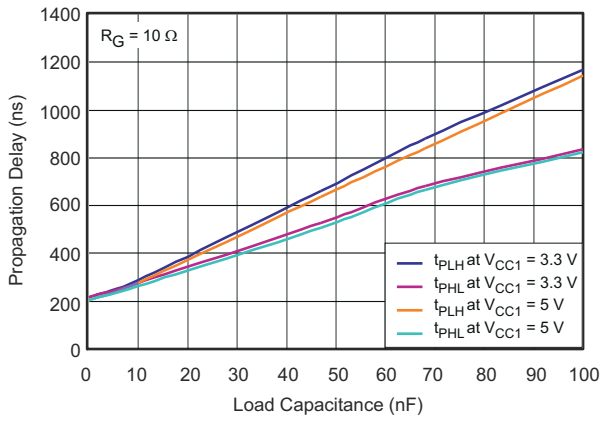


Figure 6-19. Propagation Delay vs. Load Capacitance

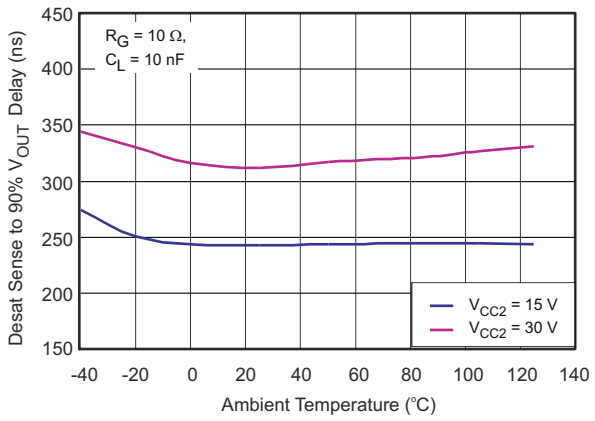


Figure 6-20. DESAT Sense to 90% V_{OUT} Delay vs Temperature

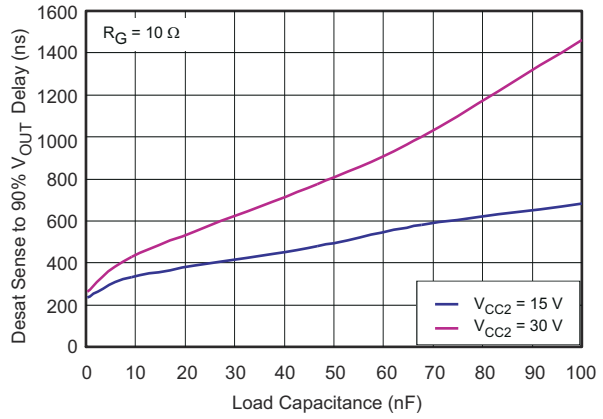


Figure 6-21. DESAT Sense to 90% V_{OUT} Delay vs Load Capacitance

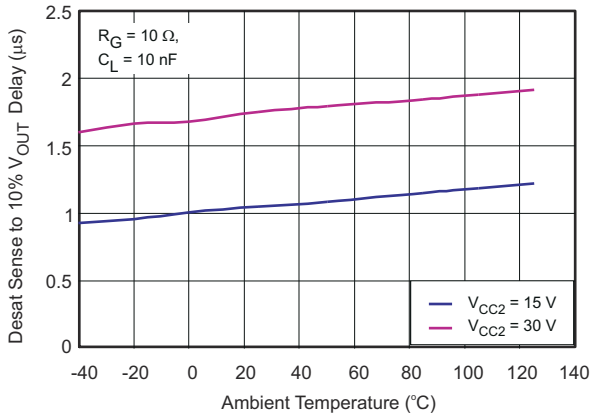


Figure 6-22. DESAT Sense to 10% V_{OUT} Delay vs Temperature

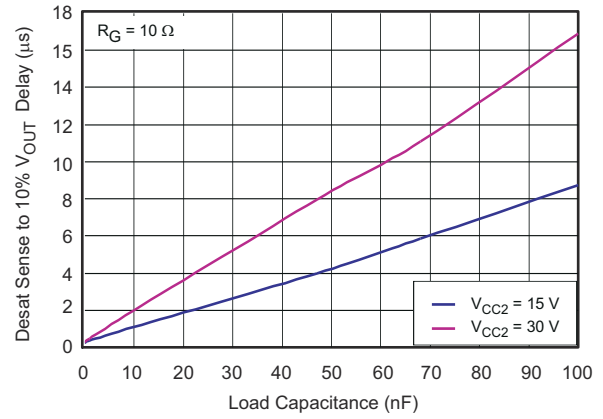


Figure 6-23. DESAT Sense to 10% V_{OUT} Delay vs Load Capacitance

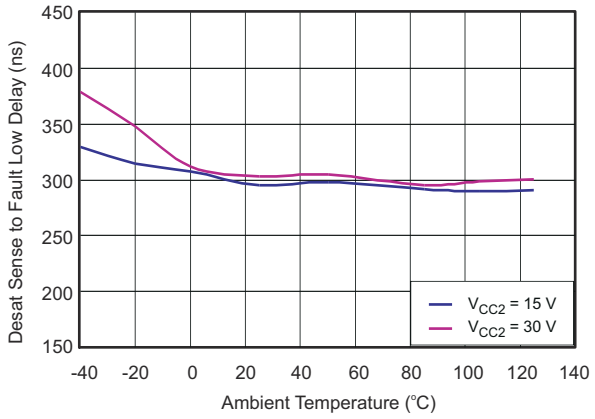


Figure 6-24. DESAT Sense to Fault Low Delay vs Temperature

6.7 Typical Characteristics (continued)

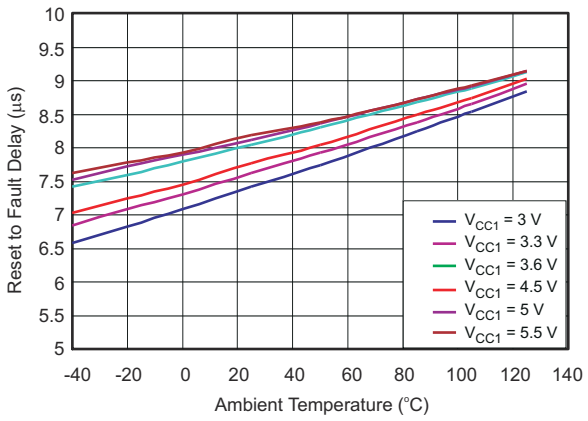


Figure 6-25. Reset to Fault Delay vs Temperature

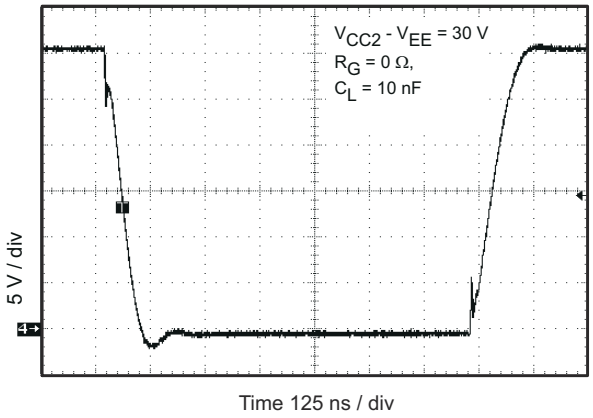


Figure 6-26. Output Waveform

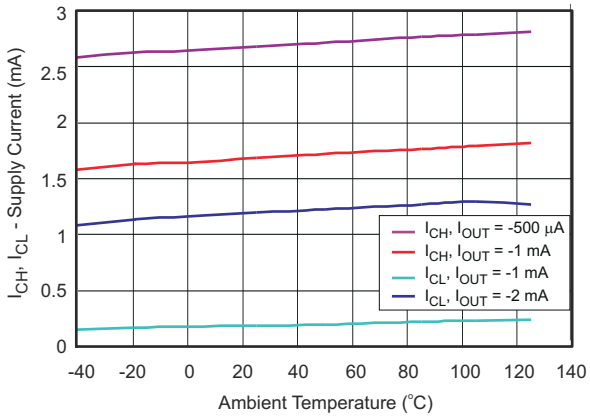


Figure 6-27. V_C Supply Current vs. Temperature

7 Parameter Measurement Information

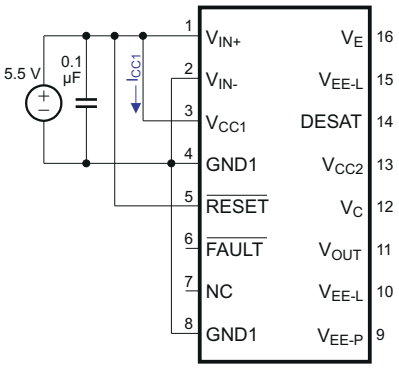


Figure 7-1. I_{CC1H} Test Circuit

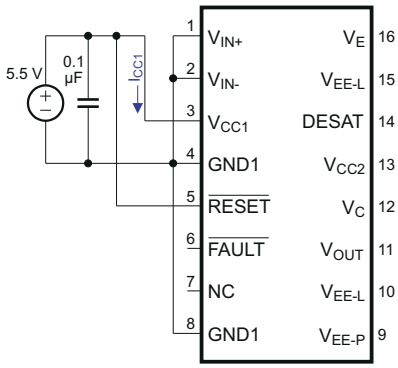


Figure 7-2. I_{CC1L} Test Circuit

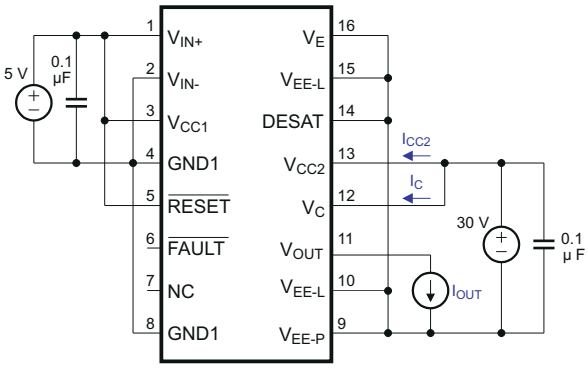


Figure 7-3. I_{CC2H}, I_{CH} Test Circuit

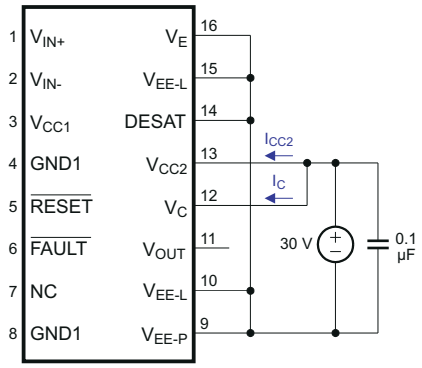


Figure 7-4. I_{CC2L}, I_{CL} Test Circuit

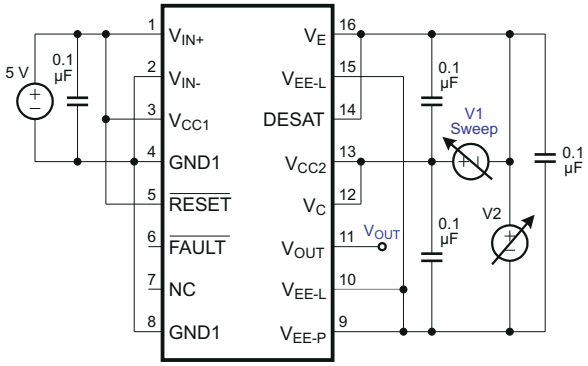


Figure 7-5. $V_{IT(UVLO)}$ Test Circuit

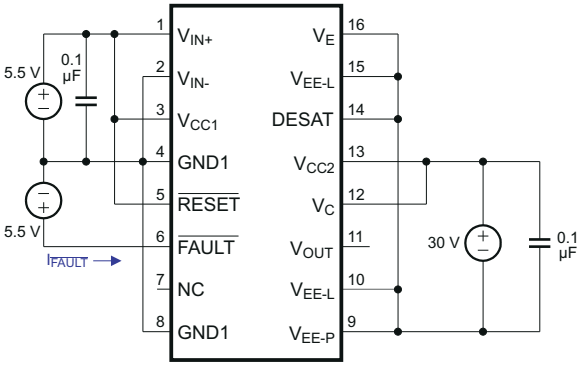


Figure 7-6. I_{FH} Test Circuit

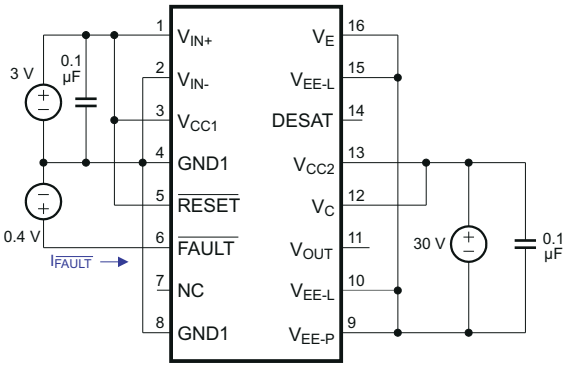


Figure 7-7. I_{FL} Test Circuit

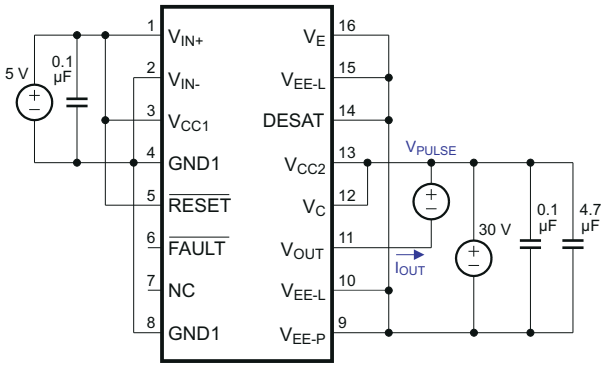


Figure 7-8. I_{OH} Test Circuit

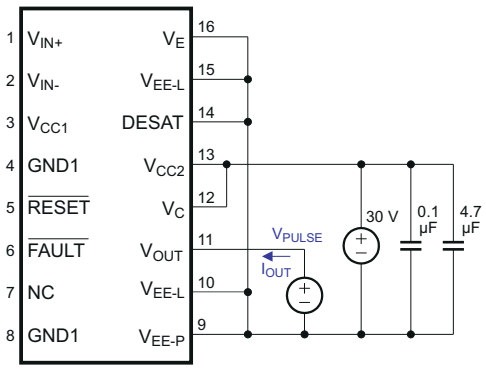


Figure 7-9. I_{OL} Test Circuit

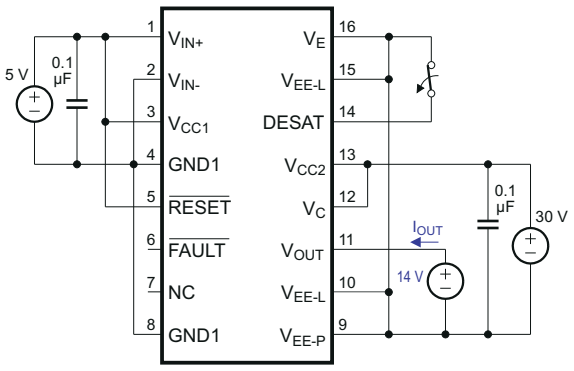


Figure 7-10. I_{OF} Test Circuit

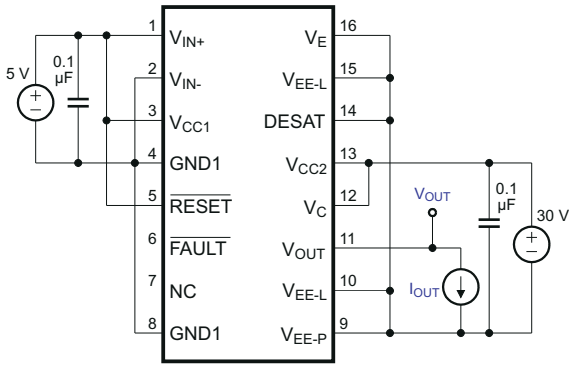


Figure 7-11. V_{OH} Test Circuit

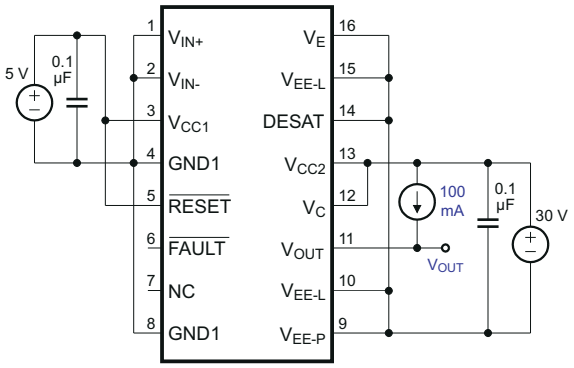


Figure 7-12. V_{OL} Test Circuit

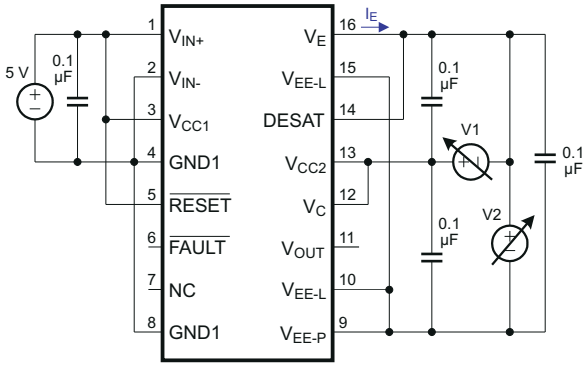


Figure 7-13. I_{EH} Test Circuit

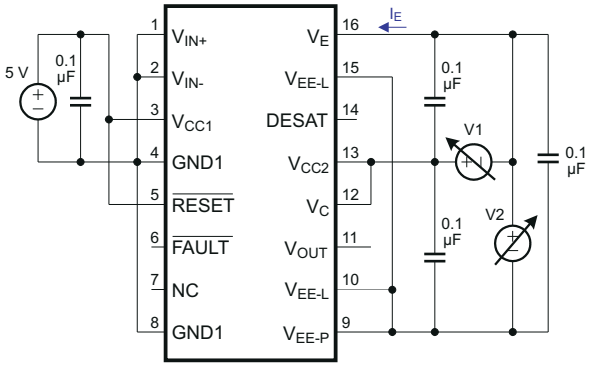


Figure 7-14. I_{EL} Test Circuit

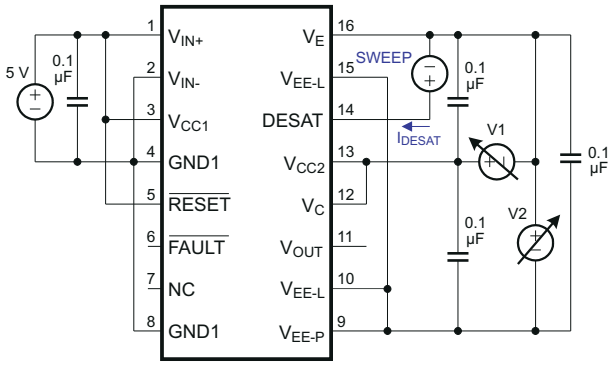


Figure 7-15. I_{CHG}, I_{DSCHG}, V_{DSTH} Test Circuit

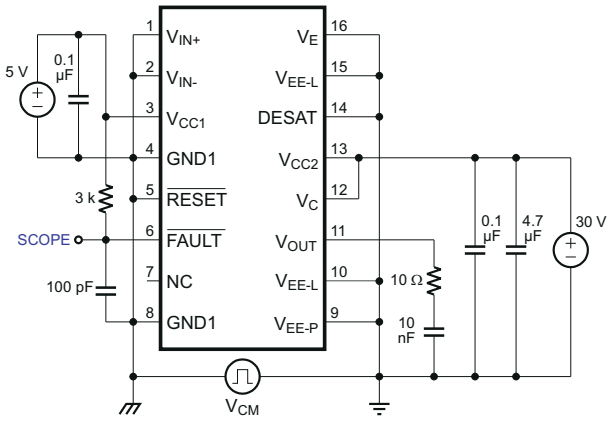


Figure 7-16. CMTI V_{FH} Test Circuit

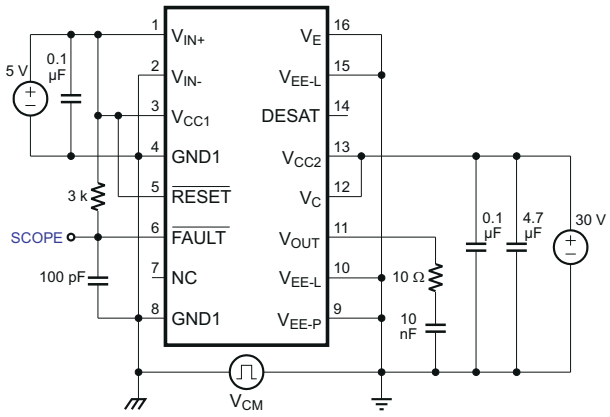


Figure 7-17. CMTI V_{FL} Test Circuit

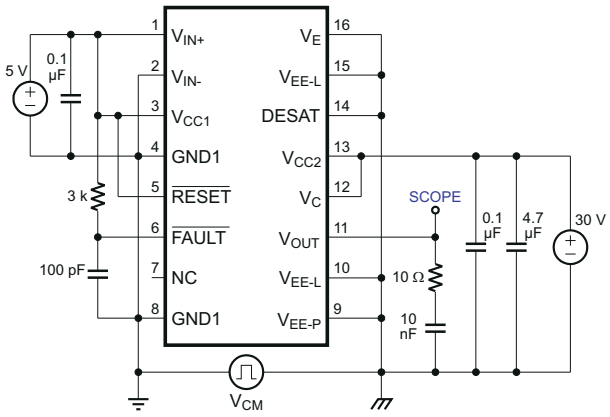


Figure 7-18. CMTI V_{OH} Test Circuit

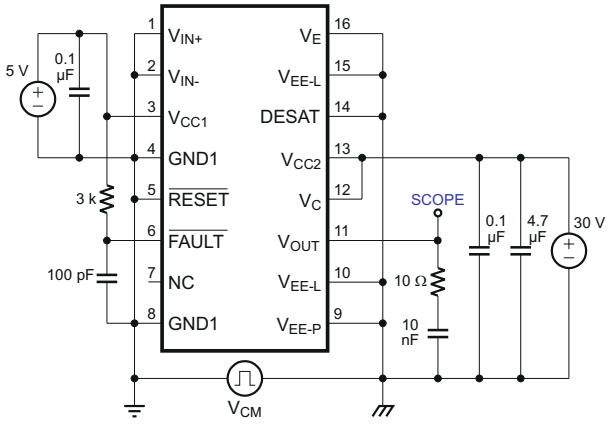


Figure 7-19. CMTI V_{OL} Test Circuit

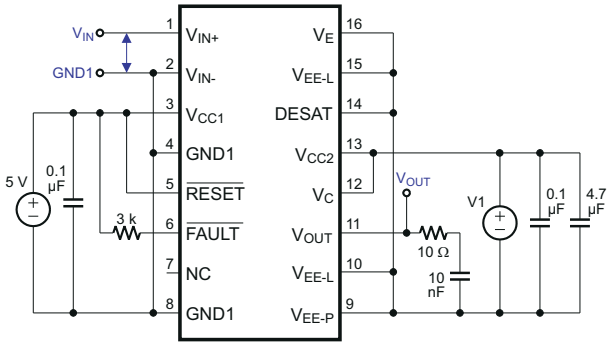


Figure 7-20. t_{PLH}, t_{PHL}, t_r, t_f Test Circuit

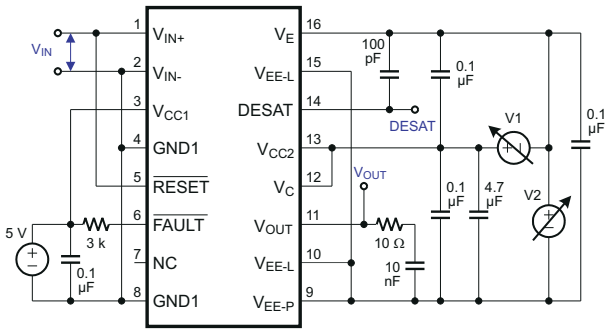


Figure 7-21. t_{DESAT}, $t_{\overline{RESET}}$ Test Circuit

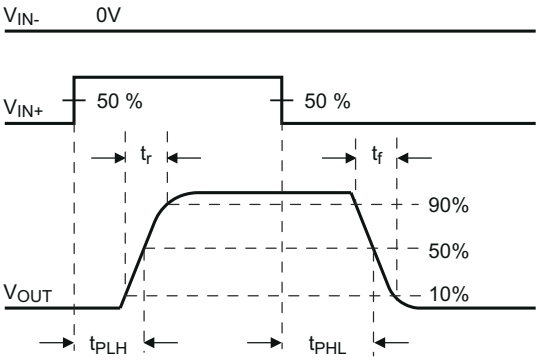


Figure 7-22. V_{OUT} Propagation Delay, Non-inverting Configuration

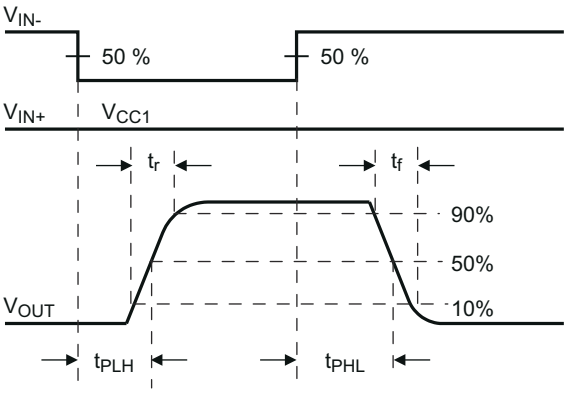


Figure 7-23. V_{OUT} Propagation Delay, Inverting Configuration

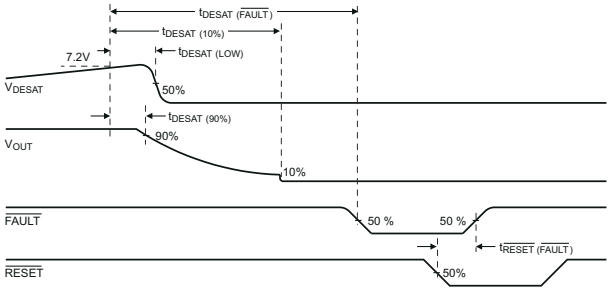


Figure 7-24. DESAT, V_{OUT}, $\overline{FAULT}$, $\overline{RESET}$ Delays

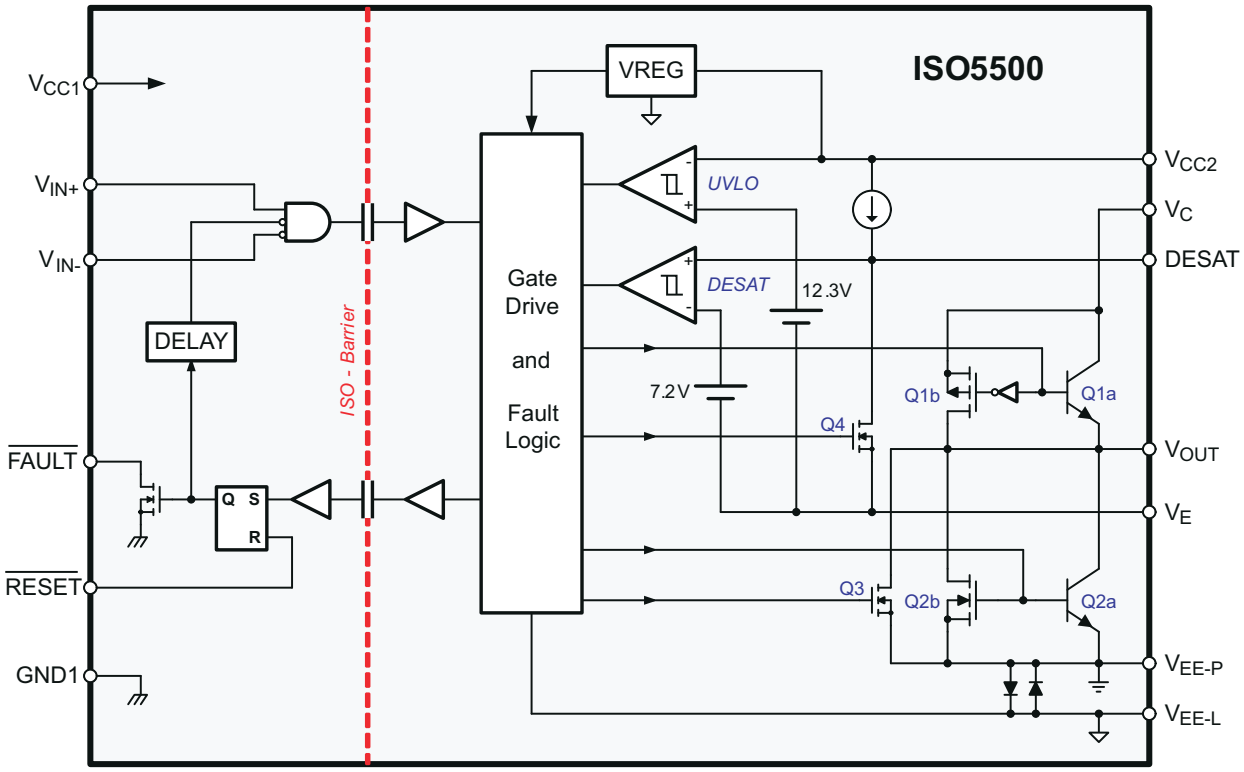
8 Detailed Description

8.1 Overview

The ISO5500 is an isolated gate driver for IGBTs and MOSFETs with power ratings of up to IC = 150 A and VCE = 600 V. Input TTL logic and output power stage are separated by a capacitive, silicon dioxide (SiO2), isolation barrier.

The IO circuitry on the input side interfaces with a micro controller and consists of gate drive control and $\overline{\text{RESET}}$ inputs, and $\overline{\text{FAULT}}$ alarm output. The power stage consists of power transistors to supply 2.5 A pullup and pulldown currents to drive the capacitive load of the external power transistors, as well as DESAT detection circuitry to monitor IGBT collector-emitter overvoltage under short circuit events. The capacitive isolation core consists of transmit circuitry to couple signals across the capacitive isolation barrier, and receive circuitry to convert the resulting low-swing signals into CMOS levels. The ISO5500 also contains undervoltage lockout circuitry to prevent insufficient gate drive to the external IGBT, and soft turnoff feature which ensures graceful reduction in IGBT current to zero when a short-circuit is detected.

8.2 Functional Block Diagram



8.3 Feature Description

Table 8-1. Package Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$L_{(I01)}$	Minimum air gap (clearance(2))	Shortest terminal to terminal distance through air	8.3			mm
$L_{(I02)}$	Minimum external tracking (creepage(2))	Shortest terminal to terminal distance across the package surface	8.1			mm
	Minimum internal gap (internal clearance)	Distance through the insulation	0.012			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	400			V
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V(1)		$>10^{12}$		Ω
C_{IO}	Barrier capacitance input-to-output	V_{IO} = 0.4 sin (2πft), f = 1 MHz(1)		1.25		pF
C_I	Input capacitance to ground	$V_I = V_{CC}/2 + 0.4$ sin (2π ft), f = 2 MHz, V_{CC} = 5V		2		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device
(2) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board do not reduce this distance.
Creepage and clearance on a printed circuit board become equal according to the measurement techniques shown in the isolation glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase their specification.

8.3.1 Insulation Characteristics for DW-16 Package

Over recommended operating conditions (unless noted otherwise)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage per DIN VDE V 0884-11		679/480	V_{PEAK}/ V_{RMS}
V_{PR}	Input to output test voltage per DIN VDE V 0884-11	After Input/Output safety test subgroup 2/3, V_{PR} = 1.2 x V_{IORM}, t = 10 s, Partial discharge < 5 pC	816/576	
		Method a, After environmental tests subgroup 1, V_{PR} = 1.6 × V_{IORM}, t = 10 s (qualification) Partial discharge < 5 pC	1088/768	
		Method b1, 100% Production test, V_{PR} = 1.875 × V_{IORM}, t = 1 sec Partial discharge < 5 pC	1275/900	
V_{IOTM}	Transient overvoltage per DIN VDE V 0884-11	V_{TEST} = V_{IOTM}, t = 60 sec (qualification), t = 1 s (100% production)	4000/2828	
V_{ISO}	Isolation voltage per UL 1577	V_{TEST} = V_{ISO}, t = 60 s (qualification)	3535/2500	
		V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production)		
R_S	Insulation resistance	V_{IO} = 500 V at T_S = 150°C	$>10^9$	Ω
	Pollution degree		2	

8.3.2 Regulatory Information

VDE	CSA	UL
Certified according to DIN VDE V 0884-11:2017-01	Approved under CSA	Recognized under UL 1577
Basic Insulation Maximum Transient Overvoltage, 4000 V_{PK} Maximum Working Voltage, 680 V_{PK}	CSA 62368-1:19, CSA 61010-1-12, UPD1: 2015, UPD2: 2016, AMD1: 2018	Component Acceptance Notice 5A, Component Recognition Program, Single Protection, 2500 V_{RMS}
Certificate Number: 40047657	Master Contract Number: 220991, Certificate Number: 2559124	File Number: E181974

8.3.3 IEC 60664-1 Rating Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic Isolation Group	Material Group	II
Installation Classification	Rated Mains Voltage ≤ 300 V_{RMS}	I-IV
	Rated Mains Voltage ≤ 600 V_{RMS}	I-III

8.3.4 Isolation Lifetime at a Maximum Continuous Working Voltage

PARAMETER	LIFETIME	SPECIFICATION	UNIT
Bipolar AC Voltage	20 years	679/480	V_{PEAK}/V_{RMS}
	25 years	657/465	
	50 years	601/425	

8.3.5 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety Limiting Current	θ_{JA} = 76°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			530	mA
		θ_{JA} = 76°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			347	
		θ_{JA} = 76°C/W, V_I = 30 V, T_J = 170°C, T_A = 25°C			64	
T_S	Case Temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Section 6.1* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Section 6.4* table is that of a device installed in the High-K Test Board for Leaded Surface-Mount Packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

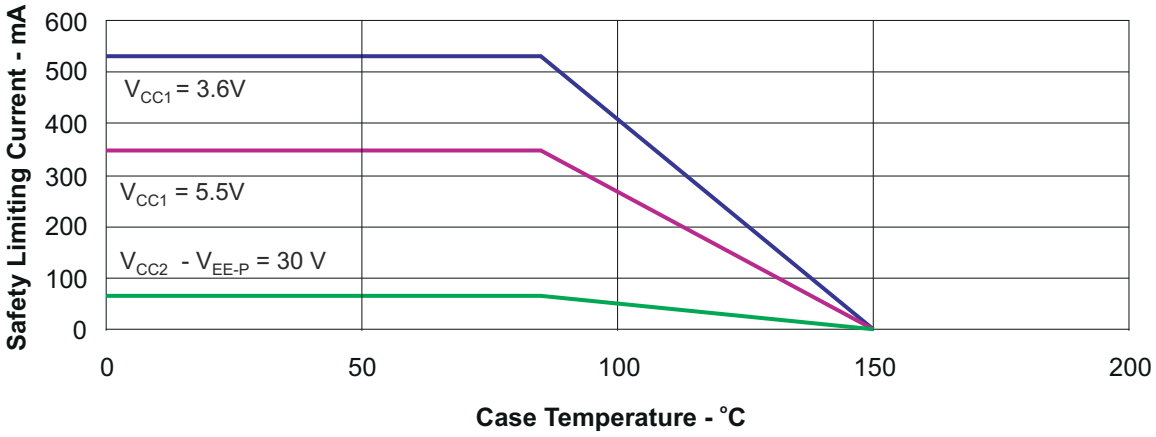


Figure 8-1. DW-16 θ_{JC} Thermal Derating Curve per DIN V VDE V 0884-10 (VDE V 0884-10)

8.3.6 Behavioral Model

Figure 8-2 and Figure 8-3 show the detailed behavioral model of the ISO5500 for a non-inverting input configuration and its corresponding timing diagram for normal operation, fault condition, and Reset.

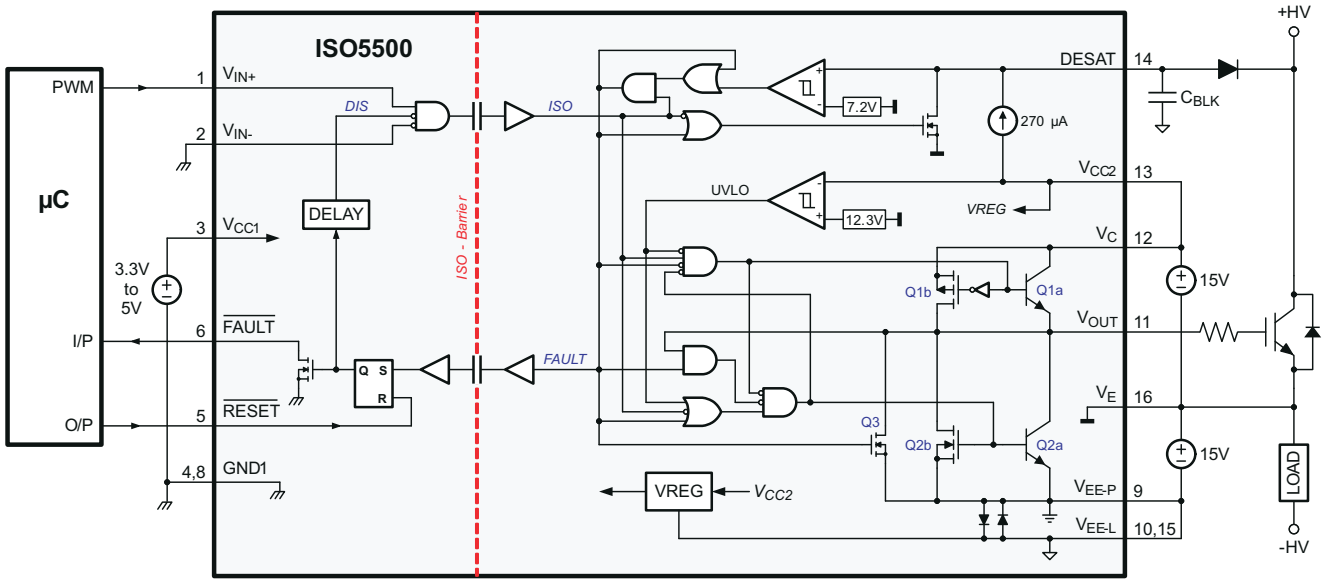


Figure 8-2. ISO5500 Behavioral Model

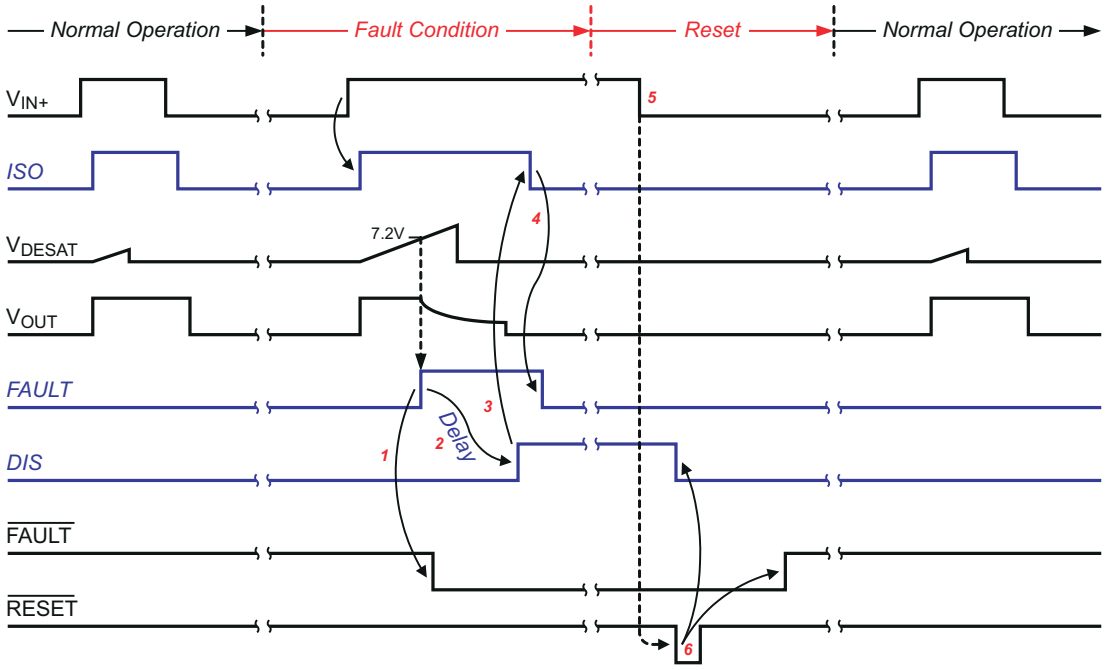


Figure 8-3. Complete Timing Diagram

8.3.7 Power Supplies

V_{CC1} and GND1 are the power supply input and output for the input side of the ISO5500. The supply voltage at V_{CC1} can range from 3 V up to 5.5 V with respect to GND1, thus supporting the direct interface to state-of-the-art 3.3 V low-power controllers as well as legacy 5 V controllers.

V_{CC2}, V_{EE-P} and V_{EE-L} are the power supply input and supply returns for the output side of the ISO5500. V_{EE-P} is the supply return for the output driver and V_{EE-L} is the return for the logic circuitry. With V_{EE-P} as the main reference potential, V_{EE-L} should always be directly connected to V_{EE-P}. The supply voltage at V_{CC2} can range from 15 V up to 30 V with respect to V_{EE-P}.

A third voltage input, V_E, serves as reference voltage input for the internal UVLO and DESAT comparators. V_E also represents the common return path for the gate voltage of the external power device. The ISO5500 is designed for driving MOSFETs and IGBTs. Because MOSFETs do not require a negative gate-voltage, the voltage potential at V_E with respect to V_{EE-P} can range from 0 V for MOSFETs and up to 15 V for IGBTs.

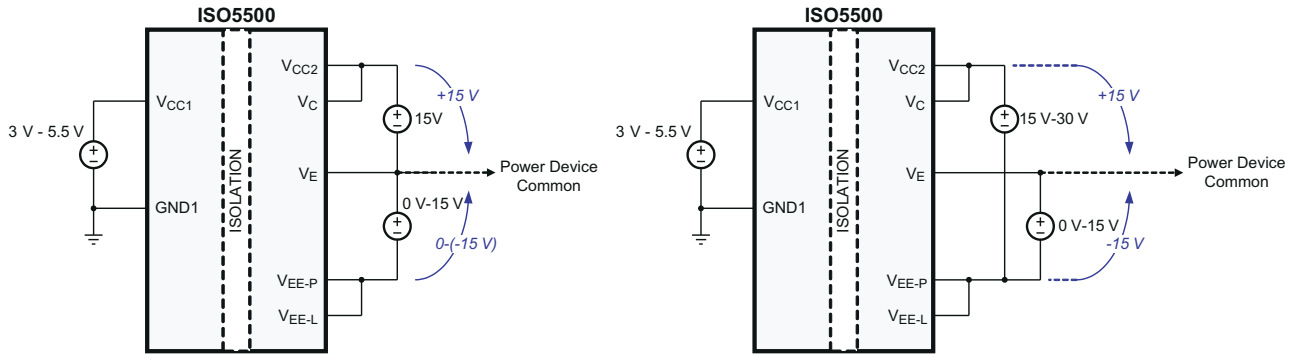


Figure 8-4. Power Supply Configurations

The output supply configuration on the left uses symmetrical ±15 V supplies for V_{CC2} and V_{EE-P} with respect to V_E. This configuration is mostly applied when deriving the output supply from the input supply via an isolated DC-DC converter with symmetrical voltage outputs. The configuration on the right, having both supplies referenced to V_{EE-P}, is found in applications where the device output supply is derived from the high-voltage IGBT supplies.

8.3.8 Control Signal Inputs

The two digital, TTL control inputs, V_{IN+} and V_{IN-}, allow for inverting and non-inverting control of the gate driver output. In the non-inverting configuration V_{IN+} receives the control input signal and V_{IN-} is connected to GND1. In the inverting configuration V_{IN-} is the control input while V_{IN+} is connected to V_{CC1}.

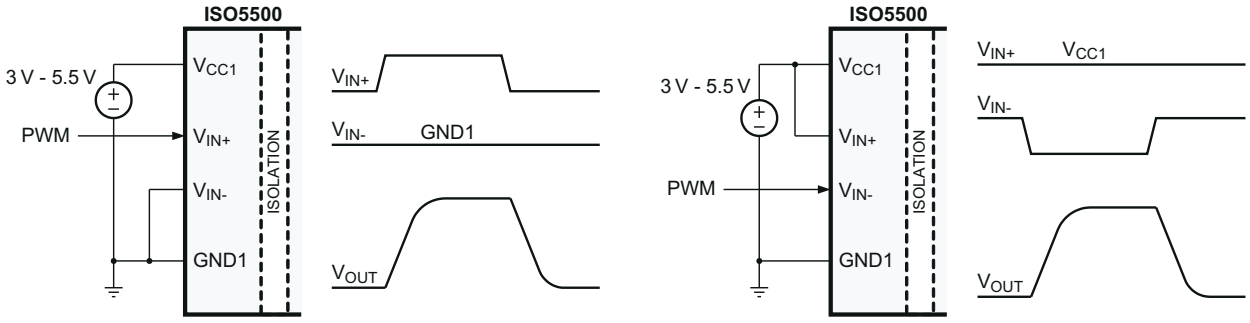


Figure 8-5. Non-inverting (left) and Inverting (right) Input Configurations

8.3.9 Output Stage

The output stage provides the actual IGBT gate drive by switching the output voltage pin, V_{OUT}, between the most positive potential, typically V_{CC2}, and the most negative potential, V_{EE-P}.

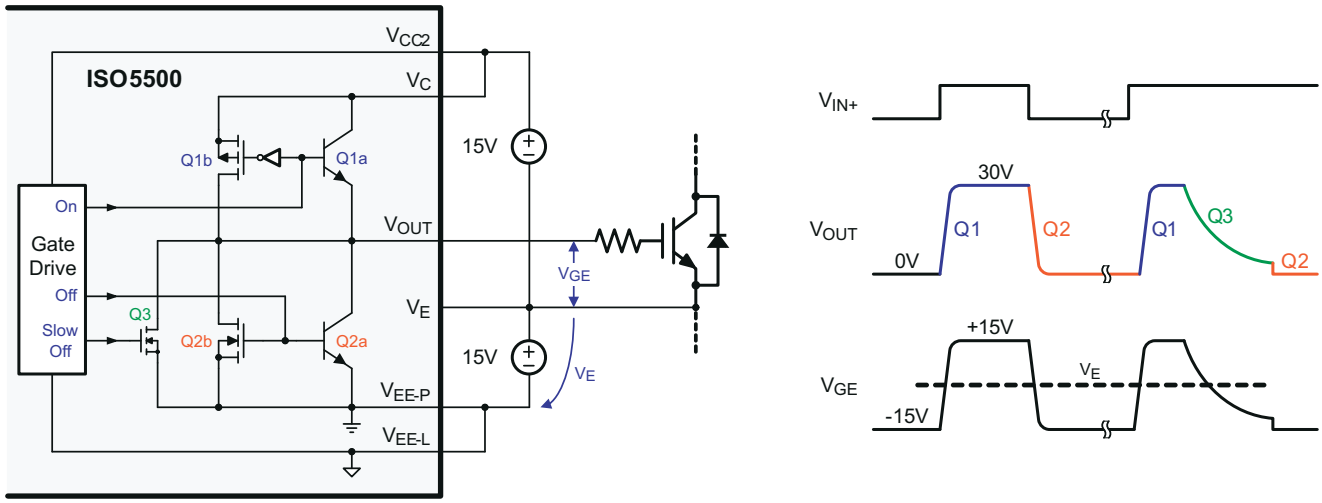


Figure 8-6. Output Stage Design and Timing

This stage consists of an upper transistor pair (Q1a and Q1b) turning the IGBT on, and a lower transistor pair (Q2a and Q2b) turning the IGBT off. Each transistor pair possesses a bipolar transistor for high current drive and a MOSFET for close-to-rail switching capability.

An additional, weak MOSFET (Q3) is used to softly turn-off the IGBT in the event of a short circuit fault to prevent large di/dt voltage transients which potentially could damage the output circuitry.

The output control signals, On, Off, and Slow-Off are provided by the gate-drive and fault-logic circuit which also includes a break-before-make function to prevent both transistor pairs from conducting at the same time.

By introducing the reference potential for the IGBT emitter, V_E, the final IGBT gate voltage, V_{GE}, assumes positive and negative values with respect to V_E.

A positive V_{GE} of typically 15 V is required to switch the IGBT well into saturation while assuring the survival of short circuit currents of up to 5–10 times the rated collector current over a time span of up to 10 µs.

Negative values of V_E, ranging from a required minimum of –5 V up to a recommended –15 V, are necessary to keep the IGBT turned off and to prevent it from unintentional conducting due to noise transients, particularly during short circuit faults. As previously mentioned, MOSFETs do not require a negative gate-voltage and thus allow the V_E-pin to be directly connected to V_{EE-P}.

The timing diagram in Figure 8-6 shows that during normal operation V_{OUT} follows the switching sequence of V_{IN+} (here shown for the non-inverting input configuration), and only the Q1 and Q2 transistor pairs applying V_{CC2} and V_{EE-P} potential to the V_{OUT}-pin respectively.

In the event of a short circuit fault, however, while the IGBT is actively driven, the Q1 pair is turned off and Q3 turns on to slowly reduce V_{OUT} in a controlled manner down to a level of approximately 2 V above V_{EE-P}. At this voltage level, the strong Q2 pair then conducts holding V_{OUT} at V_{EE-P} potential.

8.3.10 Undervoltage Lockout (UVLO)

The Under Voltage Lockout feature prevents the application of insufficient gate voltage (V_{GE-ON}) to the power device by forcing V_{OUT} low ($V_{OUT} = V_{EE-P}$) during power-up and whenever else $V_{CC2} – V_E$ drops below 12.3 V.

IGBTs and MOSFETs typically require gate voltages of V_{GE} = 15 V to achieve their rated, low saturation voltage, V_{CES}. At gate voltages below 13 V typically, their V_{CE-ON} increases drastically, especially at higher collector currents. At even lower voltages, i.e. V_{GE} < 10 V, an IGBT starts operating in the linear region and quickly overheats. Figure 8-7 shows the principle operation of the UVLO feature.

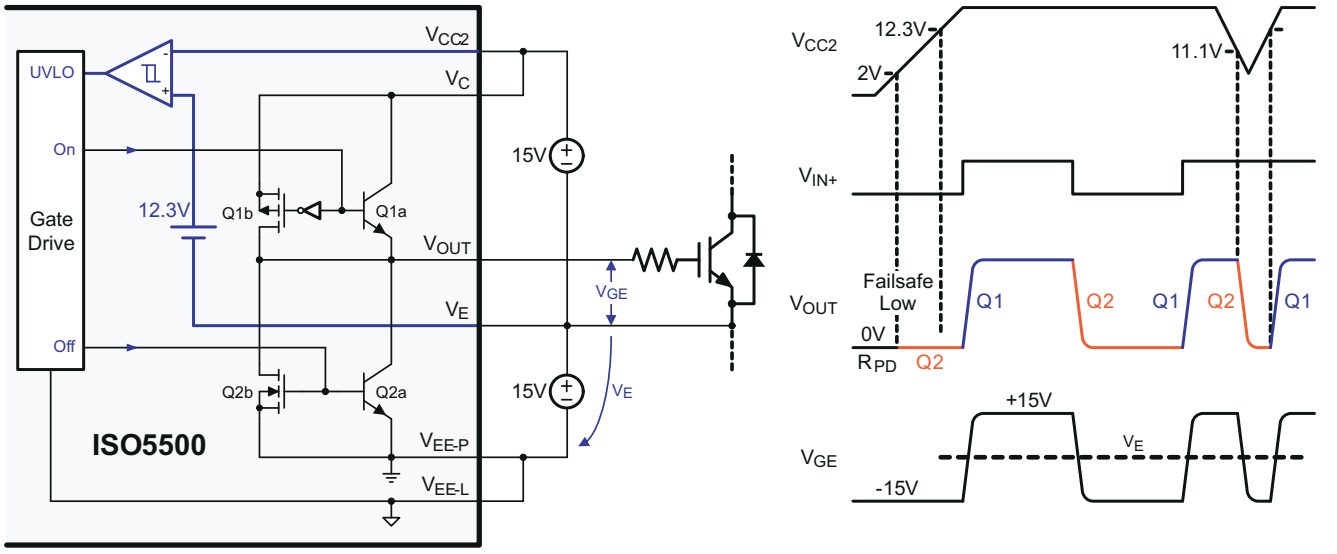


Figure 8-7. Undervoltage Lockout (UVLO) Function

Because V_{CC2} with respect to V_E represents the gate-on voltage, $V_{GE-ON} = V_{CC2} – V_E$, the UVLO comparator compares V_{CC2} to a 12.3 V reference voltage that is also referenced to V_E via the connection of the ISO5500 V_E-pin to the emitter potential of the power device.

The comparator hysteresis is 1.2 V typical and the typical values for the positive and negative going input threshold voltages are V_{TH+} = 12.3 V and $V_{TH–}$ = 11.1 V.

The timing diagram shows that at V_{CC2} levels below 2 V V_{OUT} is 0 V. Because none of the internal circuitry operates at such low supply levels, an internal 100 kΩ pull-down resistor is used to pull V_{OUT} down to V_{EE-P} potential. This initial weak clamping, known as failsafe-low output, strengthens with rising V_{CC2}. Above 2 V the Q2-pair starts conducting gradually until V_{CC2} reaches 12.3 V at which point the logic states of the control inputs V_{IN+} and $V_{IN–}$ begin to determine the state of V_{OUT}.

Another UVLO event takes place should V_{CC2} drop slightly below 11 V while the IGBT is actively driven. At that moment the UVLO comparator output causes the gate-drive logic to turn off Q1 and turn on Q2. Now V_{OUT} is clamped hard to V_{EE-P}. This condition remains until V_{CC2} returns to above 12.3 V and normal operation commences.

Note

An Undervoltage Lockout does not indicate a Fault condition.

8.3.11 Desaturation Fault Detection (DESAT)

The DESAT fault detection prevents IGBT destruction due to excessive collector currents during a short circuit fault. Short circuits caused by user misconnect, bad wiring, or overload conditions induced by the load can cause a rapid increase in IGBT current, leading to excessive power dissipation and heating. IGBTs become damaged when the current load approaches the saturation current of the device and the collector-emitter voltage, V_{CE}, rises above the saturation voltage level, V_{CE-sat}. The drastically increased power dissipation overheats and destroys the IGBT.

To prevent damage to IGBT applications, the implemented fault detection slowly reduces the overcurrent in a controlled manner during the fault condition.

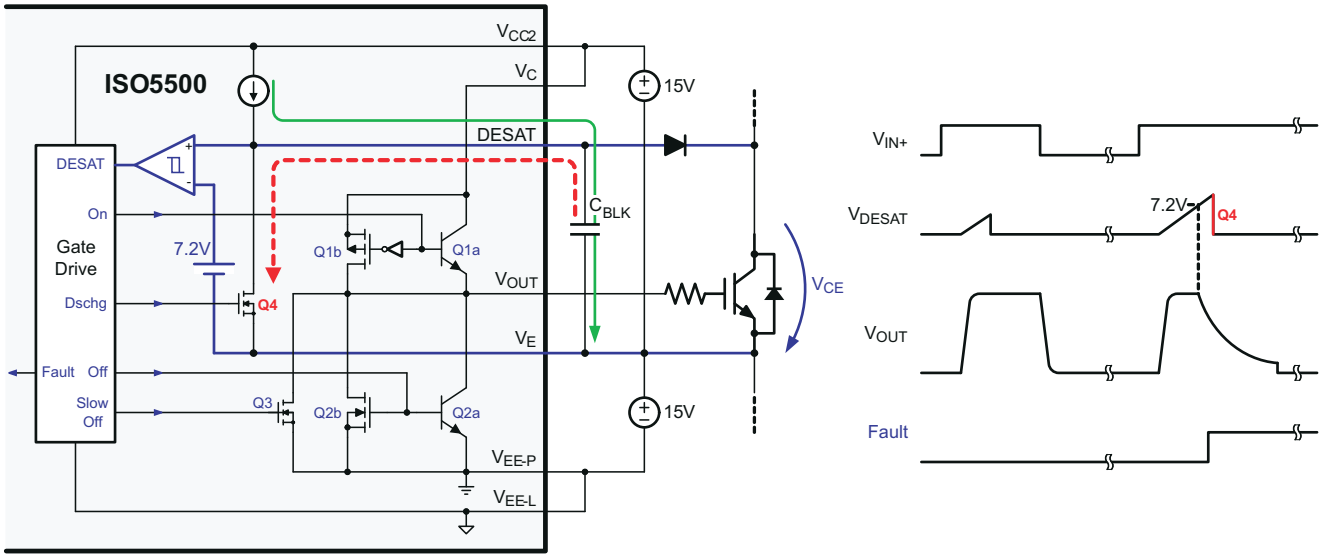


Figure 8-8. DESAT Fault Detection and Protection

The DESAT fault detection involves a comparator that monitors the IGBT's V_{CE} and compares it to an internal 7.2 V reference. If V_{CE} exceeds this reference voltage, the comparator causes the gate-drive and fault-logic to initiate a fault shutdown sequence. This sequence starts with the immediate generation of a fault signal, which is transmitted across the isolation barrier towards the Fault indicator circuit at the input side of the ISO5500.

At the same time the fault logic turns off the power-pair Q1 and turns on the small discharge MOSFETs, Q3 and Q4. Q3 slowly discharges the IGBT gate voltage which causes the high short-circuit current through the IGBT to gradually decrease, thereby preventing large di/dt induced voltage transients. Q4 discharges the blanking capacitor. Once V_{OUT} is sufficiently close to V_{EE-P} potential (at approximately 2 V), the large Q2-pair turns on in addition to Q3 to clamp the IGBT gate to V_{EE-P}.

Note

The DESAT detection circuit is only active when the IGBT is turned on. When the IGBT is turned off, and its V_{CE} is at maximum, the fault detection is simply disabled to prevent false triggering of fault signals.

8.3.12 DESAT Blanking Time

The DESAT fault detection must remain disabled for a short time period following the turn-on of the IGBT to allow its collector voltage to drop below the 7.2 V DESAT threshold. This time period, called the DESAT blanking time, t_{BLK}, is controlled by an internal charge current of I_{CHG} = 270 µA, the 7.2 V DESAT threshold, V_{DSTH}, and an external blanking capacitor, C_{BLK}.

The nominal blanking time with a recommended capacitor value of C_{BLK} = 100 pF is calculated with:

$$t_{BLK} = \frac{C_{BLK} \times V_{DSTH}}{I_{CHG}} = \frac{100\ pF \times 7.2\ V}{270\ \mu A} = 2.7\ \mu s \quad (1)$$

The capacitor value can be scaled slightly to adjust the blanking time. However, because the blanking capacitor and the DESAT diode capacitance build a voltage divider that attenuates large voltage transients at DESAT, C_{BLK} values smaller than 100 pF are not recommended. The nominal blanking time also represents the ISO5500 maximum response time to a DESAT fault condition.

If a short circuit condition exists prior to the turn-on of the IGBT, (*causing the IGBT switching into a short*) the soft shutdown sequence begins after approximately 3 µs. However, if a short circuit condition occurs while the IGBT is already on, the response time is significantly shorter due to the parasitic parallel capacitance of the DESAT

diode. The recommended value of 100 pF however, provides sufficient blanking and fault response times for most applications.

The timing diagram in Figure 8-8 shows the DESAT function for both, normal operation and a short-circuit fault condition. The use of V_{IN+} as control input implies non-inverting input configuration.

During normal operation V_{DESAT} will display a small sawtooth waveform every time V_{IN+} goes high. The ramp of the sawtooth is caused by the internal current source charging the blanking capacitor. Once the IGBT collector has sufficiently dropped below the capacitor voltage, the DESAT diode conducts and discharges C_{BLK} through the IGBT.

In the event of a short circuit fault; however, high IGBT collector voltage prevents the diode from conducting and the voltage at the blanking capacitor continues to rise until it reaches the DESAT threshold. When the output of the DESAT comparator goes high, the gate-drive and fault-logic circuit initiates the soft shutdown sequence and also produces a Fault signal that is fed back to the input side of the ISO5500.

8.3.13 $\overline{\text{FAULT}}$ Alarm

The Fault alarm unit consists of three circuit elements, a RS flip-flop to store the fault signal received from the gate-drive and fault-logic, an open-drain MOSFET output signaling the fault condition to the micro controller, and a delay circuit blocking the control inputs after the soft shutdown sequence of the IGBT has been completed.

Figure 8-9 shows the ISO5500 in a non-inverting input configuration. Because the $\overline{\text{FAULT}}$-pin is an open-drain output, it requires a pull-up resistor, R_{PU}, in the order of 3.3 kΩ to 10 kΩ. The internal signals DIS, ISO, and FAULT represent the input-disable signal, the isolator output signal, and the fault feedback signal respectively.

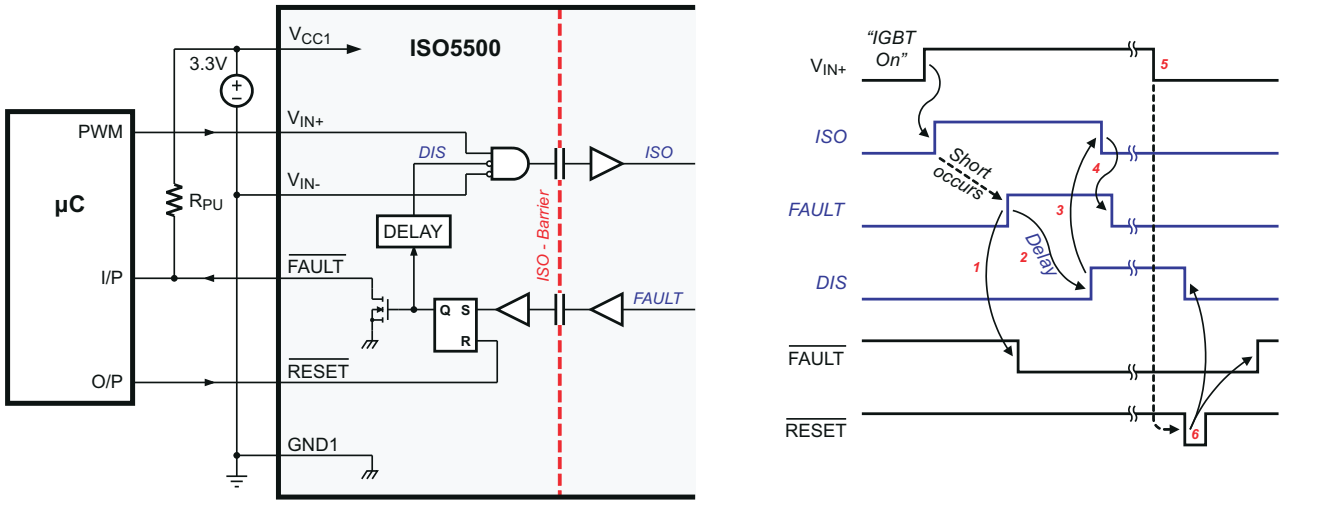


Figure 8-9. Fault Alarm Circuitry and Timing Sequence

The timing diagram shows that the micro controller initiates an IGBT-on command by taking V_{IN+} high. After propagating across the isolation barrier ISO goes high, activating the output stage.

1. Upon a short circuit condition the gate-drive and fault-logic feeds back a fault signal (*FAULT* = *high*) which sets the RS-FF driving the $\overline{\text{FAULT}}$ output active-low.
2. After a delay of approximately 3 µs, the time required to shutdown the IGBT, *DIS* becomes high and blocks the control inputs
3. This in turn drives *ISO* low
4. which, after propagating through the output fault-logic, drives *FAULT* low.

   At this time both flip-flop inputs are low and the fault signal is stored.
5. Once the failure cause has been removed the micro controller must set the control inputs into an "Output-low" state before applying the Reset pulse.
6. Taking the $\overline{\text{RESET}}$-input low resets the flip-flop, which removes the fault signal from the controller by pulling $\overline{\text{FAULT}}$ high and releases the control inputs by driving *DIS* low

8.4 Device Functional Modes

Table 8-2. Function Table

V_{IN}+	V_{IN}-	UVLO (V_{CC2} – V_E)	DESAT DETECTED ON PIN 14 (DESAT)	PIN 6 ($\overline{FAULT}$) OUTPUT	V_{OUT}
X	X	Active	X	X	Low
X	X	X	Yes	Low	Low
Low	X	X	X	X	Low
X	High	X	X	X	Low
High	Low	Not active	No	High	High

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO5500 is an isolated gate driver for high power devices such as IGBTs and MOSFETs with power ratings of up to IC = 150 A and VCE = 600 V. It is intended for use in applications such as motor control, industrial inverters and switched-mode power supplies. In these applications, sophisticated PWM control signals are required to turn the power-devices on and off, which at the system level eventually may determine, for example, the speed, position, and torque of the motor or the output voltage, frequency and phase of the inverter. These control signals are usually the outputs of a micro controller, and are at low voltage levels such as 3.3 V or 5.0 V. The gate controls required by the MOSFETs and IGBTs, on the other hand, are in the range of 15 V to 30 V, and need high current capability to be able to drive the large capacitive loads offered by those power transistors. Not only that, the gate drive needs to be applied with reference to the Emitter of the IGBT (Source for MOSFET), and by construction, the Emitter node in a gate drive system swings between 0 to the DC bus voltage, which is several 100s of volts in magnitude.

The ISO5500 is thus used to level shift the incoming 3.3-V and 5.0-V control signals from the microcontroller to the 15-V to 30-V drive required by the power transistors while ensuring high-voltage isolation between the driver side and the microcontroller side.

9.2 Typical Application

Figure 9-1 shows the typical application of a three-phase inverter using six ISO5500 isolated gate drivers. Three-phase inverters are used for variable-frequency drives to control the operating speed of AC motors and for high power applications such as High-Voltage DC (HVDC) power transmission.

The basic three-phase inverter consists of three single-phase inverter switches each comprising two ISO5500 devices that are connected to one of the three load terminals. The operation of the three switches is coordinated so that one switch operates at each 60 degree point of the fundamental output waveform, thus creating a six-step line-to-line output waveform. In this type of applications carrier-based PWM techniques are applied to retain waveform envelope and cancel harmonics.

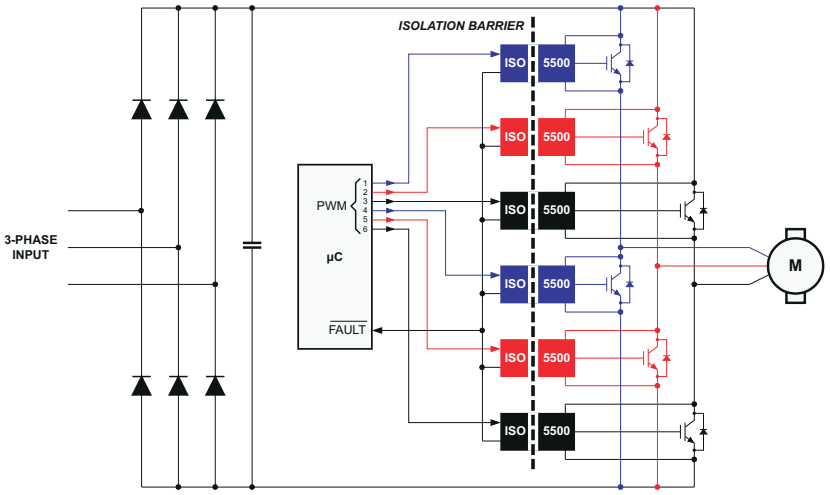


Figure 9-1. Typical Motor Drive Application

9.2.1 Design Requirements

Unlike optocoupler based gate drivers which need external current drivers and biasing circuitry to provide the input control signals, the input control to the ISO5500 is TTL and can be directly driven by the microcontroller. Other design requirements include decoupling capacitors on the input and output supplies, a pullup resistor on the common drain $\overline{\text{FAULT}}$ output signal, and a high-voltage protection diode between the IGBT collector and the DESAT input. Further details are explained in the subsequent sections.

9.2.2 Detailed Design Procedure

9.2.2.1 Recommended ISO5500 Application Circuit

The ISO5500 has both, inverting and non-inverting gate control inputs, an active low reset input, and an open drain fault output suitable for wired-OR applications. The recommended application circuit in Figure 9-2 illustrates a typical gate drive implementation using the ISO5500.

The four 0.1 µF supply bypass capacitors provide the large transient currents necessary during a switching transition. Because of the transient nature of the charging currents, low current (20 mA) power supplies for V_{CC2} and V_{EE-P} suffice. The 100 pF blanking capacitor disables DESAT detection during the off-to-on transition of the power device. The DESAT diode and its 100 Ω series resistor are important external protection components for the fault detection circuitry. The 10 Ω gate resistor limits the gate charge current and indirectly controls the IGBT collector voltage rise and fall times. The open-drain fault output has a passive 3.3 kΩ pull-up resistor and a 330pF filtering capacitor. In this application, the IGBT gate driver will shut down when a fault is detected and will not resume switching until the micro-controller applies a reset signal.

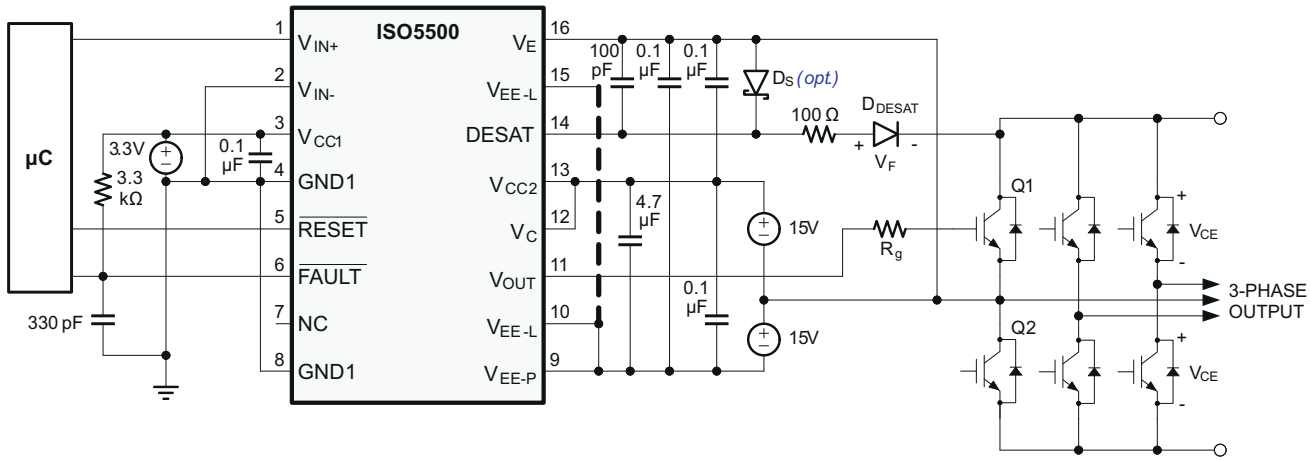


Figure 9-2. Recommended Application Circuit

9.2.2.2 $\overline{\text{FAULT}}$ Pin Circuitry

The $\overline{\text{FAULT}}$ pin is an open-drain output requiring a 3.3 kΩ pull-up resistor to provide logic high when $\overline{\text{FAULT}}$ is inactive.

Because fast common mode transients can alter the $\overline{\text{FAULT}}$-pin voltage during high state, a 330 pF capacitor connected between $\overline{\text{FAULT}}$ and GND1 is recommended to provide sufficient noise margin at the specified CMTI of 50 kV/µs. The added capacitance does not increase the $\overline{\text{FAULT}}$ response time during a fault condition.

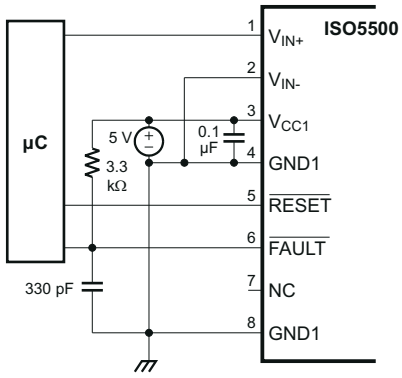


Figure 9-3. FAULT Pin Circuitry for High CMTI

9.2.2.3 Driving the Control Inputs

The amount of common-mode transient immunity (CMTI) is primarily determined by the capacitive coupling from the high-voltage output circuit to the low-voltage input side of the ISO5500. For maximum CMTI performance, the digital control inputs, V_{IN+} and $V_{IN–}$, must be actively driven by standard CMOS or TTL, push-pull drive circuits. This type of low-impedance signal source provides active drive signals that prevent unwanted switching of the ISO5500 output under extreme common-mode transient conditions. Passive drive circuits, such as open-drain configurations using pull-up resistors, must be avoided.

9.2.2.4 Local Shutdown and Reset

In applications with local shutdown and reset, the FAULT output of each gate driver is polled separately, and the individual reset lines are asserted low independently to reset the motor controller after a fault condition.

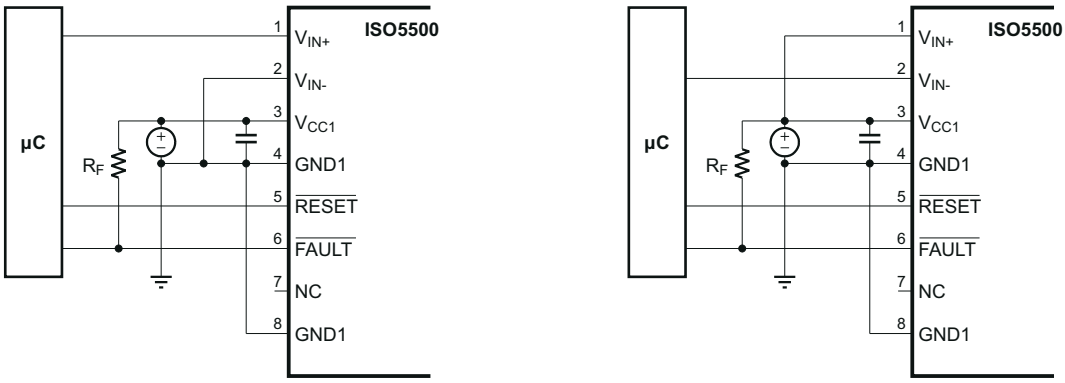


Figure 9-4. Local Shutdown and Reset for Noninverting (left) and Inverting Input Configuration (right)

9.2.2.5 Global-Shutdown and Reset

When configured for inverting operation, the ISO5500 can be configured to shutdown automatically in the event of a fault condition by tying the FAULT output to V_{IN+}. For high reliability drives, the open drain FAULT outputs of multiple ISO5500 devices can be wired together forming a single, common fault bus for interfacing directly to the micro-controller. When any of the six gate drivers of a three-phase inverter detects a fault, the active low FAULT output disables all six gate drivers simultaneously; thereby, providing protection against further catastrophic failures.

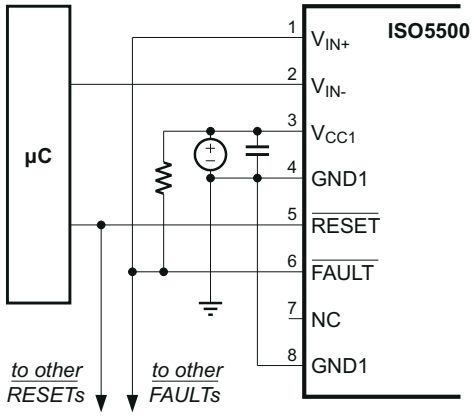


Figure 9-5. Global Shutdown with Inverting Input Configuration

9.2.2.6 Auto-Reset

Connecting $\overline{\text{RESET}}$ to the active control input (V_{IN+} for non-inverting, or $V_{IN–}$ for inverting operation) configures the ISO5500 for automatic reset capability. In this case, the gate control signal at V_{IN} is also applied to the $\overline{\text{RESET}}$ input to reset the fault latch every switching cycle. During normal IGBT operation, asserting $\overline{\text{RESET}}$ low has no effect on the output. For a fault condition, however, the gate driver remains in the latched fault state until the gate control signal changes to the 'gate low' state and resets the fault latch.

If the gate control signal is a continuous PWM signal, the fault latch will always be reset before V_{IN+} goes high again. This configuration protects the IGBT on a cycle by cycle basis and automatically resets before the next 'on' cycle. When the ISO5500 is configured for Auto Reset, the specified minimum $\overline{\text{FAULT}}$ signal pulse width is 3 µs.

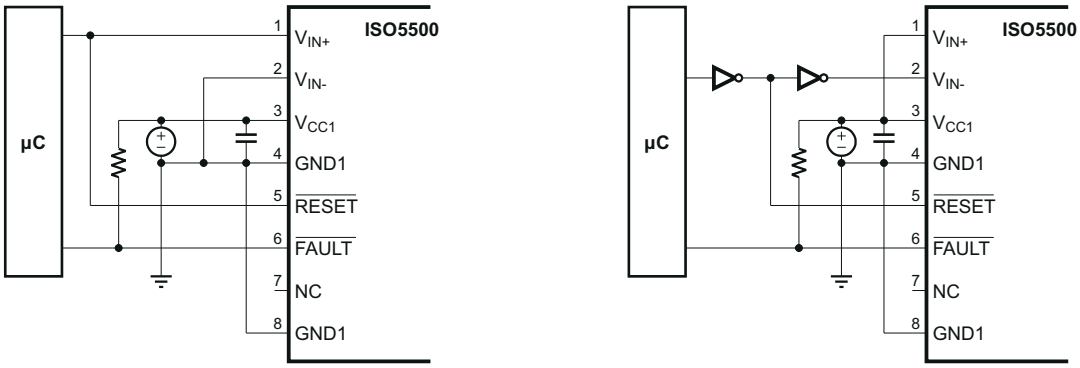


Figure 9-6. Auto Reset for Non-inverting and Inverting Input Configuration

9.2.2.7 Resetting Following a Fault Condition

To resume normal switching operation following a fault condition ($\overline{\text{FAULT}}$ output low), the gate control signal must be driven into a 'gate low' state before asserting $\overline{\text{RESET}}$ low. This can be accomplished with a micro-controller, or an additional logic gate that synchronizes the $\overline{\text{RESET}}$ signal with the appropriate input signal.

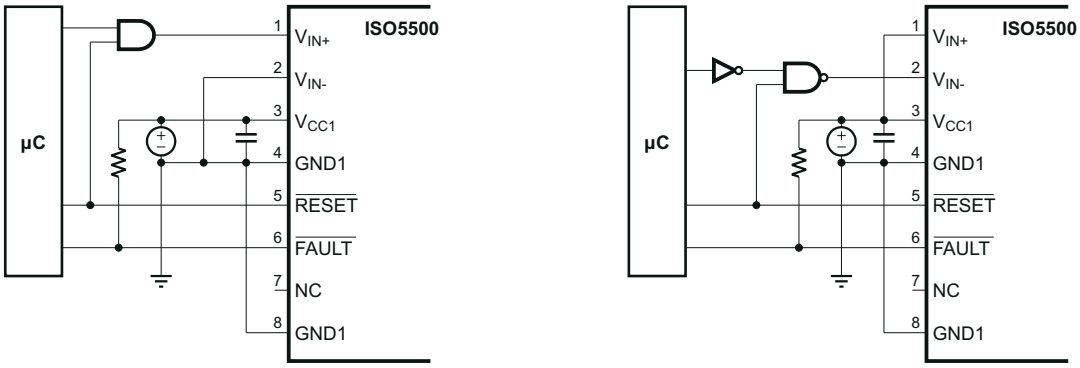


Figure 9-7. Auto Reset with Prior Gate-low Assertion for Non-inverting and Inverting Input Configuration

9.2.2.8 DESAT Pin Protection

Switching inductive loads causes large instantaneous forward voltage transients across the freewheeling diodes of IGBTs. These transients result in large negative voltage spikes on the DESAT pin which draw substantial current out of the device. To limit this current below damaging levels, a 100 Ω to 1 kΩ resistor is connected in series with the DESAT diode. The added resistance neither alters the DESAT threshold nor the DESAT blanking time.

Further protection is possible through an optional Schottky diode, whose low forward voltage assures clamping of the DESAT input to V_E potential at low voltage levels.

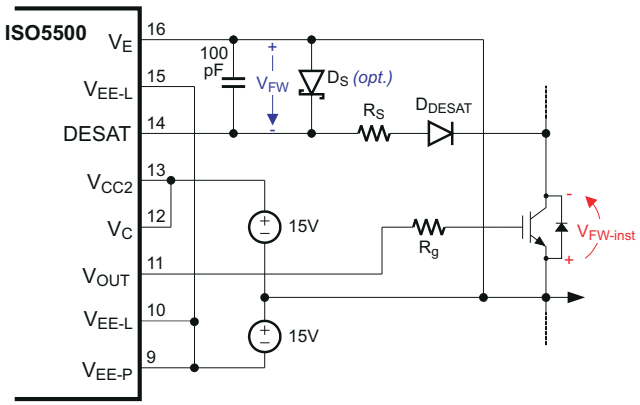


Figure 9-8. DESAT Pin Protection with Series Resistor and Optional Schottky Diode

9.2.2.9 DESAT Diode and DESAT Threshold

The DESAT diode's function is to conduct forward current, allowing sensing of the IGBT's saturated collector-to-emitter voltage, V_{CESAT}, (when the IGBT is "on") and to block high voltages (when the IGBT is "off"). During the short transition time when the IGBT is switching, there is commonly a high dV_{CE}/dt voltage ramp rate across the IGBT. This results in a charging current $I_{CHARGE} = C_{D\text{-}DESAT} \times d_{VCE}/dt$, charging the blanking capacitor.

To minimize this current and avoid false DESAT triggering, fast switching diodes with low capacitance are recommended. As the diode capacitance builds a voltage divider with the blanking capacitor, large collector voltage transients appear at DESAT attenuated by the ratio of $1+ C_{BLANK} / C_{D\text{-}DESAT}$.

Table 9-1 lists a number of fast-recovery diodes suitable for the use as DESAT diodes.

Because the sum of the DESAT diode forward-voltage and the IGBT collector-emitter voltage make up the voltage at the DESAT-pin, $V_F + V_{CE} = V_{DESAT}$, the V_{CE} level, which triggers a fault condition, can be modified by adding multiple DESAT diodes in series: $V_{CE\text{-}FAULT(TH)} = 7.2\ V – n \times VF$ (where n is the number of DESAT diodes).

When using two diodes instead of one, diodes with half the required maximum reverse-voltage rating may be chosen.

Table 9-1. Recommended DESAT Diodes

PART NUMBER	MANUFACTURER	t_{rr} (ns)	$V_{RRM-max}$ (V)	PACKAGE
STTH112	STM	75	1200	SMA, SMB, DO-41
MUR100E	Motorola	75	1000	59-04 (axial leaded)
MURS160T3	Motorola	75	600	Case 403A (SMD)
UF4007	General Semi.	75	1000	DO-204AL (axial leaded)
BYM26E	Philips	75	1000	SOD64 (axial leaded)
BYV26E	Philips	75	1000	SOD57 (axial leaded)
BYV99	Philips	75	600	SOD87 (axial leaded)

9.2.2.10 Determining the Maximum Available, Dynamic Output Power, P_{OD-max}

The ISO5500 total power consumption of P_D = 592 mW consists of the total input power, P_{ID}, the total output power, P_{OD}, and the output power under load, P_{OL}:

$$P_D = P_{ID} + P_{OD} + P_{OL} \quad (2)$$

With:

$$P_{ID} = V_{CC1-max} \times I_{CC1-max} = 5.5\ V \times 8.5\ mA = 47\ mW \quad (3)$$

and:

$$P_{OD} = (V_{CC2} - V_{EE-P}) \times I_{CC2-q} = 30\ V \times 14\ mA = 420\ mW \quad (4)$$

then:

$$P_{OL} = P_D - P_{ID} - P_{OD} = 592\ mW - 47\ mW - 420\ mW = 125\ mW \quad (5)$$

In comparison to P_{OL}, the actual dynamic output power under worst case condition, P_{OL-WC}, depends on a variety of parameters:

$$P_{OL-WC} = 0.5 \times f_{INP} \times Q_G \times (V_{CC2} - V_{EE-P}) \times \left(\frac{r_{on-max}}{r_{on-max} + R_G} + \frac{r_{off-max}}{r_{off-max} + R_G} \right) \quad (6)$$

where

- f_{INP} = signal frequency at the control input $V_{IN(\pm)}$
- Q_G = power device gate charge
- V_{CC2} = positive output supply with respect to V_E
- V_{EE-P} = negative output supply with respect to V_E
- r_{on-max} = worst case output resistance in the on-state: 4Ω
- $r_{off-max}$ = worst case output resistance in the off-state: 2.5Ω
- R_G = gate resistor

Once RG is determined, Equation 6 is to be used to verify whether $P_{OL-WC} < P_{OL}$. Figure 9-9 shows a simplified output stage model for calculating P_{OL-WC}.

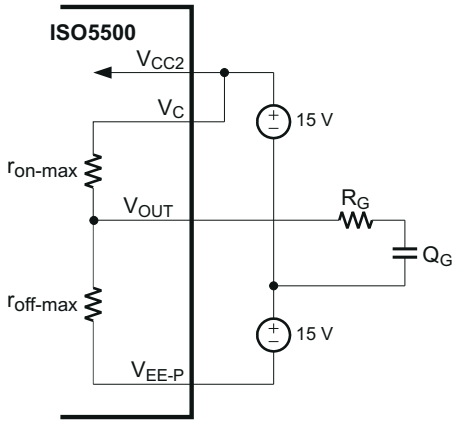


Figure 9-9. Simplified Output Model for Calculating P_{OL-WC}

9.2.2.11 Determining Gate Resistor, R_G

The value of the gate resistor determines the peak charge and discharge currents, I_{ON-PK} and I_{OFF-PK}. Due to the transient nature of these currents, their peak values only occur during the on-to-off and off-to-on transitions of the gate voltage. In order to calculate R_G for the maximum peak current, r_{on} and r_{off} must be assumed zero. The resulting charge and discharge models are shown in Figure 9-10.

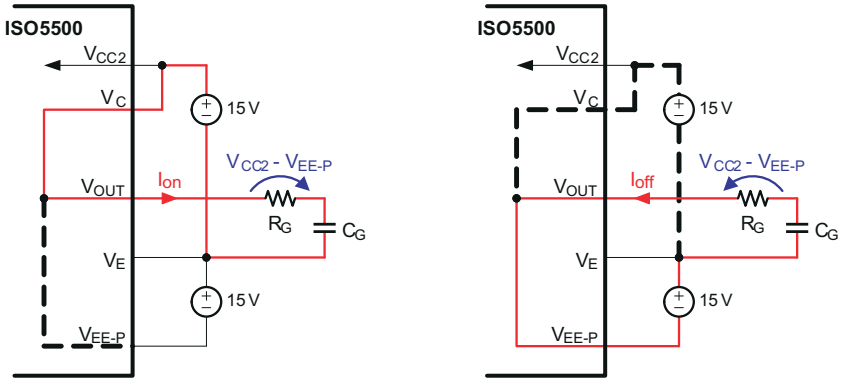


Figure 9-10. Simplified Gate Charge and Discharge Model

9.2.2.11.1 Off-to-On Transition

In the off-state, the upper plate of the gate capacitance, C_G, assumes a steady-state potential of $-V_{EE-P}$ with respect to V_E. When turning on the power device, V_{CC2} is applied to V_{OUT} and the voltage drop across R_G results in a peak charge current of $I_{ON-PK} = (V_{CC2} - V_{EE-P})/R_G$. Solving for R_G then provides the necessary resistor value for a desired on-current via:

$$R_G = \frac{V_{CC2} - V_{EE-P}}{I_{ON-PK}} \quad (7)$$

9.2.2.11.2 On-to-Off Transition

When turning the power device off, the current and voltage relations are reversed but the equation for calculating R_G remains the same.

Once R_G has been calculated, it is necessary to check whether the resulting, worst-case power consumption, P_{OD-WC}, (derived in Equation 6) is below the calculated maximum, P_{OL} = 125 mW (calculated in Equation 5).

9.2.2.12 Example

The example below considers an IGBT drive with the following parameters:

I_{ON-PK} = 2 A, Q_G = 650 nC, f_{INP} = 20 kHz, V_{CC2} = 15V, V_{EE-P} = –5 V

Applying Equation 7, the value of the gate resistor is calculated with

$$R_G = \frac{15V - (-5V)}{2A} = 10\ \Omega \tag{8}$$

Then, calculating the worst-case output power consumption as a function of R_G, using Equation 6 yields

$$P_{OL-WC} = 0.5 \times 20\ kHz \times 650\ nC \times (15\ V - (-5V)) \times \left(\frac{4\ \Omega}{4\ \Omega + 10\Omega} + \frac{2.5\ \Omega}{2.5\ \Omega + 10\ \Omega} \right) = 63\ mW \tag{9}$$

Because P_{OL-WC} = 63 mW is well below the calculated maximum of P_{OL} = 125 mW, the resistor value of R_G = 10Ω is fully suitable for this application.

9.2.2.13 Determining Collector Resistor, R_C

Despite equal charge and discharge currents, many power devices possess longer turn-off propagation and fall times than turn-on propagation and rise times. In order to compensate for the difference in switching times, it might be necessary to significantly reduce the charge current, I_{ON-PK}, versus the discharge current, I_{OFF-PK}.

Reducing I_{ON-PK} is accomplished by inserting an external resistor, R_C, between the V_C- pin and the V_{CC2}- pin of the ISO5500.

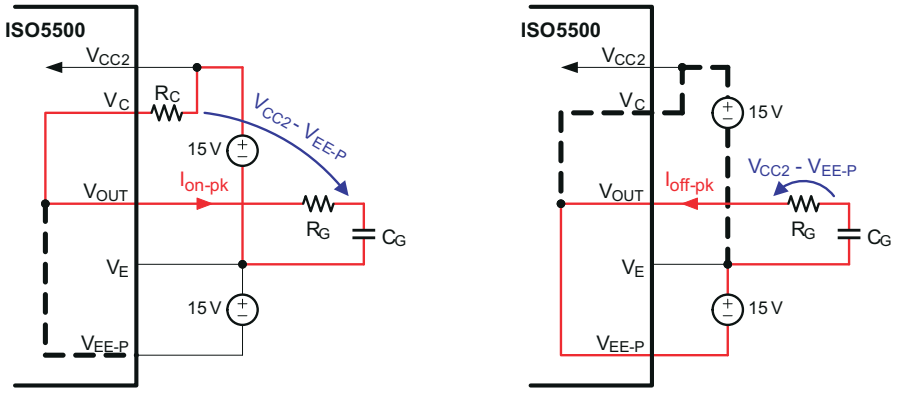


Figure 9-11. Reducing I_{ON-PK} by Inserting Resistor R_C

Figure 9-11 (right) shows that during the on-transition, the (V_{CC2} – V_{EE-P}) voltage drop occurs across the series resistance of R_C + R_G, thus reducing the peak charge current to: I_{ON-PK} = (V_{CC2} – V_{EE-P}) /(R_C + R_G). Solving for R_C provides:

$$R_C = \frac{V_{CC2} - V_{EE-P}}{I_{ON-PK}} - R_G \tag{10}$$

To stay below the maximum output power consumption, R_G must be calculated first via:

$$R_G = \left| \frac{V_{CC2} - V_{EE-P}}{I_{OFF-PK}} \right| \tag{11}$$

and the necessary comparison of P_{OL-WC} versus P_{OL} must be completed.

Once R_G is determined, calculate R_C for a desired on-current using Equation 10.

Another method is to insert Equation 11 into Equation 10 and arriving at:

$$R_C = R_G \times \left(\frac{I_{OFF\text{-}PK}}{I_{ON\text{-}PK}} - 1 \right) \tag{12}$$

9.2.2.13.1 Example

Reducing the peak charge current from the previous example to $I_{ON\text{-}PK}$ = 1.5 A, requires a R_C value of:

$$R_C = 10\ \Omega \times \left(\frac{2\ A}{1.5\ A} - 1 \right) = 3.33\ \Omega \tag{13}$$

9.2.2.14 Higher Output Current Using an External Current Buffer

To increase the IGBT gate drive current, a non-inverting current buffer (such as the npn/pnp buffer shown in Figure 9-12) may be used. Inverting types are not compatible with the desaturation fault protection circuitry and must be avoided. The MJD44H11/MJD45H11 pair is appropriate for currents up to 8 A, the D44VH10/ D45VH10 pair for up to 15 A maximum.

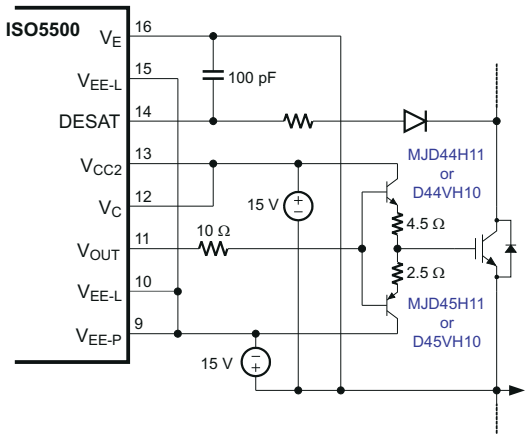


Figure 9-12. Current Buffer for Increased Drive Current

9.2.3 Application Curve

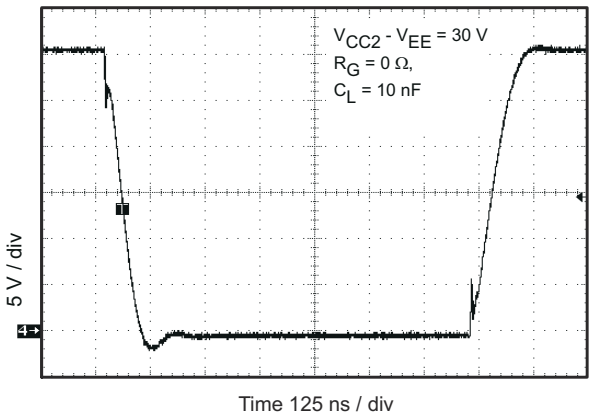


Figure 9-13. Output Waveform

10 Power Supply Recommendations

To provide the large transient currents necessary during a switching transition on the gate driver output, 0.1-µF bypass capacitors are recommended between input supply and ground (V_{CC1} and GND1), and between output supplies and ground (V_{CC2} and V_E, V_{CC2} and V_{EE-P} and V_{EE-P} and V_E). These capacitors are shown in Figure 9-2. These capacitors should be placed as close to the supply and ground pins as possible.

11 Layout

11.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 11-1). Layer stacking should be in the following order (top-to-bottom): high-current or sensitive signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-current or sensitive traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the gate driver and the microcontroller and power transistors. Gate driver control input, Gate driver output V_{OUT} and DESAT should be routed in the top layer.
- Placing a solid ground plane next to the sensitive signal layer provides an excellent low-inductance path for the return current flow. On the driver side, use VE as the ground plane.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in2. On the gate-driver V_{EE-P} and V_{CC2} can be used as power planes. They can share the same layer on the PCB as long as they are not connected together.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

For more detailed layout recommendations, including placement of capacitors, impact of vias, reference planes, routing etc. see Application Note SLLA284, *Digital Isolator Design Guide*.

11.2 PCB Material

Standard FR-4 epoxy-glass is recommended as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.3 Layout Example

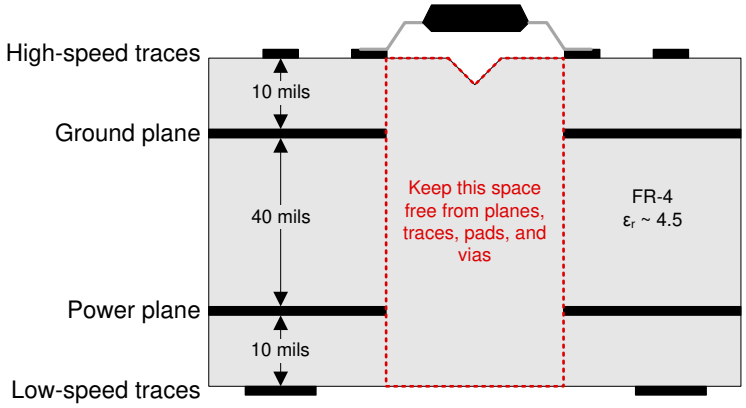


Figure 11-1. Recommended Layer Stack

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *ISO5500 Evaluation Module (EVM) User's Guide*, SLLU136
- *Digital Isolator Design Guide*, SLLA284

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO5500DW	LIFEBUY	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5500DW	
ISO5500DWR	LIFEBUY	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ISO5500DW	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

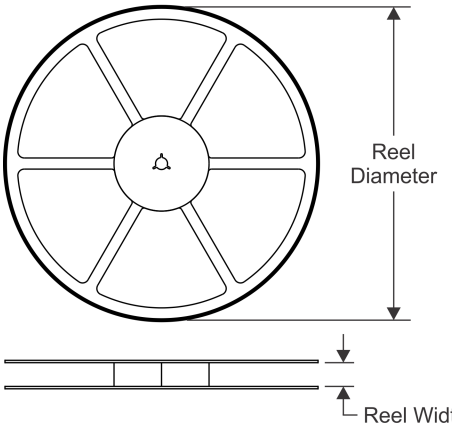
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

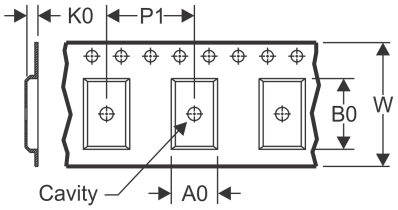
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

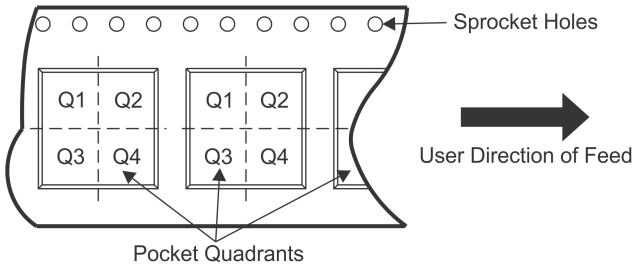


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

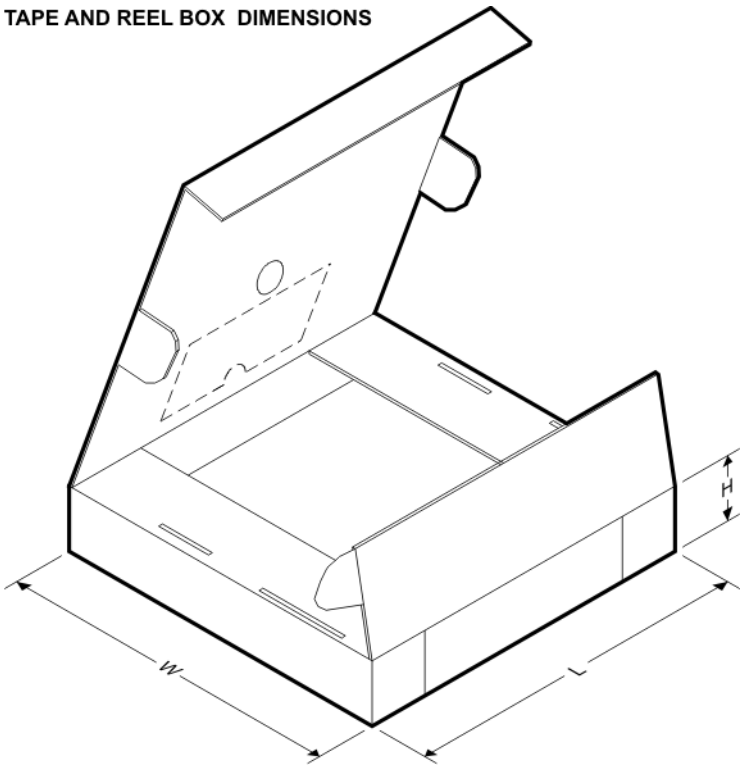
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO5500DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

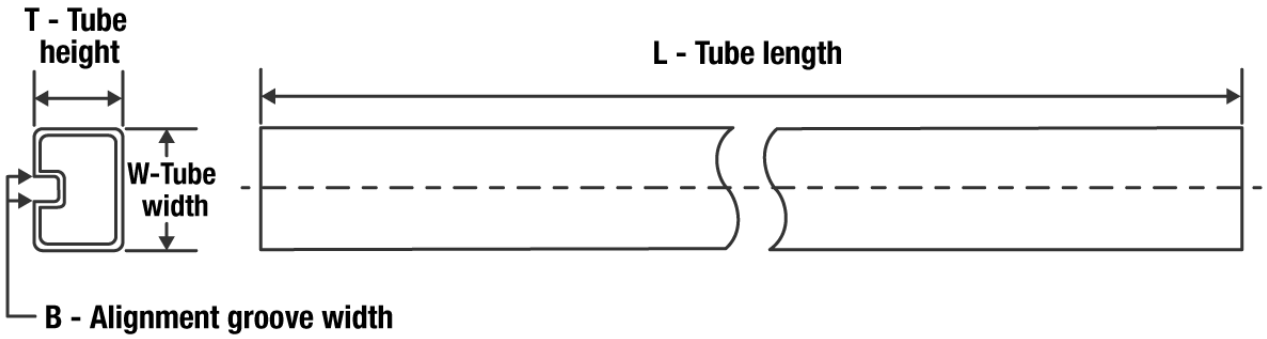
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO5500DWR	SOIC	DW	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ISO5500DW	DW	SOIC	16	40	506.98	12.7	4826	6.6

GENERIC PACKAGE VIEW

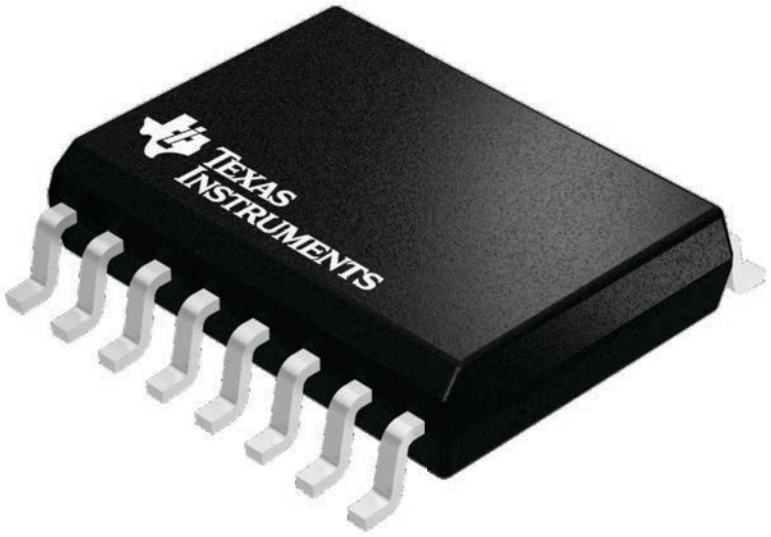
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

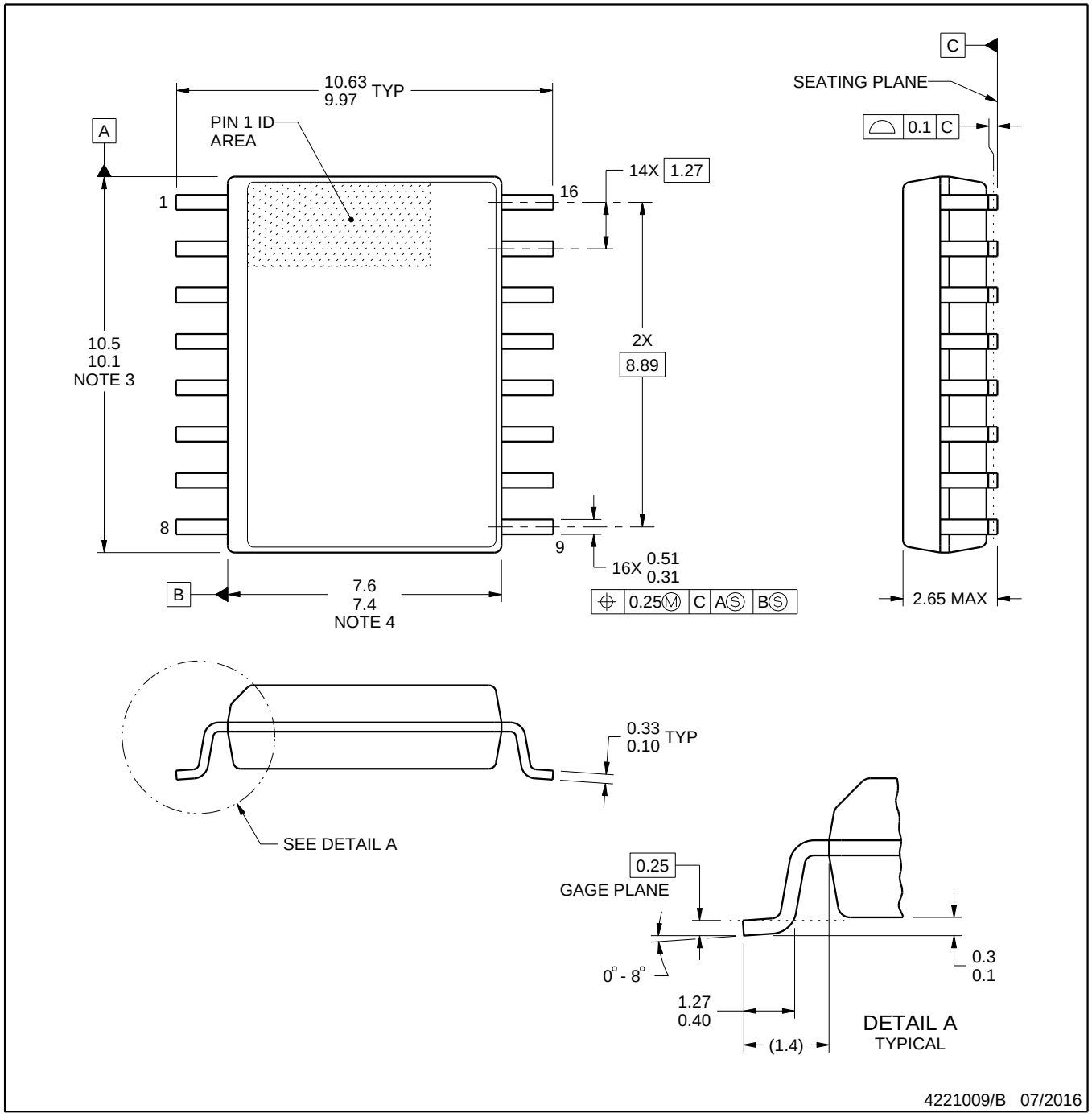
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



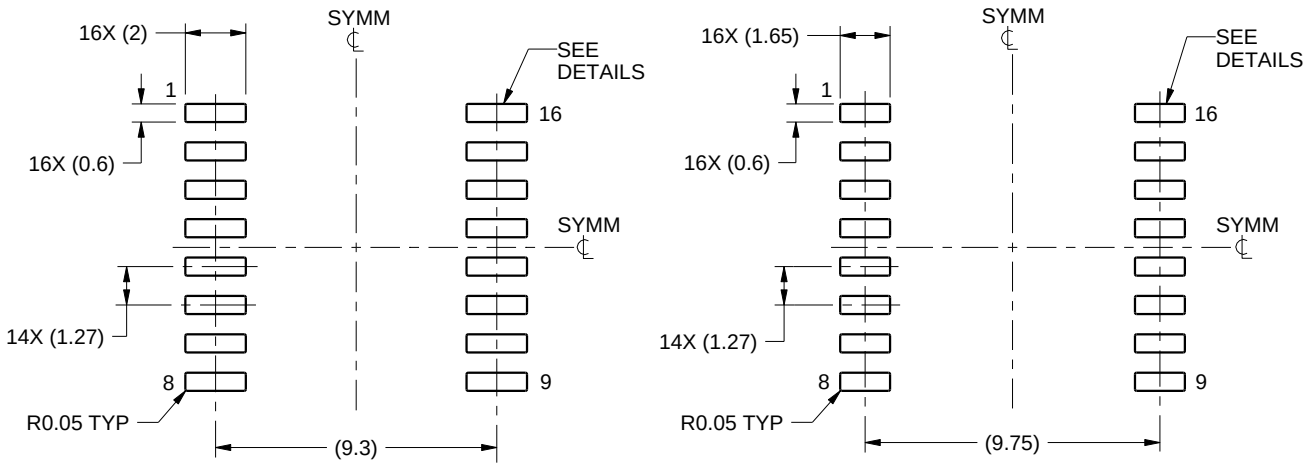
4224780/A

SOIC



NOTES:

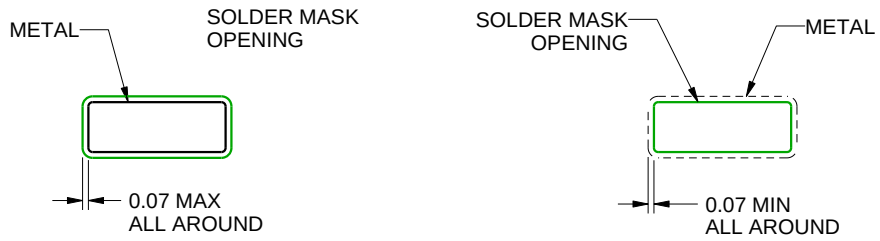
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

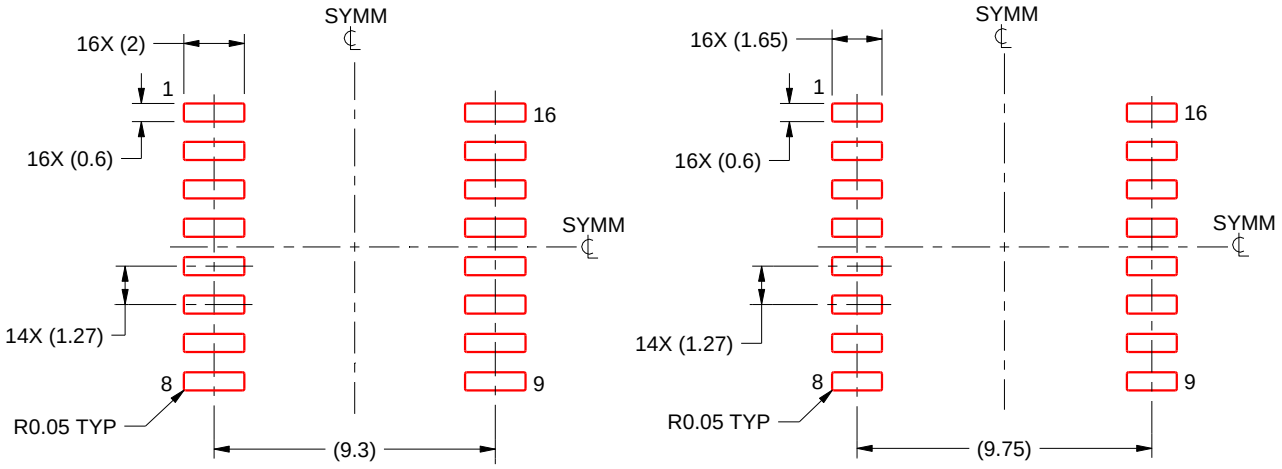
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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