MC2206310-002-C

Mellanox® MC2206310-002 Compatible TAA Compliant 40GBase-AOC QSFP+ Active Optical Cable (850nm, MMF, 2m)

Features

- Full duplex 4 channel 850nm parallel active optical cable
- Transmission data rate up to 10.3Gbit/s per channel
- SFF-8436 QSFP+ compliant
- Hot pluggable electrical interface
- Up to 100m Reach over multi-mode fiber
- Differential AC-coupled high-speed data interface
- 4 channels 850nm VCSEL array
- 4 channels PIN photo detector array
- Low power consumption <1.5W
- Operating case temperature 0°C to +70°C
- 3.3V power supply voltage
- RoHS 6 compliant

Applications

- InfiniBand transmission at 4ch SDR, DDR and QDR
- 40GBASE-SR4 Ethernet
- Data Centers

Product Description

This is a Mellanox® MC2206310-002 compatible 40GBase-AOC QSFP+ to QSFP+ active optical cable that operates over multi-mode fiber with a maximum reach of 2.0m (6.6ft). At a wavelength of 850nm, it has been programmed, uniquely serialized, and data-traffic and application tested to ensure it is 100% compliant and functional. This active optical cable is TAA (Trade Agreements Act) compliant, and is built to comply with MSA (Multi-Source Agreement) standards. We stand behind the quality of our products and proudly offer a limited lifetime warranty.

ProLabs' active optical cables are RoHS compliant and lead-free.

TAA refers to the Trade Agreements Act (19 U.S.C. & 2501-2581), which is intended to foster fair and open international trade. TAA requires that the U.S. Government may acquire only "U.S. – made or designated country end products.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	-0.5		4.0	V
Input Voltage	VIN	-0.3		Vcc+0.3	V
Storage Temperature	Tstg	-20		85	°C
Case Operating Temperature	Tc	0		70	°C
Humidity (Non-Condensing)	RH	5		95	%

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case Temperature	Tc	-5		70	°C
Data Rate Per Lane	DR	2.5		10.3	Gbps
Humidity	RH	5		85	%
Power Dissipation	P_{DISS}			1.5	W
Fiber Band Radius		3			cm

Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Differential Input Impedance	ZIN	90	100	110	Ω	2
Differential Output Impedance	ZOUT	90	100	110	Ω	3
Differential Input Voltage Amplitude	ΔVIN	300		1100	mVp-p	
Differential Output Voltage Amplitude	ΔVOUT	500		800	mVp-p	
Skew				300	ps	
Bit Error Rate	BR			E^{-12}		
Input Logic Level - High	VIH	2.0		Vcc	V	
Input Logic Level - Low	VIL	0		0.8	V	
Output Logic Level - High	VOH	Vcc-0.5		Vcc	V	
Output Logic Level - Low	VOL	0		0.4	V	

Notes:

1. BER=10^{-12} and PRBS 2^{31}-1 @10.3125Gbps.
2. Differential input voltage amplitude is measured between Txn+ and Txn-.
3. Differential output voltage amplitude is measured between Rxn+ and Rxn-.

Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
Transmitter						
Center Wavelength	λC	840	850	860	nm	
RMS Spectral Width	Δλ			0.65	nm	
Average Launch Power Per Channel	POUT	-7.5		-2.5	dBm	
Difference in Launch Power Between Any Two Lanes (OMA)					dB	
Extinction Ratio	ER	3			dB	
Peak Power Per Lane				4	dBm	
Transmitter and Dispersion Penalty (TDP) Per Lane	TDP			3.5	dB	
Average Launch Power of Off Transmitter Per Lane				-30	dB	
Transmitter Eye Mask Definition: (X1, X2, X3, Y1, Y2, Y3)		(0.23, 0.34, 0.43, 0.27, 0.33, 0.4)				Hit Ratio = $5x10^{-5}$
Receiver						
Center Wavelength	λC	840	850	860	nm	
Stressed Receiver Sensitivity in OMA Per Lane				-5.4		1
Maximum Average Power at Receiver Input Per Lane				2.4		
Receiver Reflectance				-12		
Peak Power Per Lane				4		
LOS Assert		-30				
LOS De-Assert – OMA				7.5		
LOS Hysteresis		0.5				

Note:

1. Measured with conformance test signal at TP3 for BER = $10E^{-12}$.

Pin Descriptions

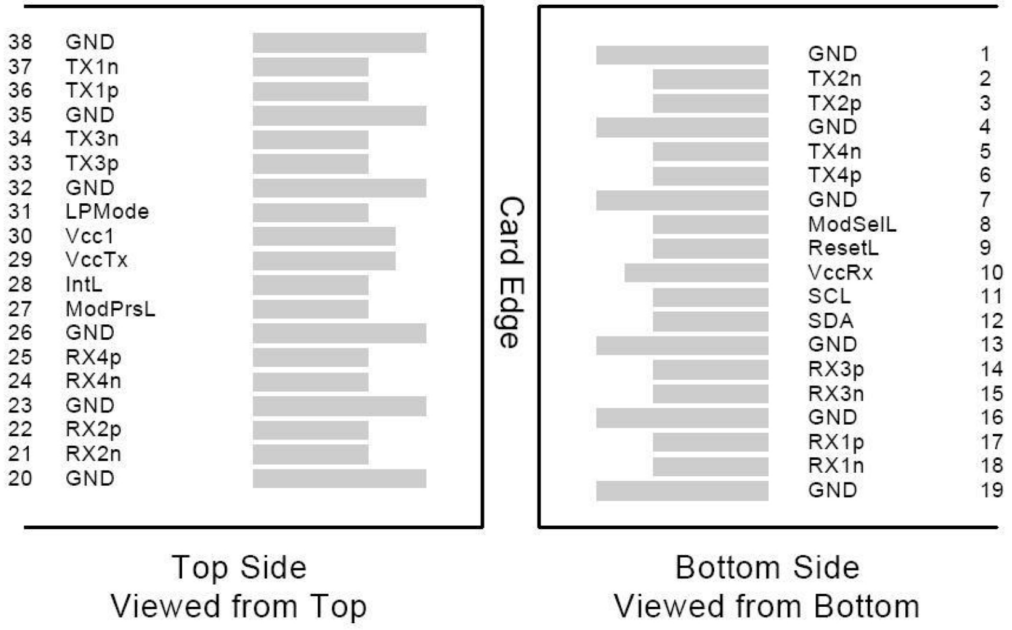
Pin	Logic	Symbol	Name/Description	Note
1		GND	Module Ground.	1
2	CML-I	Tx2-	Transmitter Inverted Data Input.	
3	CML-I	Tx2+	Transmitter Non-Inverted Data Input.	
4		GND	Module Ground.	1
5	CML-I	Tx4-	Transmitter Inverted Data Input.	
6	CML-I	Tx4+	Transmitter Non-Inverted Data Input.	
7		GND	Module Ground.	1
8	LVTTL-I	ModSelL	Module Select.	2
9	LVTTL-I	ResetL	Module Reset.	2
10		VccRx	+3.3V Receiver Power Supply.	
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock.	2
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data.	2
13		GND	Module Ground.	1
14	CML-O	Rx3+	Receiver Non-Inverted Data Output.	
15	CML-O	Rx3-	Receiver Inverted Data Output.	
16		GND	Module Ground.	1
17	CML-O	Rx1+	Receiver Non-Inverted Data Output.	
18	CML-O	Rx1-	Receiver Inverted Data Output.	
19		GND	Module Ground.	1
20		GND	Module Ground.	1
21	CML-O	Rx2-	Receiver Inverted Data Output.	
22	CML-O	Rx2+	Receiver Non-Inverted Data Output.	
23		GND	Module Ground.	1
24	CML-O	Rx4-	Receiver Inverted Data Output.	
25	CML-O	Rx4+	Receiver Non-Inverted Data Output.	
26		GND	Module Ground.	1
27	LVTTL-O	ModPrsL	Module Present. Internally pulled down to the GND.	
28	LVTTL-O	IntL	Interrupt Output. Should be pulled up on the host board.	2
29		VccTx	+3.3V Transmitter Power Supply.	
30		Vcc1	+3.3V Power Supply.	
31	LVTTL-I	LPMode	Low-Power Mode.	2
32		GND	Module Ground.	1
33	CML-I	Tx3+	Transmitter Non-Inverted Data Input.	
34	CML-I	Tx3-	Transmitter Inverted Data Input.	
35		GND	Module Ground.	1

36	CML-I	Tx1+	Transmitter Non-Inverted Data Input.	
37	CML-I	Tx1-	Transmitter Inverted Data Input.	

Notes:

1. GND is the symbol for signal and supply (power). Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1, and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. VccRx, Vcc1, and VccTx may be internally connected within the QSFP+. The connector pins are each rated for a maximum current of 500mA.

Pin Assignment and Pin Description



ModSelL Pin

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus. When the ModSelL is “high," the module will not respond to any 2-wire interface communication from the host. ModSelL has an internal pull-up in the module.

ResetL Pin

Reset. LPMode_Reset has an internal pull-up in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module

indicates a completion of the reset interrupt. The module indicates this by posting an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion), the module will post this completion of reset interrupt without requiring a reset.

LPMode Pin

Operate in the low-power mode (less than 1.5 W power consumption). This pin, when active on "high," will decrease power consumption to less than 1W.

ModPrsL Pin

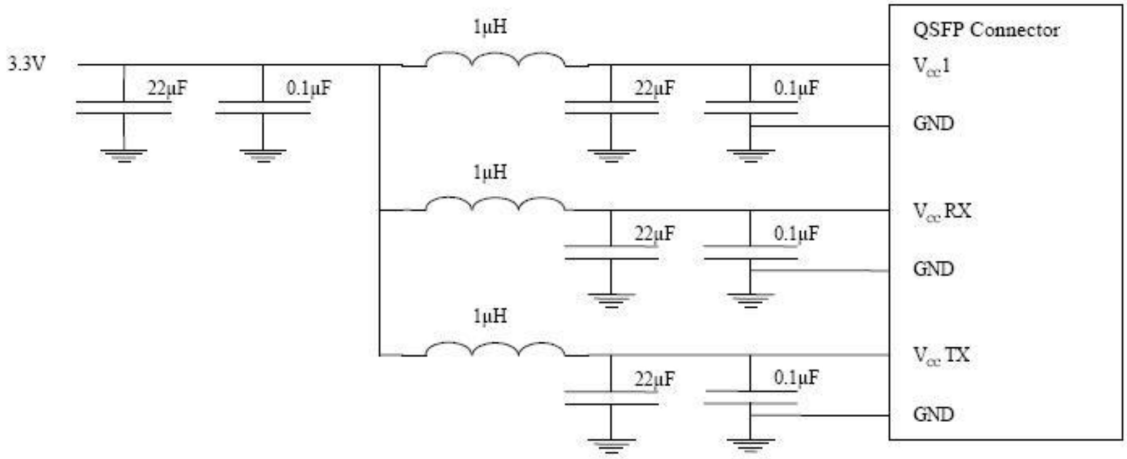
ModPrsL is pulled up to the Vcc on the host board and grounded in the module. The ModPrsL is asserted “low” when the module is inserted and de-asserted “high” when the module is physically absent from the host connector.

IntL Pin

IntL is an output pin. When “low,” it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt by using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled up to the Vcc on the host board.

Power Supply Filtering

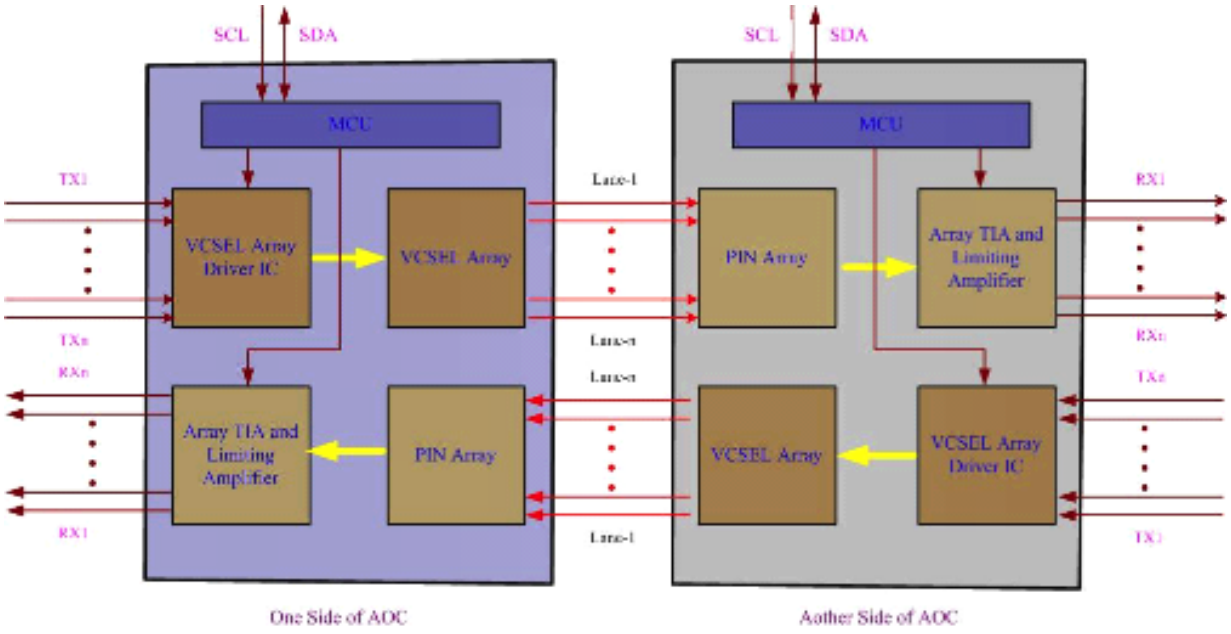
The host board should use the power supply filtering shown below:



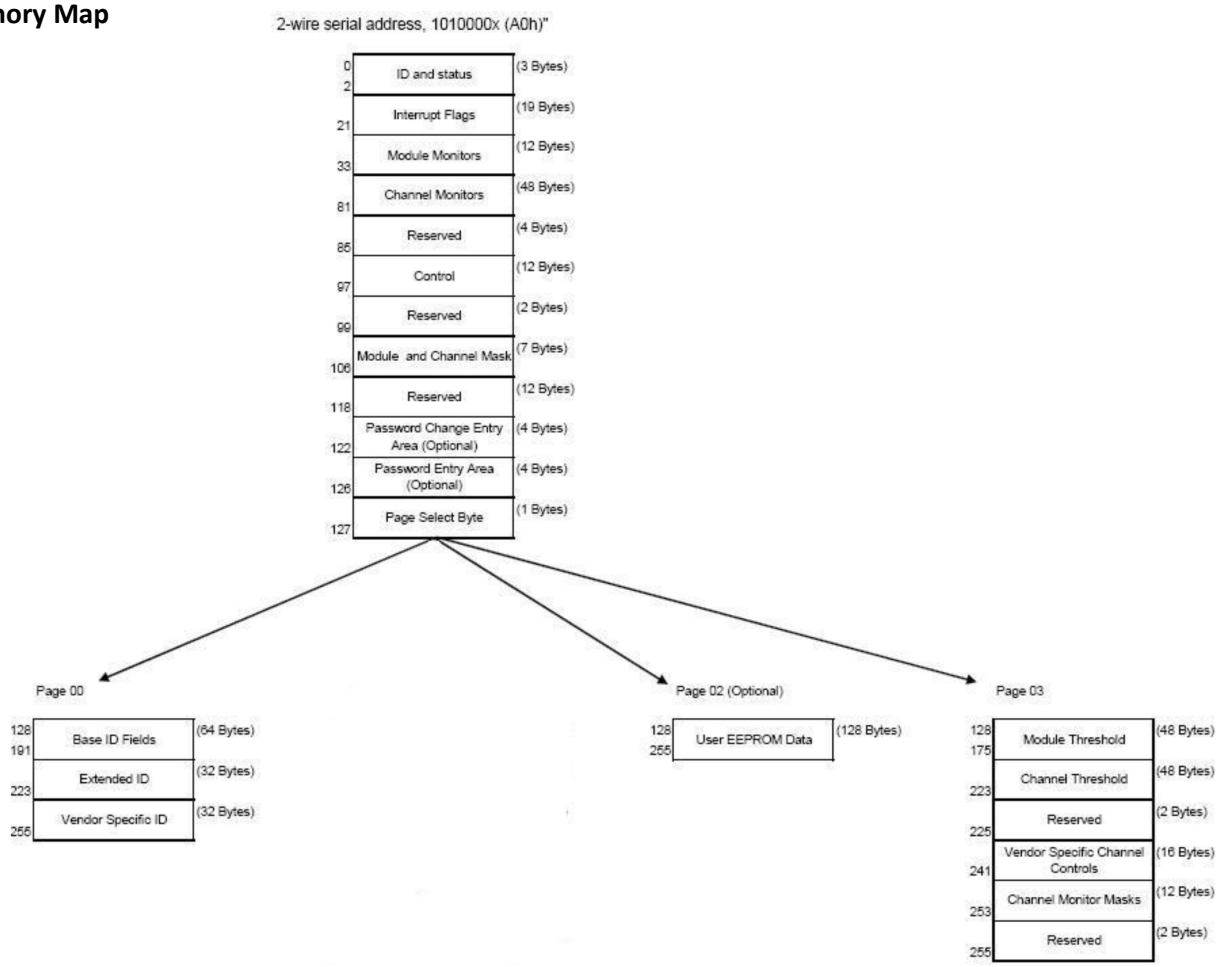
DIAGNOSTIC MONITORING INTERFACE

The digital diagnostics monitoring function is available on all QSFP AOCs. A 2-wire serial interface provides users contact with the module. The structure of the memory is shown below. The memory space is arranged into a lower, single-page address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, such as Interrupt Flags and Monitors. Less time critical time entries, such as serial ID information and threshold settings, are available with the Page Select function. The interface address used is A0xh and is mainly used for time critical data like interrupt handling in order to enable a one-time-read for all data related to an interrupt situation. After an Interrupt, IntL, has been asserted, the host can read out the flag field to determine the affected channel and type of flag.

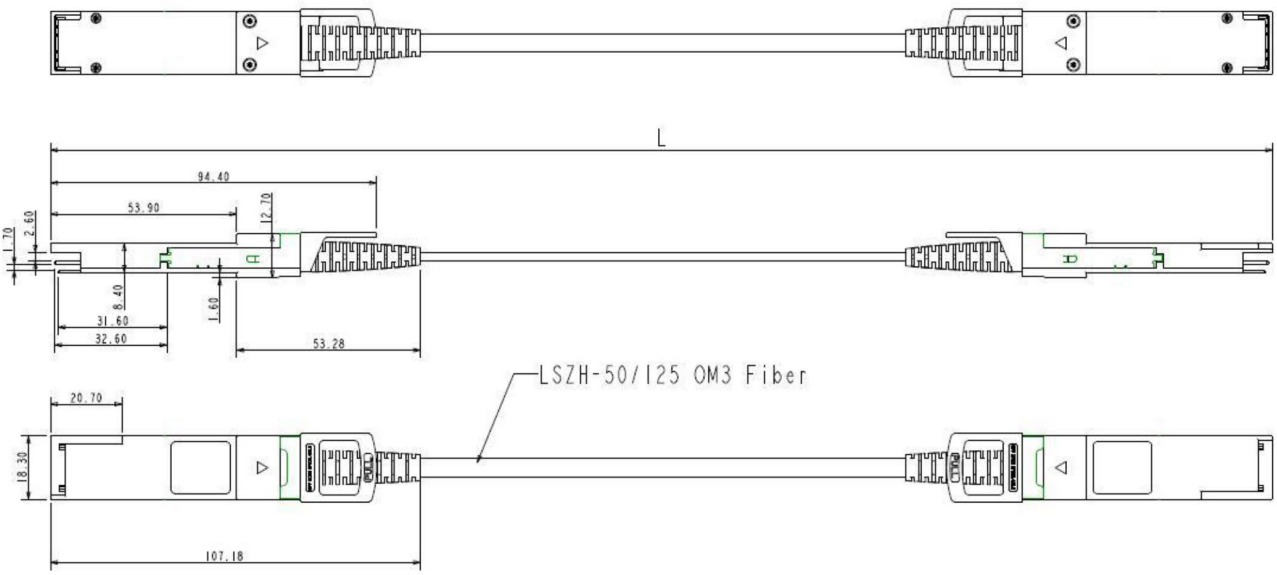
Module Block Diagram



Memory Map



Mechanical Specifications



About ProLabs

Our experience comes as standard; for over 15 years ProLabs has delivered optical connectivity solutions that give our customers freedom and choice through our ability to provide seamless interoperability. At the heart of our company is the ability to provide state-of-the-art optical transport and connectivity solutions that are compatible with over 90 optical switching and transport platforms.

Complete Portfolio of Network Solutions

ProLabs is focused on innovations in optical transport and connectivity. The combination of our knowledge of optics and networking equipment enables ProLabs to be your single source for optical transport and connectivity solutions from 100Mb to 400G while providing innovative solutions that increase network efficiency. We provide the optical connectivity expertise that is compatible with and enhances your switching and transport equipment.

Trusted Partner

Customer service is our number one value. ProLabs has invested in people, labs and manufacturing capacity to ensure that you get immediate answers to your questions and compatible product when needed. With Engineering and Manufacturing offices in the U.K. and U.S. augmented by field offices throughout the U.S., U.K. and Asia, ProLabs is able to be our customers best advocate 24 hours a day.

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