LM2904H, LM2904AH

Datasheet

Low-power, dual operational amplifier

DFN8 2 x 2 wettable flanks

TSSOP8

Maturity status link
LM2904H
LM2904AH

Related products	
LM2904WH	For enhanced ESD performances

Features

- AEC-Q100 qualified
- Frequency compensation implemented internally
- Large DC voltage gain: 100 dB
- Wide bandwidth (unity gain): 1.1 MHz (temperature compensated)
- Very low supply current/amplifier, essentially independent of supply voltage
- Low input bias current: 20 nA (temperature compensated)
- Low input offset current: 2 nA
- Input common-mode voltage range includes negative rail
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0 V to [(V_{CC+}) -1.5 V]

Description

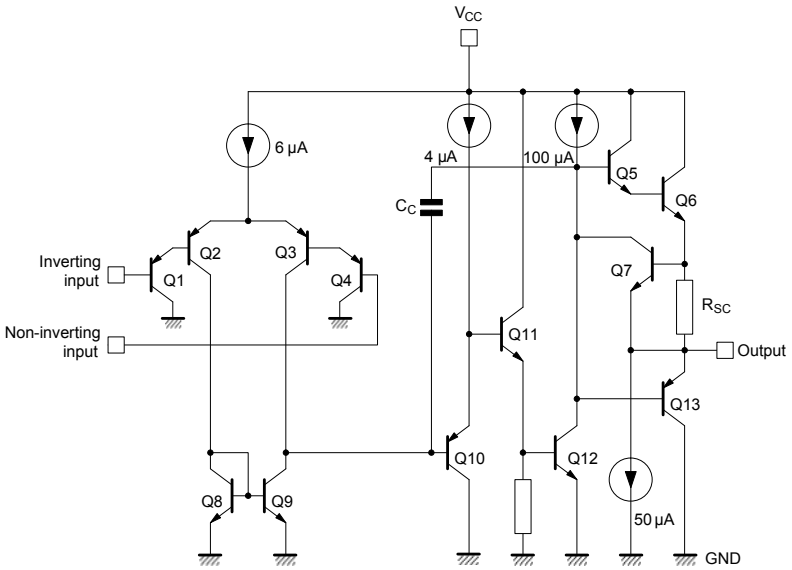
This circuit consists of two independent, high gain operational amplifiers (op amps) that have frequency compensation implemented internally. They are designed specifically for automotive and industrial control systems. The circuit operates from a single power supply over a wide range of voltages. The low power supply drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which can now be more easily implemented in single power supply systems. For example, these circuits can be directly supplied from the standard 5 V which is used in logic systems and easily provides the required interface electronics without requiring any additional power supply.

In the linear mode, the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from a single power supply.

1 Schematic diagram

Figure 1. **Schematic diagram (1/2 LM2904H/AH)**



2 Package pin connections

Figure 2. **TSSOP8 package pin connections (top view)**

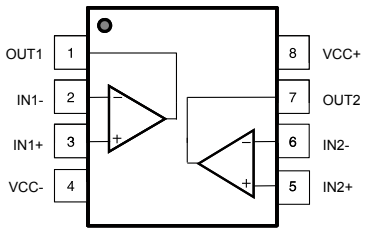
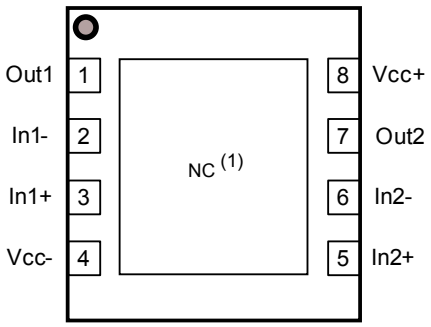


Figure 3. **DFN8 2x2 package pin connections (top view)**



(1) The exposed pad of the DFN8 2x2 can be connected to (VCC-) or left floating.

3 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	±16 or 32	V
V_{id}	Differential input voltage (2)	±32	
V_{in}	Input voltage	-0.3 to 32	
	Output short-circuit duration (3)	Infinite	s
I_{in}	Input current: V_{in} driven negative (4)	5 mA in DC or 50 mA in AC (duty cycle = 10 %, T = 1 s)	mA
	Input current: V_{in} driven positive above AMR value (5)	0.4	
T_{stg}	Storage temperature range	-65 to 150	°C
T_j	Maximum junction temperature	160	
R_{thja}	Thermal resistance junction to ambient (6) TSSOP8 DFN8 2x2 wettable flank	 120 57	°C/W
R_{thjc}	Thermal resistance junction to case (6) TSSOP8 DFN8 2x2 wettable flank	 37 26	
ESD	HBM: human body model (7)	300	V
	MM: machine model (8)	200	
	CDM: charged device model (9)	1.5	kV

1. *All voltage values, except differential voltage are with respect to network ground terminal.*
2. *Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.*
3. *Short-circuits from the output to V_{CC} can cause excessive heating if (V_{cc+}) > 15 V. The maximum output current is approximately 40 mA, independent of the magnitude of V_{CC}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.*
4. *This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward-biased and thereby acting as input diode clamp. In addition to this diode action, there is NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V_{CC} voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.*
5. *The junction base/substrate of the input PNP transistor polarized in reverse must be protected by a resistor in series with the inputs to limit the input current to 400 µA max (R = (Vin-32 V)/400 µA).*
6. *Short-circuits can cause excessive heating and destructive dissipation. Values are typical.*
7. *Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.*
8. *Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.*
9. *Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.*

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	3 to 30	V
V_{icm}	Common-mode input voltage range	0 to (V_{CC+}) - 1.5	
T_{oper}	Operating free-air temperature range	-40 to 150	°C

4 Electrical characteristics

Table 3. V_{CC+} = 5 V, V_{CC-} = ground, V_O = 1.4 V, T_{amb} = 25 °C (unless otherwise specified), T_{min} = -40 °C, and T_{max} = 150 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input offset voltage, T_{amb} = 25 °C, LM2904AH (1)		1	2	mV
	Input offset voltage, $T_{min} \le T_{amb} \le T_{max}$ LM2904AH (1)			6	
	Input offset voltage, T_{amb} = 25 °C, LM2904H (1)		2	7	
	Input offset voltage, $T_{min} \le T_{amb} \le T_{max}$ LM2904H (1)			9	
$\Delta V_{io}/\Delta T$	Input offset voltage drift		7	40	µV/°C
I_{io}	Input offset current, T_{amb} = 25 °C		2	30	nA
	Input offset current, $T_{min} \le T_{amb} \le T_{max}$			40	
$\Delta I_{io}/\Delta T$	Input offset current drift		10	300	pA/°C
I_{ib}	Input bias current, T_{amb} = 25 °C (2)		20	150	nA
	Input bias current, $T_{min} \le T_{amb} \le T_{max}$ (2)			200	
A_{vd}	Large signal voltage gain, V_{CC+} = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V, T_{amb} = 25 °C	50	100		V/mV
	Large signal voltage gain, V_{CC+} = 15 V, R_L = 2 kΩ, V_o = 1.4 V to 11.4 V, $T_{min} \le T_{amb} \le T_{max}$	25			
SVR	Supply voltage rejection ratio ($R_S \le$ 10 kΩ), T_{amb} = 25 °C	65	100		dB
	Supply voltage rejection ratio ($R_S \le$ 10 kΩ),$T_{min} \le T_{amb} \le T_{max}$	65			
I_{CC}	Supply current, all amp, no load, T_{amb} = 25 °C, V_{CC+} = 5 V		0.7	1.2	mA
	Supply current, all amp, no load, $T_{min} \le T_{amb} \le T_{max}$, V_{CC+} = 30 V			2	
V_{icm}	Input common mode voltage range (V_{CC+} = 30 V), T_{amb} = 25 °C (3)	0		(V_{CC+}) - 1.5	V
	Input common mode voltage range (V_{CC+} = 30 V), $T_{min} \le T_{amb} \le T_{max}$	0		(V_{CC+}) - 2	
CMR	Common-mode rejection ratio (R_S = 10 kΩ), T_{amb} = 25 °C	70	85		dB
	Common-mode rejection ratio (R_S = 10 kΩ), $T_{min} = T_{amb} = T_{max}$	60			
I_{source}	Output short-circuit current, V_{CC+} = 15 V, V_o = 2 V, V_{id} = 1 V	20	40	60	mA
I_{sink}	Output sink current, V_O = 2 V, V_{CC+} = 5 V	10	20		
	Output sink current, V_O = 0.2 V, V_{CC+} = 15 V	12	50		µA
V_{OH}	High level output voltage (V_{CC+} = 30 V), T_{amb} = 25 °C, R_L = 2 kΩ	26			V
	High level output voltage (V_{CC+} = 30 V), $T_{min} \le T_{amb} \le T_{max}$	26	27		
	High level output voltage (V_{CC+} = 30 V), T_{amb} = 25 °C, R_L = 10 kΩ	27			
	High level output voltage (V_{CC+} = 30 V), $T_{min} \le T_{amb} \le T_{max}$	27	28		
V_{OL}	Low level output voltage (R_L = 10 kΩ), T_{amb} = 25 °C		5	20	mV
	Low level output voltage (R_L = 10 kΩ), $T_{min} \le T_{amb} \le T_{max}$			20	
SR	Slew rate, V_{CC+} = 15 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_L =100 pF, unity gain, T_{amb} = 25 °C	0.3	0.6		V/µs
	Slew rate, V_{CC+} = 15 V, V_{in} = 0.5 to 3 V, R_L = 2 kΩ, C_L =100 pF, unity gain, $T_{min} \le T_{amb} \le T_{max}$	0.2			
GBP	Gain bandwidth product, f = 100 kHz, V_{CC+} = 30 V, V_{in} = 10 mV, R_L = 2 kΩ, C_L = 100 pF	0.7	1.1		MHz
THD	Total harmonic distortion, f = 1 kHz, A_V = 20 dB, R_L = 2 kΩ, V_o = 2 V_{pp}, C_L = 100 pF, V_{CC+} = 30 V		0.02		%
e_n	Equivalent input noise voltage, f = 1 kHz, R_S = 100 Ω, V_{CC+} = 30 V		55		nV/√ Hz

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{O1}/V_{O2}	Channel separation, 1 kHz ≤ f ≤ 20 kHz (4)		120		dB

1. *V_O = 1.4 V, R_S = 0 Ω, 5 V < V_{CC+} < 30 V, 0 V < V_{ic} < (V_{CC+}) - 1.5 V.*
2. *The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output, so there is no change in the loading charge on the input lines.*
3. *The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is (V_{CC+}) – 1.5 V, but either or both inputs can go to 32 V without damage.*
4. *Due to the proximity of external components, ensure that the stray capacitance does not cause coupling between these external parts. This can typically be detected at higher frequencies because this type of capacitance increases.*

5 Electrical characteristic curves

Figure 4. Open-loop frequency response

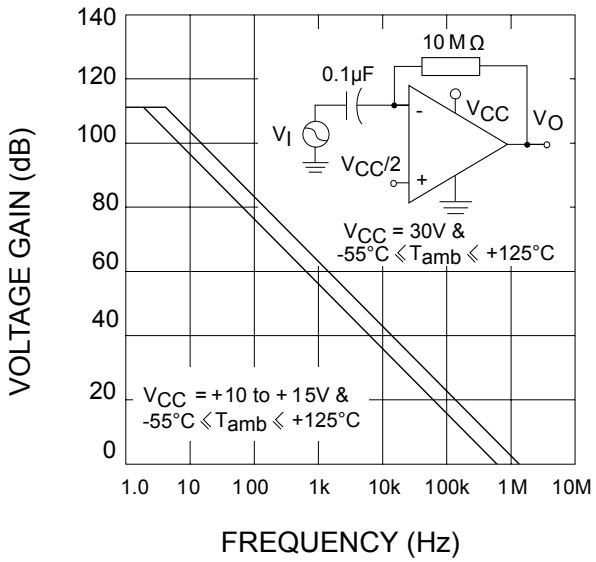


Figure 5. Large signal frequency response

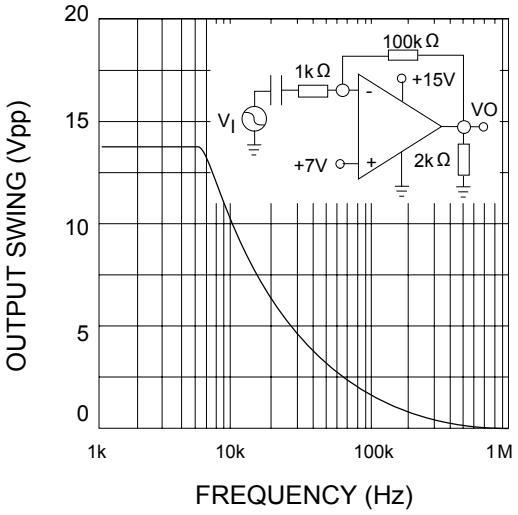


Figure 6. Voltage follower large signal response

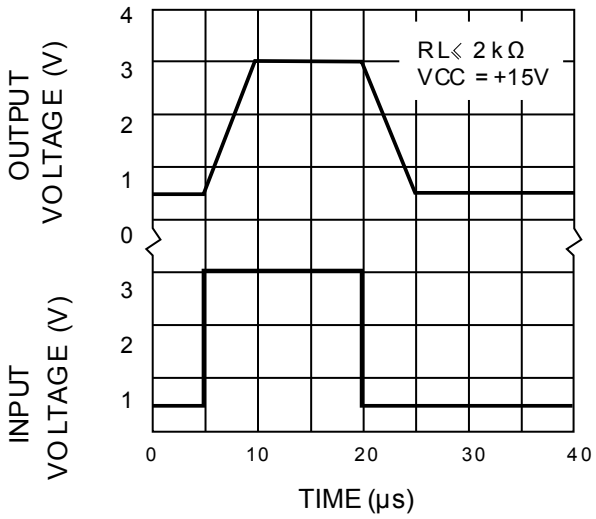


Figure 7. Current sinking output characteristics

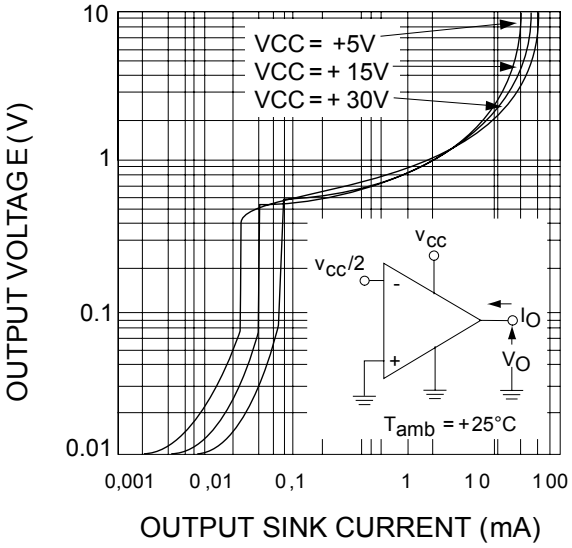


Figure 8. Voltage follower small signal response

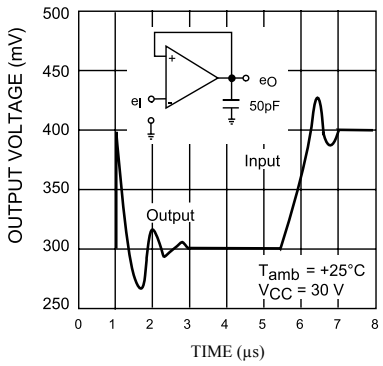


Figure 9. Current sourcing output characteristics

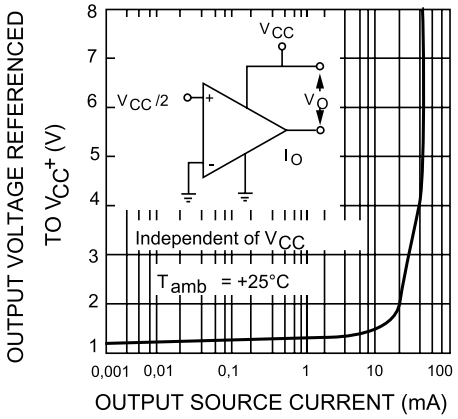


Figure 10. Input current versus temperature

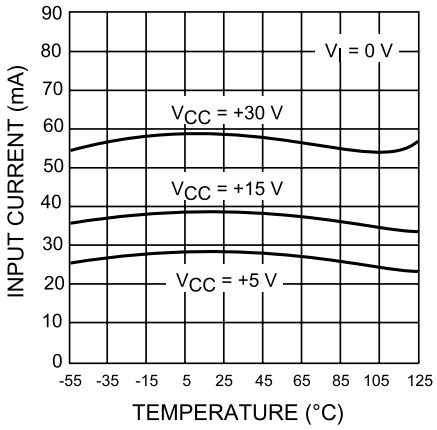


Figure 11. Current limiting

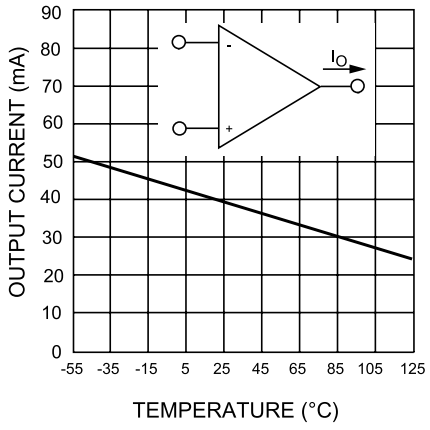


Figure 12. Input voltage range

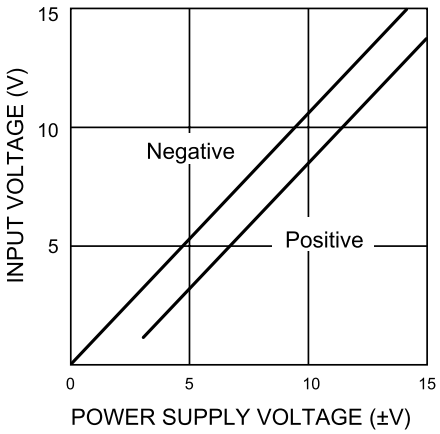


Figure 13. Supply current

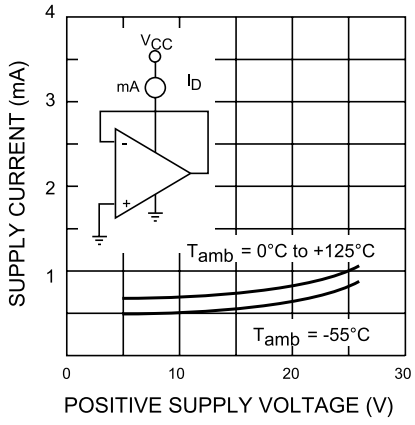


Figure 14. Voltage gain

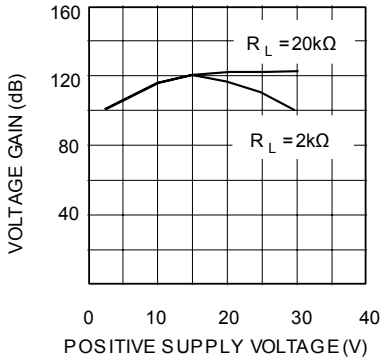


Figure 15. Input current versus supply voltage

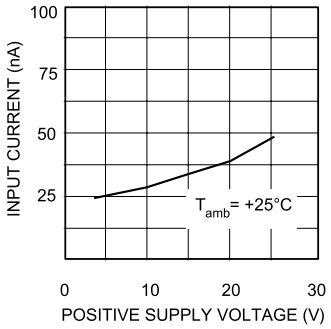


Figure 16. Gain bandwidth product

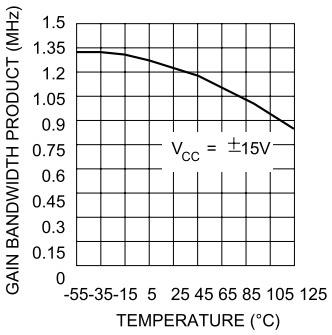


Figure 17. Power supply rejection ratio

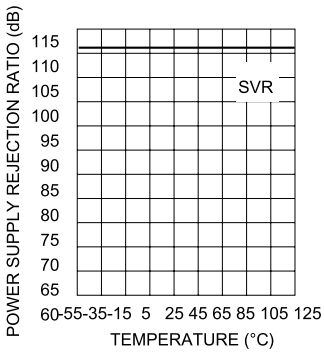


Figure 18. Common-mode rejection ratio

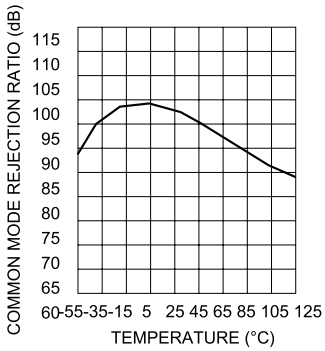
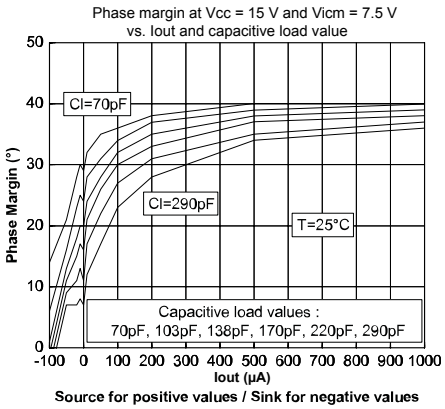


Figure 19. Phase margin vs. capacitive load



6 Typical single-supply applications

Figure 20. AC coupled inverting amplifier

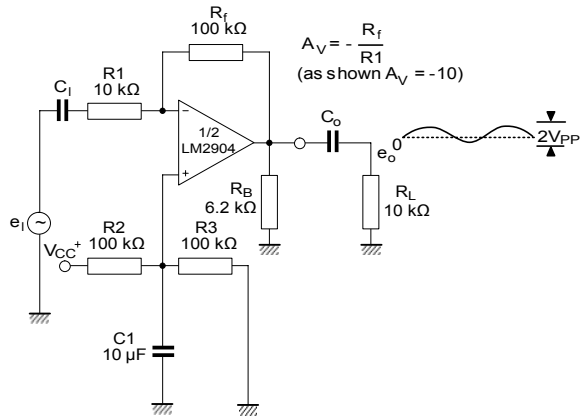


Figure 21. AC coupled non-inverting amplifier

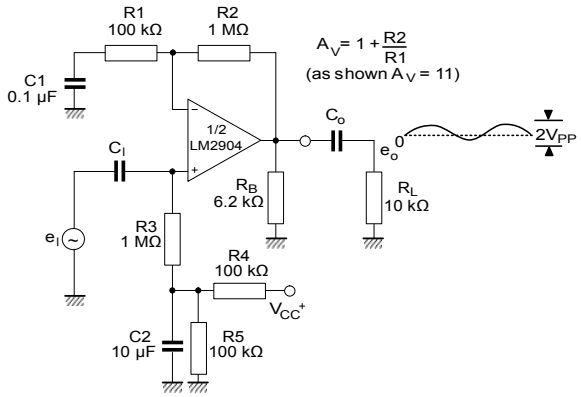


Figure 22. Non-inverting DC gain

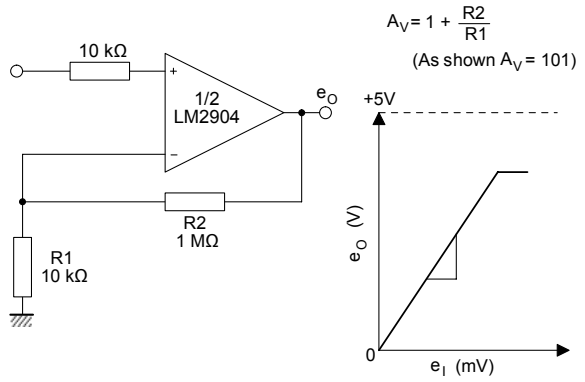


Figure 23. DC summing amplifier

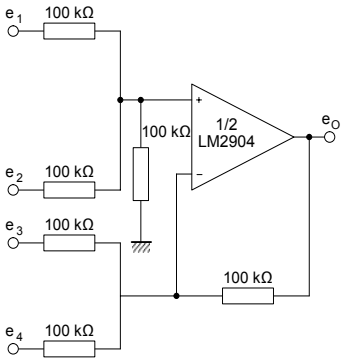


Figure 24. High input Z, DC differential amplifier

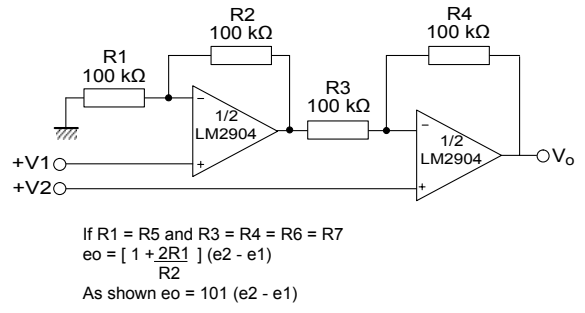


Figure 25. Using symmetrical amplifiers to reduce input current

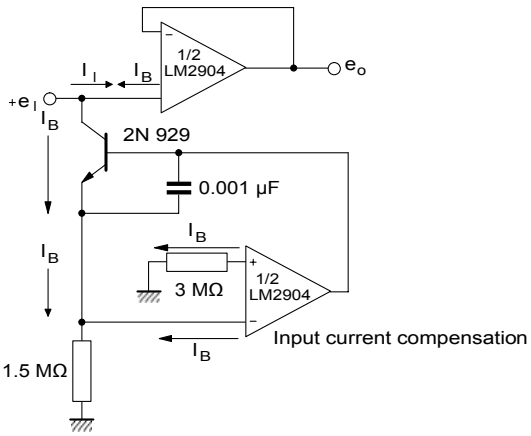


Figure 26. Low drift peak detector

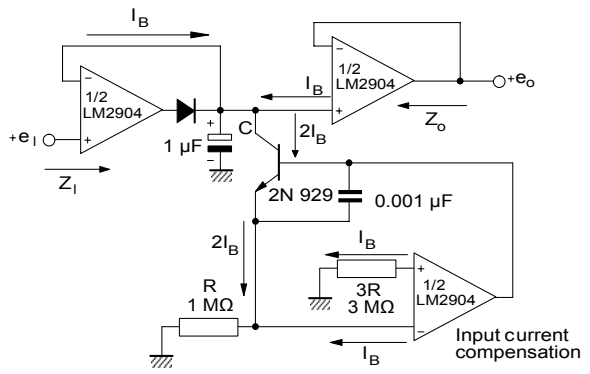
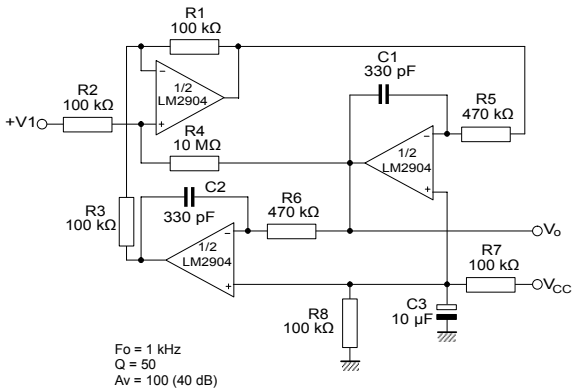


Figure 27. Active bandpass filter



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 TSSOP8 package information

Figure 28. **TSSOP8 package outline**

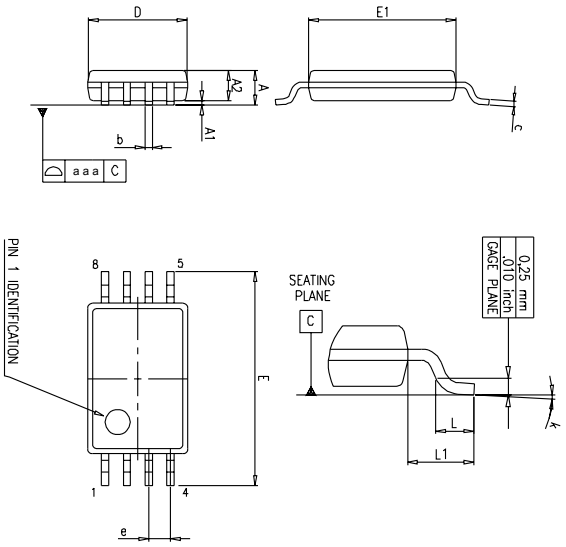


Table 4. **TSSOP8 package mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	6.20	6.40	6.60	0.244	0.252	0.260
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.0256	
k	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1			0.039	
aaa		0.10			0.004	

7.2 DFN8 2 x 2 wettable flank package information

Figure 29. **DFN8 2 x 2 wettable flank package outline**

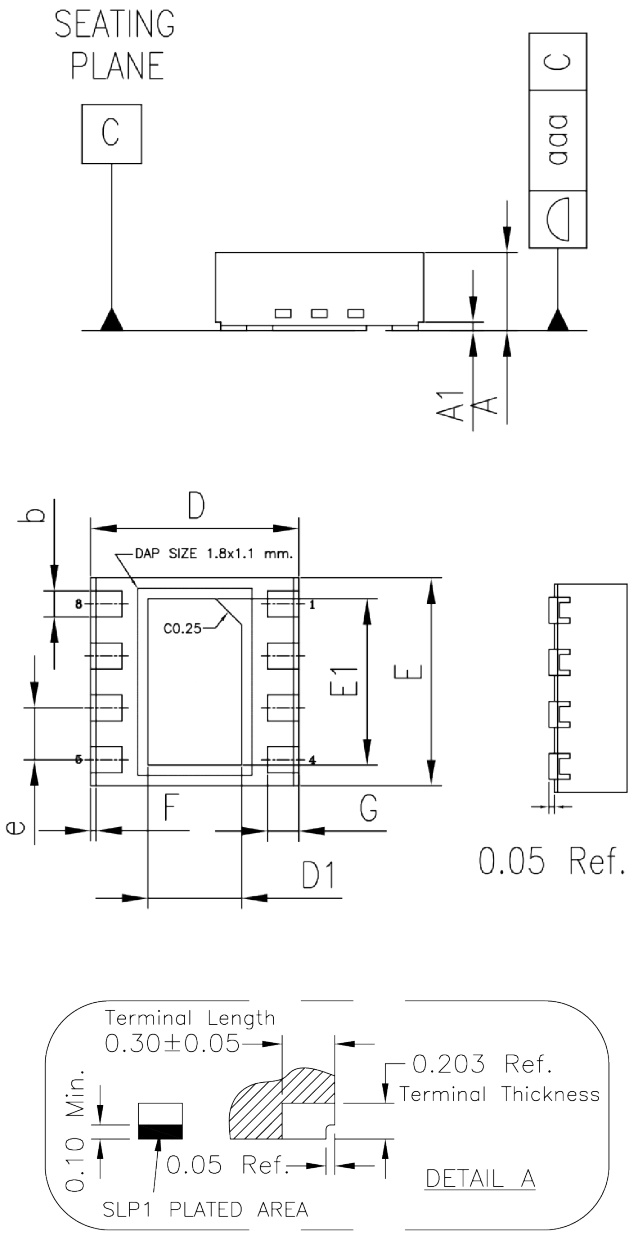
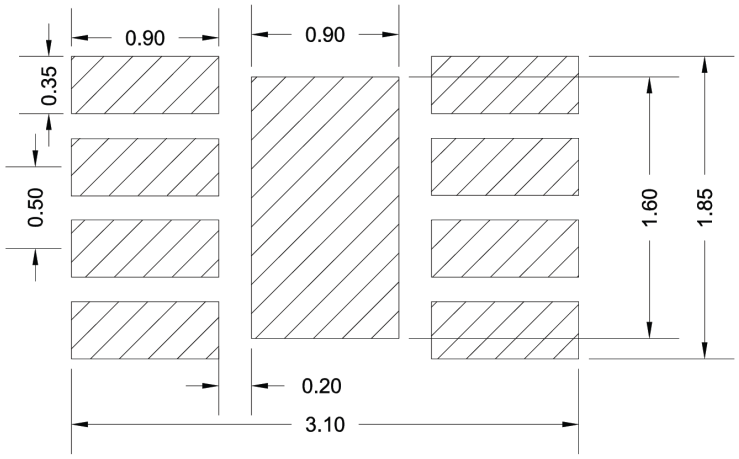


Table 5. DFN8 2 x 2 wettable flank package mechanical data

Ref.	Dimensions					
	Millimiters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.10			0.004		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	1.95	2.00	2.05	0.077	0.079	0.081
D1	0.80	0.90	1.00	0.031	0.035	0.039
E	1.95	2.00	2.05	0.077	0.079	0.081
E1	1.50	1.60	1.70	0.059	0.063	0.067
e		0.50			0.020	
F		0.05			0.002	
G	0.25	0.30	0.35	0.010	0.012	0.014
aaa		0.10			0.004	

Figure 30. DFN8 2 x 2 wettable flank recommended footprint



8 Ordering information

Table 6. Order codes

Order code	Temperature range	Package	Packing	Marking
LM2904AHYPT (1)	-40 °C to 150 °C	TSSOP8	Tape and reel	LM4AH
LM2904HYPT (1)				2904H
LM2904AHYQ6T (1)		DFN8 2x2 wettable flank		K2N

1. *Qualified and characterized according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 and Q002 or equivalent.*

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
19-Oct-2015	1	Initial release
05-Nov-2015	2	Updated datasheet layout Table 1: removed T_{oper} parameter Table 3: updated table title
16-Feb-2016	3	Datasheet status changed to "production data" Table 3: unit of V_{OL} parameter changed from “V” to ‘mV”
29-Feb-2016	4	Updated product status footnote Table 5: replaced footnote 1
15-Oct-2018	5	Added new order code LM2904H in Table 5. Order codes and VIO parameter inSection 4 Electrical characteristics
05-May-2023	6	Updated figure and features on the cover page, Table 1 and Table 6. Order codes. Added new package DFN8 2x2 wettable flank Section 7.2 DFN8 2 x 2 wettable flank package information and figure Figure 3.

Contents

List of tables

List of figures